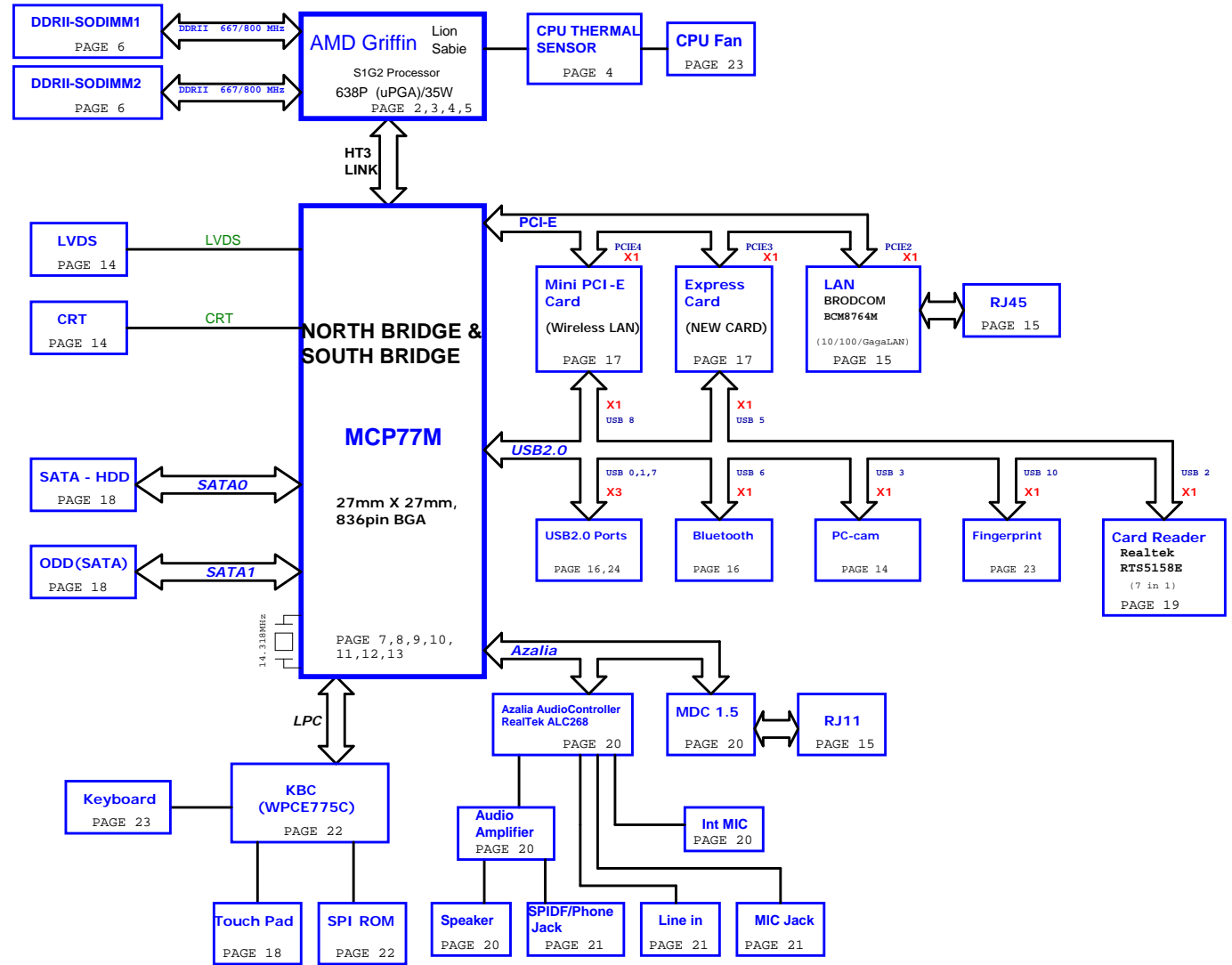


Z05 SYSTEM BLOCK DIAGRAM



- CPU CORE / VDDNB (ISL6265A) PAGE 26
- NB_CORE +1.1V (RT8202) PAGE 28
- +1.1V_NB (RT8202) PAGE 27
- DDR II SMDDR_VTERM 1.8VSUS(TPSS51116REG) PAGE 29
- SYSTEM POWER (ISL6237) PAGE 25
- SYSTEM CHARGER (ISL6251A) PAGE 24



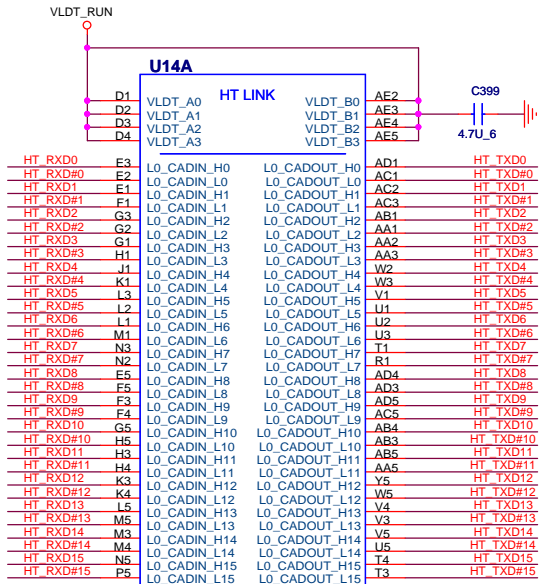
- PCB STACK UP**
- LAYER 1 : TOP
 - LAYER 2 : GND
 - LAYER 3 : IN1
 - LAYER 4 : IN2
 - LAYER 5 : VCC
 - LAYER 6 : BOT

Quanta Computer Inc.
 PROJECT : Z05
 Block Diagram
 Date: Friday, March 07, 2008 Sheet 1 of 34

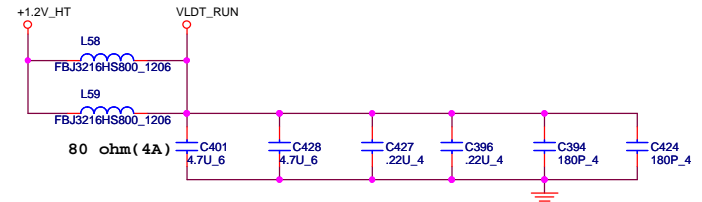


PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



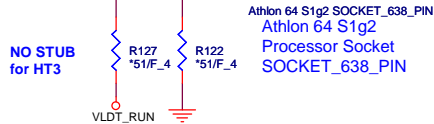
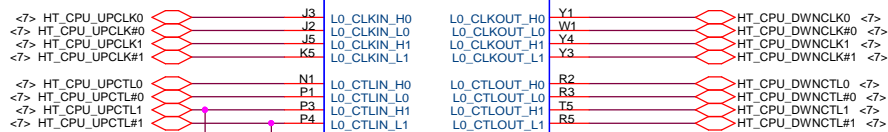
Note: on MCP77, (HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.



LAYOUT: Place bypass cap on topside of board



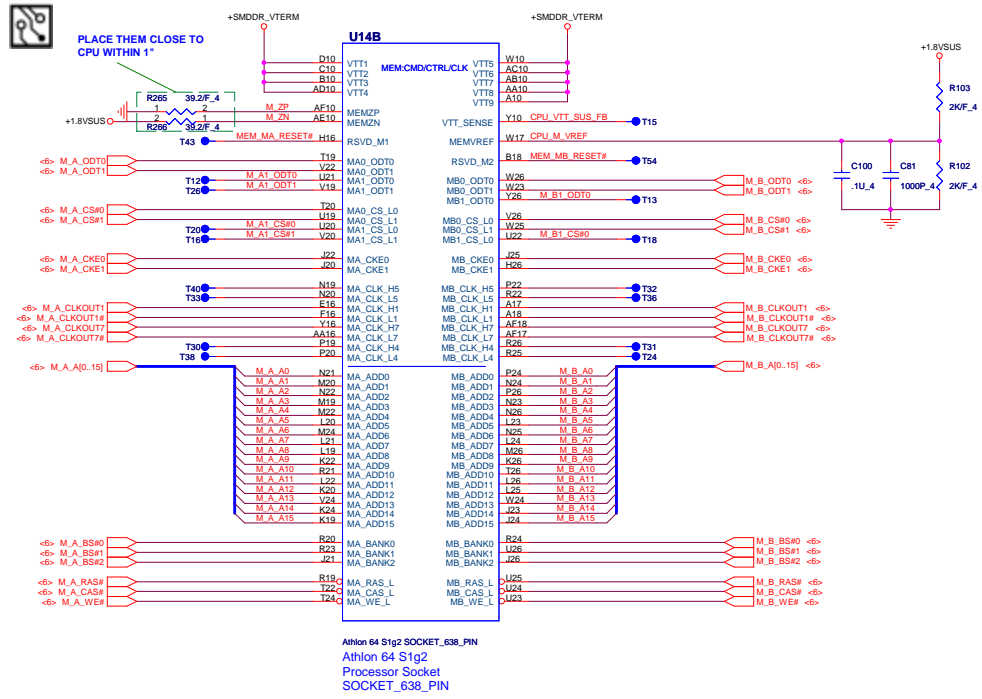
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



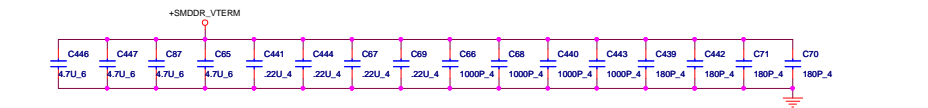
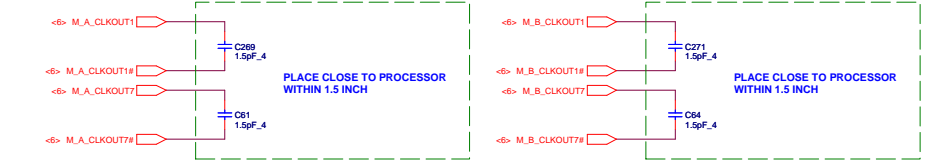
Quanta Computer Inc.
PROJECT : Z05

| | | |
|--------------------|---------------------------|---------------|
| Size | Document Number | Rev 1A |
| AMD Griffin HT I/F | | |
| Date: | Mondsy, February 25, 2008 | Sheet 2 of 34 |

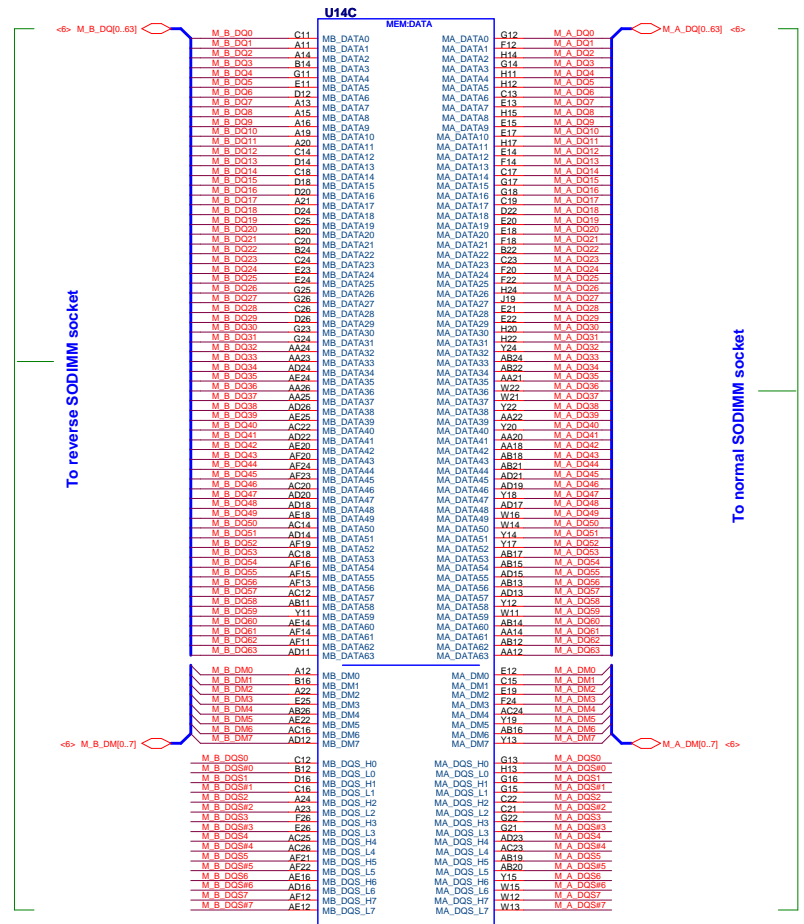
VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2 Processor Socket
SOCKET_638_PIN



Processor DDR2 Memory Interface



To reverse SODIMM socket

To normal SODIMM socket

M.B.DQ00-M.B.DQ07

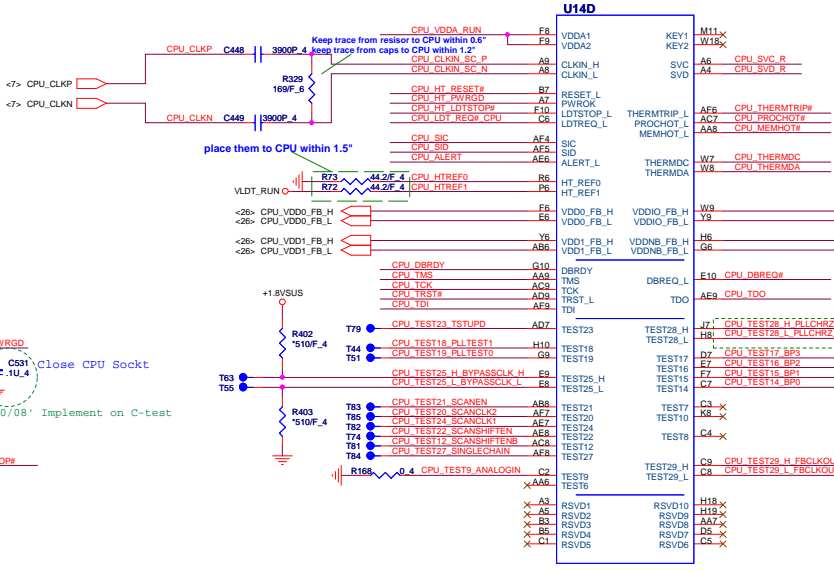
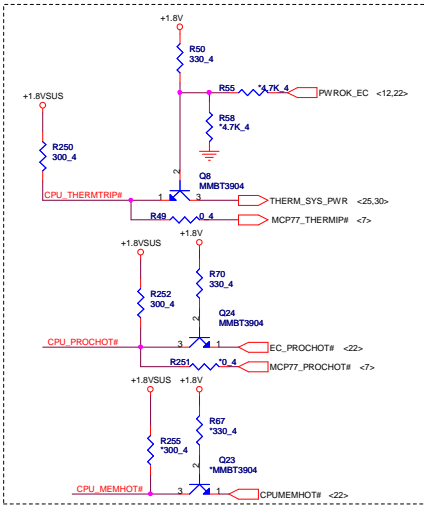
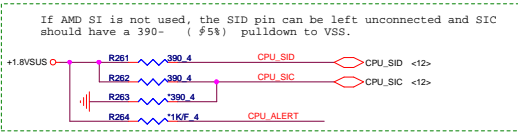
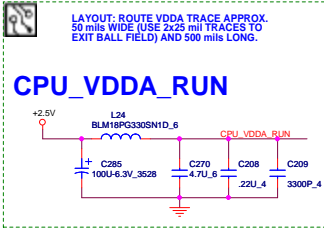
M.A.DQ00-M.A.DQ07

M.B.DQS0-M.B.DQS7

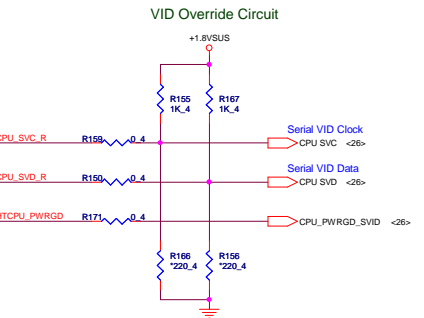
M.A.DQS0-M.A.DQS7

Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2 Processor Socket
SOCKET_638_PIN

ATHLON Control and Debug

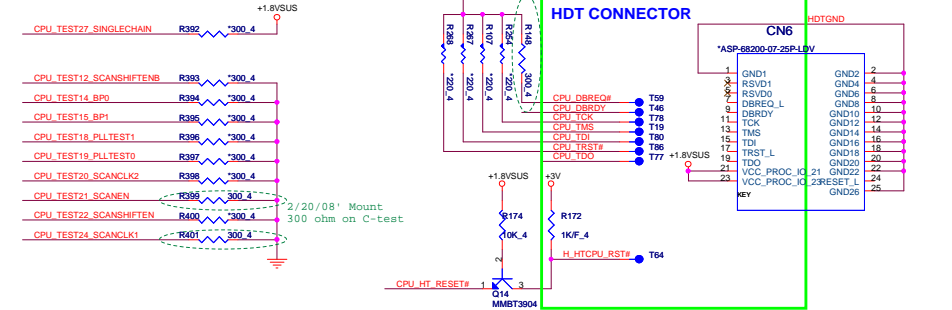
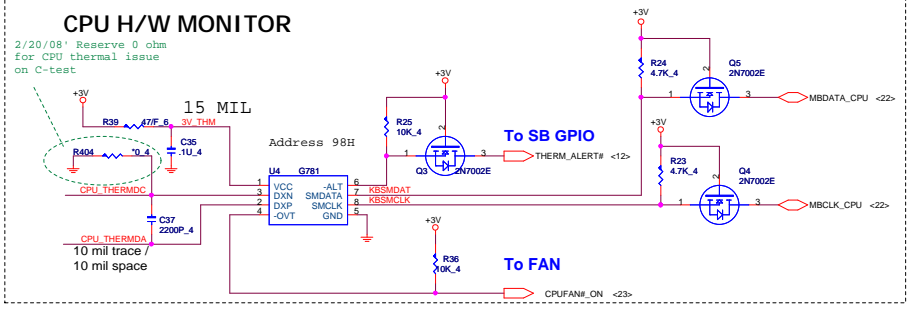


route as differential as short as possible testpoint under package



VFIX MODE

| SVC | SVD | Voltage Output(CPU Power) |
|-----|-----|---------------------------|
| 0 | 0 | 1.4V |
| 0 | 1 | 1.2V |
| 1 | 0 | 1.0V |
| 1 | 1 | 0.8V |



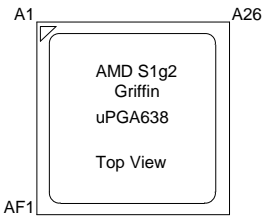
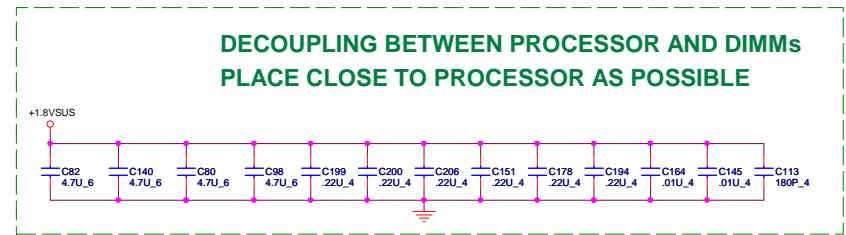
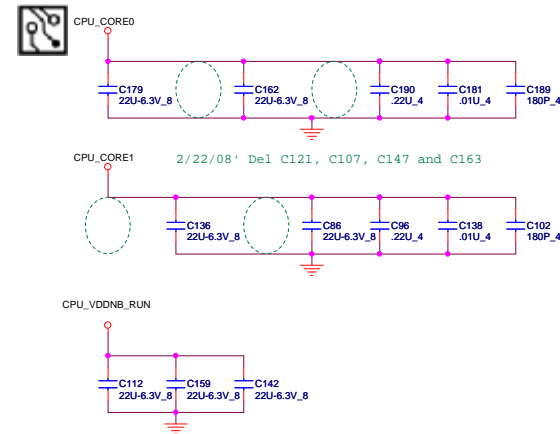
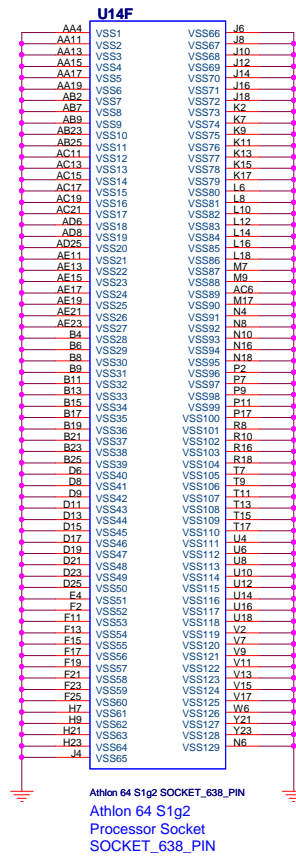
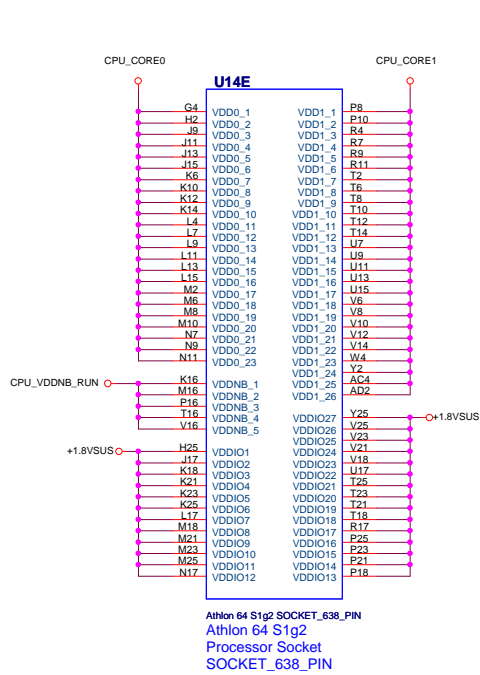
Quanta Computer Inc.

PROJECT : Z05

AMD Griffin CTRL & DEBUG

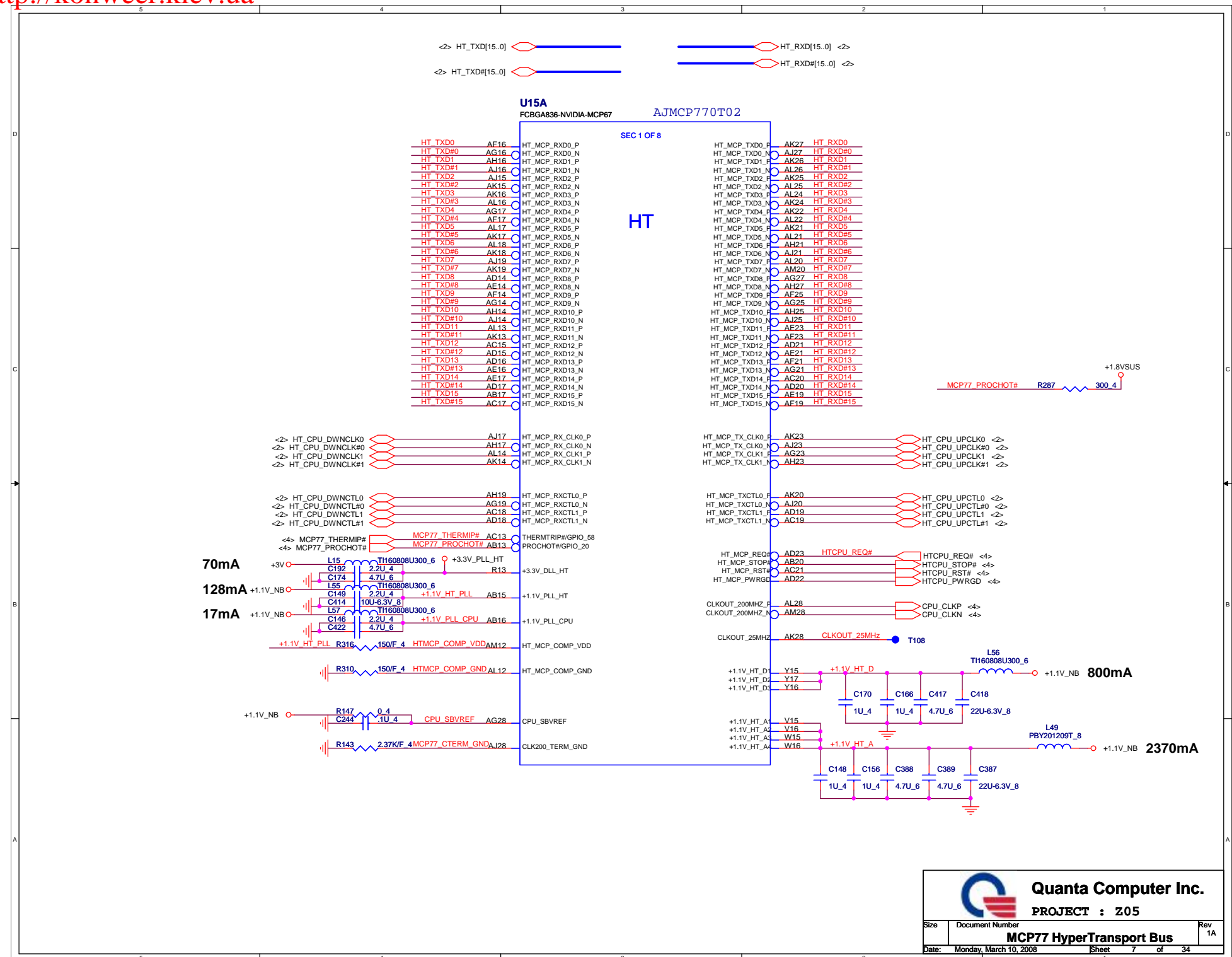
Date: Monday, February 26, 2008 Sheet 4 of 34


PROCESSOR POWER AND GROUND

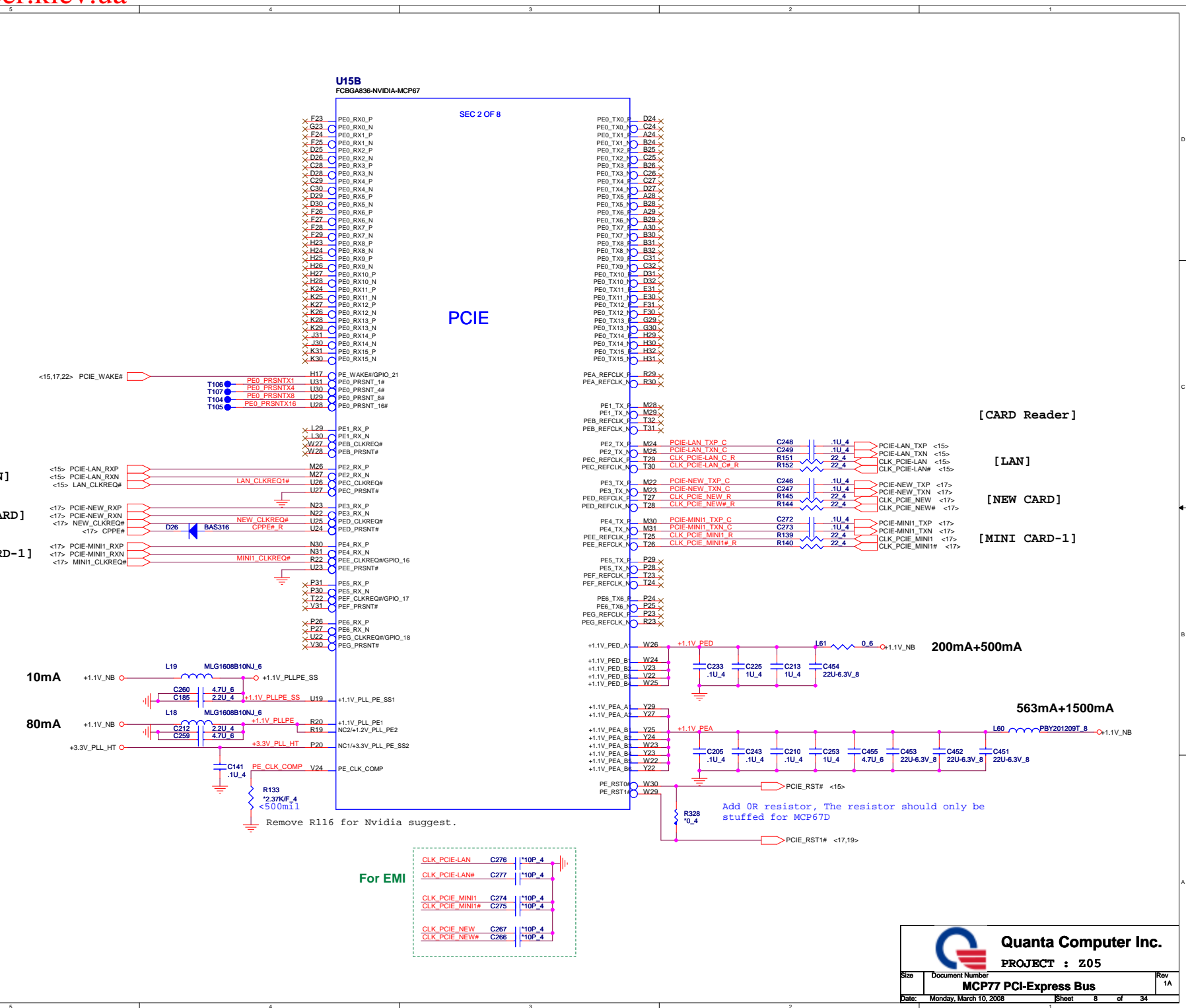


Quanta Computer Inc.
PROJECT : Z05

| | | |
|-------|----------------------------------|---------------|
| Size | Document Number | Rev |
| | AMD Griffin PWR & GND | 1A |
| Date: | Monday, February 25, 2008 | Sheet 5 of 34 |

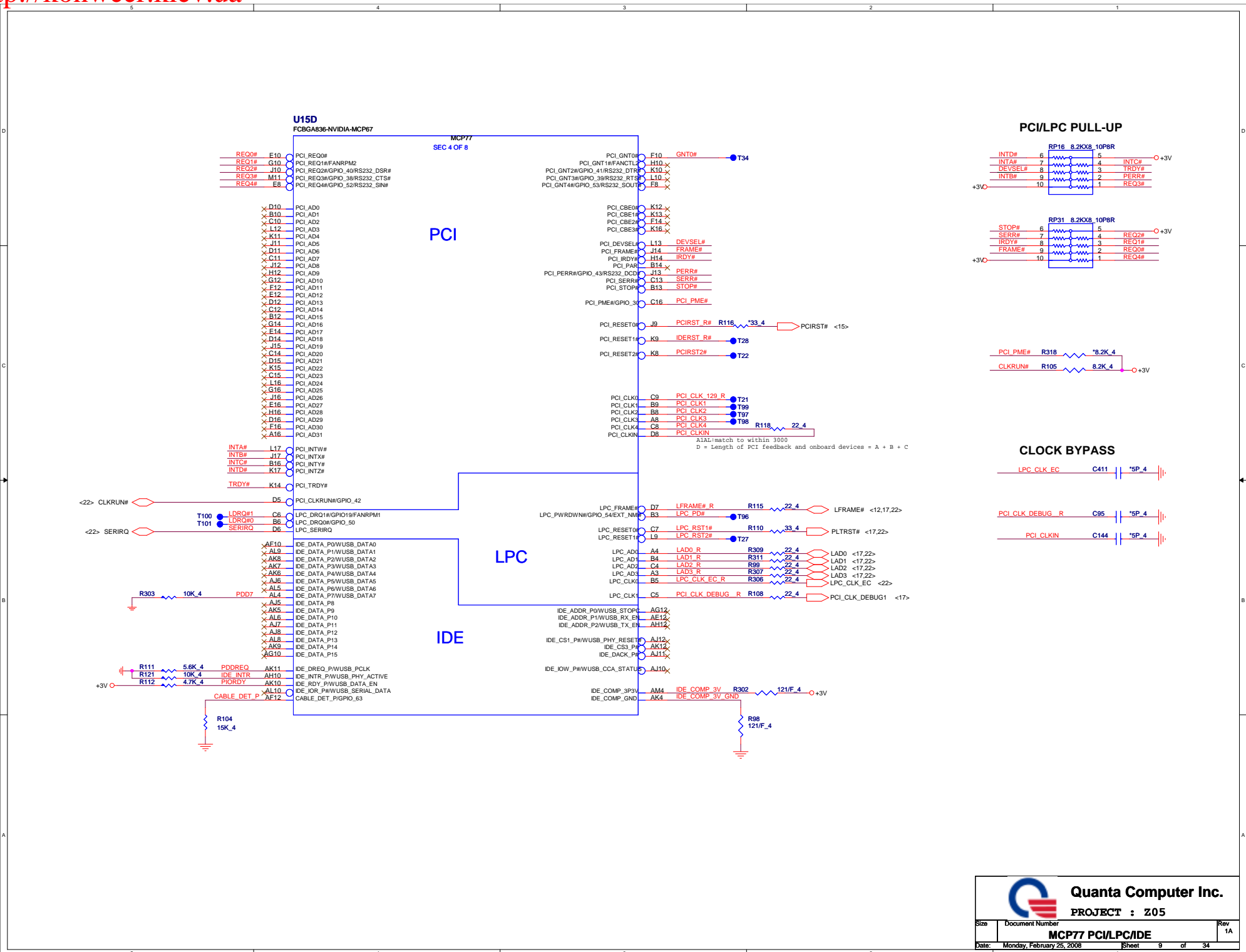


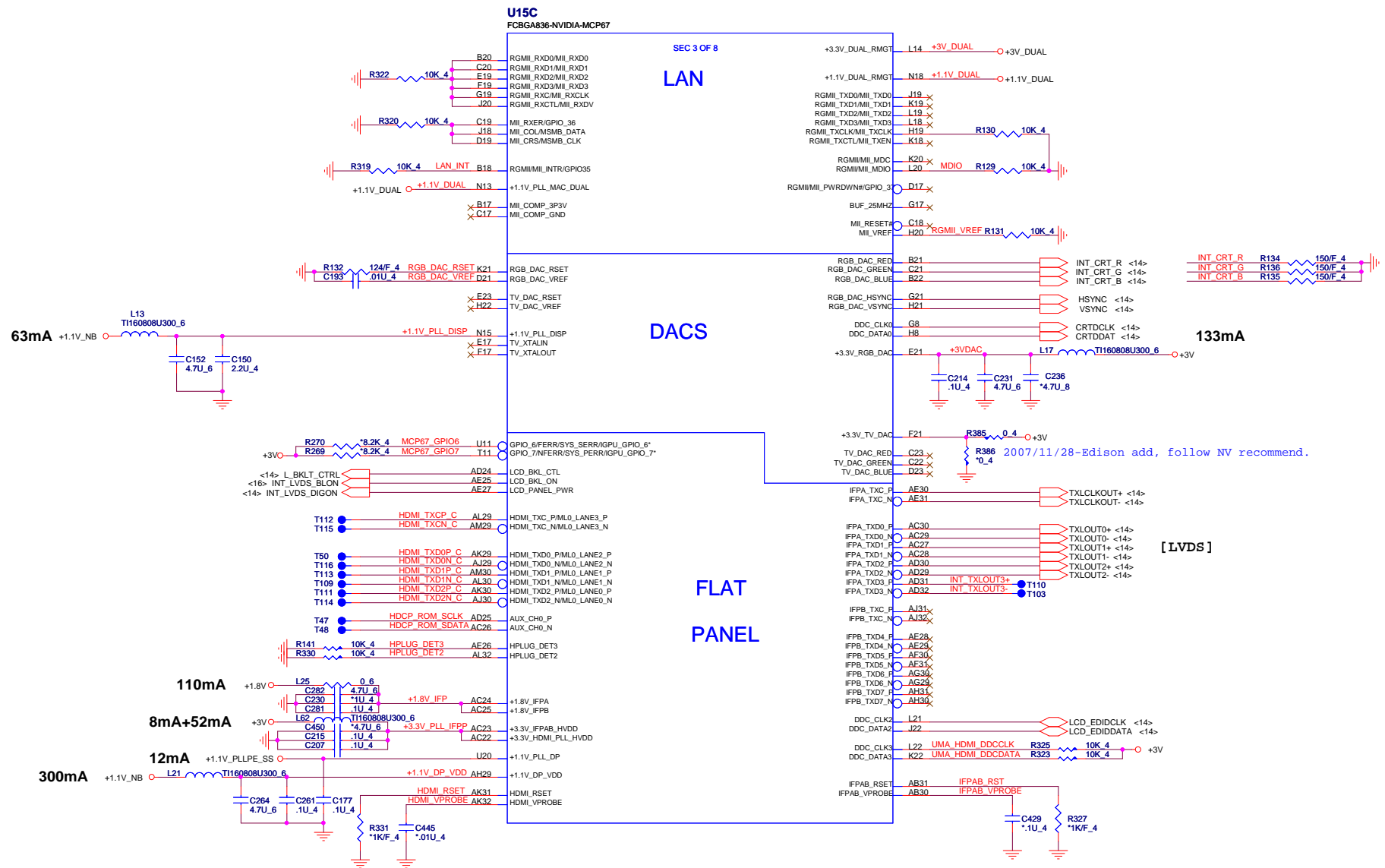
| | | | | | |
|--|------------------------|---------------------------------|-----------------|-----|----|
|  Quanta Computer Inc. PROJECT : Z05 | | Size | Document Number | Rev | |
| | | MCP77 HyperTransport Bus | | 1A | |
| Date: | Monday, March 10, 2008 | Sheet | 7 | of | 34 |

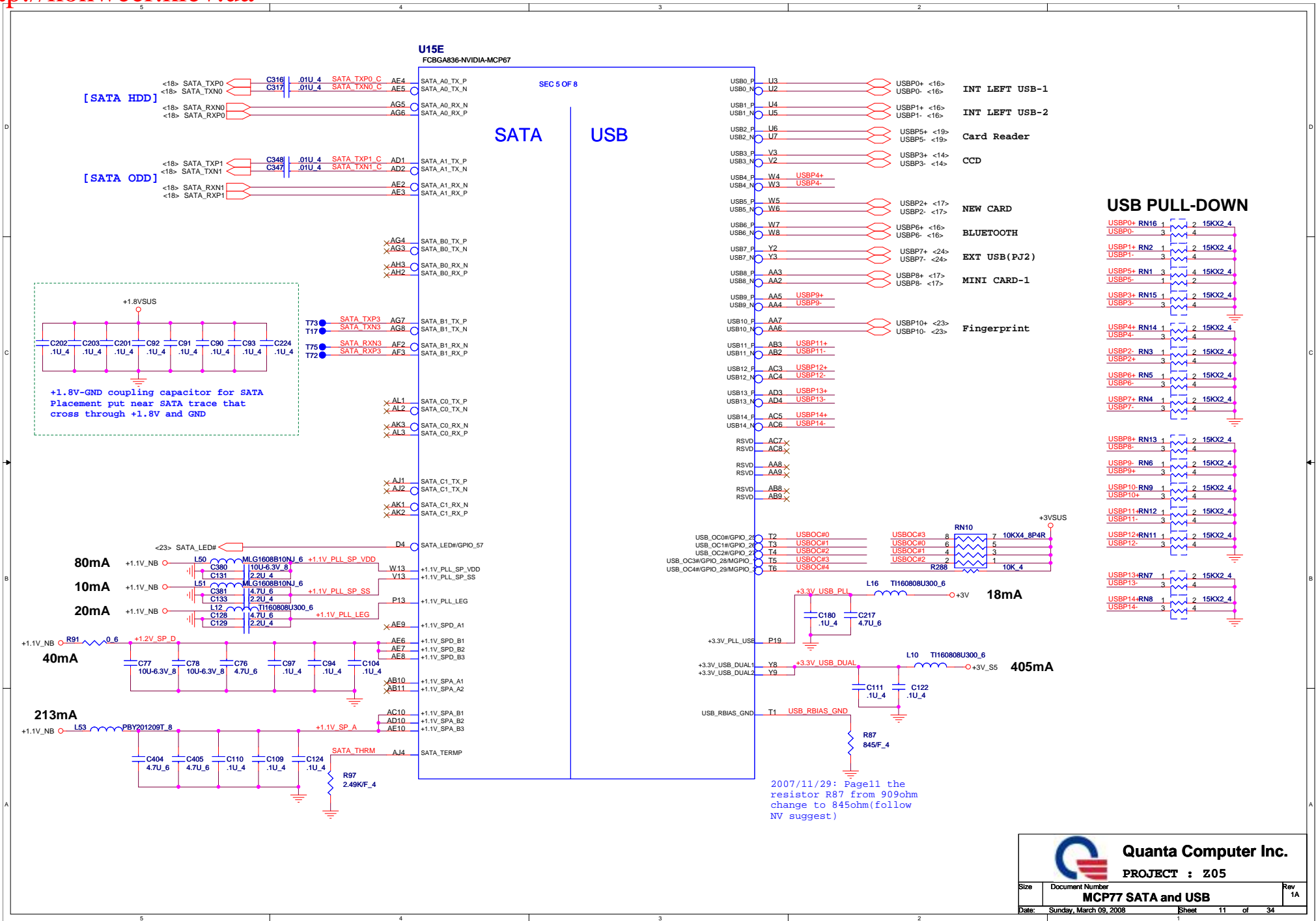


Quanta Computer Inc.
PROJECT : Z05

| | | |
|-------|------------------------------|---------------|
| Size | Document Number | Rev |
| | MCP77 PCI-Express Bus | 1A |
| Date: | Monday, March 10, 2008 | Sheet 8 of 34 |







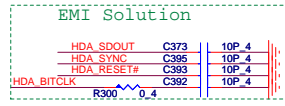
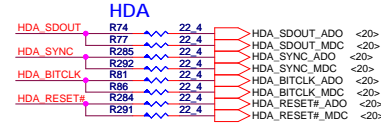
U15F

FCBGA836-NVIDIA-MCP67

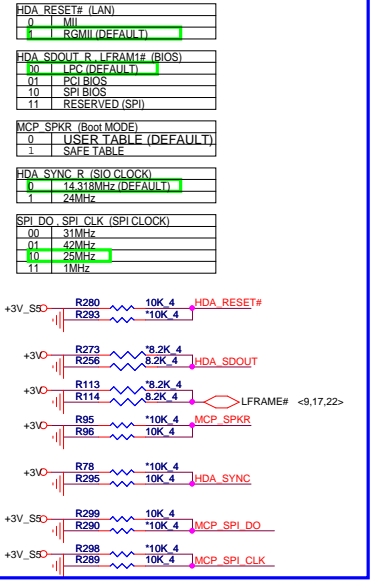
SEC 6 of 8

HDA

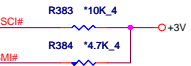
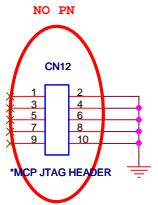
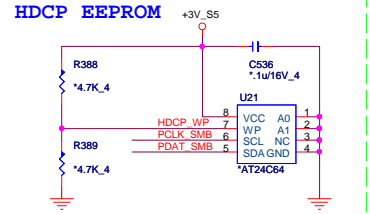
MISC



MCP77 STRAPPING

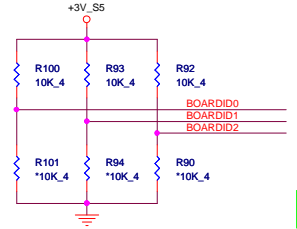
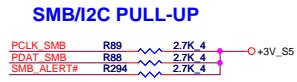


Acer Suggest Reserve HDCP EEPROM 2007/12/05



Delay 10ms after S5 powerOK

2007/11/28-Edison: Removethese part
R315, R317, R326, R324, C423, Q28, Q29



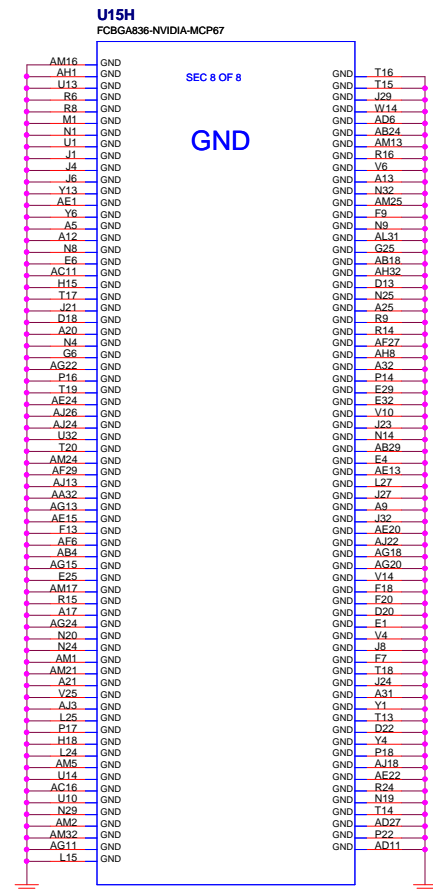
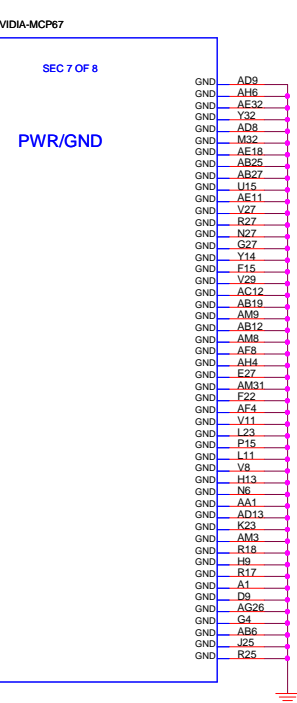
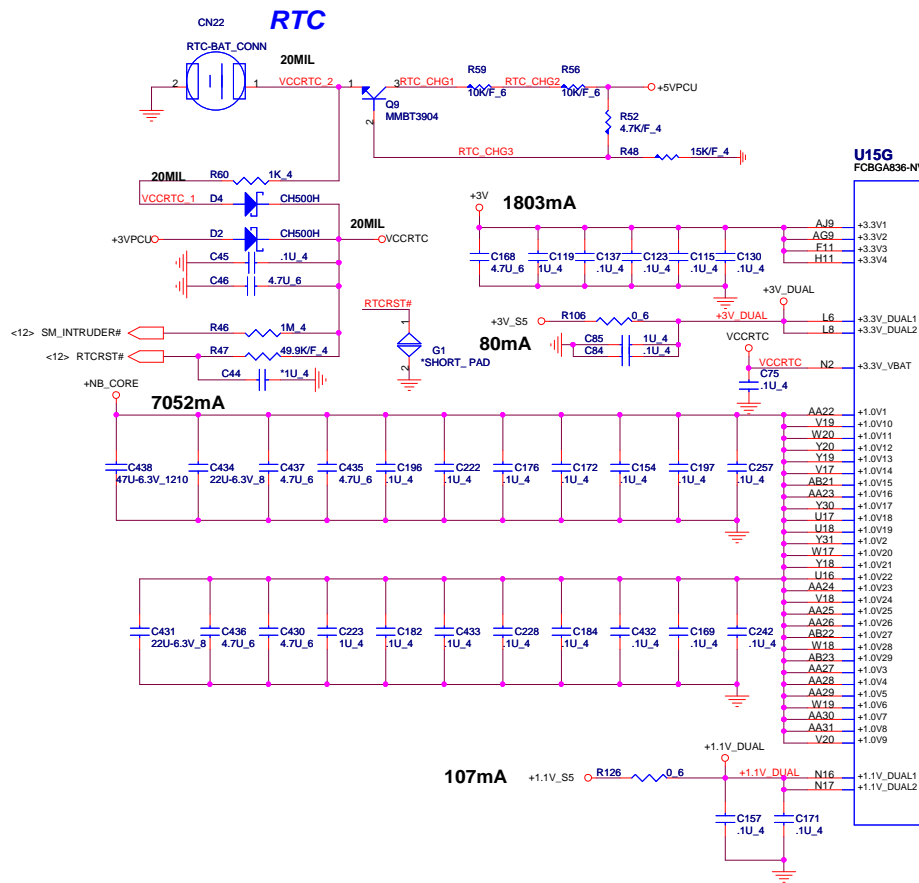
M/B ID for 14"/17"

| ID0 | ID1 | ID2 | M/B |
|-----|-----|-----|---------------------------|
| 0 | 0 | 0 | 17" D |
| 0 | 0 | 1 | X |
| 0 | 1 | 0 | 15" D |
| 1 | 0 | 0 | 15" U |
| 1 | 0 | 1 | 14" Dual Core CPU & MXM |
| 1 | 1 | 0 | 14" Dual Core CPU & UMA |
| 1 | 1 | 1 | 14" Single Core CPU & UMA |

Quanta Computer Inc.
PROJECT : Z05

| | | |
|-------|-------------------------------|----------------|
| Size | Document Number | Rev |
| | MCP77 HDA/SMB/PMU/GPIO | 1A |
| Date: | Sunday, March 08, 2008 | Sheet 12 of 34 |

MCP77 POWER PLANE/GND & BYPASS

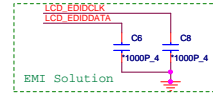
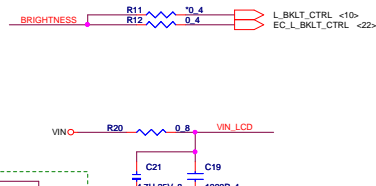
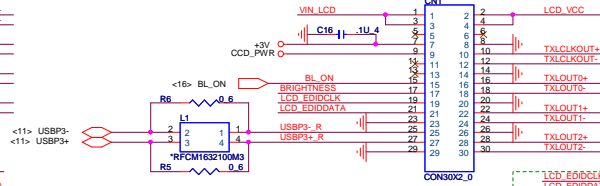
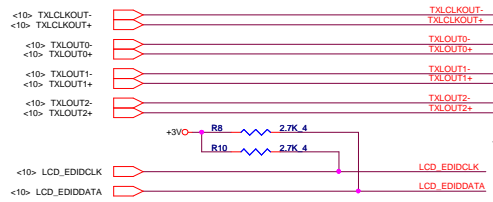


Quanta Computer Inc.
PROJECT : Z05

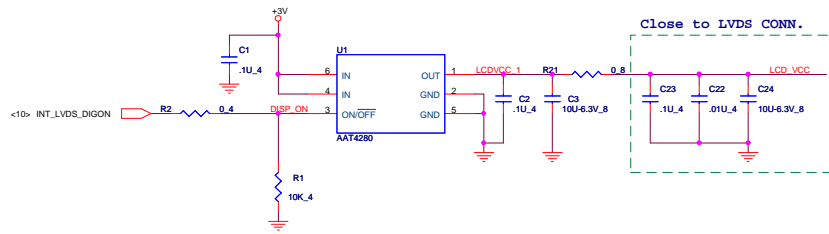
| | | |
|-------|----------------------------|----------------|
| Size | Document Number | Rev |
| | MCP77 POWER/GND/RTC | 1A |
| Date: | Monday, February 25, 2008 | Sheet 13 of 34 |

LVDS

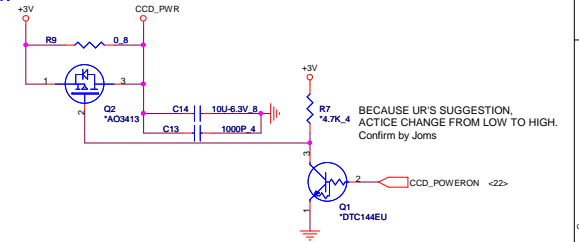
SINGLE_CH



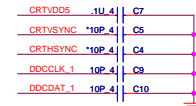
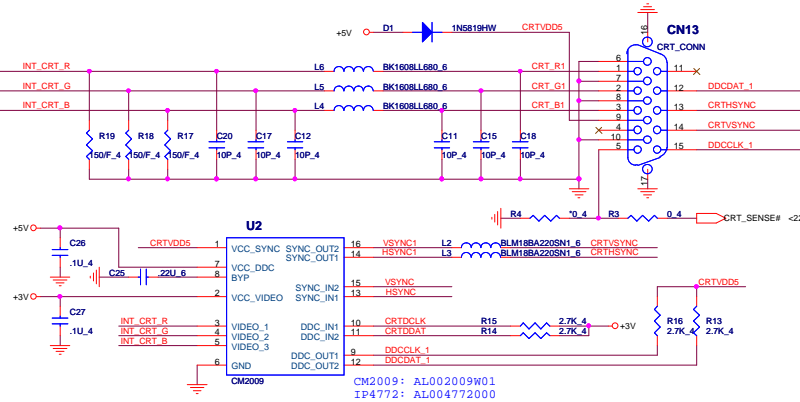
LCD POWER



CAMERA MODULE POWER

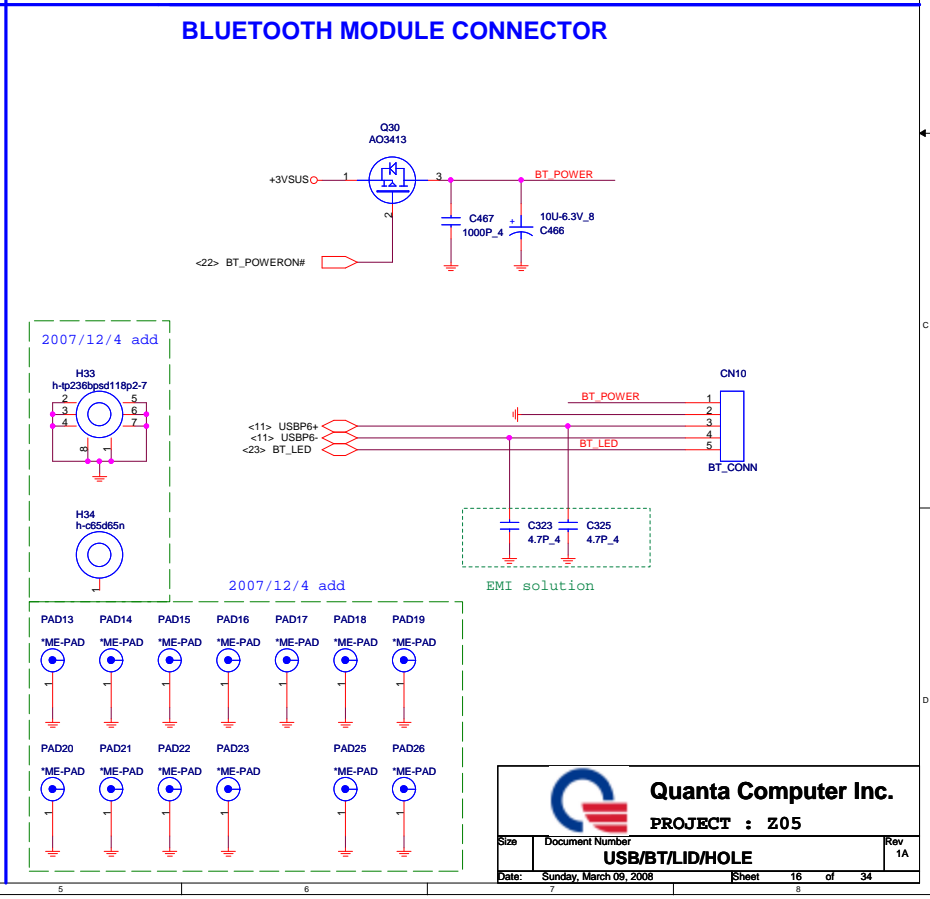
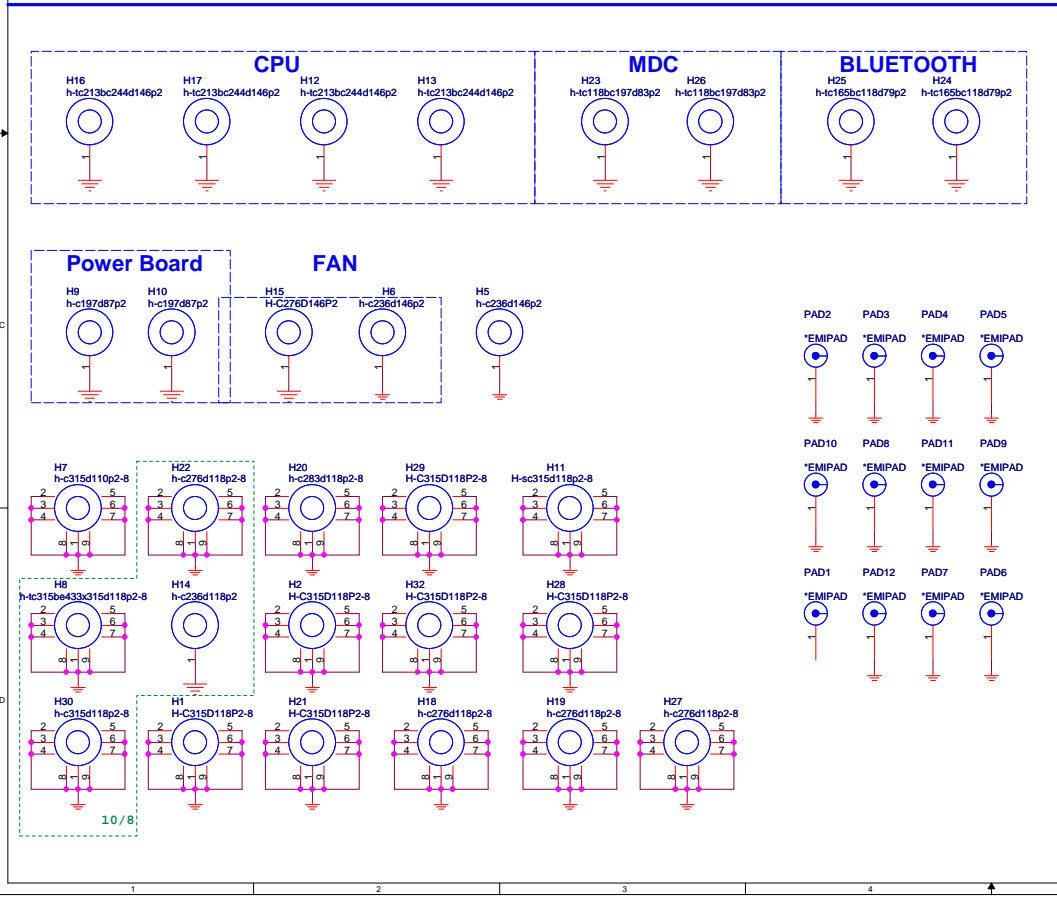
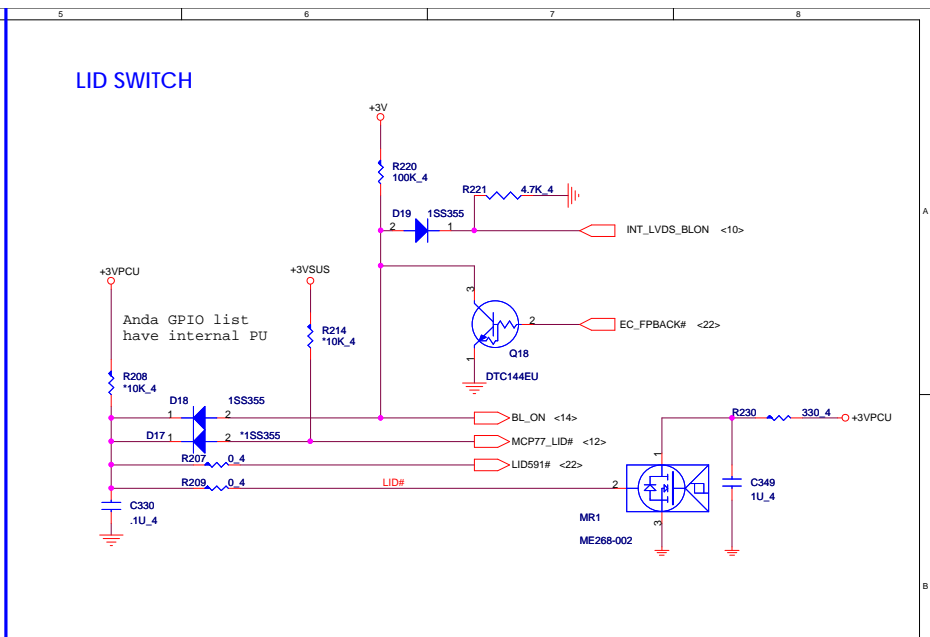
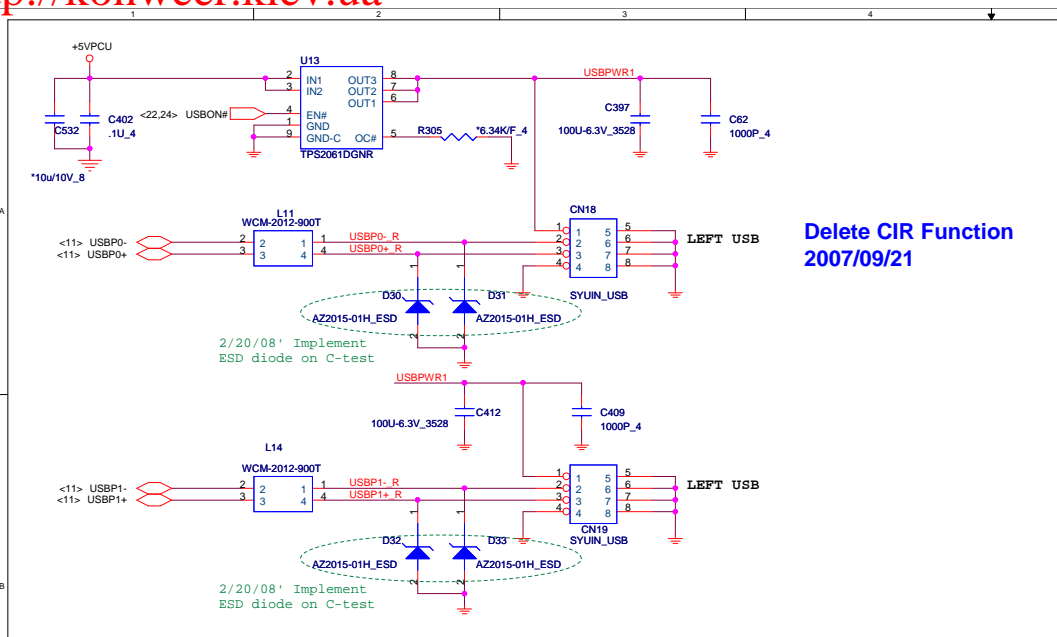


CRT



TV Out (SVHS) MiniDIN 7-pin

Delete TVOUT MiniDIN



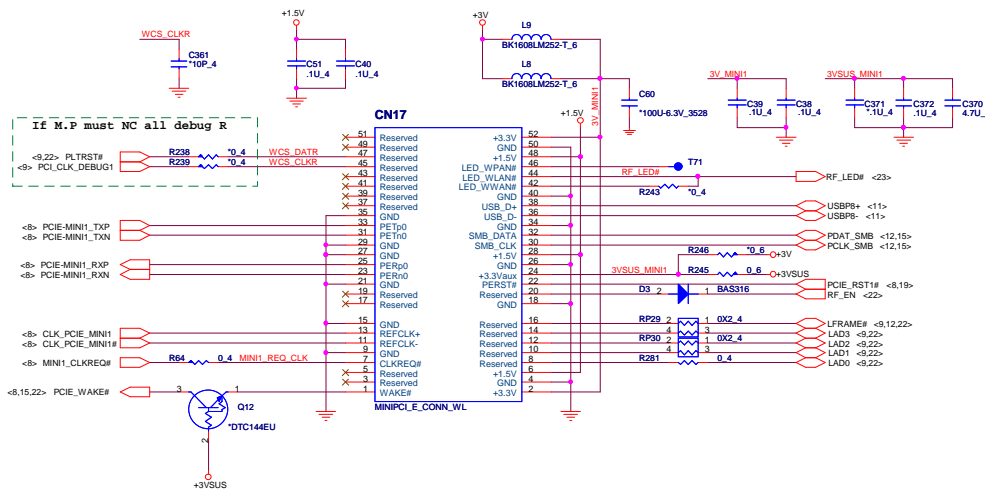
Quanta Computer Inc.

PROJECT : Z05

| | | |
|-------|------------------------|----------------|
| Size | Document Number | Rev |
| | USB/BT/LID/HOLE | 1A |
| Date: | Sunday, March 08, 2008 | Sheet 16 of 34 |

MINI-Card

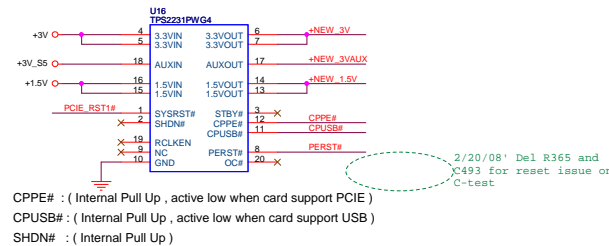
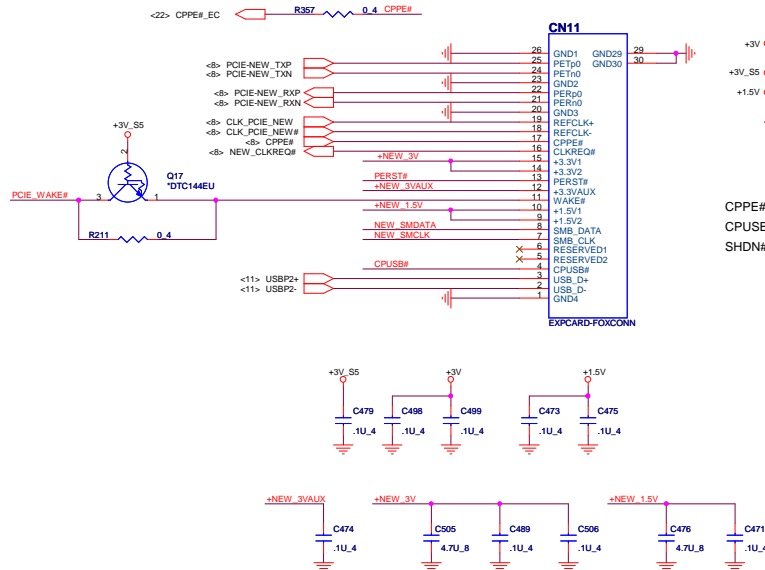
MINI-Card Port-1



Delete MINI-Card Port-2

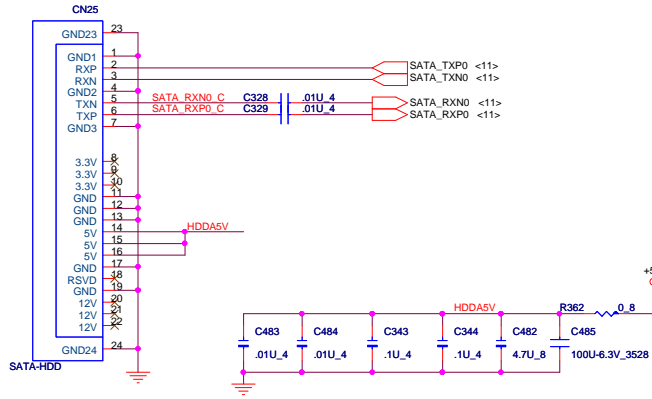
New card

NEW CARD'S POWER SWITCH

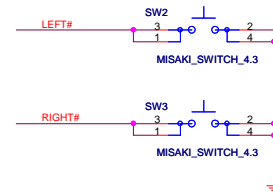


CPPE# : (Internal Pull Up , active low when card support PCIe)
 CPUSB# : (Internal Pull Up , active low when card support USB)
 SHDN# : (Internal Pull Up)

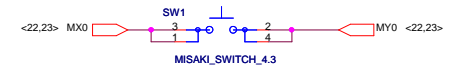
SATA HDD



TP SWITCH

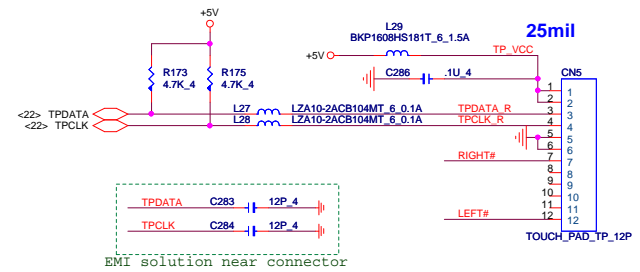


E-KEY

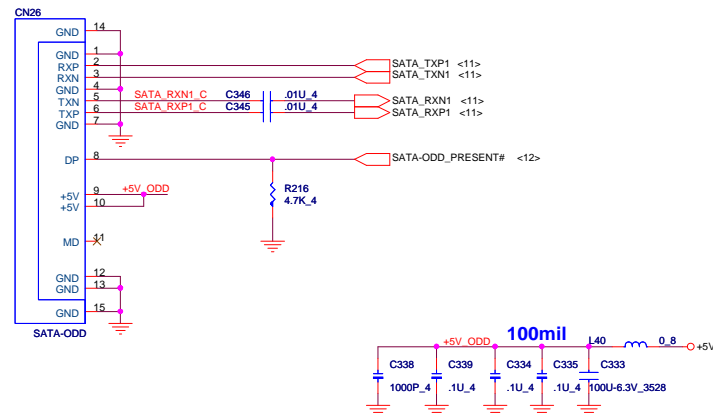


MX0 MY0:E-Key

TP CONN

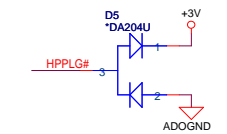
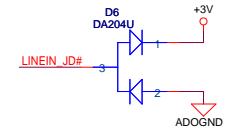
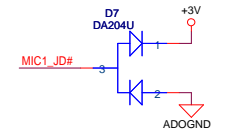
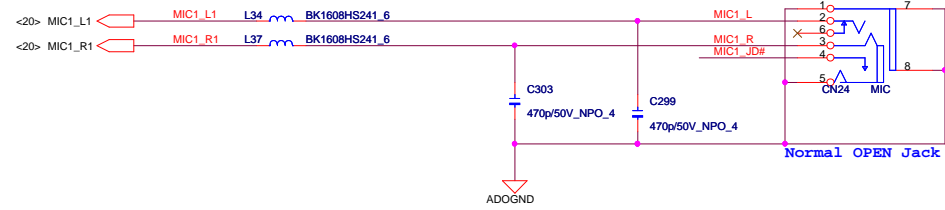


ODD (SATA)

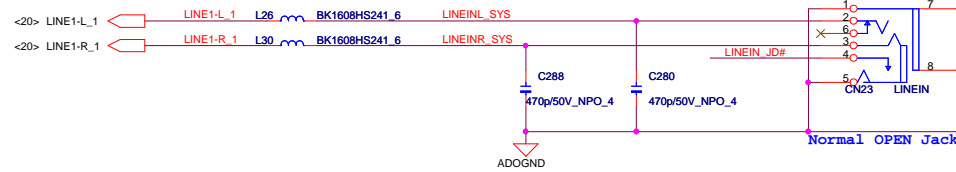


| | | | |
|---------------------------------|--|--|---------------------------------------|
| | | Quanta Computer Inc. PROJECT : Z05 | |
| | | Size: Document Number | SATA-HDD & SATA-ODD&TP |
| Date: Monday, February 25, 2008 | | Sheet: 18 | of: 34 |

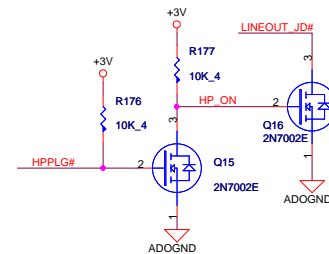
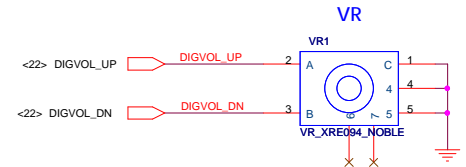
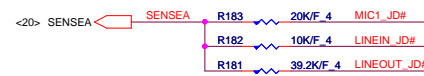
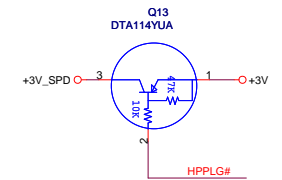
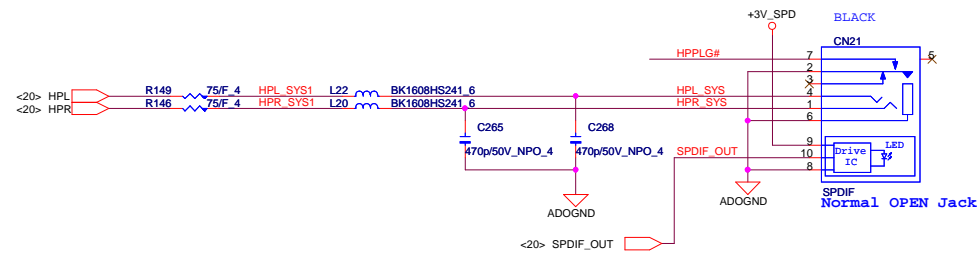
MIC



LINE IN



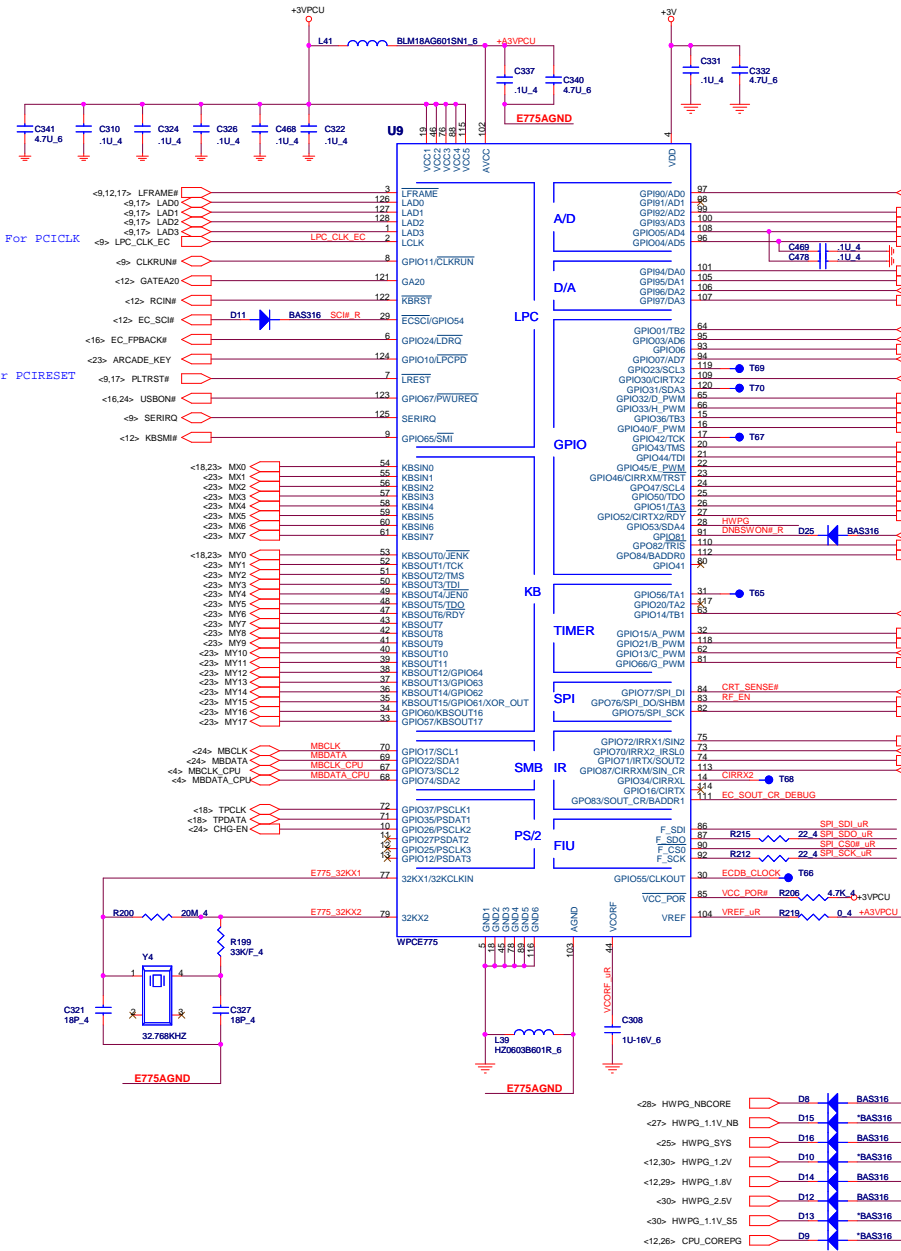
HeadPhone OUT/SPDIF



Quanta Computer Inc.
PROJECT : Z05

| | | |
|-------|---------------------------|----------------|
| Size | Document Number | Rev |
| | Audio Jack | 1A |
| Date: | Monday, February 25, 2008 | Sheet 21 of 34 |

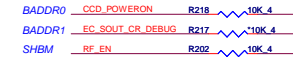
WPCE775C



I/O ADDRESS SETTING

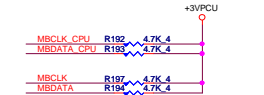
| I/O Address | | |
|-------------|--------------------|-------|
| BADDR1-0 | Index | Data |
| 0 0 | XOR TREE TEST MODE | |
| 0 1 | CORE DEFINED | |
| 1 0 | 2Eh | 2Fh |
| 1 1 | 164Eh | 164Fh |

SHBM=0: Enable shared memory with host BIOS

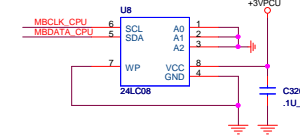


Disabled (*) if using FW-H device on LPC.
Enabled (†) if using SPI flash for both system BIOS and EC firmware

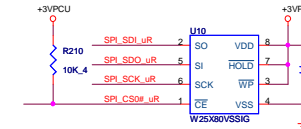
SMBUS PULL-UP



ACER ID



SPI FLASH



INTERNAL KEYBOARD STRIP SET

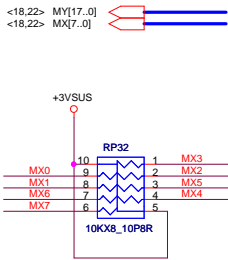
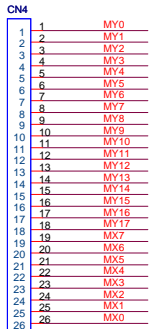


Quanta Computer Inc.
PROJECT : Z05

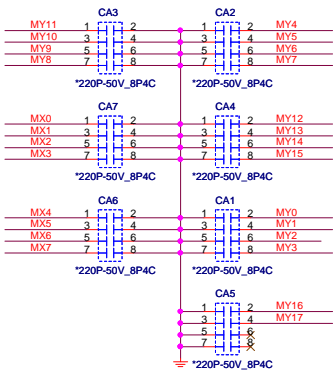
Size: Document Number
EC WPCE775C_ODG & SPI
Rev 1A

Date: Monday, February 26, 2008 Sheet 22 of 34

INT K/B

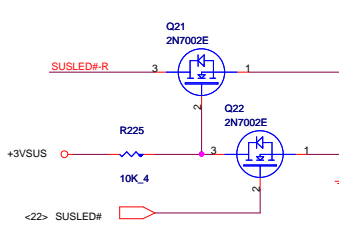
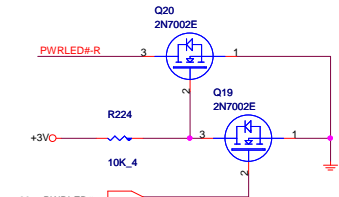
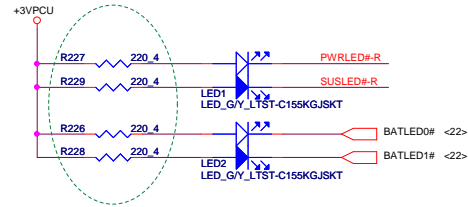


FFC_26P_KB

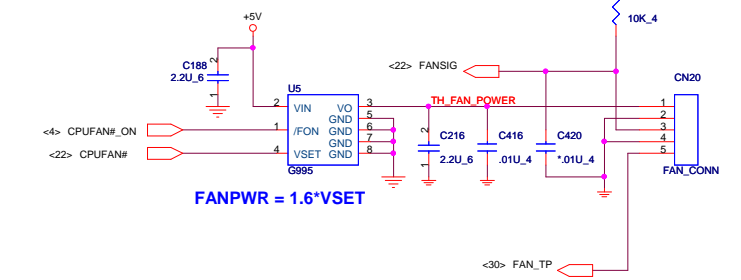


LED

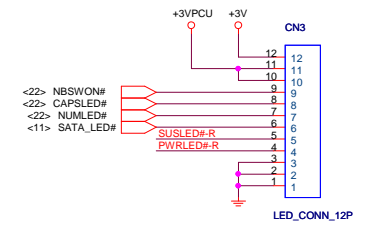
2/21/08' Change from 330ohm to 220ohm on C-test



CPU FAN



LED BOARD CONN.



Debug

Delete Debug Port(PCI & IDE)

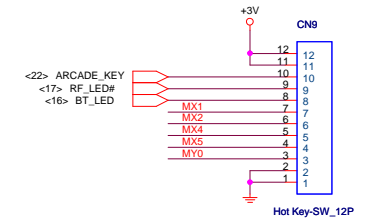
Fingerprint BOARD CONN.

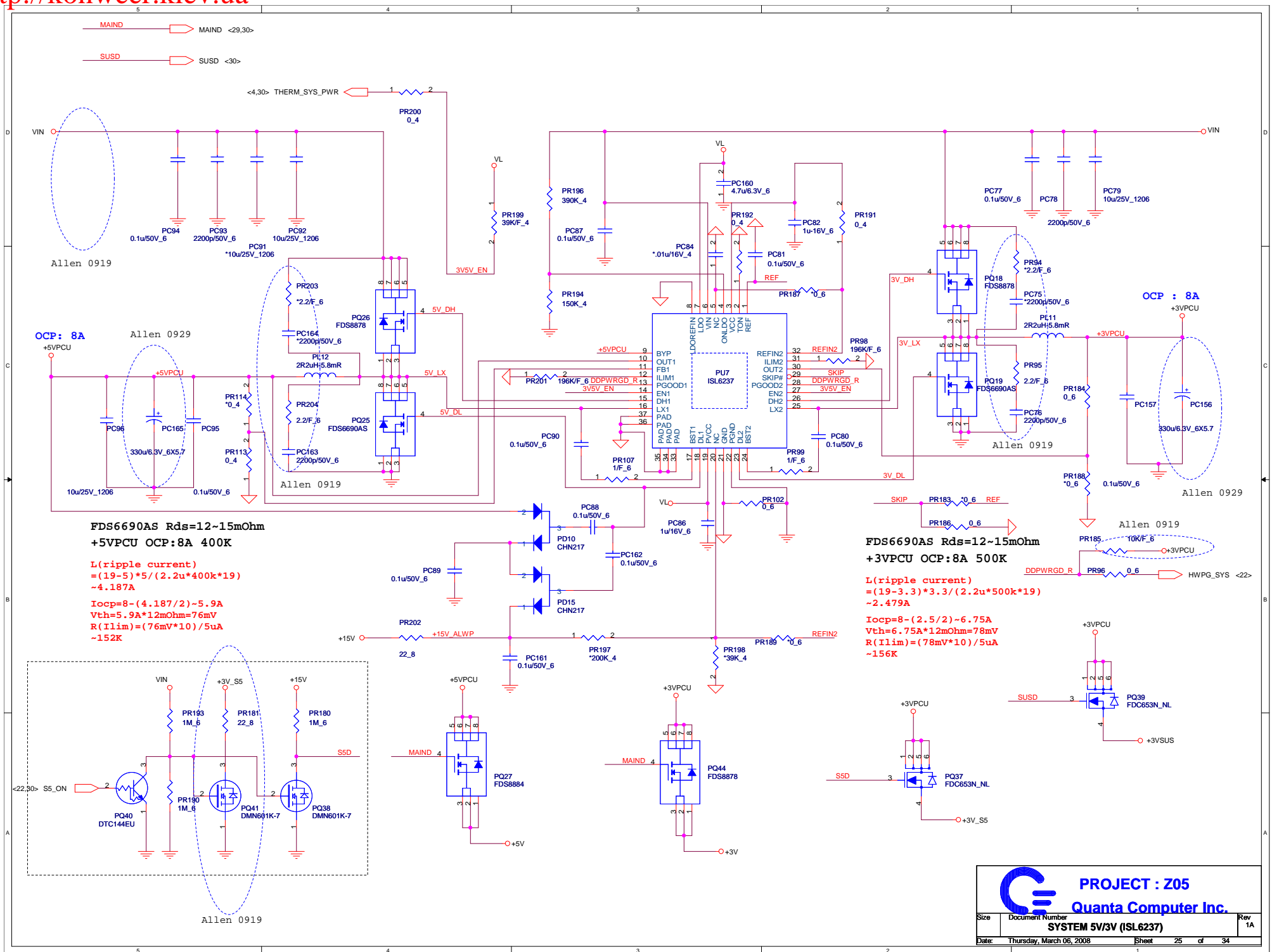


Button BOARD CONN.

BUTTON MATRIX

| | |
|-----|-----------|
| | MY0 |
| MX1 | MAIL |
| MX2 | WWW |
| MX4 | WIRELESS |
| MX5 | BLUETOOTH |





PROJECT : Z05
Quanta Computer Inc.

| | | |
|-------|-------------------------------|----------------|
| Size | Document Number | Rev |
| | SYSTEM 5V/3V (ISL6237) | 1A |
| Date: | Thursday, March 06, 2008 | Sheet 25 of 34 |

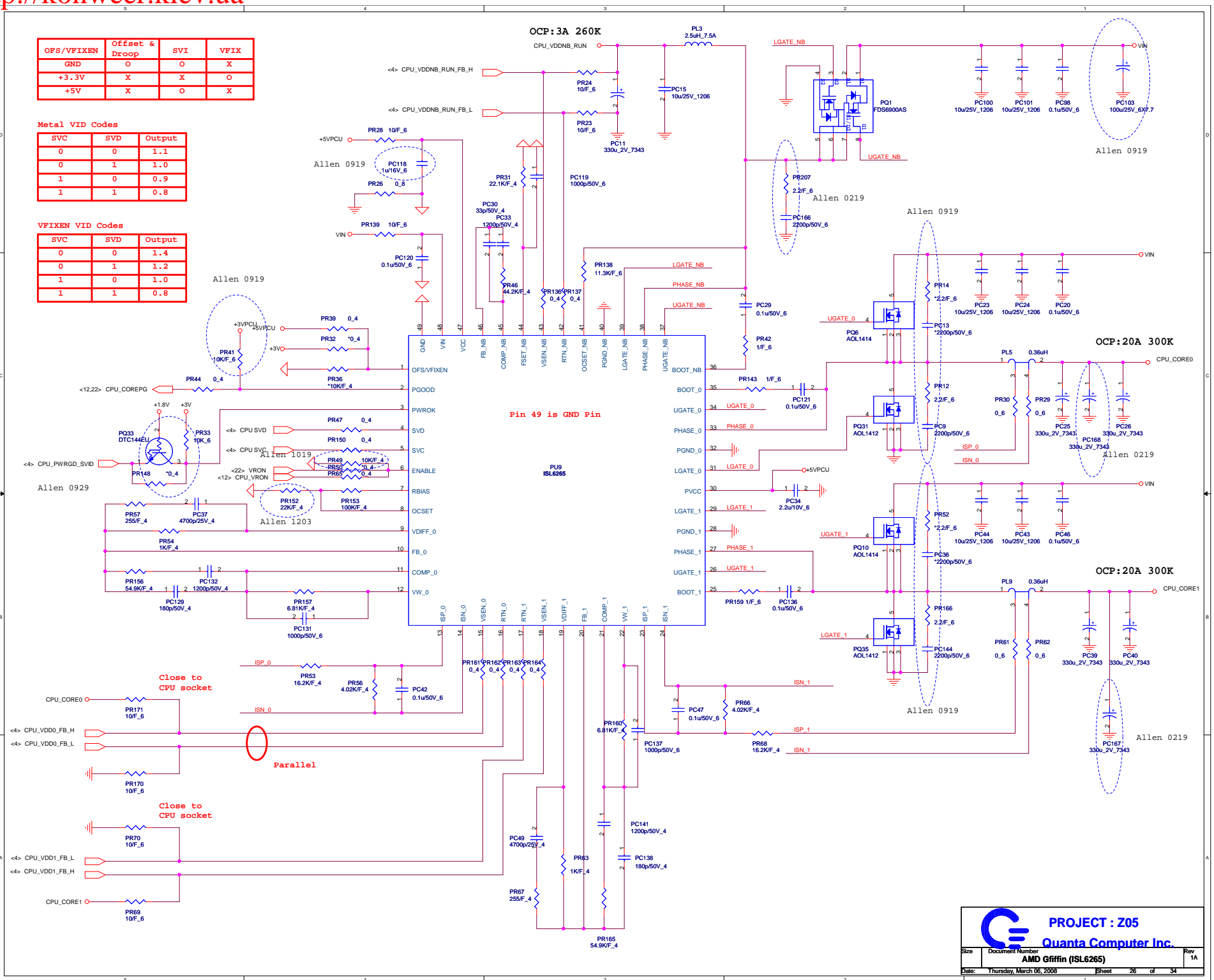
| OFS/VFIXEN | Offset & Droop | SVI | VFIX |
|------------|----------------|-----|------|
| GND | 0 | 0 | X |
| +3.3V | X | X | 0 |
| +5V | X | 0 | X |

Metal VID Codes

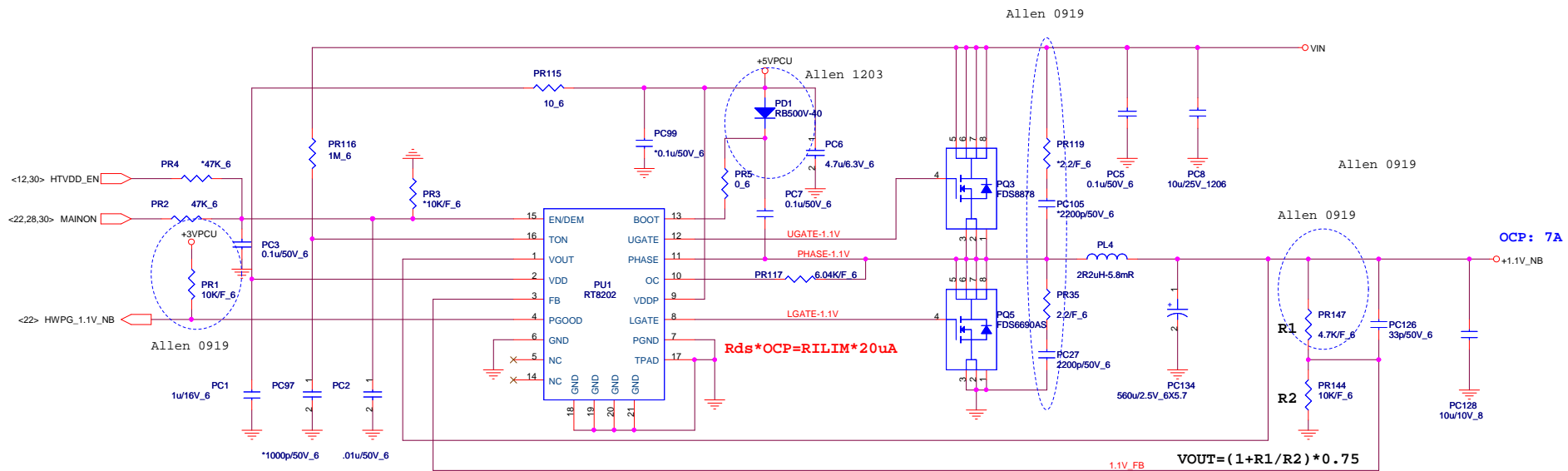
| SVC | SVD | Output |
|-----|-----|--------|
| 0 | 0 | 1.1 |
| 0 | 1 | 1.0 |
| 1 | 0 | 0.9 |
| 1 | 1 | 0.8 |

VFIXEN VID Codes

| SVC | SVD | Output |
|-----|-----|--------|
| 0 | 0 | 1.4 |
| 0 | 1 | 1.2 |
| 1 | 0 | 1.0 |
| 1 | 1 | 0.8 |



PROJECT : Z05
Quanta Computer Inc.
 AMD Gffinn (ISL6265)
 Size: Document Number: Rev 1A
 Date: Thursday, March 06, 2008 Sheet 26 of 34



$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

FDS6690AS Rds=12-15mOhm

OCP=7-0.8A

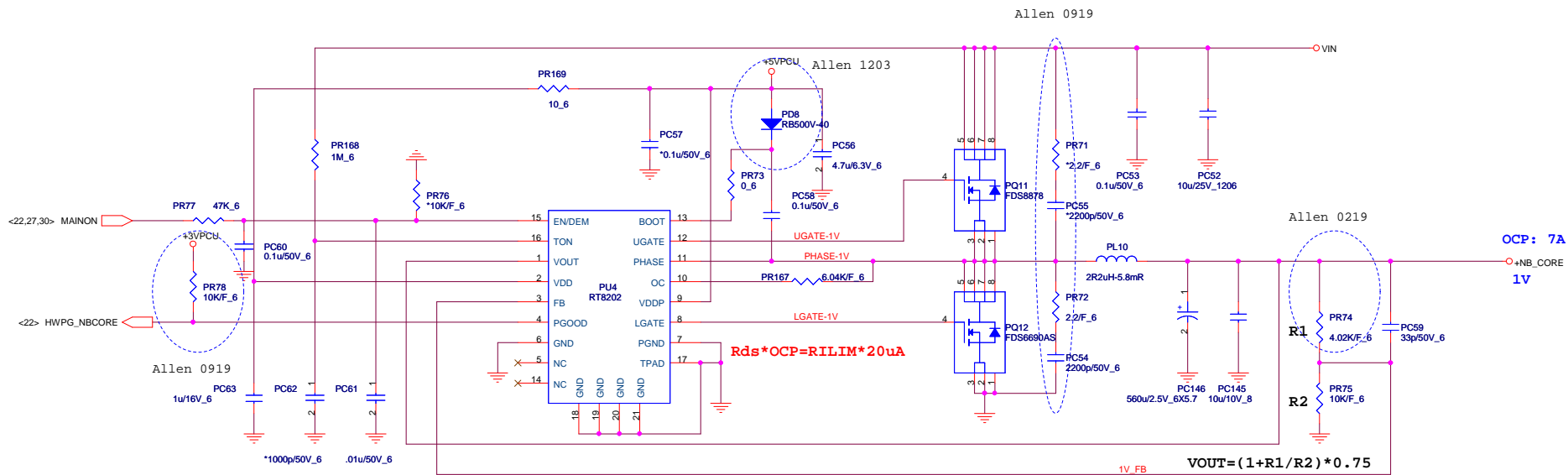
L(ripple current)
 $= (19-1) * 1 / (2.2u * 272k * 19)$
 ~1.58A

$12m * 6 = RILIM * 20uA$
 RILIM=3.6K(2.5~8K)



PROJECT : Z05
 Quanta Computer Inc.

| | | |
|-------|---------------------------|----------------|
| Size | Document Number | Rev |
| | NB_VCC (RT8202) | 1A |
| Date: | Monday, February 25, 2008 | Sheet 27 of 34 |



$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

FDS6690AS Rds=12-15mOhm

OCP=7-0.8A


$$L(\text{ripple current}) = (19-1) * 1 / (2.2u * 272k * 19) \approx 1.58A$$

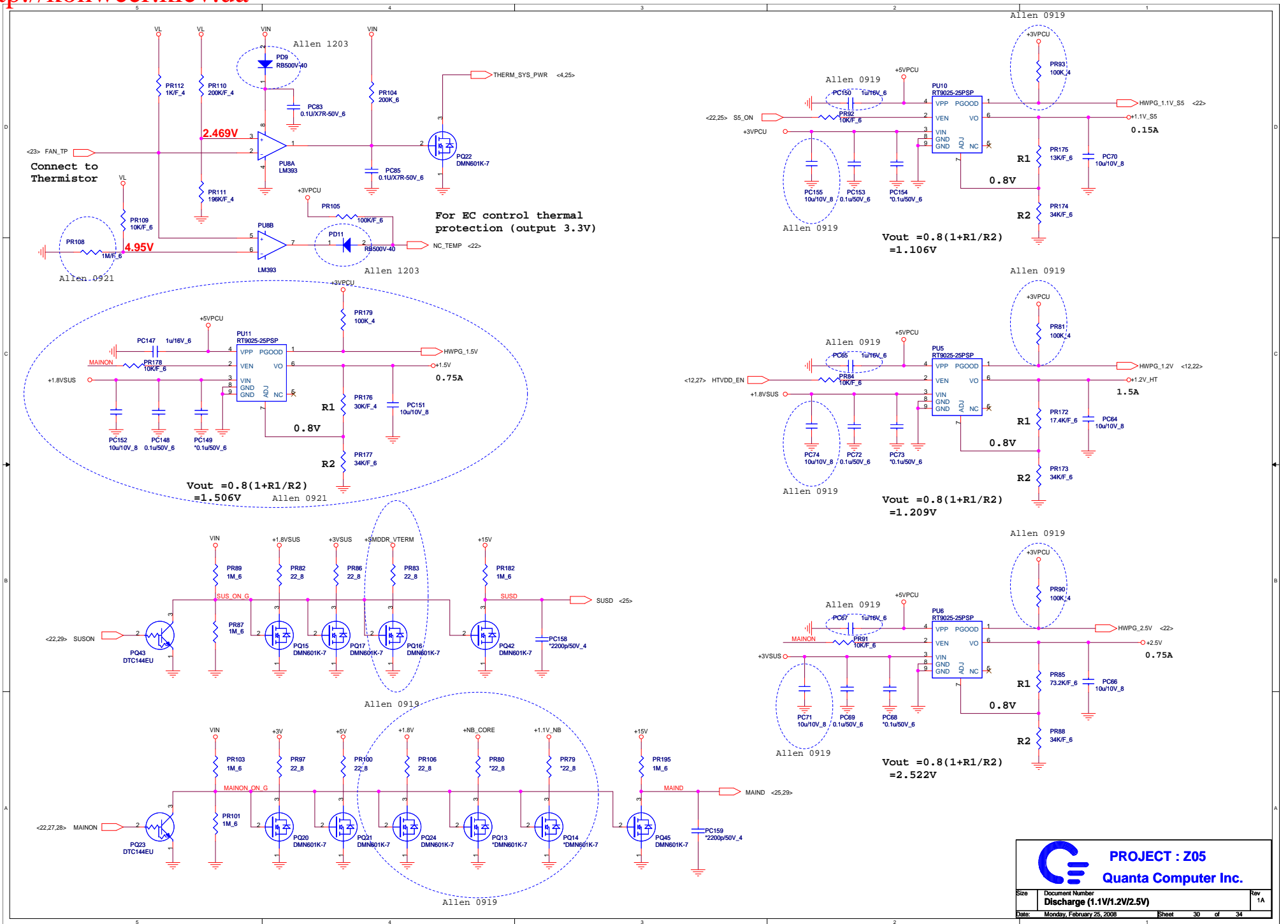
$$12m * 6 = RILIM * 20uA$$

$$RILIM = 3.6K (2.5 \sim 8K)$$

$$Rds * OCP = RILIM * 20uA$$

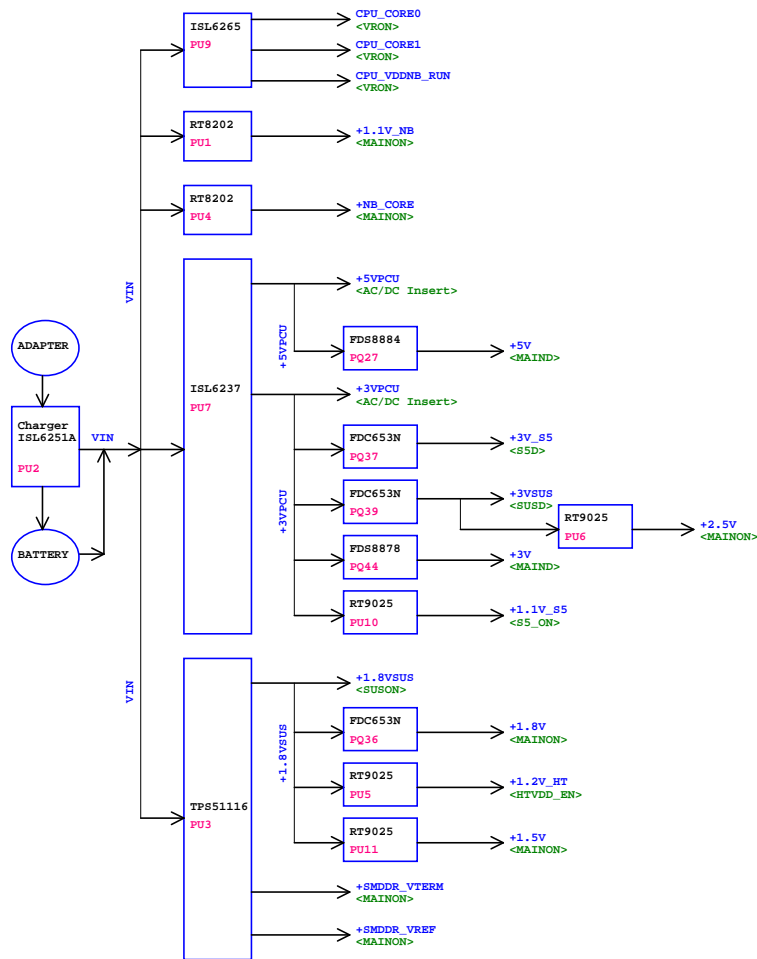
$$VOUT = (1 + R1/R2) * 0.75$$

| | | | |
|---|---------------------------|----------------------|----------|
|  | | PROJECT : Z05 | |
| | | Quanta Computer Inc. | |
| Size | Document Number | Rev | |
| | NB_VCC (RT8202) | 1A | |
| Date: | Monday, February 25, 2008 | Sheet | 28 of 34 |



PROJECT : Z05
Quanta Computer Inc.

| | | |
|-------|-----------------------------------|----------------|
| Size | Document Number | Rev |
| | Discharge (1.1V/1.2V/2.5V) | 1A |
| Date: | Monday, February 25, 2008 | Sheet 30 of 34 |



1. +1.1V_S5MCP77M Power(+1.1V_DUAL)
2. +5VPCUPower IC VCC, USB PORT POWER(S3 control)
3. +5VAudio, FAN, Touch pad, SATA HDD, ODD, CRT
4. +3V_S5MCP77M, New Card, LAN Power
5. +3VPCUKBC WPCE755C,SPI ROM, LED, LID Switch, Fingerprint Module
6. +3VSUSBluetooth, Mini Card, MDC
7. +3VCPU Thermal Sense, MCP77M, System Memory, LCD Panel, PC Camera, Mini card, New Card, Audio, Codec, Card Reader, KBC WPCE775C, LED
8. +2.5VCPU VDDA
9. +3V_LANLAN Power(BCM5764M)
10. +1.2V_LANLAN Power(BCM5764M)
11. +2.5V_LANLAN Power(BCM5787M)
12. +1.5VMini Card, New Card
13. +1.8VSUSCPU VDD I/O, System Memory
14. SMDDR_VTEMCPU Memory Interface , SYSTEM DDR DIMM Memory Termination
15. +1.8VMCP77M LCD Interface
16. +1.1V_NBMCP77M (HT Interface, PCI-E Interface, I/O Power, SATA Interface)
17. +NB_COREMCP77M Core Power
18. +1.2V_HTCPU HT Power
19. CPU_CORE0 CPU Power
20. CPU_CORE1 CPU Power
21. CPU_VDDNB_RUNCPU NB Power
- 22.