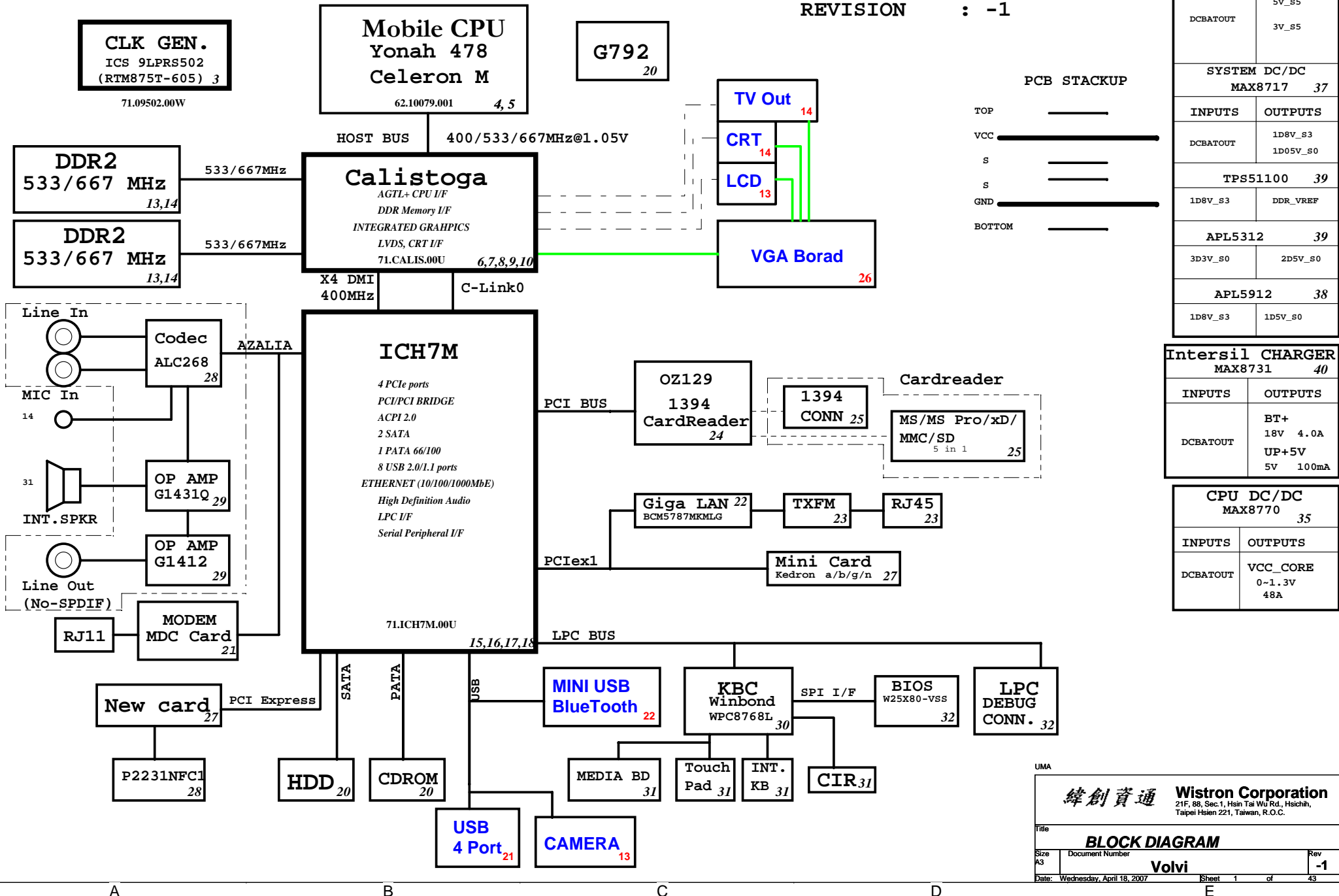


# Volvi Block Diagram

Project code: 91.4U701.001  
PCB P/N : 07200  
REVISION : -1



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Title: **BLOCK DIAGRAM**

Size: A3 Document Number: **Volvi** Rev: **-1**

Date: Wednesday, April 18, 2007 Sheet 1 of 43

ICH7M Konfunctional Strap Definitions ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:Offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting PWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Devoice 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high, the security measures will be in effect.This should only be used in manufacturing environments.

ICH7M Integrated Pull-up and Pull-down Resistors ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration Crestline EDS 20954 1.0 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWROK in signal.

History

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

PCI Routing

	IDSEL	INT	REQ	GNT
OZ129	AD22	INT_PIRQ#	PCI_REQ#0	PCI_GNT#0

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Title

**Reference**

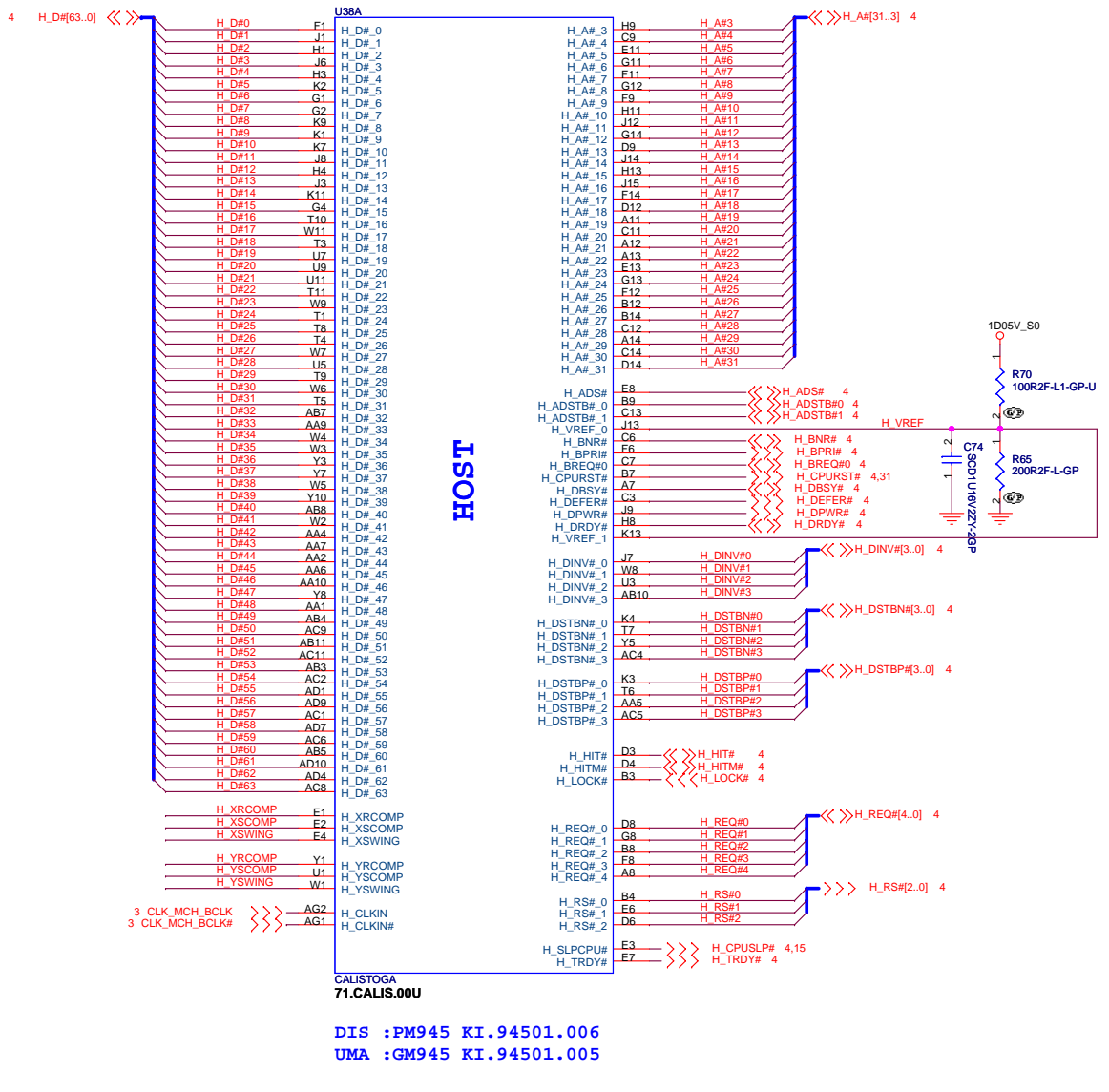
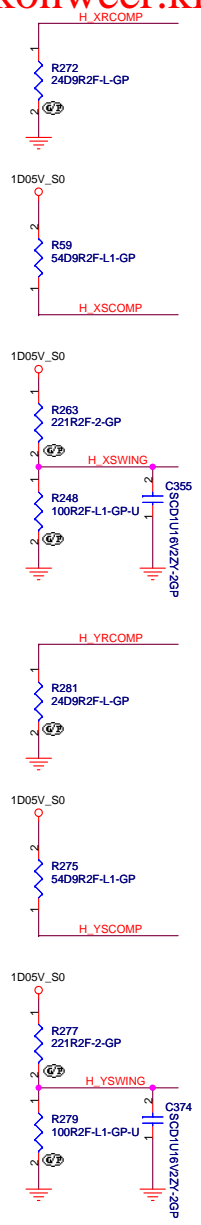
Size A3 Document Number **Volvi** Rev **-1**

Date: Wednesday, April 18, 2007 Sheet 2 of 42







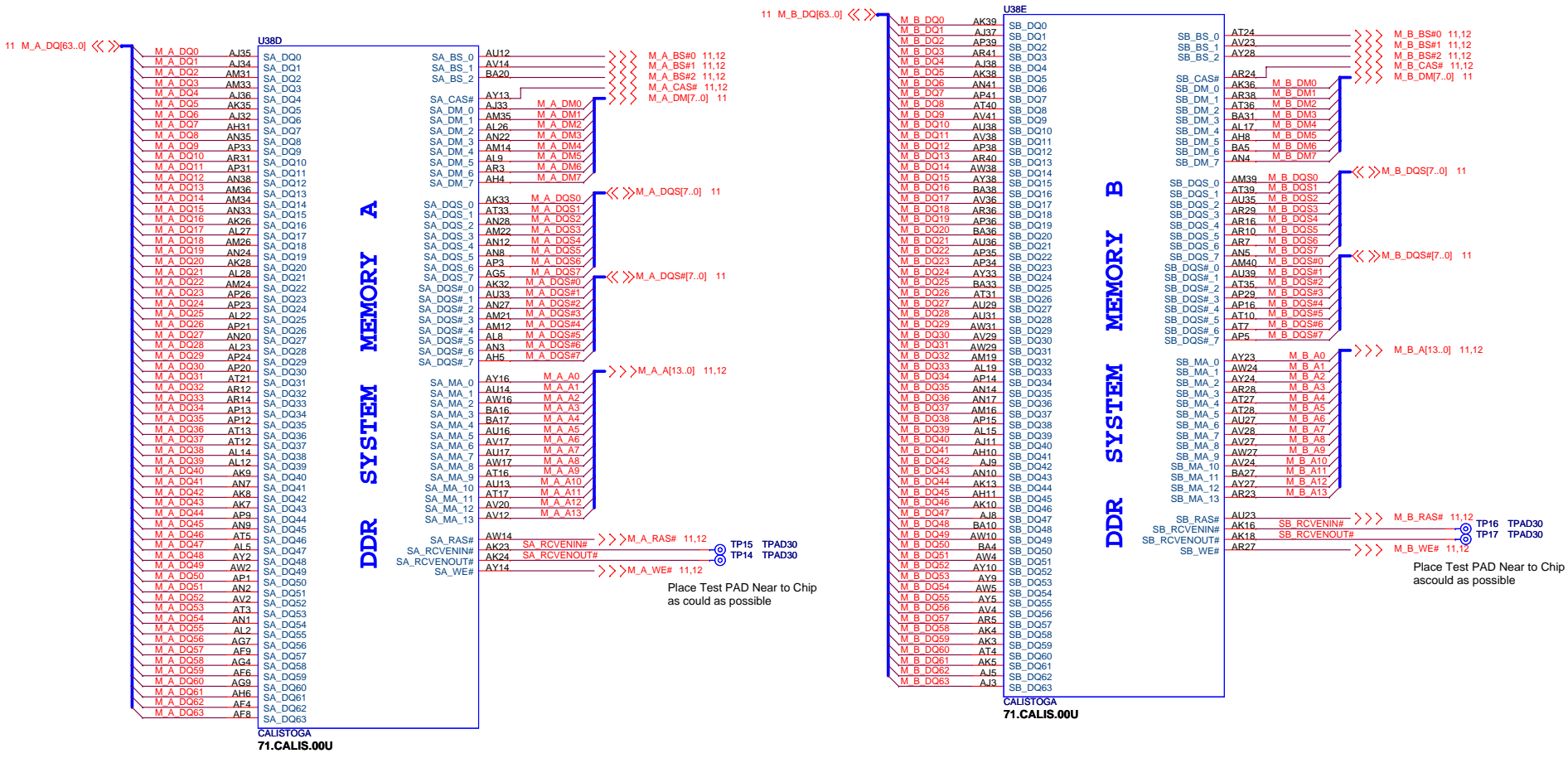


Place them near to the chip (< 0.5")

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Title			
<b>GMCH (1 of 5)</b>			
Size	Document Number		Rev
			-1
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Title: **GMCH (3 of 5)**

Size: Document Number: Rev: -1

Date: Wednesday, April 18, 2007 Sheet 8 of 42

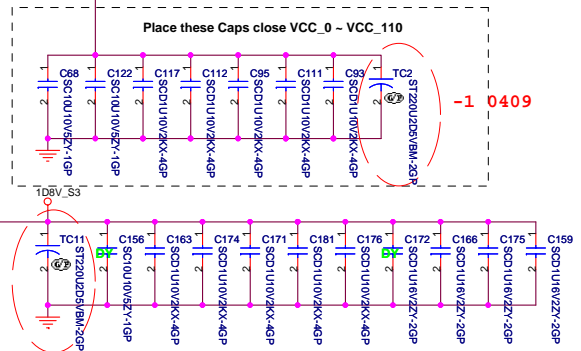


W33	VCC_1
P33	VCC_2
N33	VCC_3
L33	VCC_4
Y32	VCC_5
W32	VCC_6
P32	VCC_7
N32	VCC_8
L32	VCC_9
Y31	VCC_10
W31	VCC_11
P31	VCC_12
N31	VCC_13
L31	VCC_14
Y30	VCC_15
W30	VCC_16
P30	VCC_17
N30	VCC_18
L30	VCC_19
Y29	VCC_20
W29	VCC_21
P29	VCC_22
N29	VCC_23
L29	VCC_24
Y28	VCC_25
W28	VCC_26
P28	VCC_27
N28	VCC_28
L28	VCC_29
Y27	VCC_30
W27	VCC_31
P27	VCC_32
N27	VCC_33
L27	VCC_34
Y26	VCC_35
W26	VCC_36
P26	VCC_37
N26	VCC_38
L26	VCC_39
Y25	VCC_40
W25	VCC_41
P25	VCC_42
N25	VCC_43
L25	VCC_44
Y24	VCC_45
W24	VCC_46
P24	VCC_47
N24	VCC_48
L24	VCC_49
Y23	VCC_50
W23	VCC_51
P23	VCC_52
N23	VCC_53
L23	VCC_54
Y22	VCC_55
W22	VCC_56
P22	VCC_57
N22	VCC_58
L22	VCC_59
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W21	VCC_61
P21	VCC_62
N21	VCC_63
L21	VCC_64
Y20	VCC_65
W20	VCC_66
P20	VCC_67
N20	VCC_68
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Y19	VCC_70
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Y16	VCC_85
W16	VCC_86
P16	VCC_87
N16	VCC_88
L16	VCC_89
Y15	VCC_90
W15	VCC_91
P15	VCC_92
N15	VCC_93
L15	VCC_94
Y14	VCC_95
W14	VCC_96
P14	VCC_97
N14	VCC_98
L14	VCC_99
Y13	VCC_100
W13	VCC_101
P13	VCC_102
N13	VCC_103
L13	VCC_104
Y12	VCC_105
W12	VCC_106
P12	VCC_107
N12	VCC_108
L12	VCC_109
Y11	VCC_110

AD27	VCC_NCTF0
AC27	VCC_NCTF1
AB27	VCC_NCTF2
AA27	VCC_NCTF3
Y27	VCC_NCTF4
W27	VCC_NCTF5
V27	VCC_NCTF6
U27	VCC_NCTF7
T27	VCC_NCTF8
R27	VCC_NCTF9
Q27	VCC_NCTF10
P27	VCC_NCTF11
O27	VCC_NCTF12
N27	VCC_NCTF13
M27	VCC_NCTF14
L27	VCC_NCTF15
K27	VCC_NCTF16
J27	VCC_NCTF17
I27	VCC_NCTF18
H27	VCC_NCTF19
G27	VCC_NCTF20
F27	VCC_NCTF21
E27	VCC_NCTF22
D27	VCC_NCTF23
C27	VCC_NCTF24
B27	VCC_NCTF25
A27	VCC_NCTF26
Z27	VCC_NCTF27
Y27	VCC_NCTF28
X27	VCC_NCTF29
W27	VCC_NCTF30
V27	VCC_NCTF31
U27	VCC_NCTF32
T27	VCC_NCTF33
S27	VCC_NCTF34
R27	VCC_NCTF35
Q27	VCC_NCTF36
P27	VCC_NCTF37
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L27	VCC_NCTF41
K27	VCC_NCTF42
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I27	VCC_NCTF44
H27	VCC_NCTF45
G27	VCC_NCTF46
F27	VCC_NCTF47
E27	VCC_NCTF48
D27	VCC_NCTF49
C27	VCC_NCTF50
B27	VCC_NCTF51
A27	VCC_NCTF52
Z27	VCC_NCTF53
Y27	VCC_NCTF54
X27	VCC_NCTF55
W27	VCC_NCTF56
V27	VCC_NCTF57

AC41	VSS_0
AA41	VSS_1
Y41	VSS_2
W41	VSS_3
V41	VSS_4
U41	VSS_5
T41	VSS_6
S41	VSS_7
R41	VSS_8
Q41	VSS_9
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D41	VSS_22
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U41	VSS_83
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M41	VSS_91
L41	VSS_92
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J41	VSS_94
I41	VSS_95
H41	VSS_96

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AG34	VSS_181
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AE34	VSS_183
AD34	VSS_184
AC34	VSS_185
AB34	VSS_186
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Y34	VSS_188
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V34	VSS_190
U34	VSS_191
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R34	VSS_194
Q34	VSS_195
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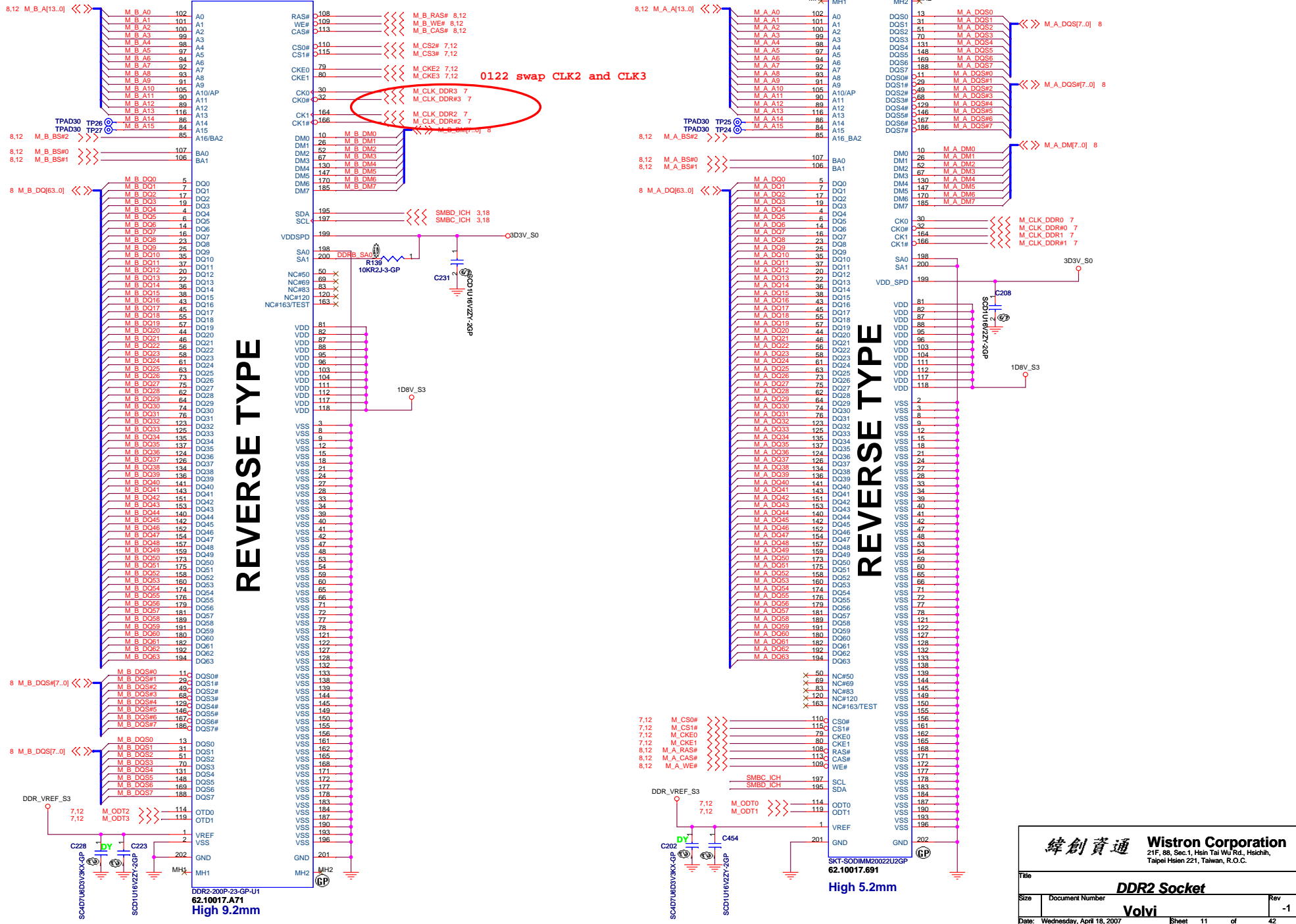


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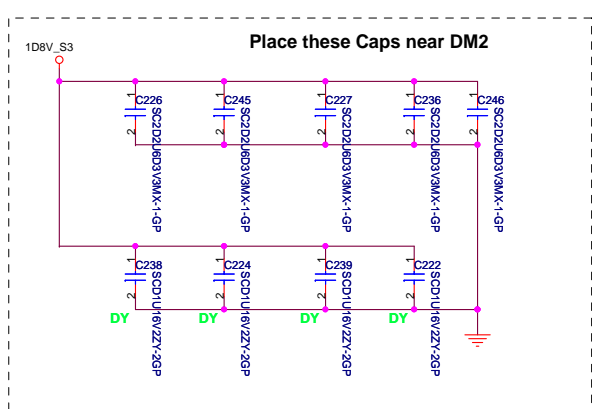
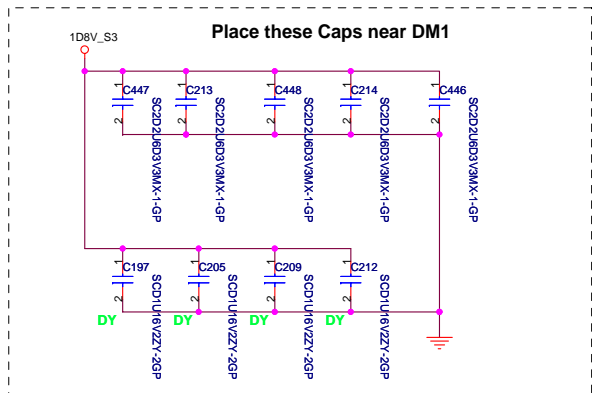
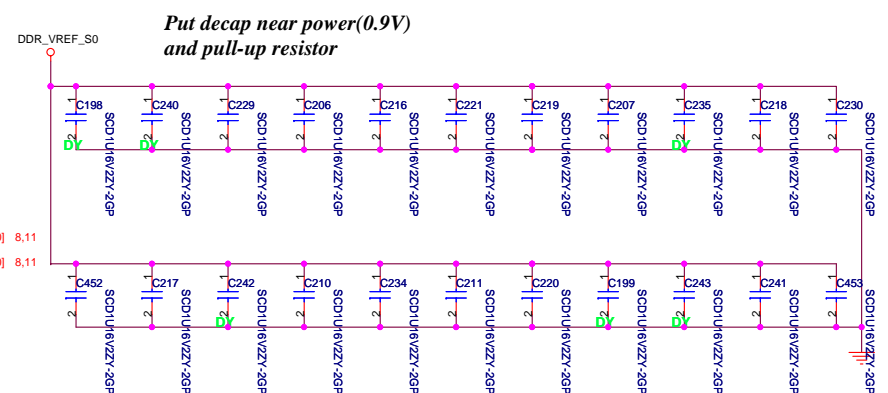
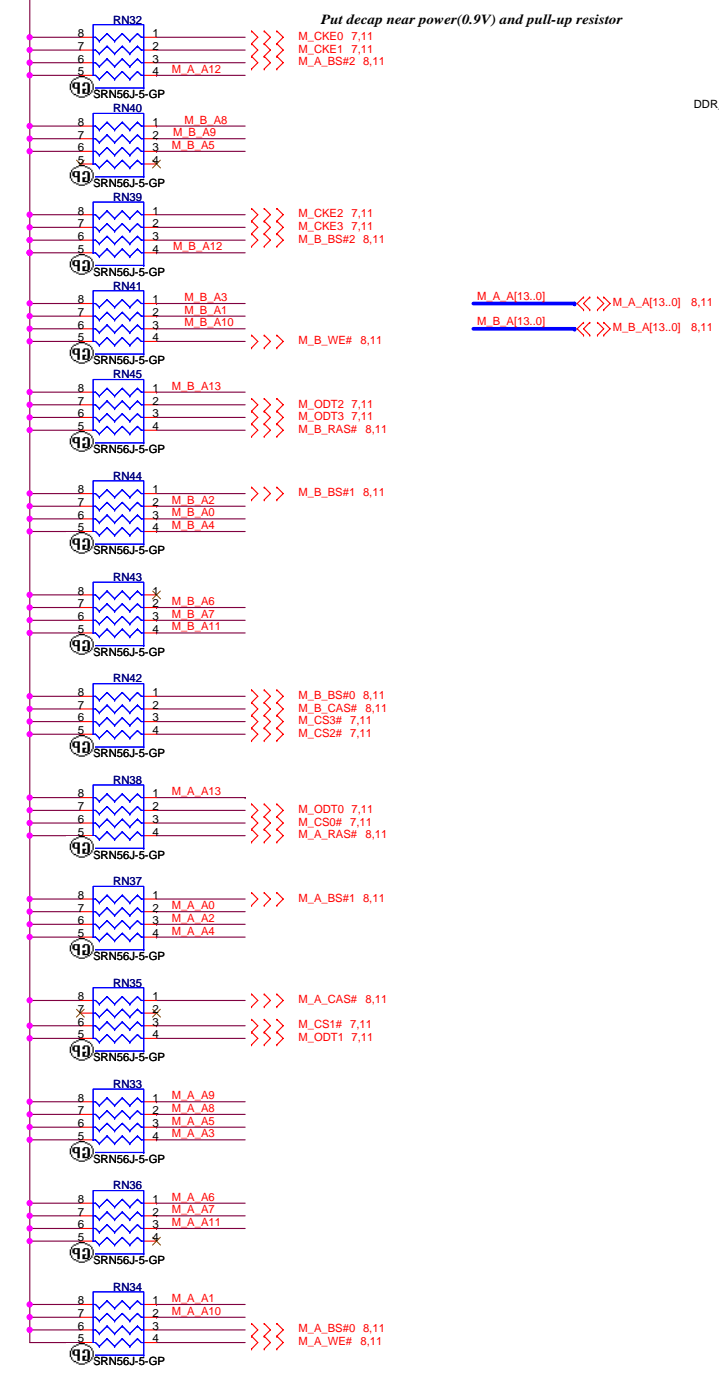
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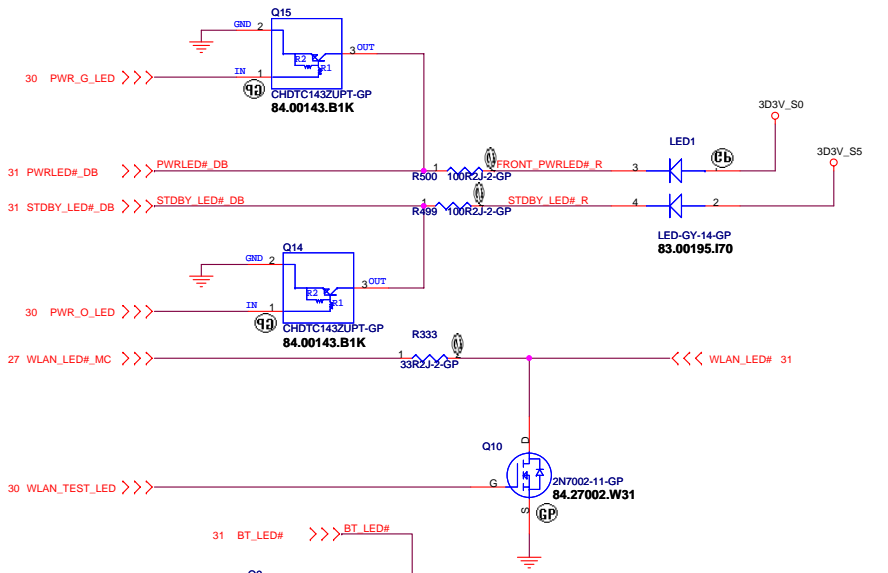
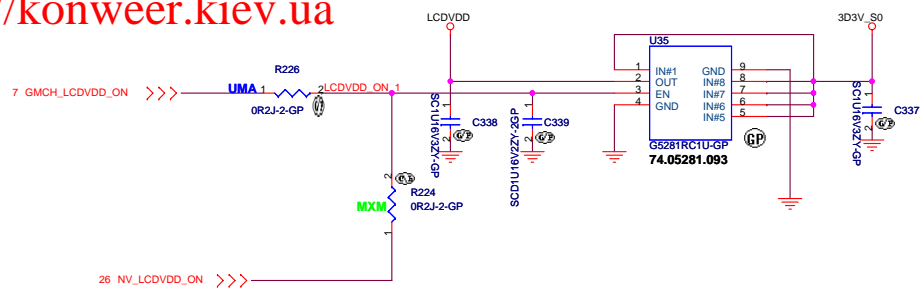
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Title		<b>DDR2 Socket</b>	
Size	Document Number	Rev	
		<b>Volvi</b>	
Date: Wednesday, April 18, 2007	Sheet	11	of 42

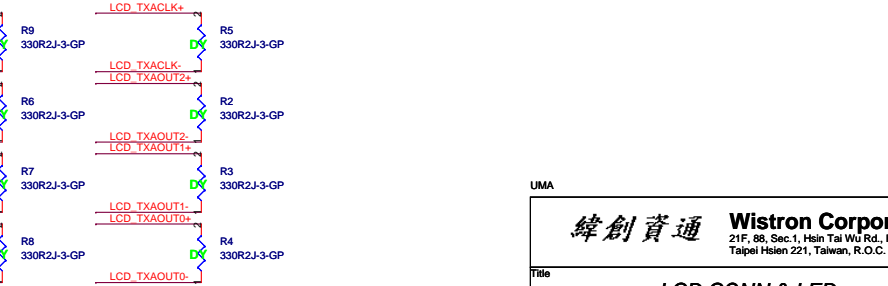
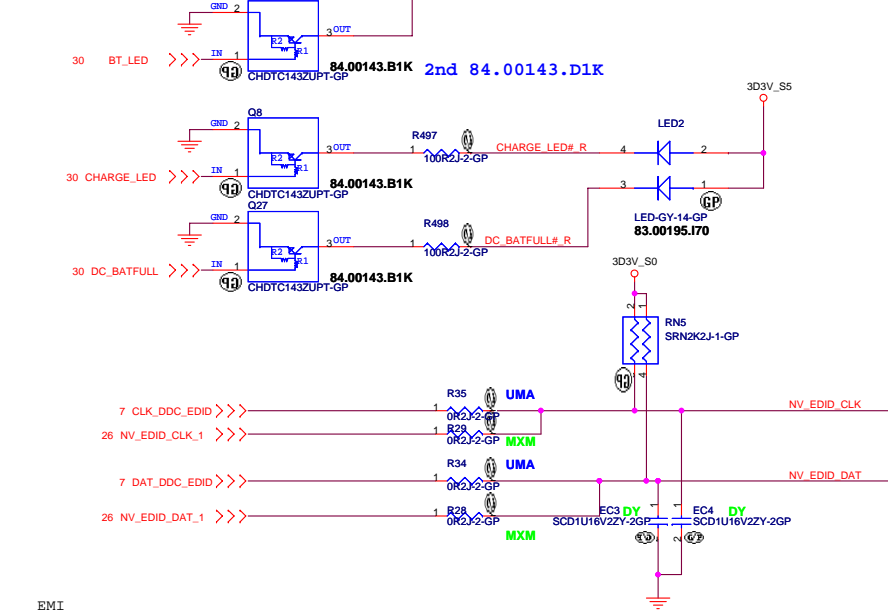
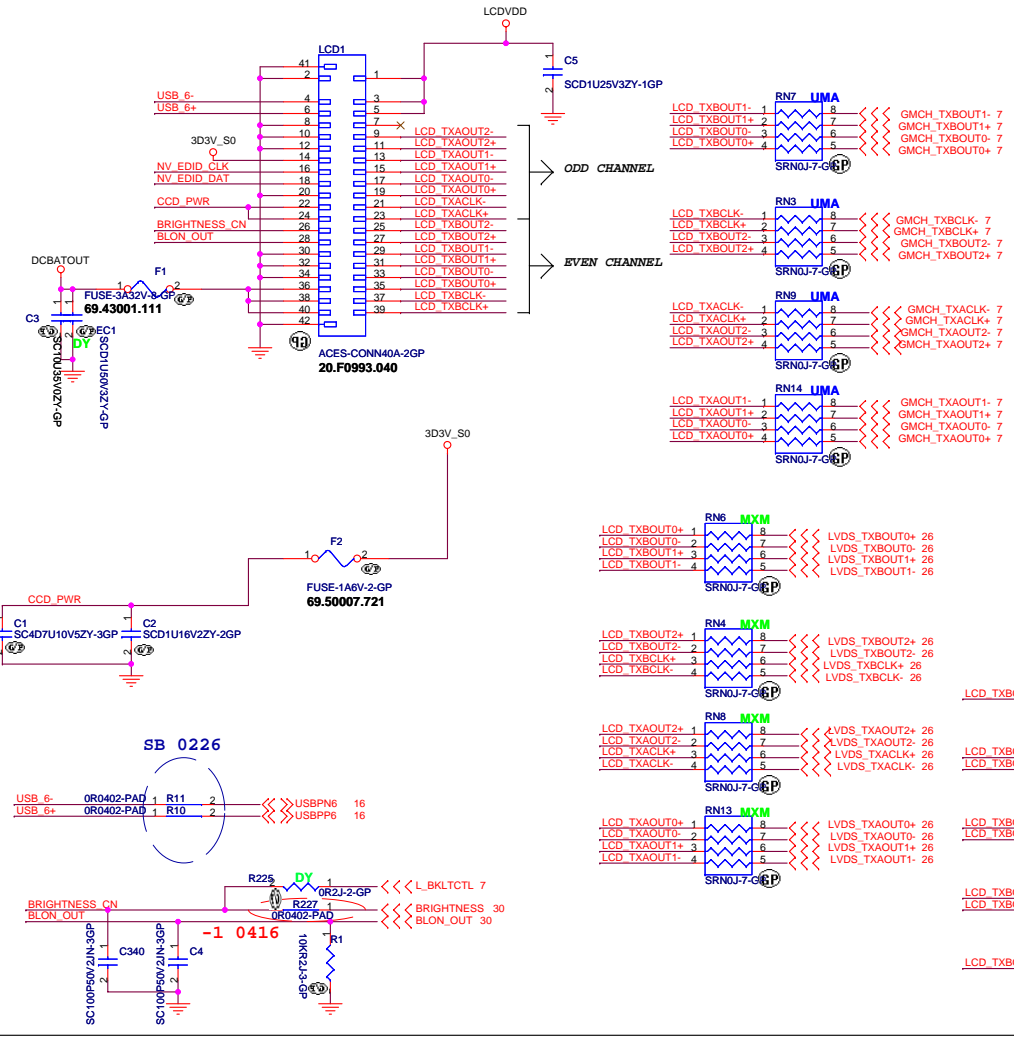


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Title		<b>DDR2 Termination Resistor</b>	
Size	Document Number	<b>Volvi</b>	Rev -1
Date: Wednesday, April 18, 2007	Sheet 12	of	42



### LCD/INVERTER CONN



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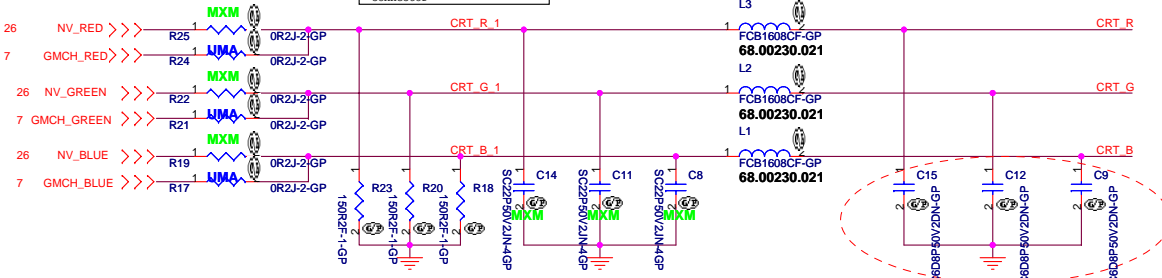
Title: **LCD CONN & LED**

Size: Document Number: **Volvi** Rev: **-1**

Date: Wednesday, April 18, 2007 Sheet 13 of 42

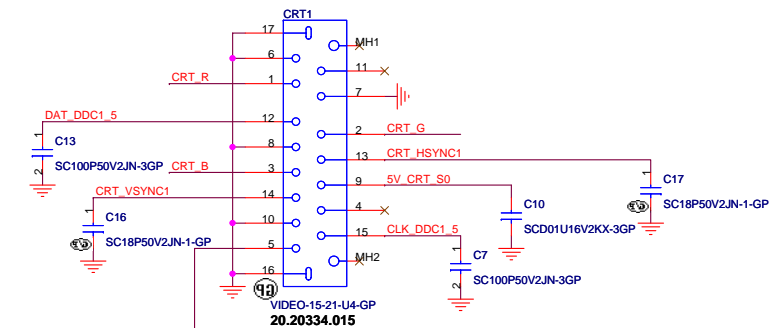
Layout Note:  
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

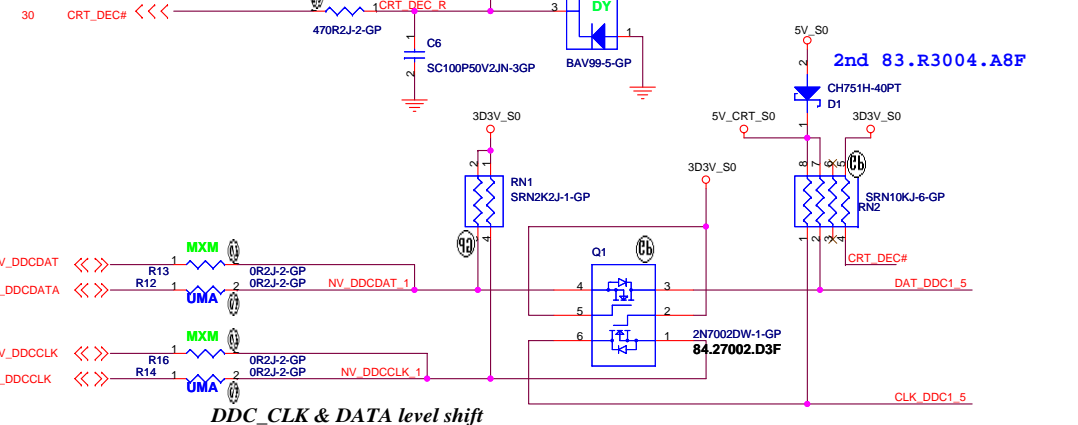
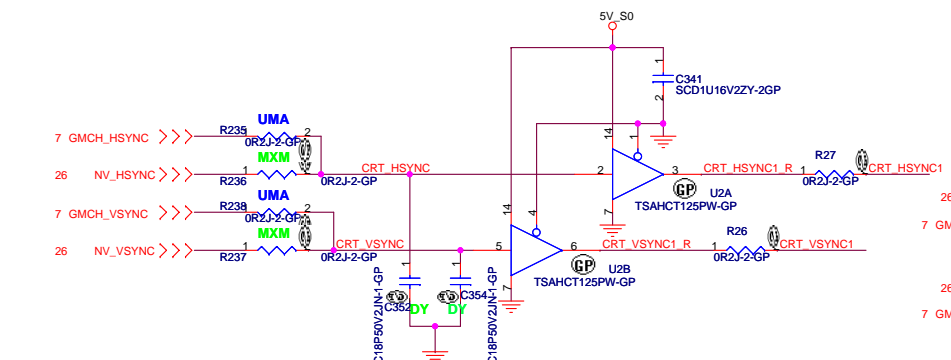


Layout Note:  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

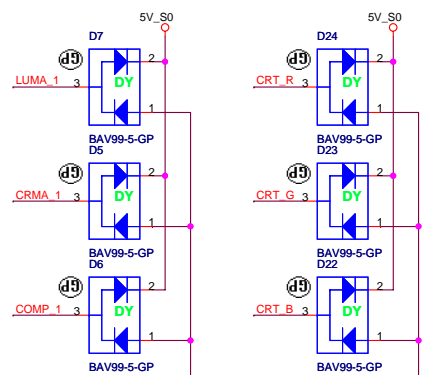
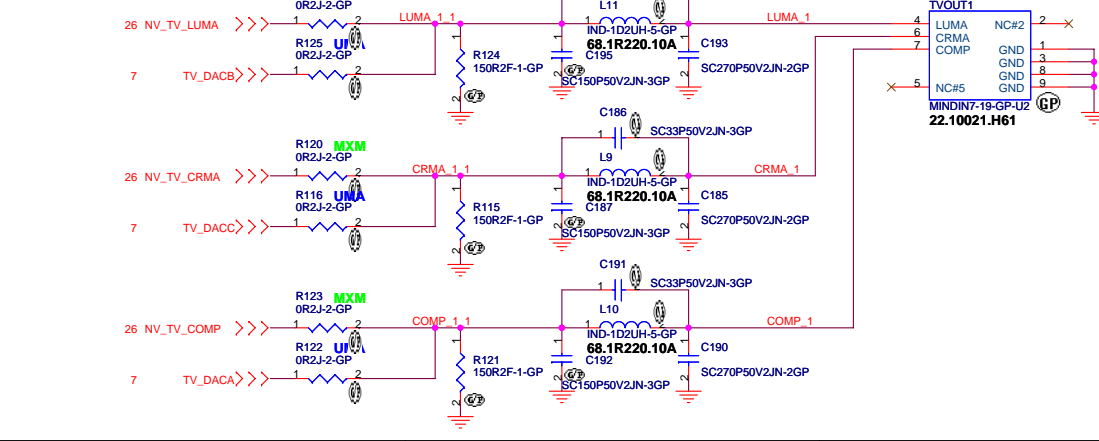
C15 to 18P  
C12 to 27P  
C9 to 27P  
For ATI MXM M66M R,G,B



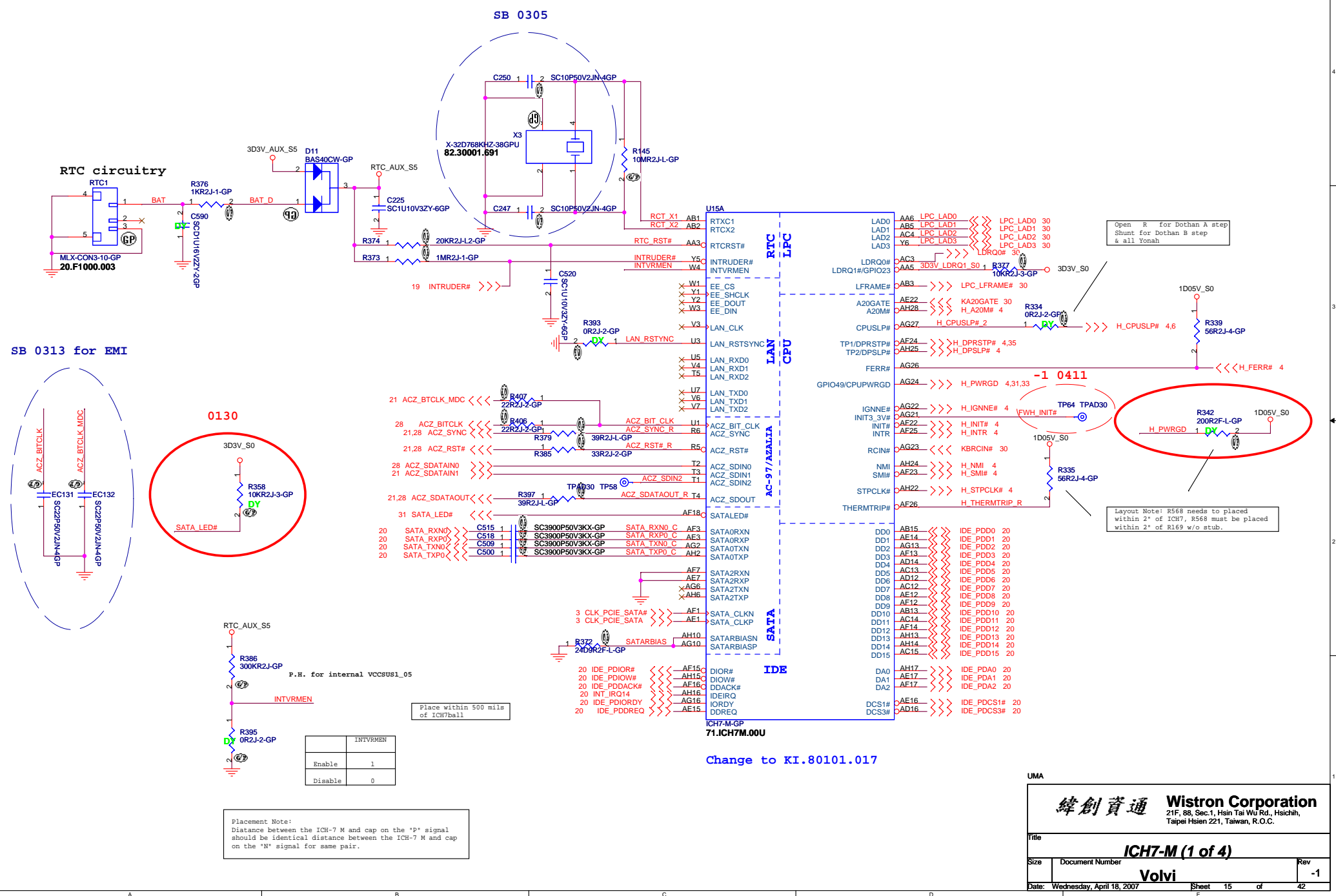
### Hsync & Vsync level shift



### TV CONN



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Title: <b>CRT/TV Connector</b>	
Size: Document Number	Rev: -1
Date: Wednesday, April 18, 2007	
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Open R for Dothan A step  
Shunt for Dothan B step  
& all Yonah.

Layout Note: R568 needs to be placed  
within 2" of ICH7, R568 must be placed  
within 2" of R169 w/o stub.

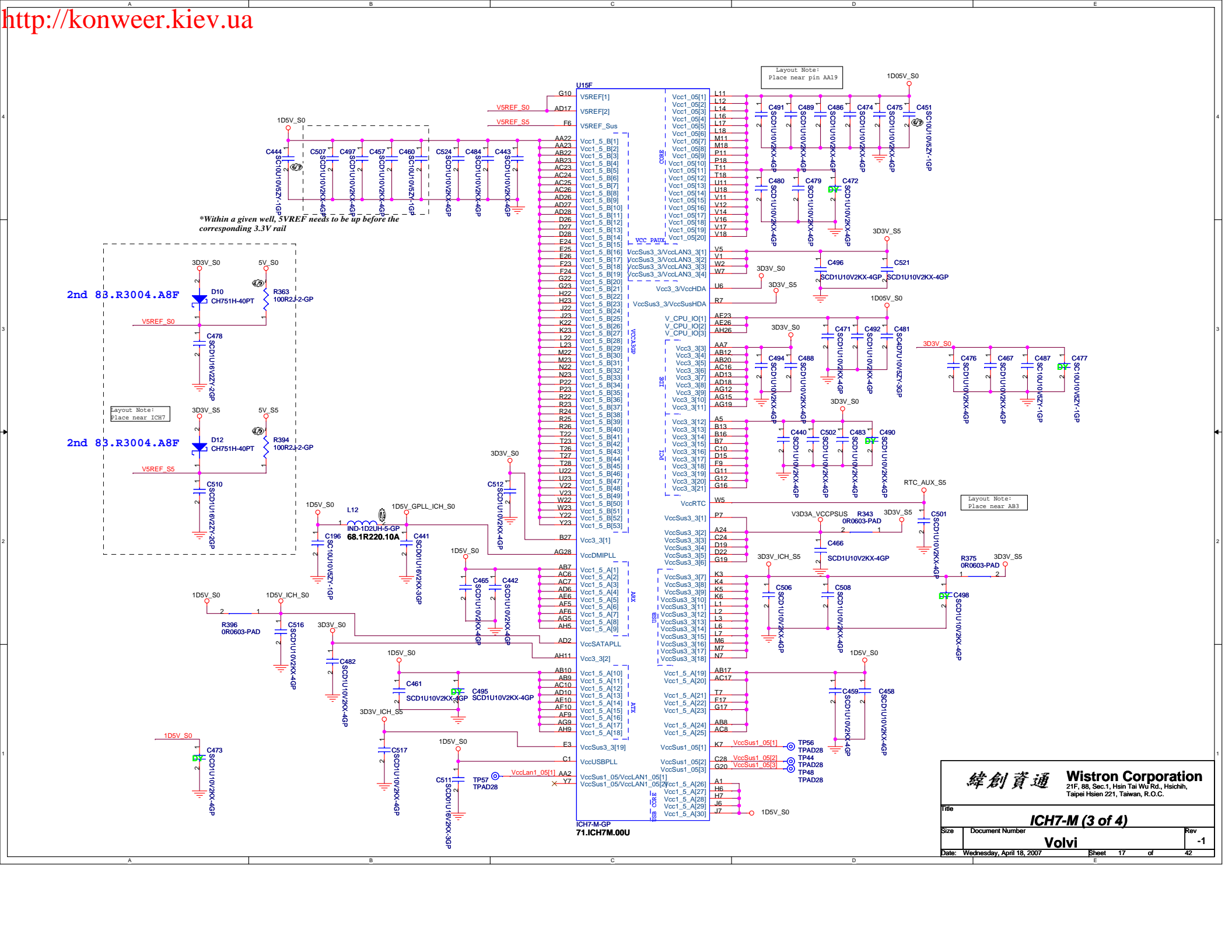
Place within 500 mils  
of ICH7ball1

Placement Note:  
Distance between the ICH-7 M and cap on the 'P' signal  
should be identical distance between the ICH-7 M and cap  
on the 'N' signal for same pair.

	INTVRMEN
Enable	1
Disable	0

LAD0	AA6_LPC_LAD0	LPC_LAD0	30
LAD1	AA5_LPC_LAD1	LPC_LAD1	30
LAD2	AA4_LPC_LAD2	LPC_LAD2	30
LAD3	Y6_LPC_LAD3	LPC_LAD3	30
LDRQ0#	AC3	LDRQ0#	30
LDRQ1#/GPIO23	AA5_3D3V_LDRQ1_S0	R377	10KR2J-3-GP
LFRAME#	AB3	LPC_LFRAME#	30
A20GATE	AE22	KA20GATE	30
CPUSLP#	AG27	H_CPUSLP#	2
TP1/DPRSTP#	AE24	H_DPRSTP#	4,35
TP2/DPSLP#	AH25	H_DPSLP#	4
FERR#	AG26	H_FERR#	4
GPIO49/CPUPWRGD	AG24	H_PWRGD	4,31,33
IGNNE#	AG22	H_IGNNE#	4
INIT3_3V#	AG21	FWH_INIT#	TP64 TPAD30
INTR#	AE22	H_INTR#	4
RCIN#	AG23	KBCRCIN#	30
NMI	AH24	H_NMI	4
SMI#	AE23	H_SMI#	4
STPCLK#	AH22	H_STPCLK#	4
THERMTRIP#	AE26	H_THERMTRIP	R
DD0	AB15	IDE_PDD0	20
DD1	AE14	IDE_PDD1	20
DD2	AG13	IDE_PDD2	20
DD3	AE13	IDE_PDD3	20
DD4	AD14	IDE_PDD4	20
DD5	AC13	IDE_PDD5	20
DD6	AD12	IDE_PDD6	20
DD7	AC12	IDE_PDD7	20
DD8	AE12	IDE_PDD8	20
DD9	AE12	IDE_PDD9	20
DD10	AB13	IDE_PDD10	20
DD11	AC14	IDE_PDD11	20
DD12	AE14	IDE_PDD12	20
DD13	AH13	IDE_PDD13	20
DD14	AH14	IDE_PDD14	20
DD15	AC15	IDE_PDD15	20
DA0	AH17	IDE_PDA0	20
DA1	AE17	IDE_PDA1	20
DA2	AE17	IDE_PDA2	20
DCS1#	AE16	IDE_PDCS1#	20
DCS3#	AD16	IDE_PDCS3#	20





\*Within a given well, SVREF needs to be up before the corresponding 3.3V rail

Layout Note:  
Place near ICH7

Layout Note:  
Place near AB3

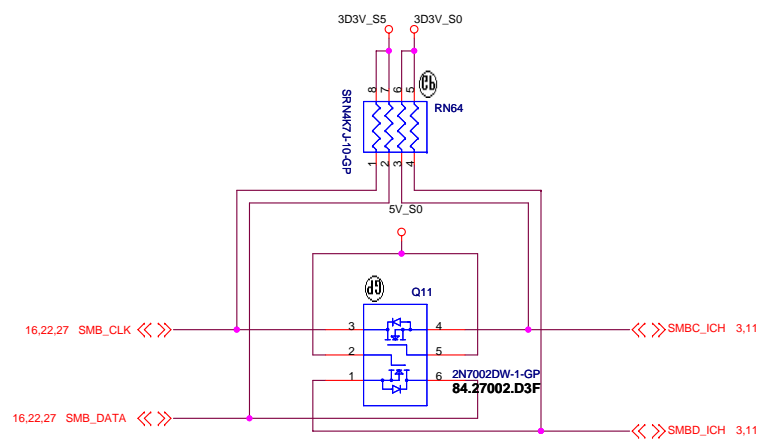
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Title		
<b>ICH7-M (3 of 4)</b>		
Size	Document Number	Rev
		-1
Date: Wednesday, April 18, 2007		Sheet 17 of 42

**Volvi**

U15E			
A4	VSS[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
E11	VSS[5]	VSS[102]	R13
R14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B28	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T15
D18	VSS[16]	VSS[113]	T16
D21	VSS[17]	VSS[114]	T17
D24	VSS[18]	VSS[115]	U4
E1	VSS[19]	VSS[116]	U12
E2	VSS[20]	VSS[117]	U13
E4	VSS[21]	VSS[118]	U14
E8	VSS[22]	VSS[119]	U15
E16	VSS[23]	VSS[120]	U16
F3	VSS[24]	VSS[121]	U17
F4	VSS[25]	VSS[122]	U24
F5	VSS[26]	VSS[123]	U25
F12	VSS[27]	VSS[124]	U26
F27	VSS[28]	VSS[125]	V2
F28	VSS[29]	VSS[126]	V13
G1	VSS[30]	VSS[127]	V15
G2	VSS[31]	VSS[128]	V24
G5	VSS[32]	VSS[129]	V27
G6	VSS[33]	VSS[130]	V28
G9	VSS[34]	VSS[131]	W6
G14	VSS[35]	VSS[132]	W24
G18	VSS[36]	VSS[133]	W25
G21	VSS[37]	VSS[134]	W26
G24	VSS[38]	VSS[135]	Y3
G25	VSS[39]	VSS[136]	Y24
G26	VSS[40]	VSS[137]	Y27
H3	VSS[41]	VSS[138]	Y28
H4	VSS[42]	VSS[139]	AA1
H5	VSS[43]	VSS[140]	AA24
H24	VSS[44]	VSS[141]	AA25
H27	VSS[45]	VSS[142]	AA26
H28	VSS[46]	VSS[143]	AB4
J1	VSS[47]	VSS[144]	AB6
J6	VSS[48]	VSS[145]	AB11
J24	VSS[49]	VSS[146]	AB14
J25	VSS[51]	VSS[148]	AB16
J26	VSS[52]	VSS[149]	AB19
K24	VSS[53]	VSS[150]	AB21
K27	VSS[54]	VSS[151]	AB24
K28	VSS[55]	VSS[152]	AB27
L13	VSS[56]	VSS[153]	AB28
L15	VSS[57]	VSS[154]	AC2
L24	VSS[58]	VSS[155]	AC5
L25	VSS[59]	VSS[156]	AC9
L26	VSS[60]	VSS[157]	AC11
M3	VSS[61]	VSS[158]	AD1
M4	VSS[62]	VSS[159]	AD3
M5	VSS[63]	VSS[160]	AD4
M12	VSS[64]	VSS[161]	AD7
M13	VSS[65]	VSS[162]	AD8
M14	VSS[66]	VSS[163]	AD11
M15	VSS[67]	VSS[164]	AD15
M16	VSS[68]	VSS[165]	AD19
M17	VSS[69]	VSS[166]	AD23
M24	VSS[70]	VSS[167]	AE2
M27	VSS[71]	VSS[168]	AE4
M28	VSS[72]	VSS[169]	AE8
N1	VSS[73]	VSS[170]	AE11
N2	VSS[74]	VSS[171]	AE13
N5	VSS[75]	VSS[172]	AE18
N6	VSS[76]	VSS[173]	AE21
N11	VSS[77]	VSS[174]	AE24
N12	VSS[78]	VSS[175]	AE25
N13	VSS[79]	VSS[176]	AE2
N14	VSS[80]	VSS[177]	AE4
N15	VSS[81]	VSS[178]	AF8
N16	VSS[82]	VSS[179]	AF11
N17	VSS[83]	VSS[180]	AF27
N18	VSS[84]	VSS[181]	AF28
N24	VSS[85]	VSS[182]	AG1
N25	VSS[86]	VSS[183]	AG3
N26	VSS[87]	VSS[184]	AG7
P3	VSS[88]	VSS[185]	AG11
P4	VSS[89]	VSS[186]	AG14
P12	VSS[90]	VSS[187]	AG17
P13	VSS[91]	VSS[188]	AG20
P14	VSS[92]	VSS[189]	AG25
P15	VSS[93]	VSS[190]	AH1
P16	VSS[94]	VSS[191]	AH3
P17	VSS[95]	VSS[192]	AH7
P24	VSS[96]	VSS[193]	AH12
P27	VSS[97]	VSS[194]	AH23
			AH27

ICH7-M-GP  
71.ICH7M.00U



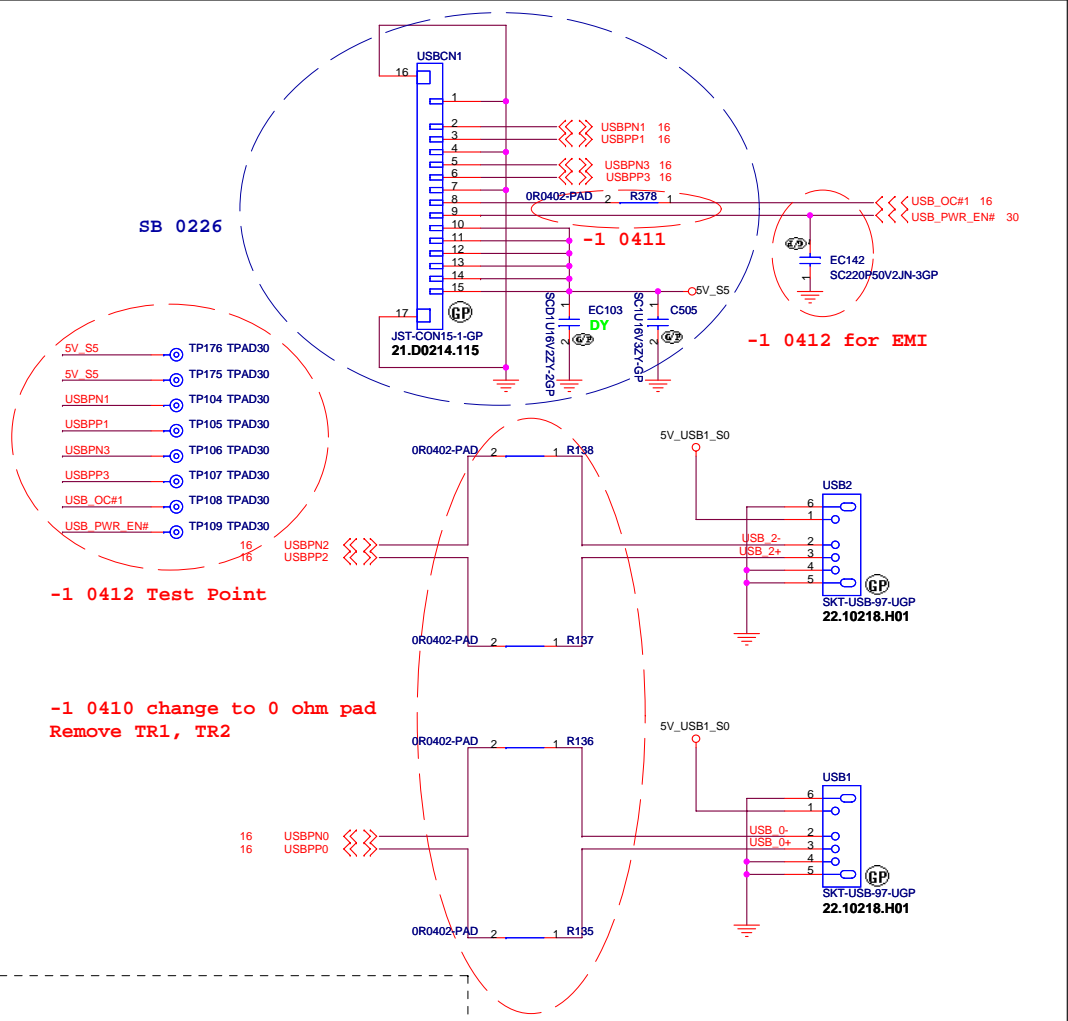
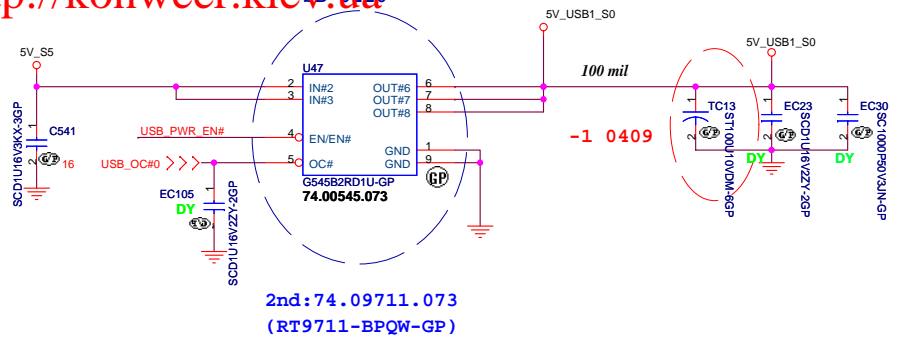
Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

**SMBUS**

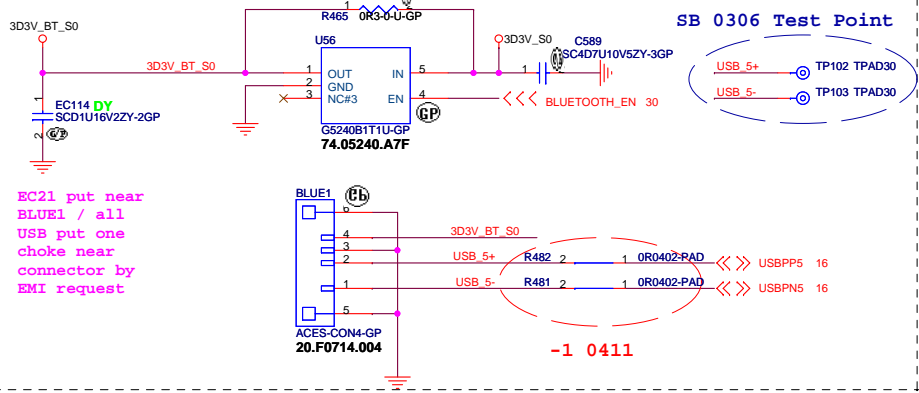
<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>ICH7-M (4 of 4)</b>			
Size	Document Number	Rev	-1
<b>Volvi</b>			
Date: Wednesday, April 18, 2007			
		Sheet	18 of 42



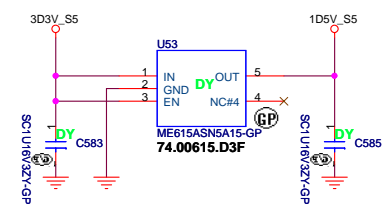
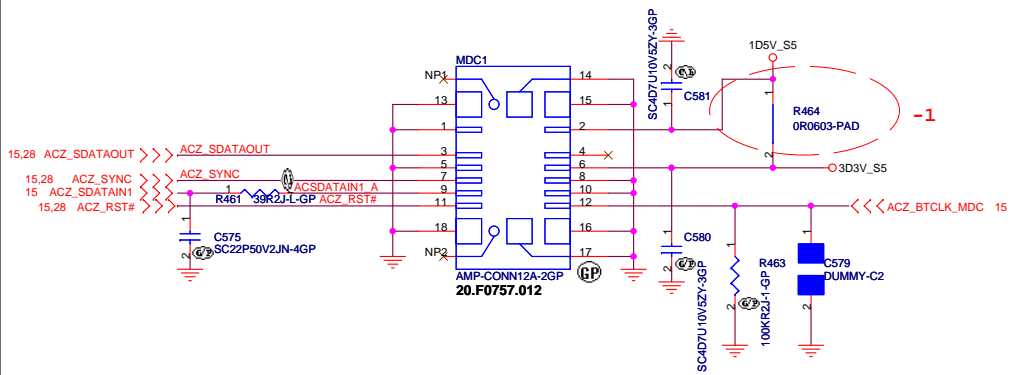


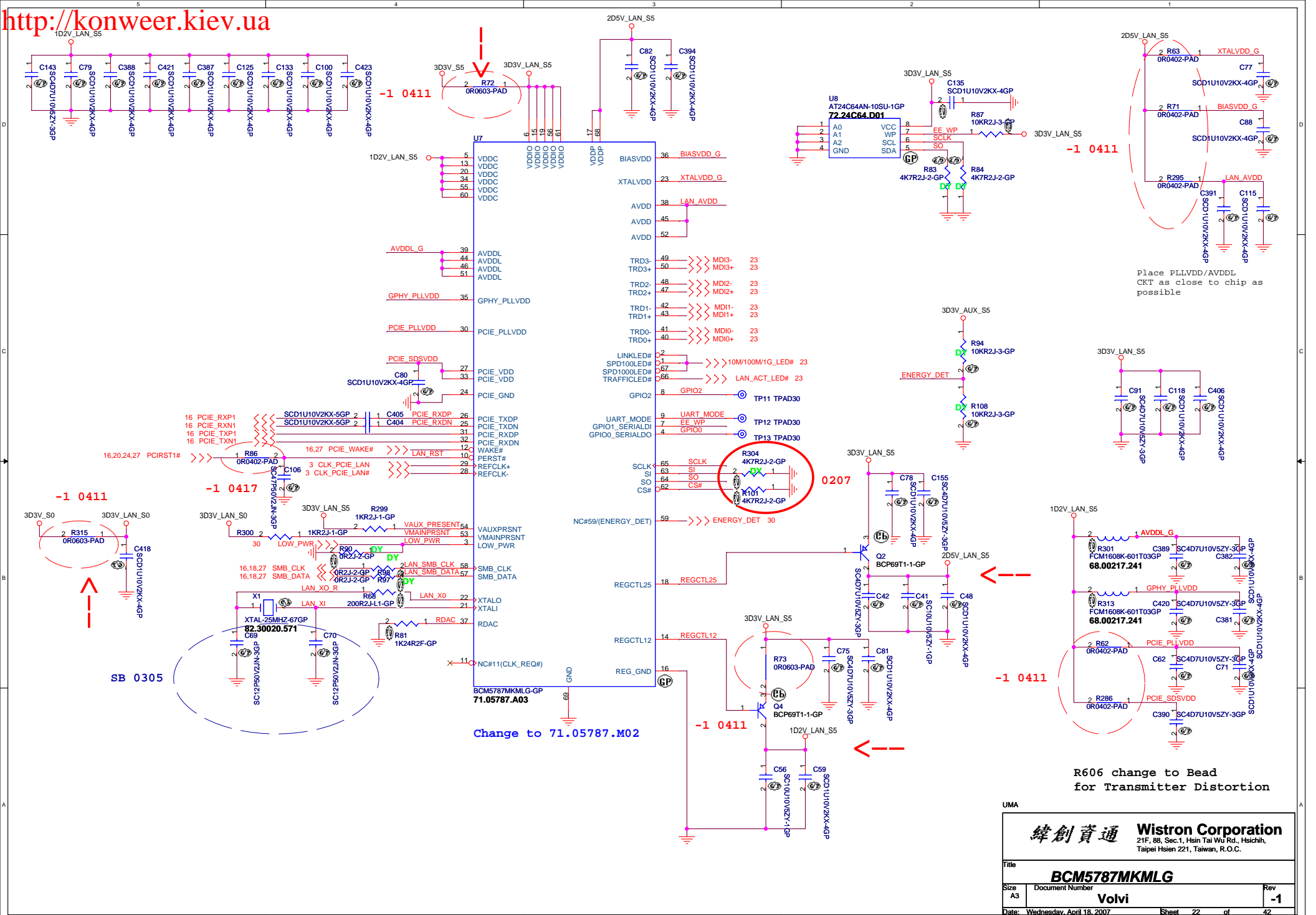


**BLUETOOTH MODULE**



**MDC 1.5 CONN**





Place PLLVDD/AVDDL CKT as close to the chip as possible

Change to 71.05787.M02

R606 change to Bead for Transmitter Distortion

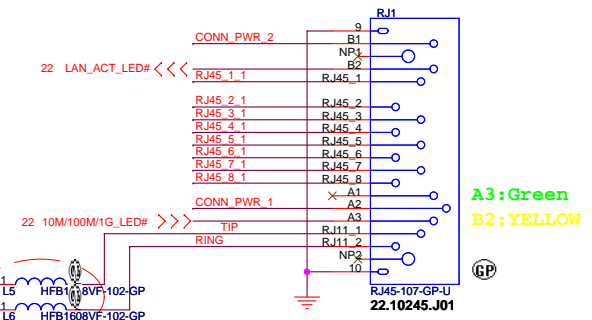
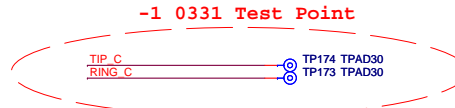
UMA

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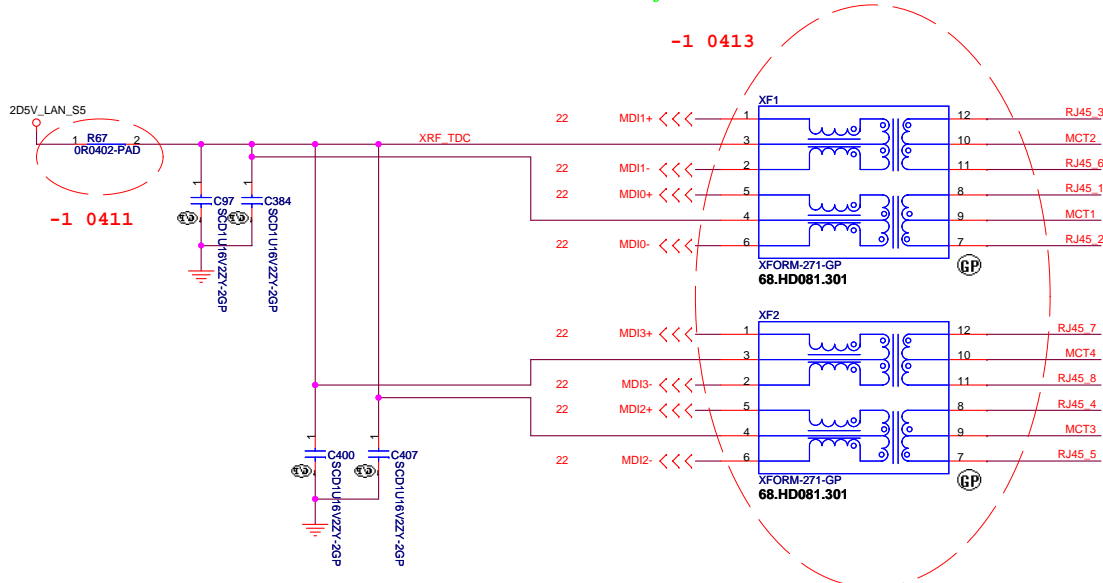
Title	<b>BCM5787MKMLG</b>	
Size	Document Number	Rev
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Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

# LAN Connector

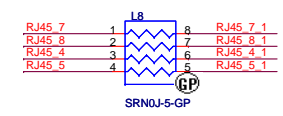
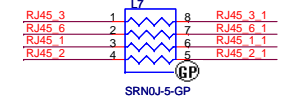


## GIGA Lan Transformer



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits  
 LAN Data: Yellow(B2), when LAN is transferring data.

### For EMI



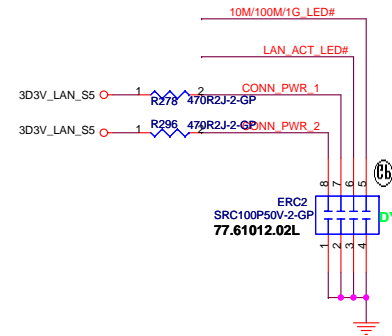
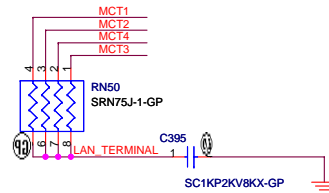
- 1.route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC\_TIP,DOC\_RING,TIP,RING:

W/S : 10/100 @ Surface layers  
 10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



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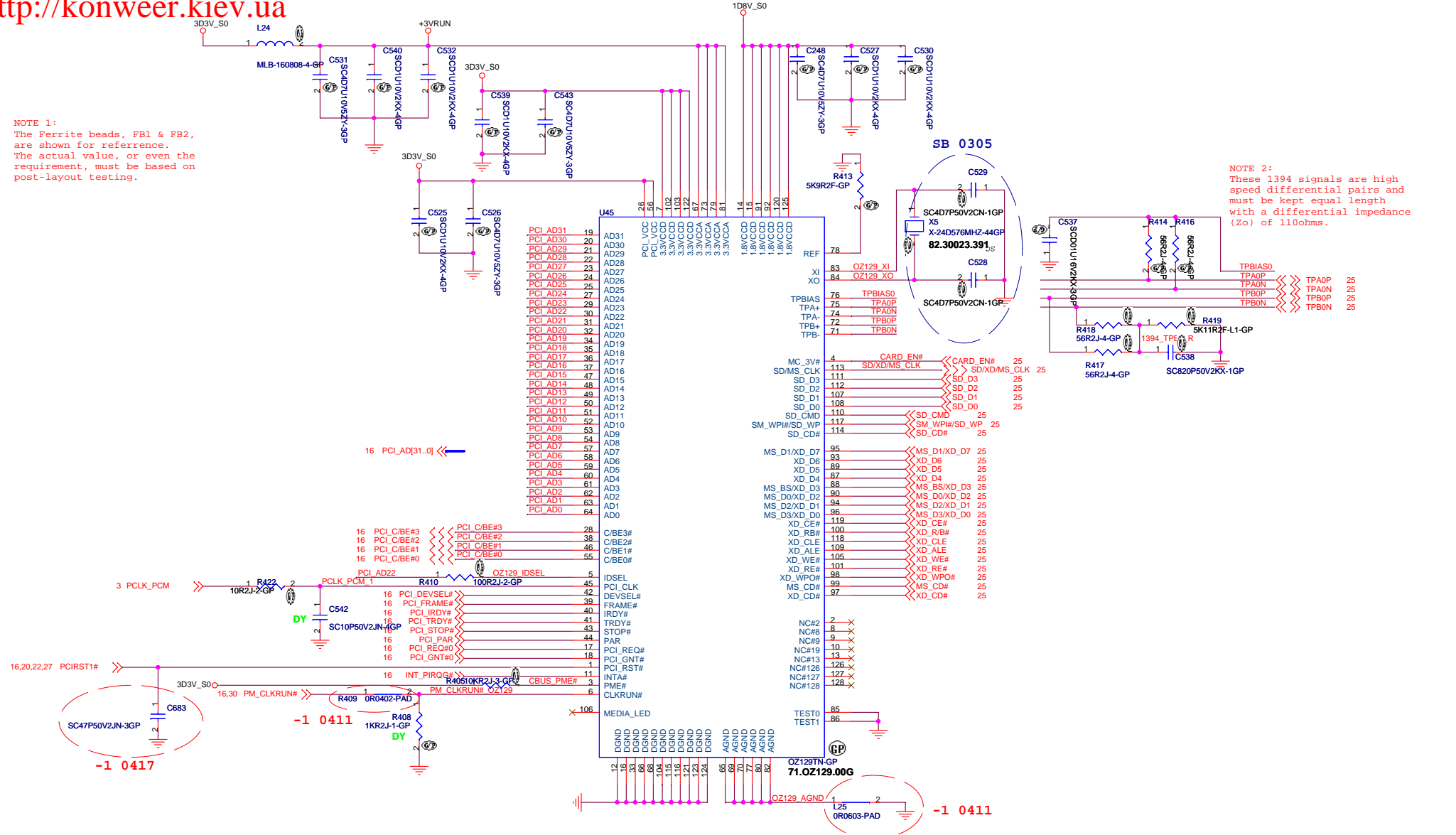
Title: **LAN Connector**

Size A3 Document Number **Volvi** Rev **-1**

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NOTE 1:  
The Ferrite beads, FB1 & FB2,  
are shown for reference.  
The actual value, or even the  
requirement, must be based on  
post-layout testing.

NOTE 2:  
These 1394 signals are high  
speed differential pairs and  
must be kept equal length  
with a differential impedance  
(Zo) of 110ohms.



IDSEL:AD22  
INTA-->:INT\_PIRQ#  
GNT:PCI\_GNT#0  
REQ:PCI\_REQ#0

UMA

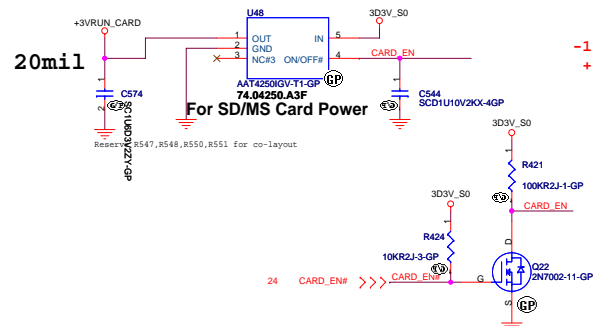
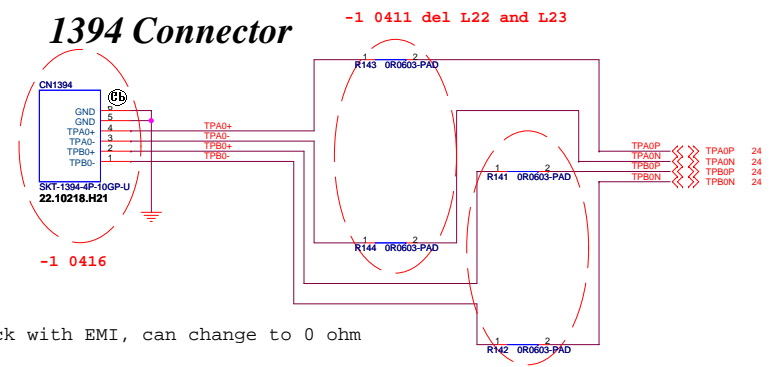
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **OZ129T**

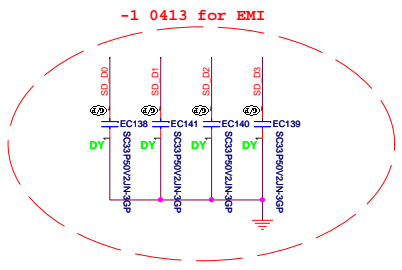
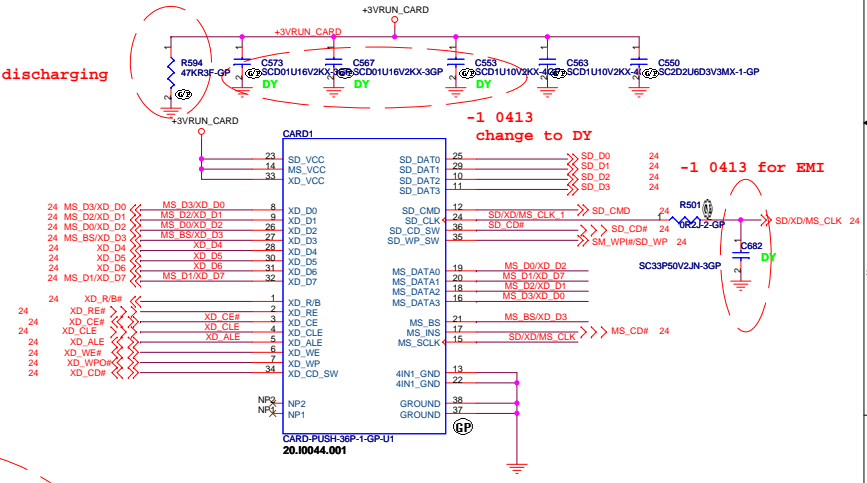
Size: Document Number: **Volvi** Rev: **-1**

Date: Wednesday, April 18, 2007 Sheet 24 of 42

### 1394 Connector



-1 0413  
+3VRUN\_CARD discharging



LIMA

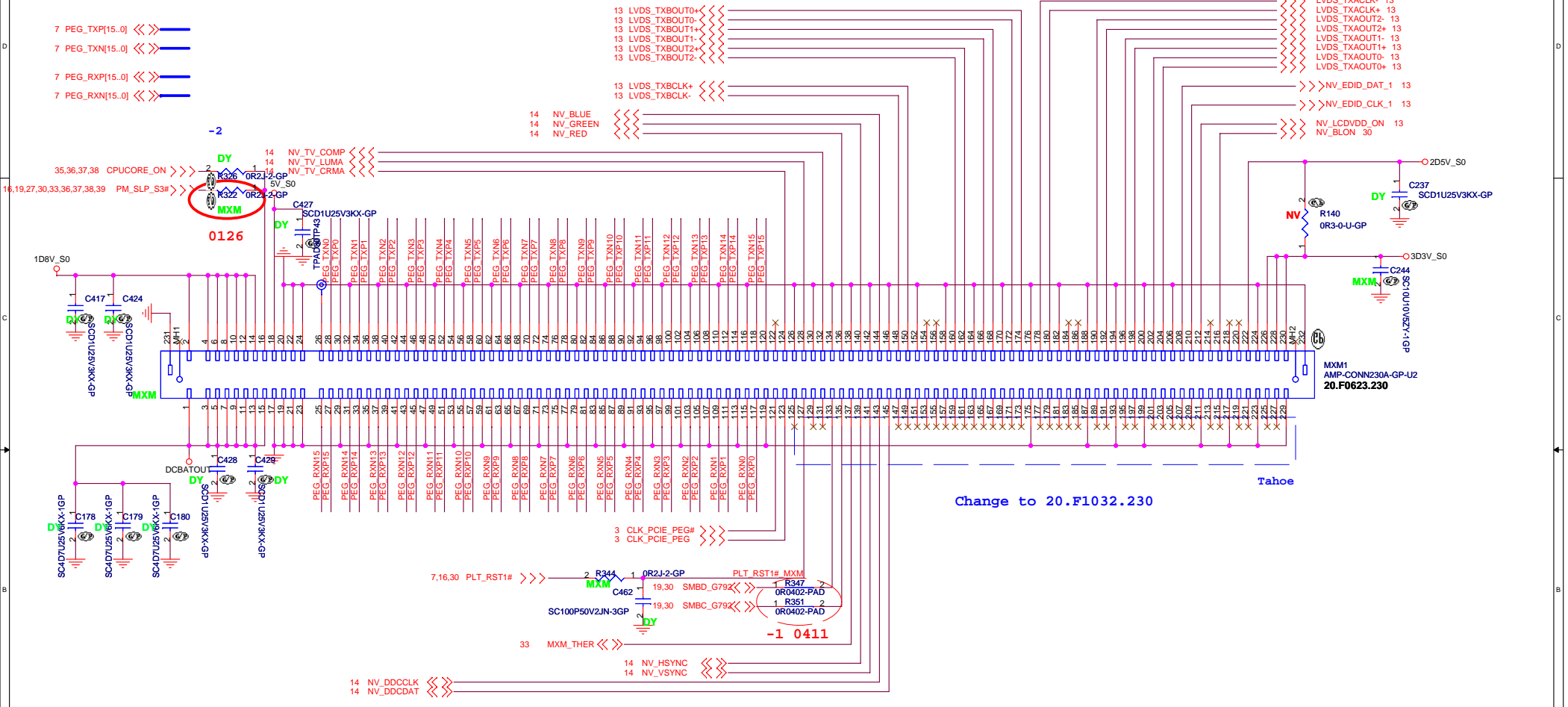
緯創資通 **Wistron Corporation**  
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Title: **1394 / CARD READER**

Size: Document Number: **Volvi** Rev: **-1**

Date: Wednesday, April 18, 2007 Sheet: 25 of 42

Put near graphic connector



Tahoe

Change to 20.F1032.230

UMA

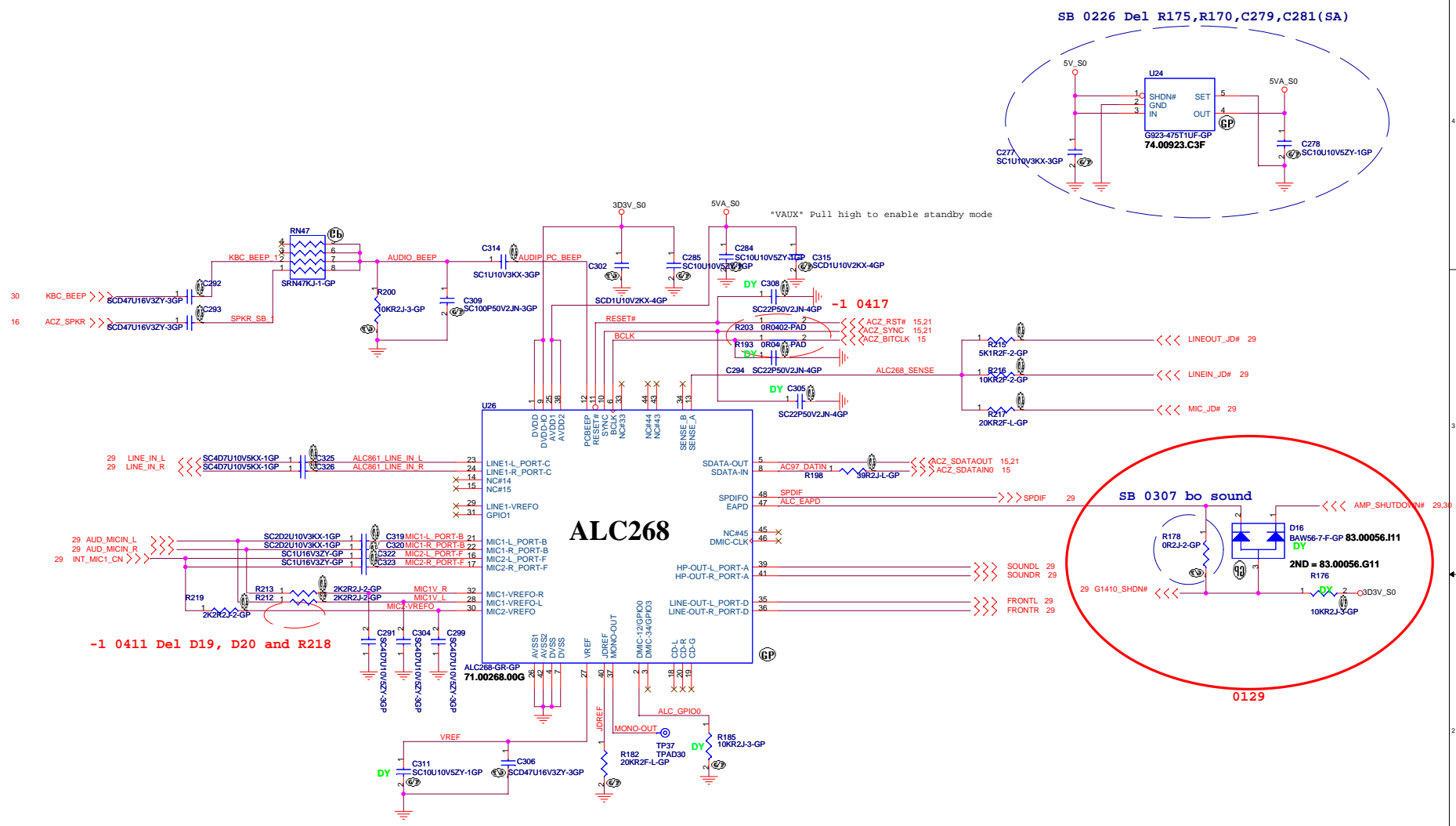
**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Graphic MXM CONN**

Size: A3 Document Number: **Volvi** Rev: -1

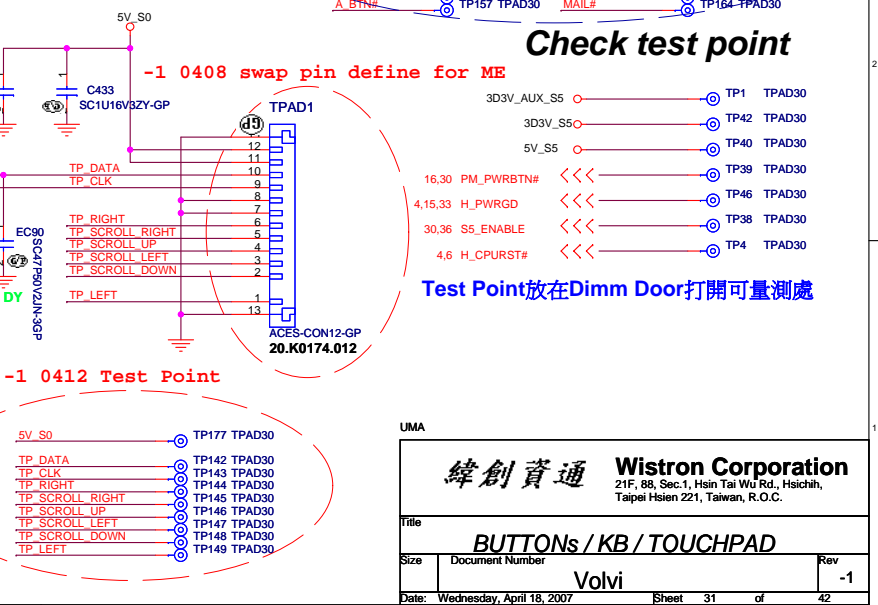
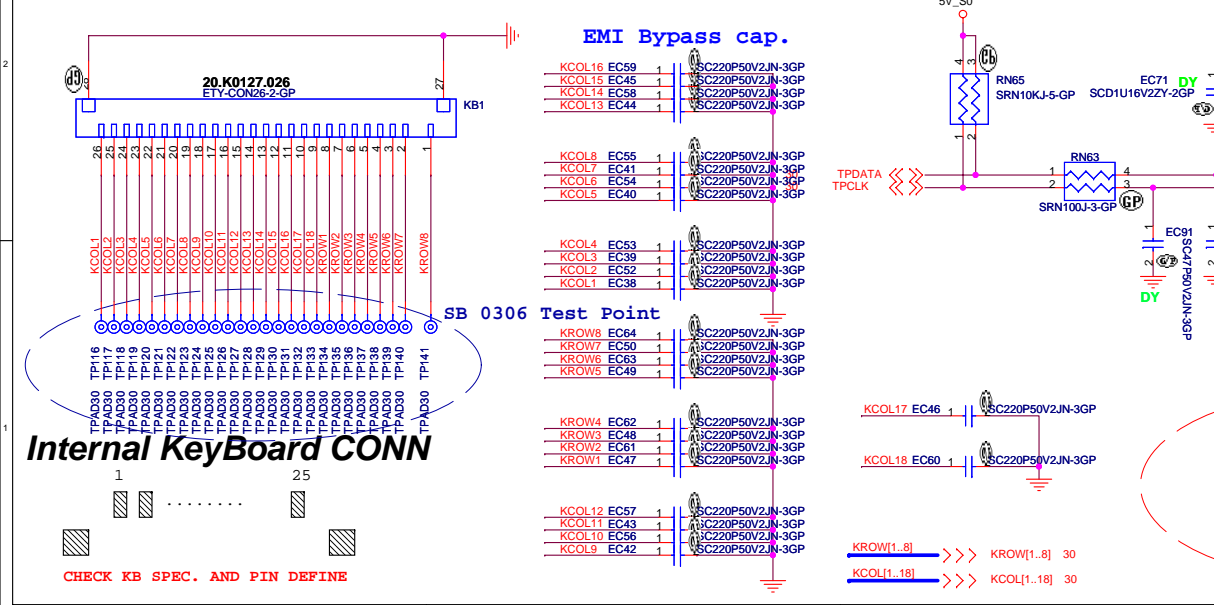
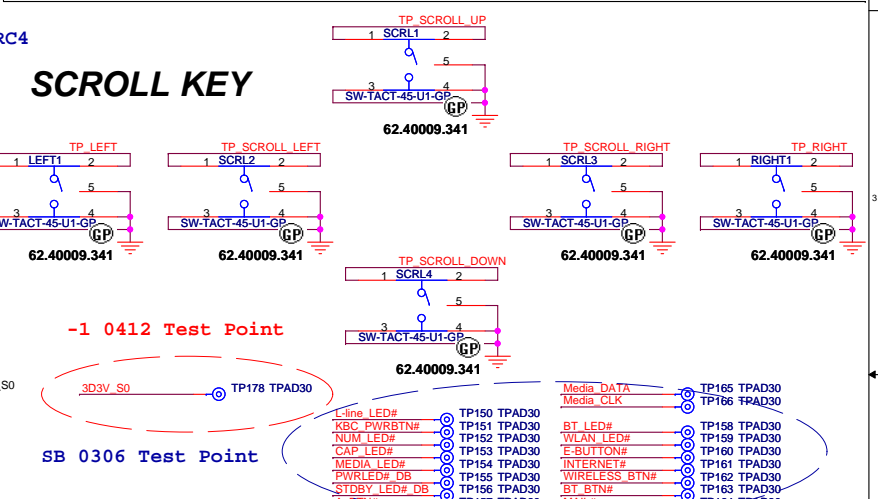
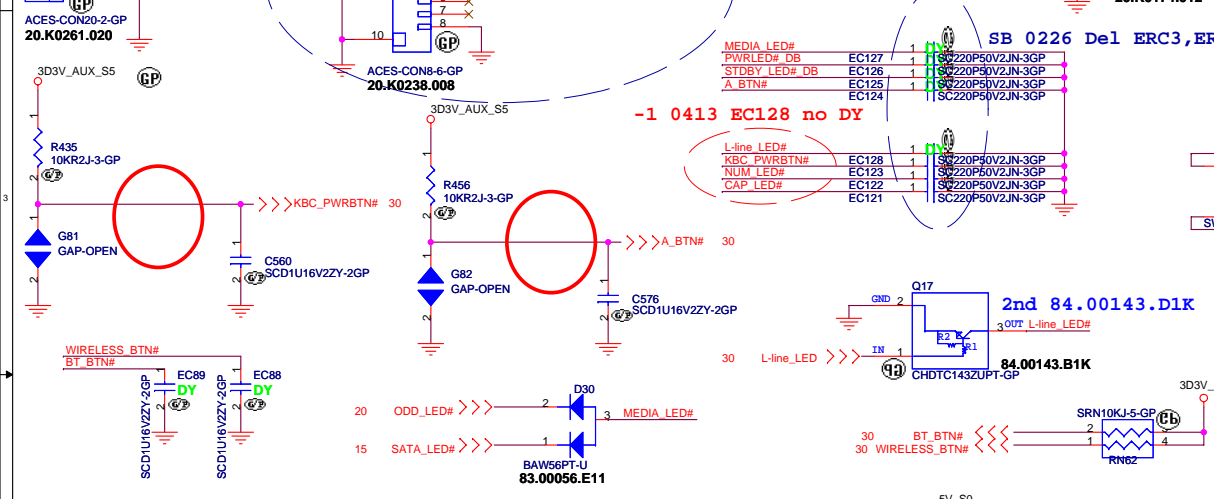
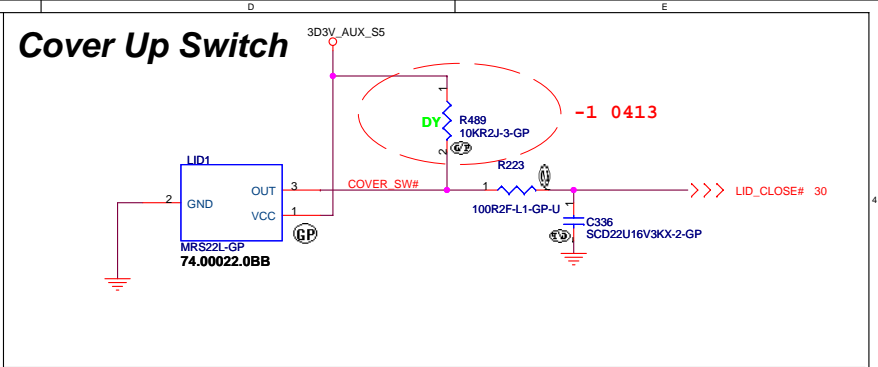
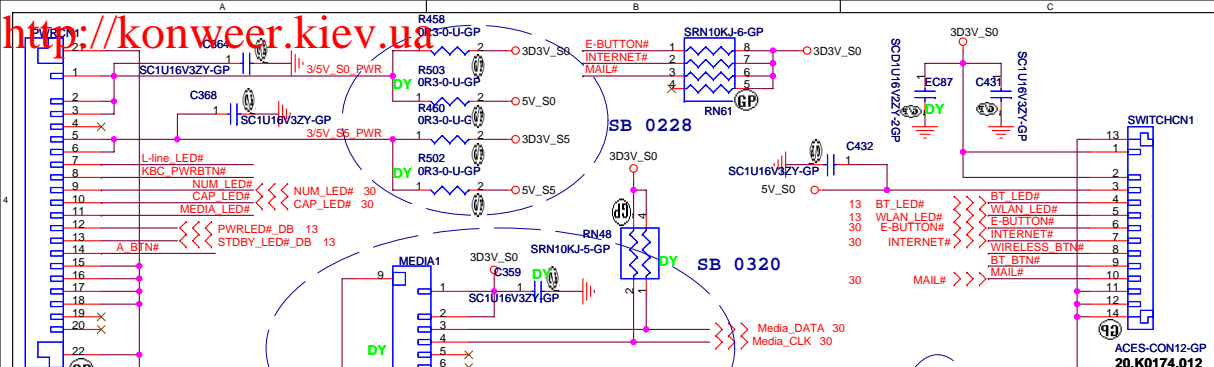
Date: Wednesday, April 18, 2007 Sheet 26 of 42











### Internal Keyboard CONN

CHECK KB SPEC. AND PIN DEFINE

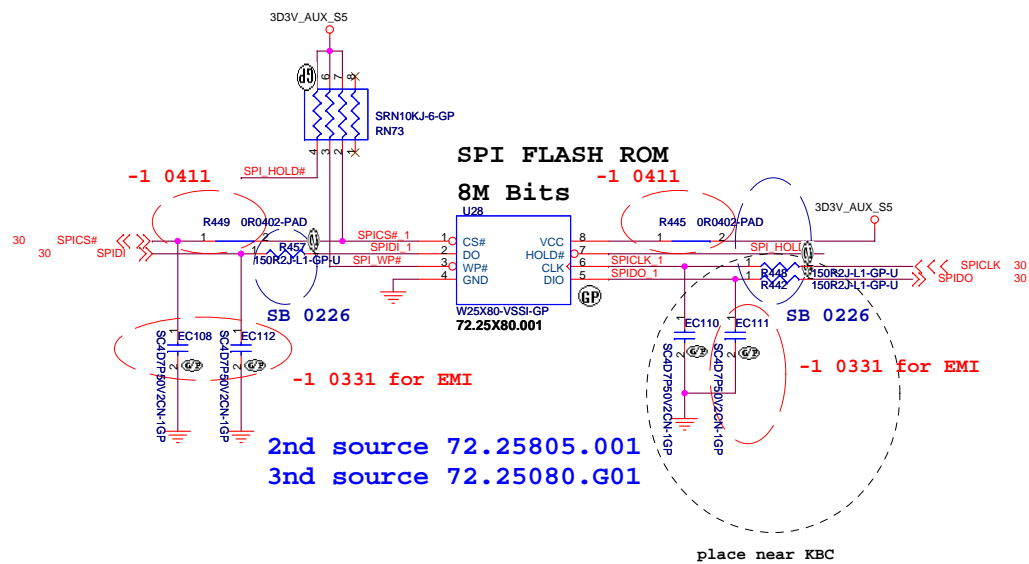
UMA

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Title: **BUTTONS / KB / TOUCHPAD**

Size: Document Number: **Volvi** Rev: -1

Date: Wednesday, April 18, 2007 Sheet 31 of 42

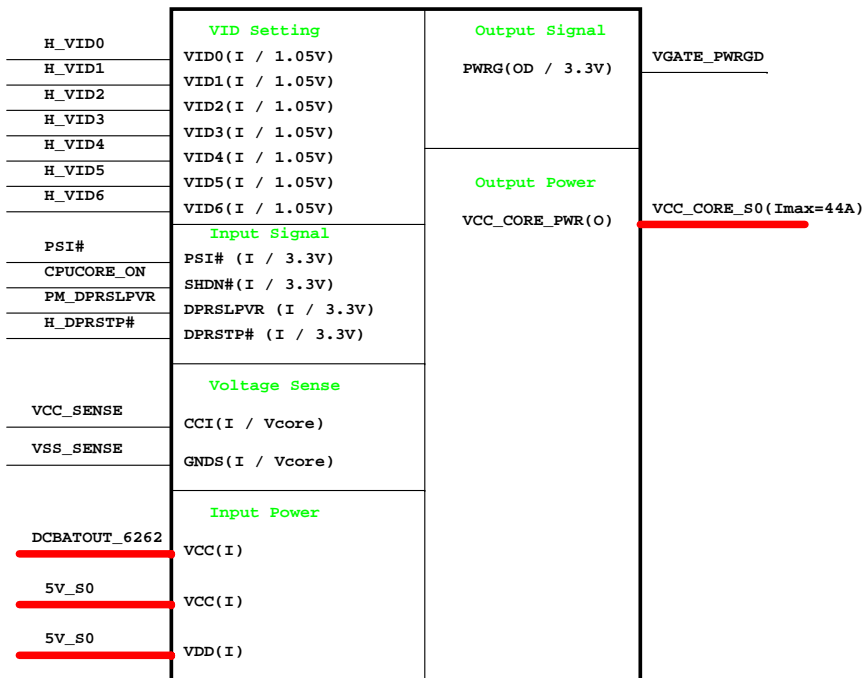


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Title		
BIOS		
Size A3	Document Number <b>Volvi</b>	Rev -1
Date: Wednesday, April 18, 2007		Sheet 32 of 42

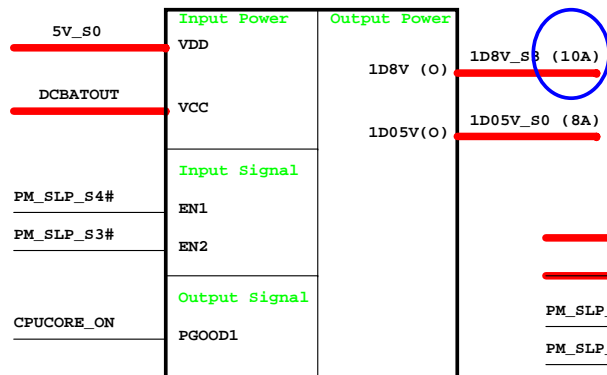


CPU\_CORE  
MAX8770

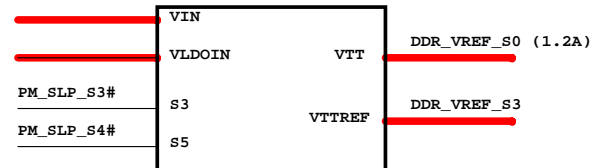


MAX8717  
1D8V\_S3 / 1D05V\_S0

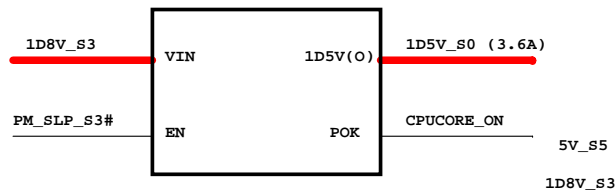
2007.1.19



TPS51100  
DDR\_VREF\_S0



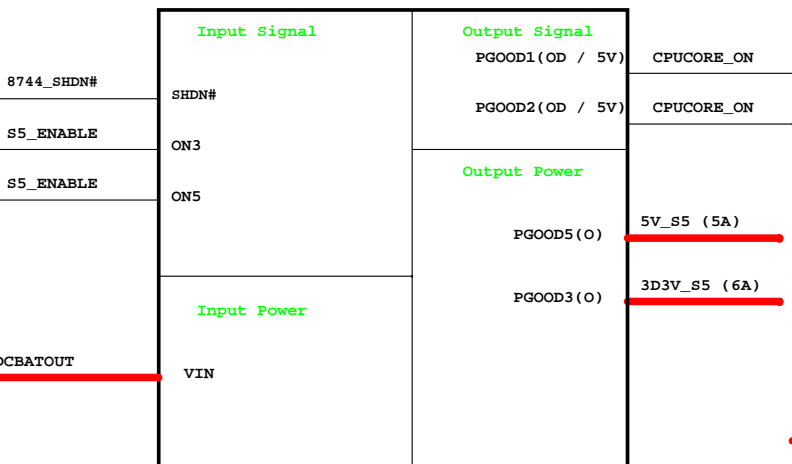
APL5912  
1D5V\_S0



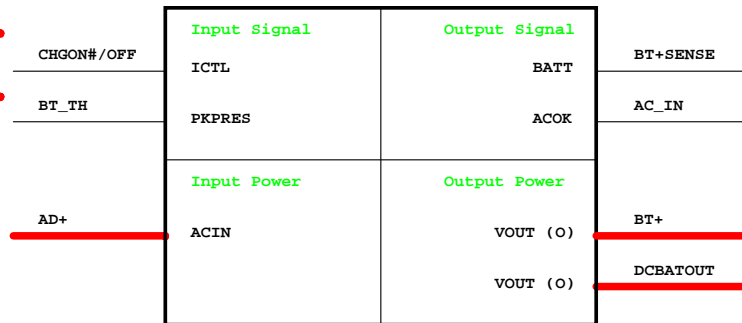
APL5312  
2D5V\_S0



MAX8744  
5V\_S5 / 3D3V\_S5



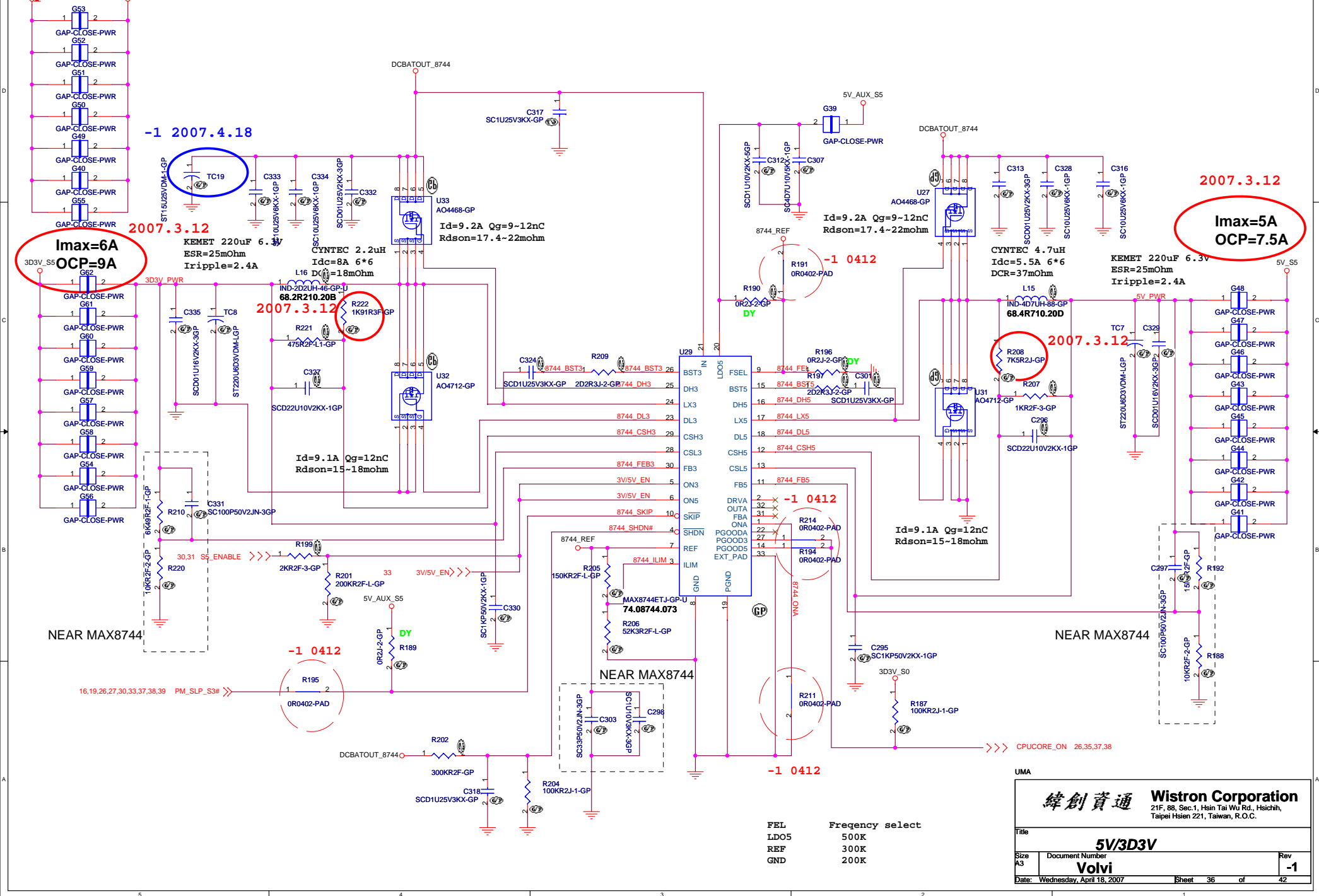
Charger MAX8731A



UMA

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<b>Power Block Diagram</b>			
Size A3	Document Number	Rev -1	
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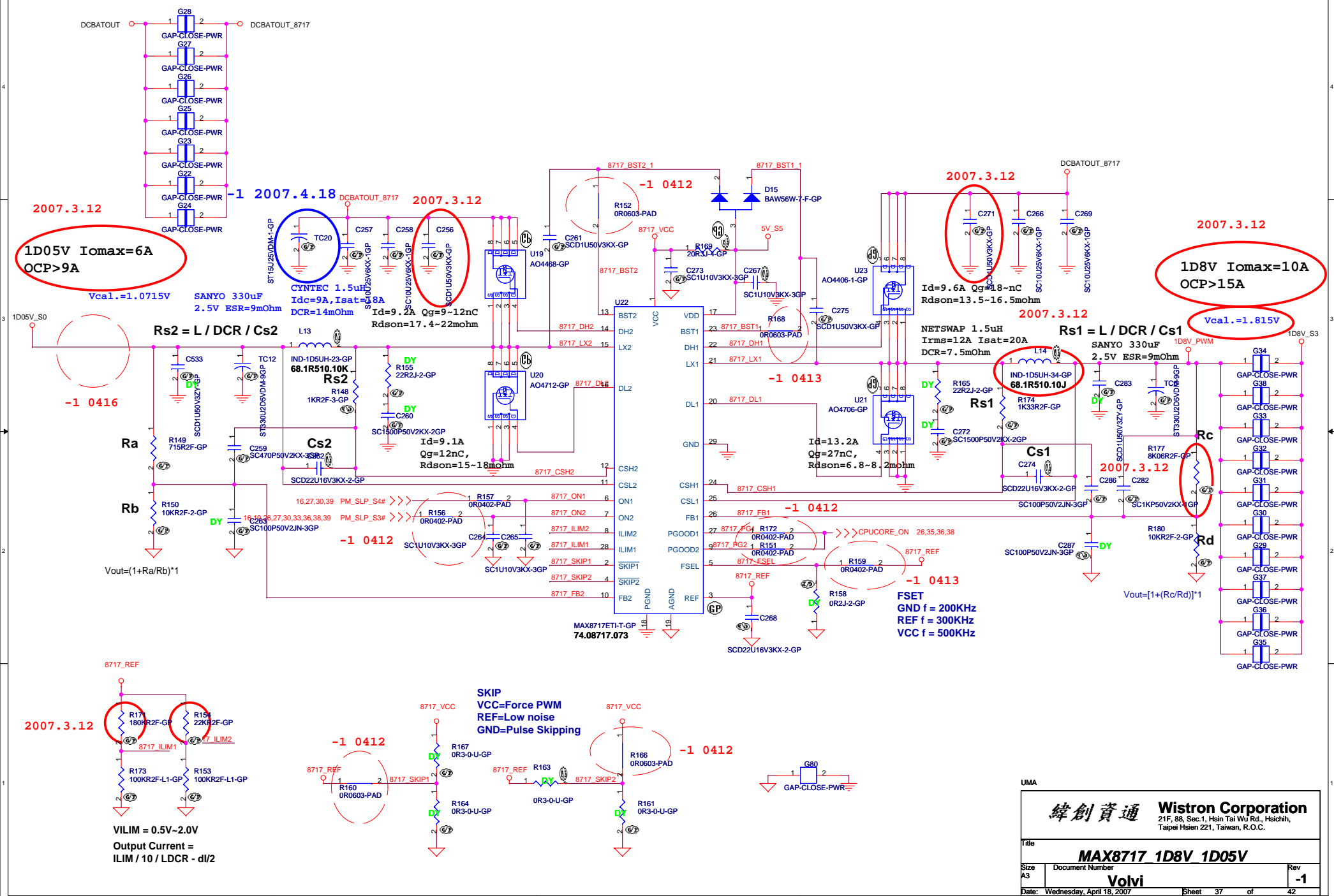
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Title: **5V/3D3V**

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FEL	Frequency select
LDO5	500K
REF	300K
GND	200K



2007.3.12  
**1D05V Iomax=6A**  
**OCP>9A**  
 Vcal.=1.0715V  
 SANYO 330uF  
 2.5V ESR=9mOhm

2007.3.12  
**1D8V Iomax=10A**  
**OCP>15A**  
 Vcal.=1.815V

-1 0416

-1 0412

-1 0412

-1 0413

2007.3.12

-1 0412

-1 0412

VILIM = 0.5V-2.0V  
 Output Current =  
 ILIM / 10 / LDCR - di/2

SKIP  
 VCC=Force PWM  
 REF=Low noise  
 GND=Pulse Skipping

FSET  
 GND f = 200KHz  
 REF f = 300KHz  
 VCC f = 500KHz

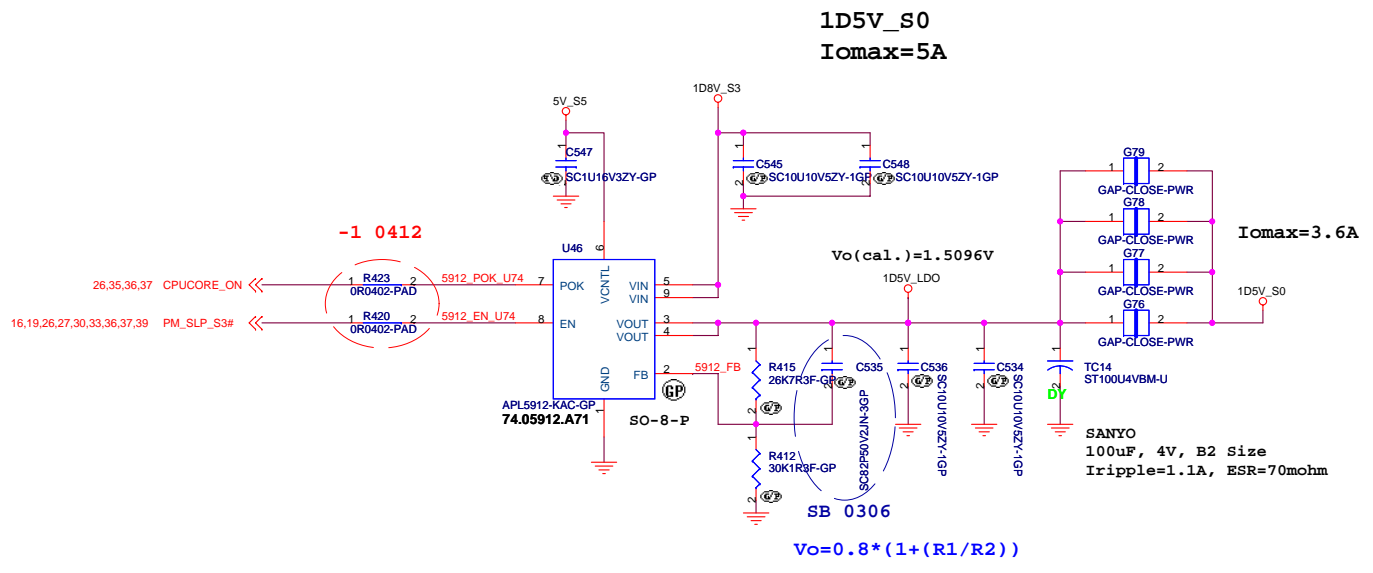
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Title  
**MAX8717 1D8V 1D05V**

Size A3 Document Number Rev  
**Volvi** -1

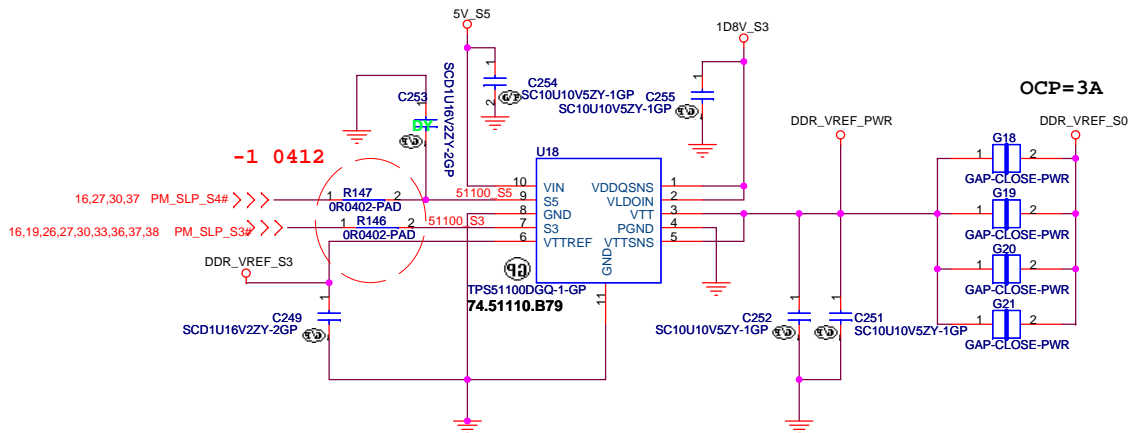
Date: Wednesday, April 18, 2007 Sheet 37 of 42



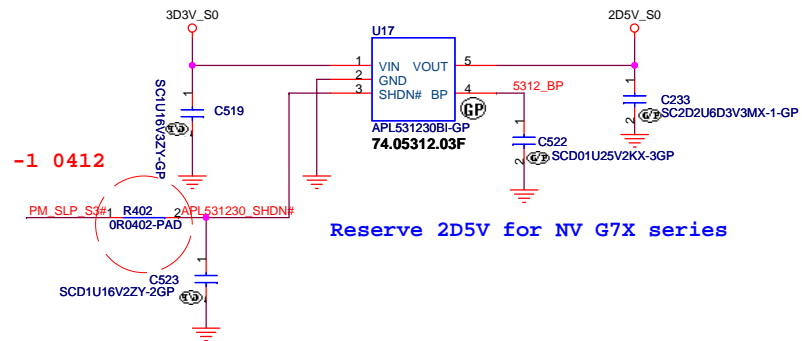
UMA

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<b>Title APW5912_1D5V</b>	
Size	Document Number
<b>Volvi</b>	
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### 0D9V\_S3 Iomax=0.5A



### 2D5V Iomax=130mA



Reserve 2D5V for NV G7X series

UMA

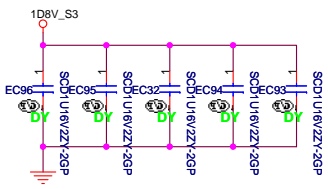
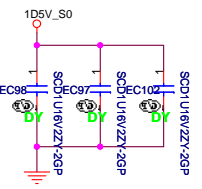
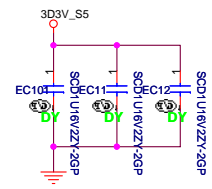
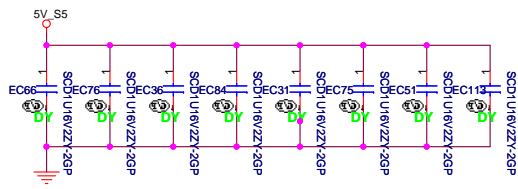
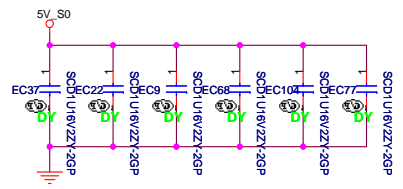
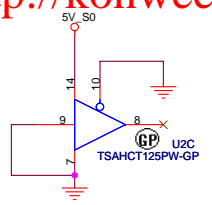
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Title: **2D5V / 0D9V**

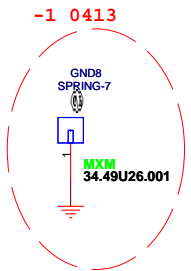
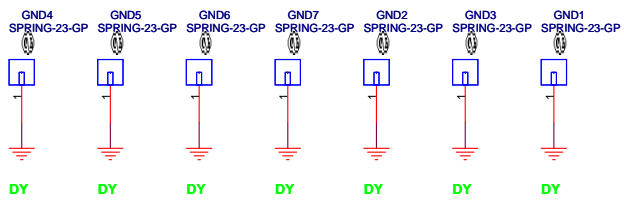
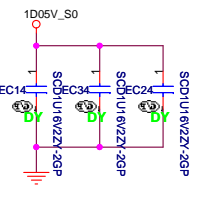
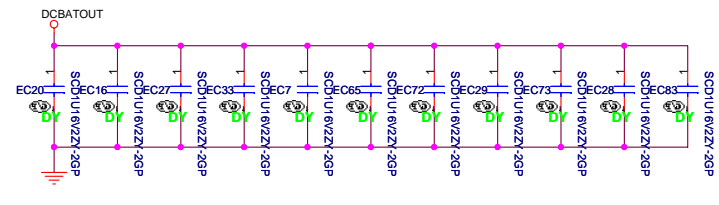
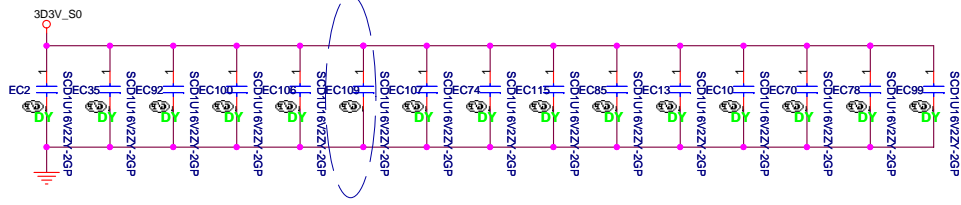
Size B Document Number **Volvi** Rev **-1**

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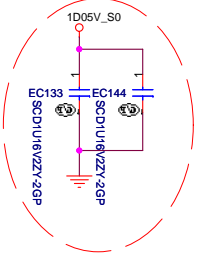




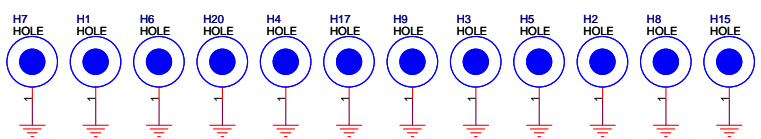
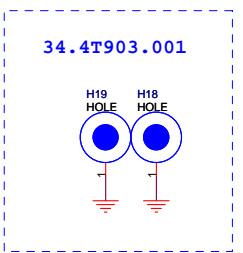
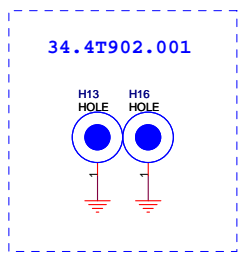
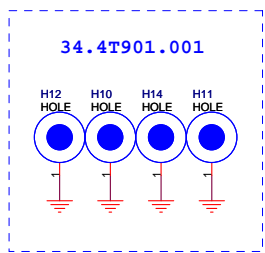
SB 0312 for EMI



-1 0417 for EMI



UMA DY



UMA

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Title: **EMI/Spring/Boss**

Size: Document Number: **Volvi** Rev: **-1**

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