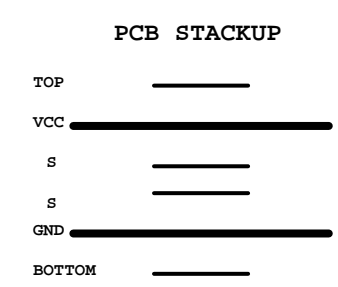
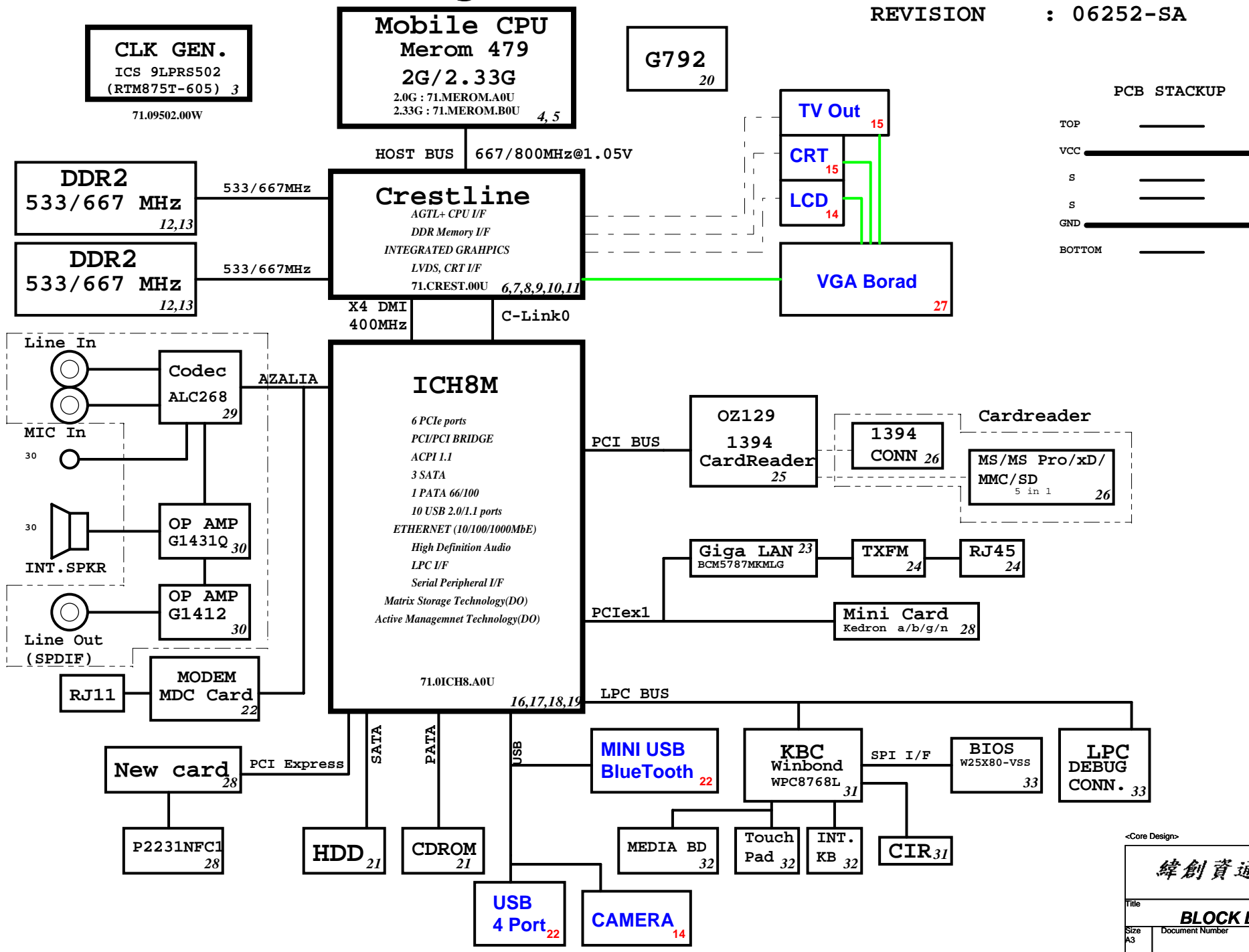


Tahoe Block Diagram

Project code: 91.4T901.001
 PCB P/N : 48.4T901.0SA
 REVISION : 06252-SA



SYSTEM DC/DC MAX8744		38
INPUTS	OUTPUTS	
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)	
SYSTEM DC/DC Max8717		39
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)	
TPS51100		41
1D8V_S3	DDR_VREF_S0(1.5A) DDR_VREF_S3	
APL5915		41
1D8V_S3	1D25V_S0(2A)	
APL531230		
3D3V_S0	2D5V_S0(300mA)	
APW5912		40
3D3V_S5	1D5V_S3(7.5A)	
CHARGER MAX8731		41
INPUTS	OUTPUTS	
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA	
CPU DC/DC MAX8770		35,36
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE_S0 0~1.3V 47A	

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE X1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWROK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCI Routing

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

USB Table

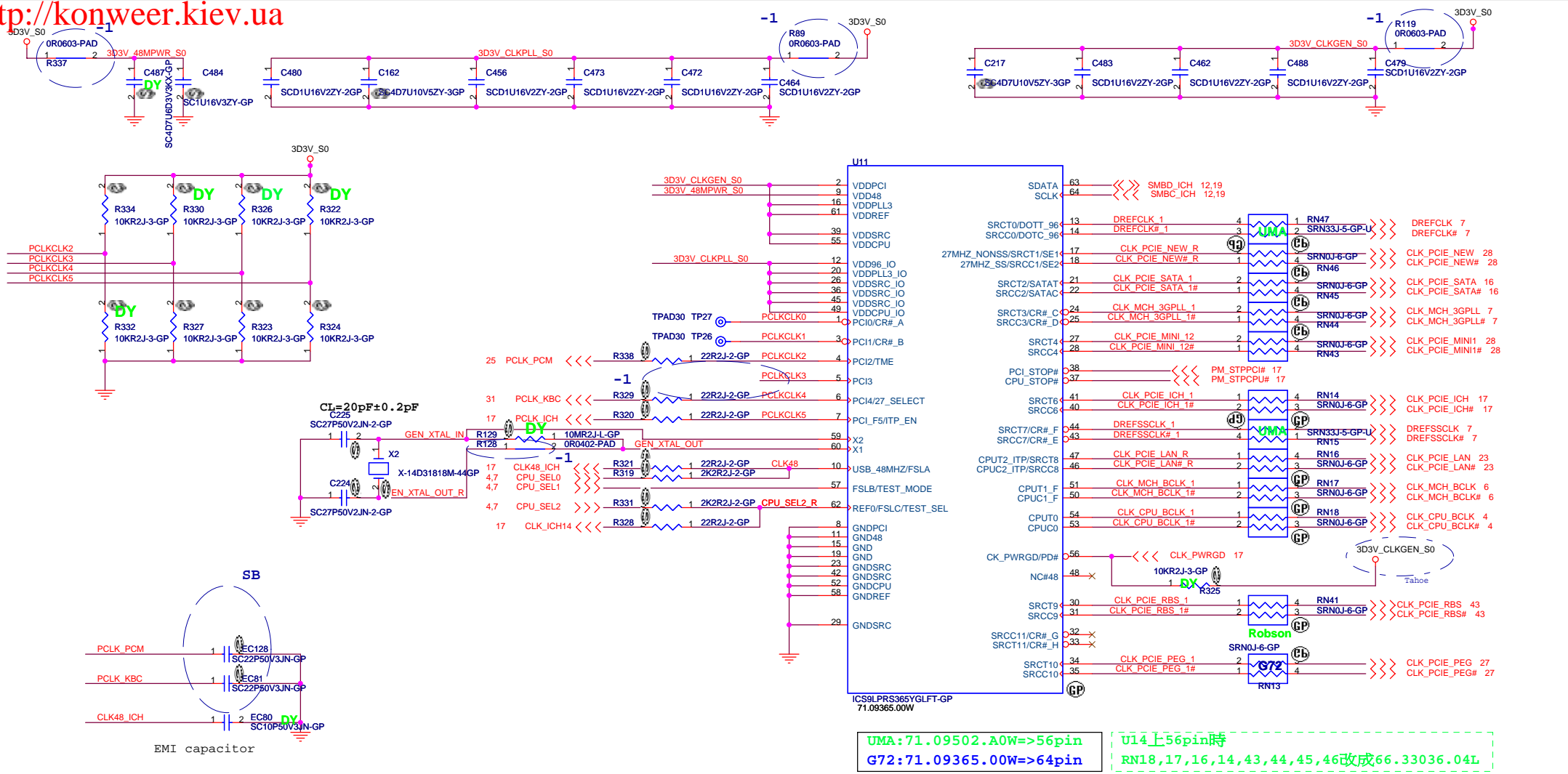
USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	FT
4	USB3
5	BLUETOOTH
6	NC
7	MINICARD
8	WEBCAM
9	NEW1

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Reference			
Title	Document Number		Rev
	Tahoe		-1
Date: Friday, April 27, 2007	Sheet 2	of 44	



UMA:71.09502.A0W=>56pin
 G72:71.09365.00W=>64pin
 UI4上56pin時
 RN18,17,16,14,43,44,45,46改成66.33036.04L

ICS9LPRS502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

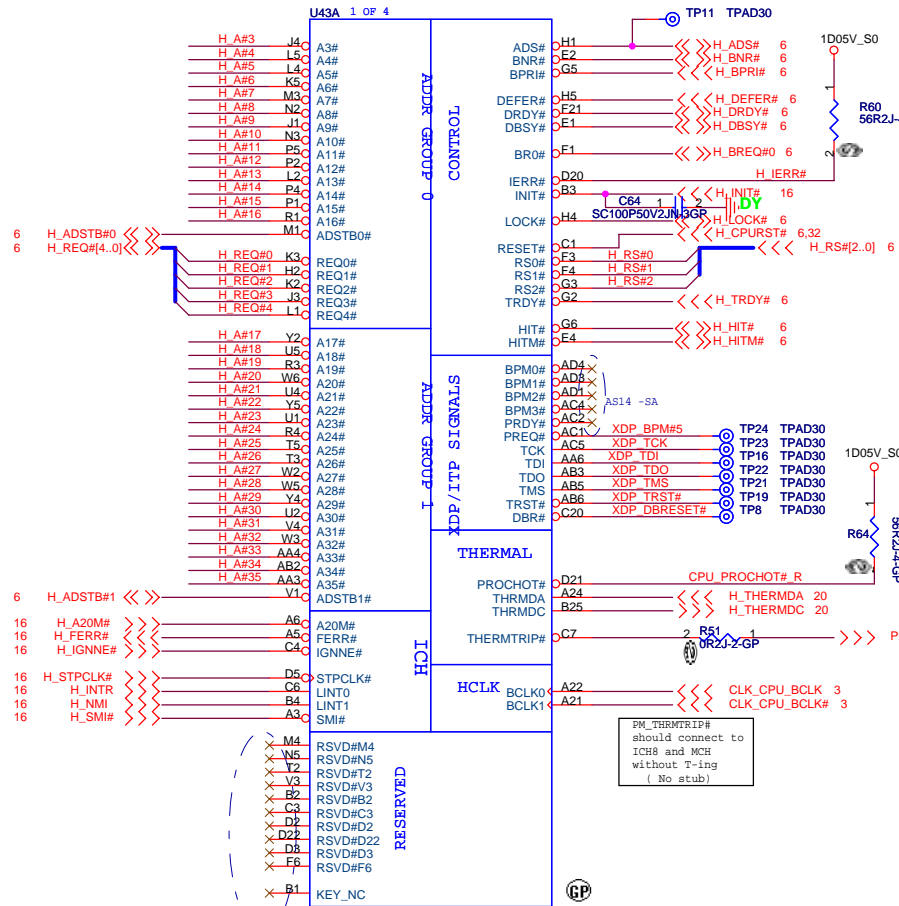
UMA

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator
 Sheet 3 of 44
 Date: Friday, April 27, 2007
 Rev: -1

6 H_A#(35..3) <<>> H_A#(35..3)

H_DINV#(3..0) <<>> H_DINV#(3..0) 6
H_DSTBN#(3..0) <<>> H_DSTBN#(3..0) 6
H_DSTBP#(3..0) <<>> H_DSTBP#(3..0) 6
H_D#(63..0) <<>> H_D#(63..0) 6



Place testpoint on H_IERR# with a GND 0.1" away

H_THERMDA

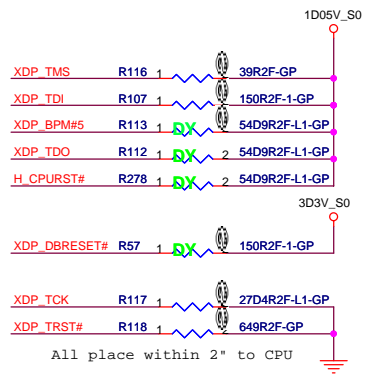
H_THERMDC

Layout Note: "CPU_GTLREF0" 0.5" max length.

PM_THRMTRIP# should connect to ICH8 and MCH without T-ling (No stub)

Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"



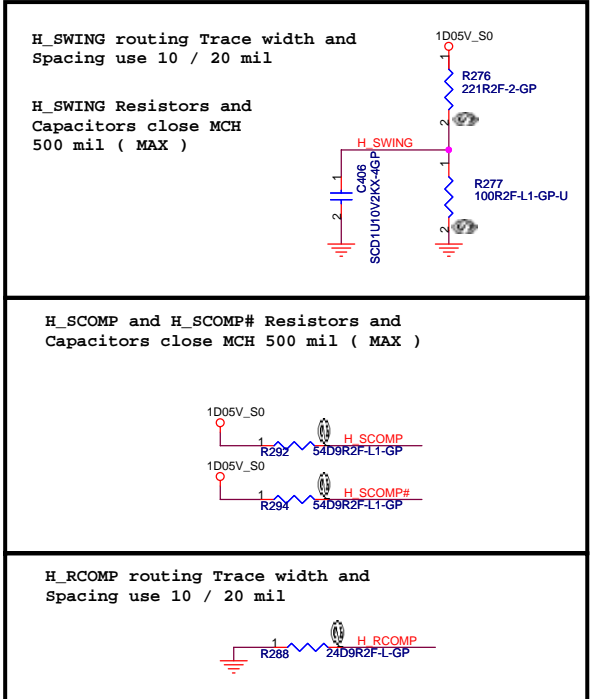
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (1 of 2)**

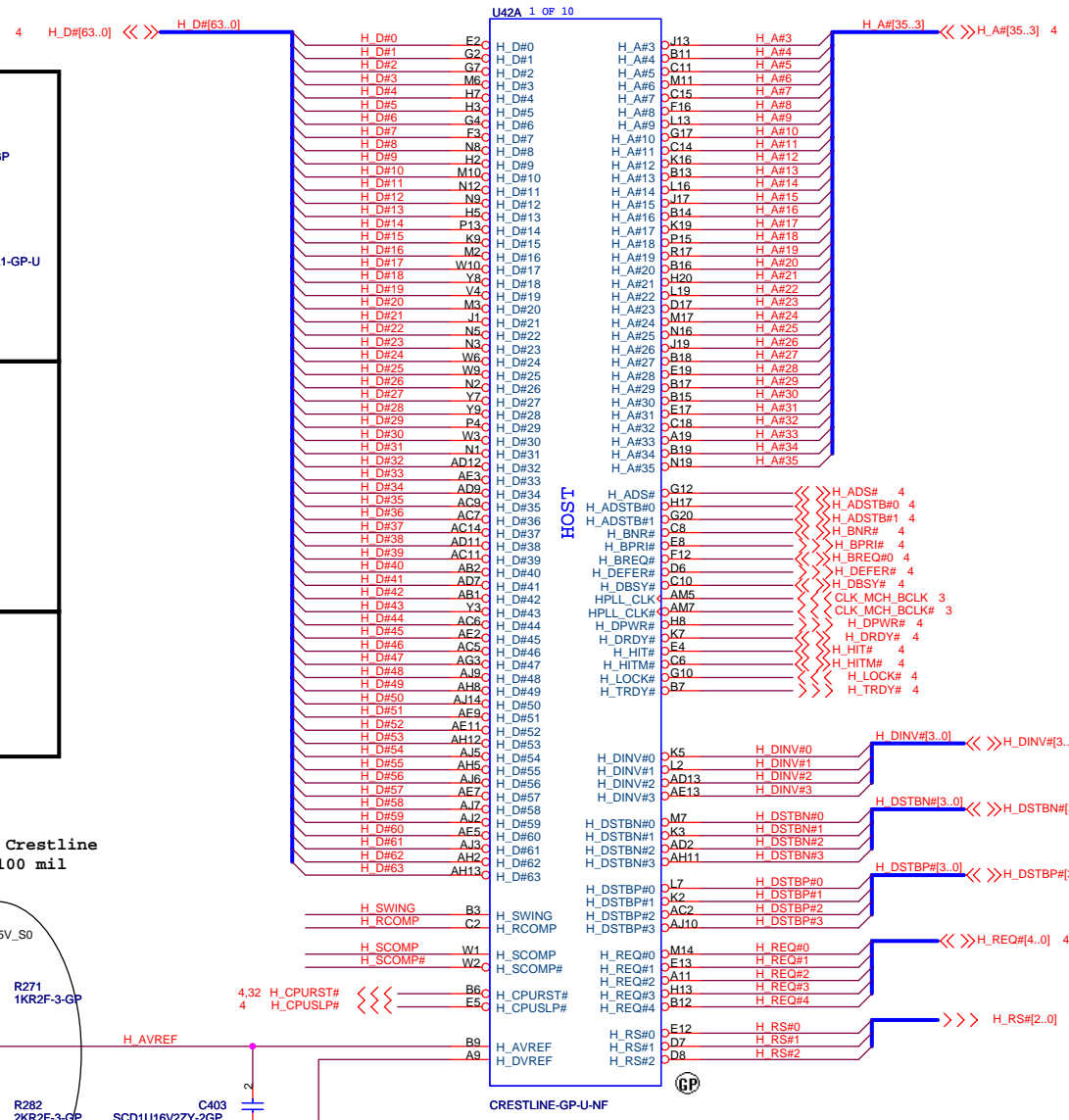
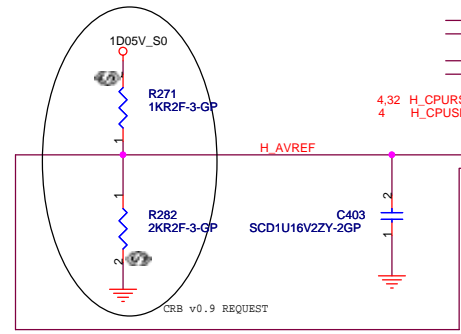
Size: Document Number: **Tahoe** Rev: -1

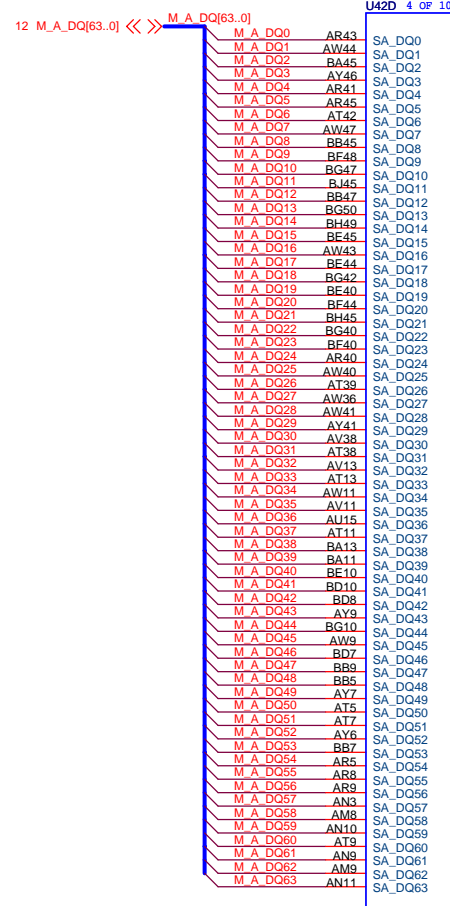
Date: Friday, April 27, 2007 Sheet 4 of 44



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil

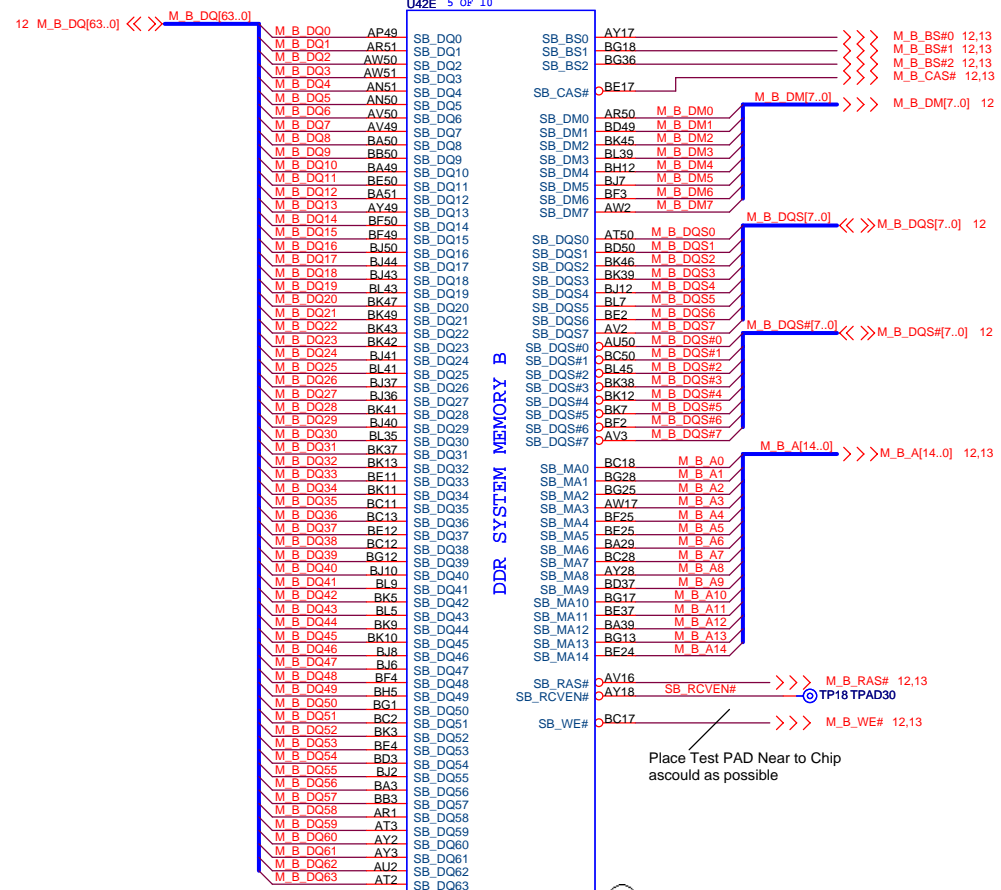




CRESTLINE-GP-U-NF

DDR SYSTEM MEMORY A

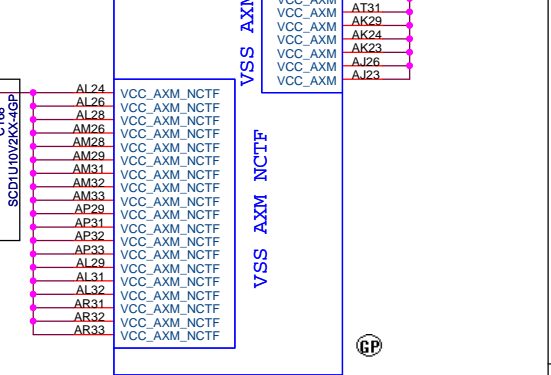
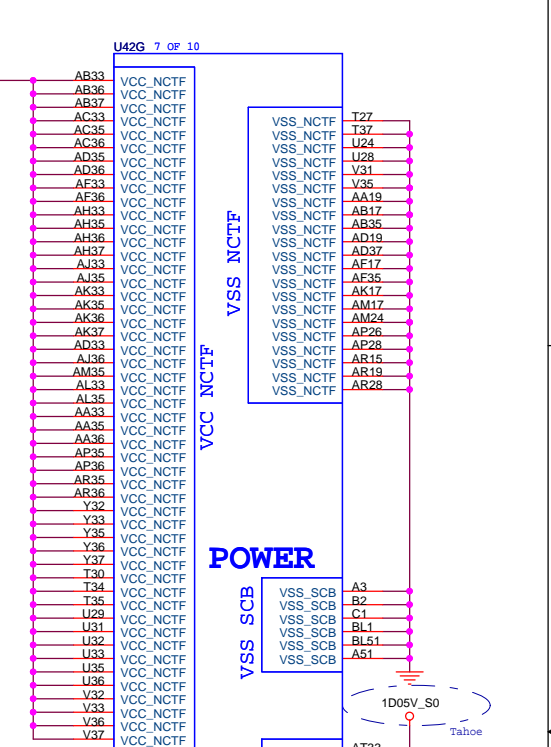
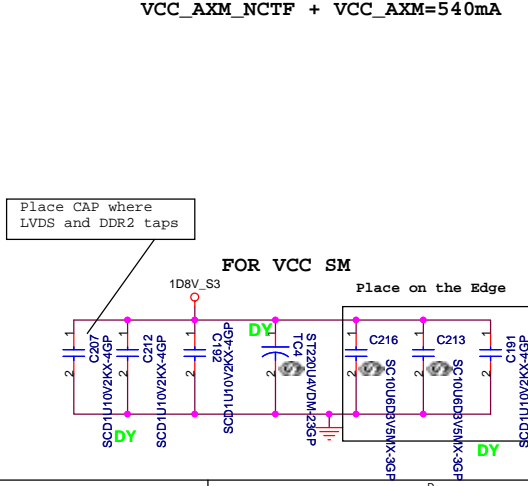
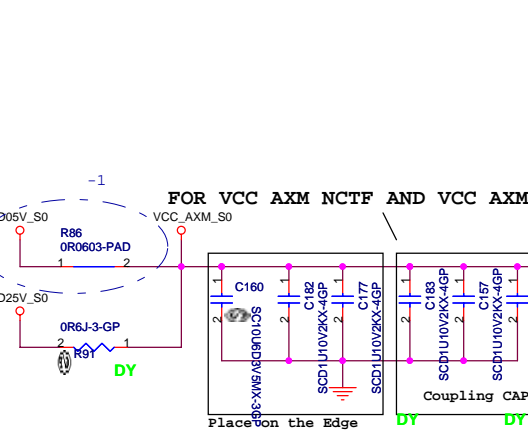
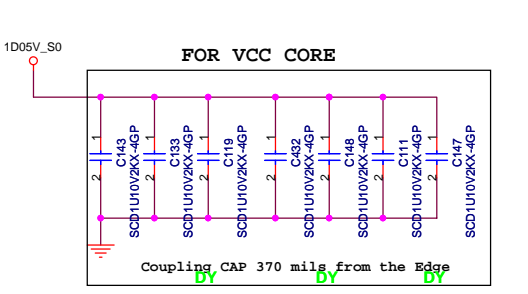
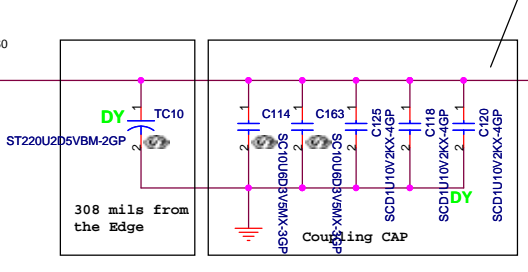
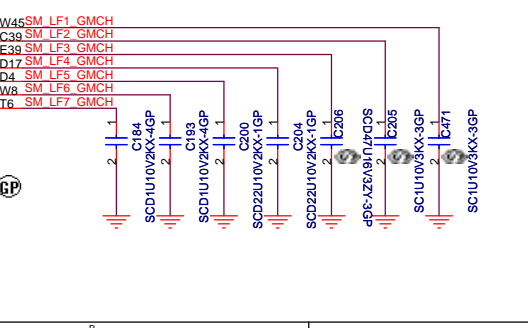
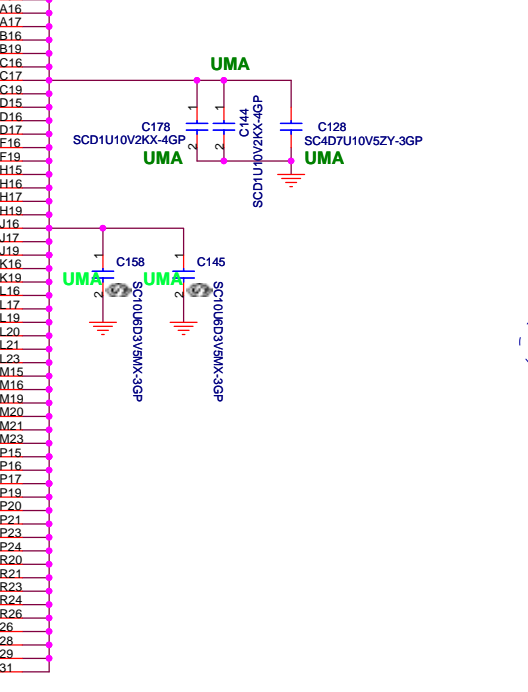
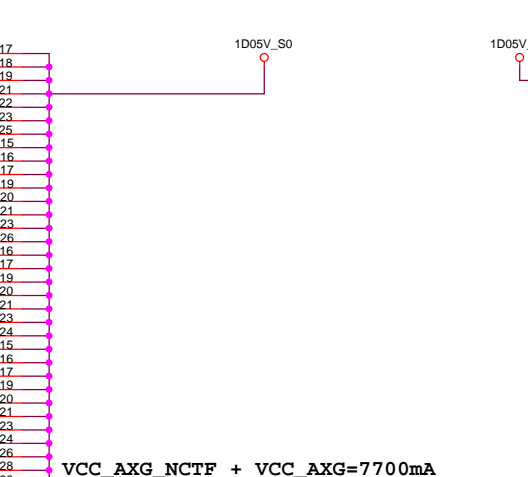
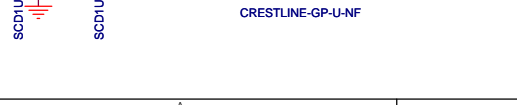
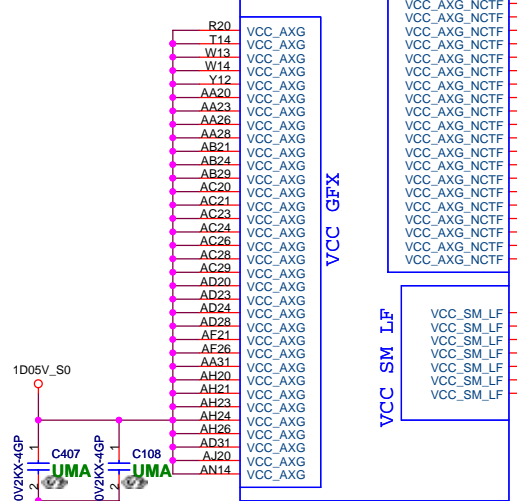
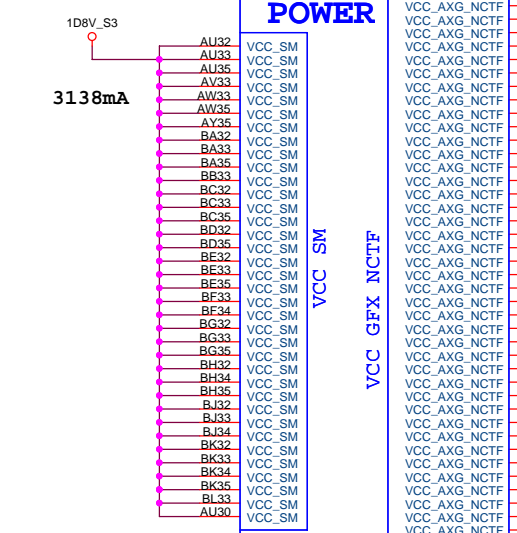
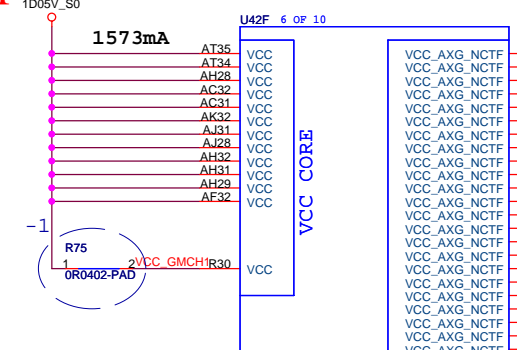
Place Test PAD Near to Chip as could as possible



CRESTLINE-GP-U-NF

DDR SYSTEM MEMORY B

Place Test PAD Near to Chip as could as possible



CRESTLINE-GP-U-NF

GP

1D05V_S0 Tahoe

1D8V_S3

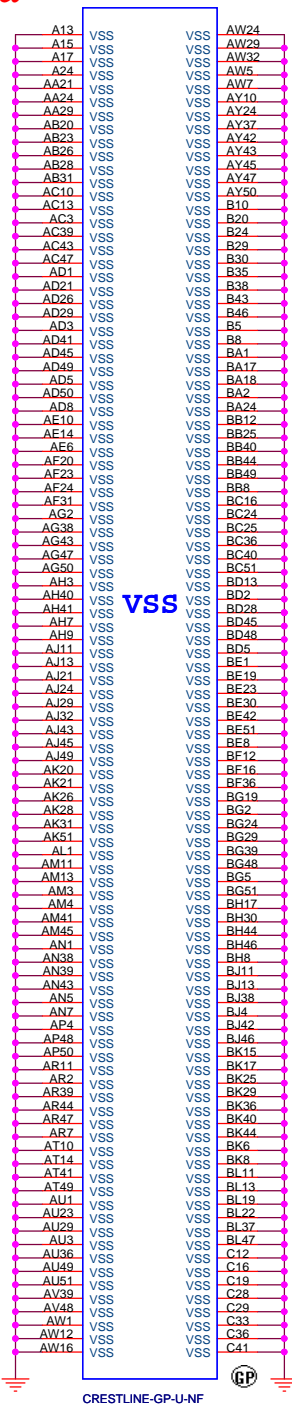
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

GMCH (4 of 6)

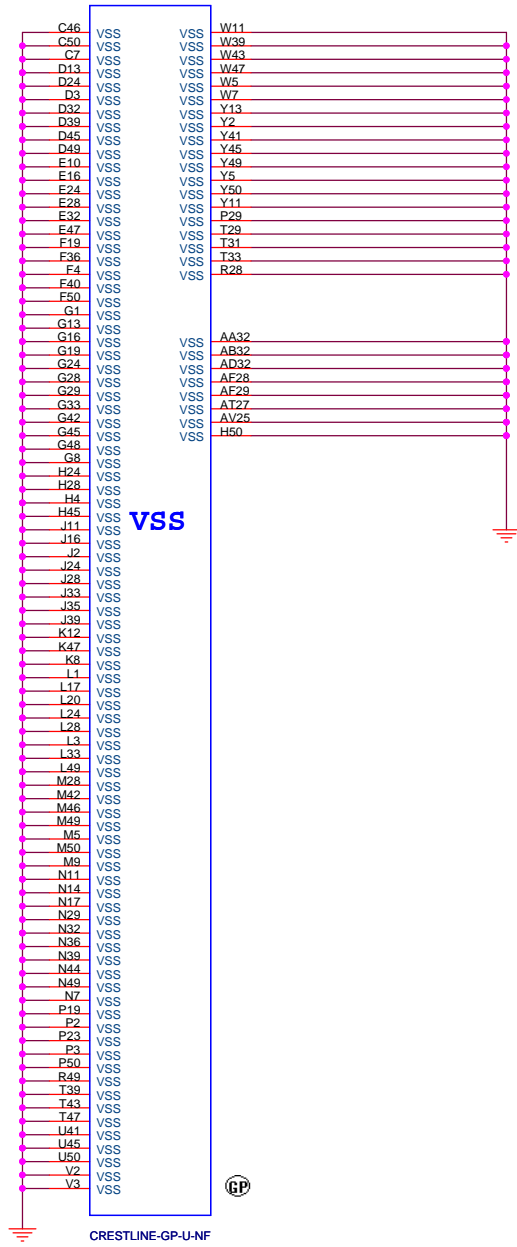
Tahoe

Friday, April 27, 2007

Sheet 9 of 44



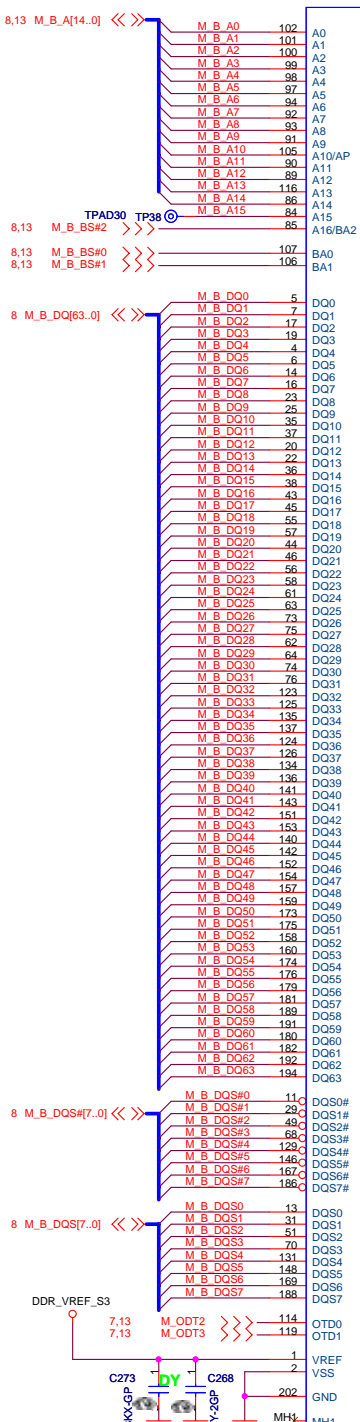
VSS



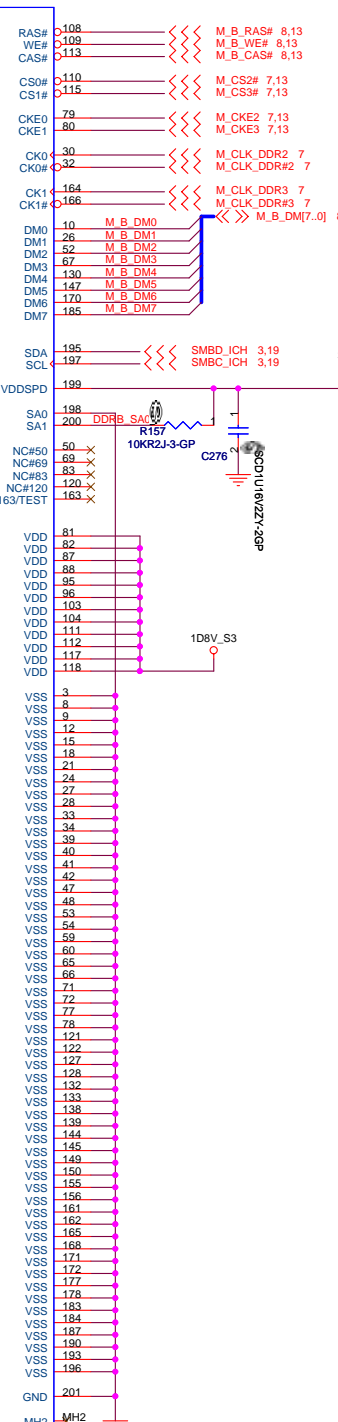
VSS



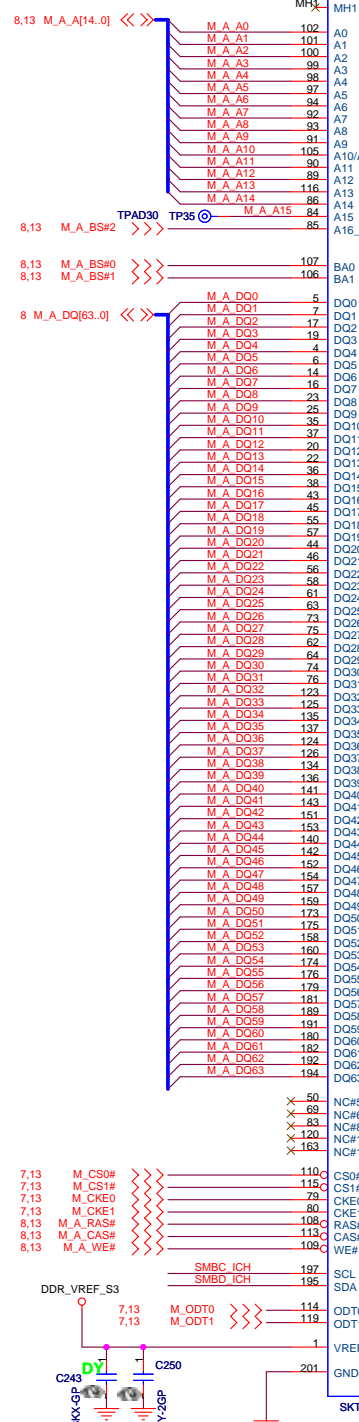
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
GMCH (6 of 6)	
Size	Document Number
Tahoe	
Date: Friday, April 27, 2007	Rev -1
Sheet 11	of 44



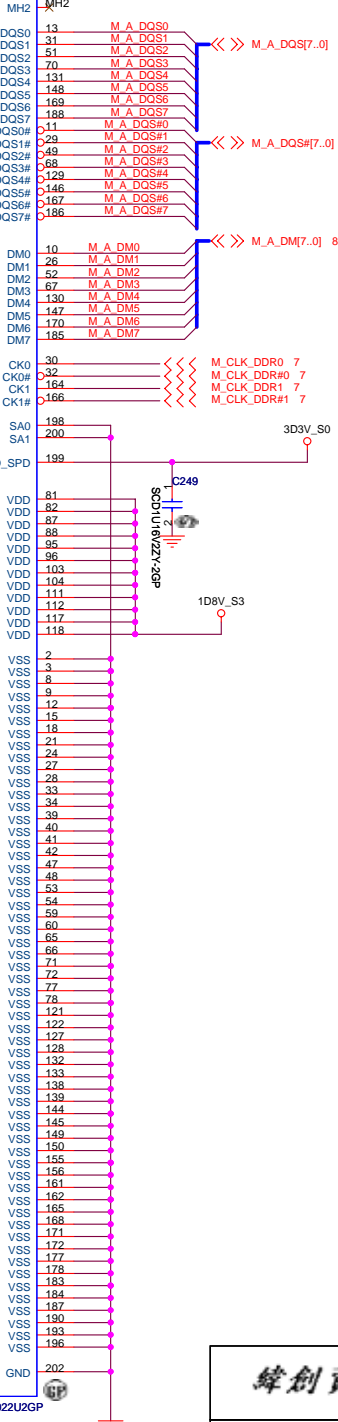
REVERSE TYPE



DDR2-200P-23-GP-U1
62.10017.A71
High 9.2mm



REVERSE TYPE



SKT-SODIMM2002U2GP
62.10017.691
High 5.2mm

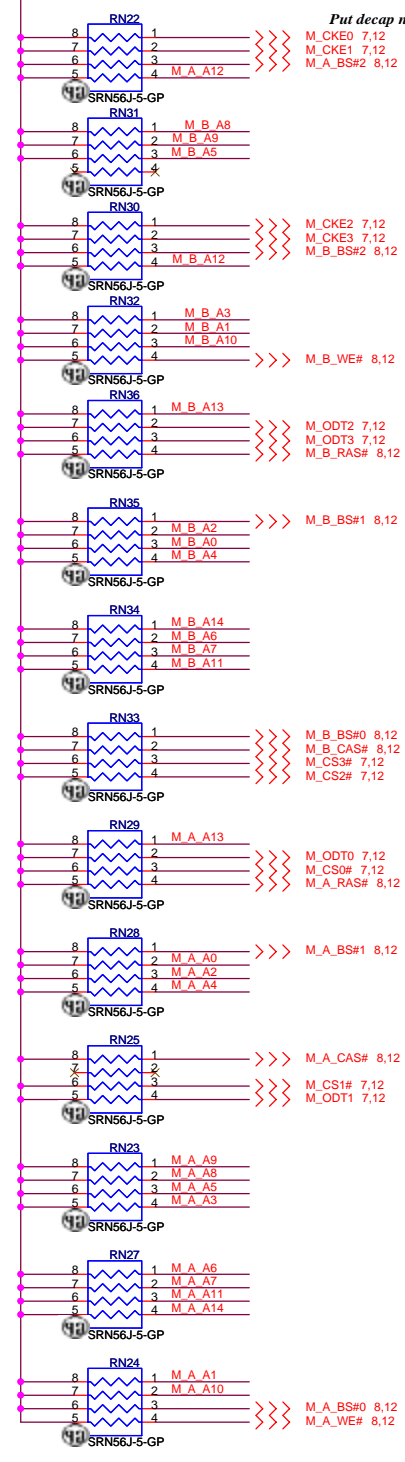
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2 Socket**

Size: Document Number: **Tahoe** Rev: **-1**

Date: Friday, April 27, 2007 Sheet 12 of 44

PARALLEL TERMINATION

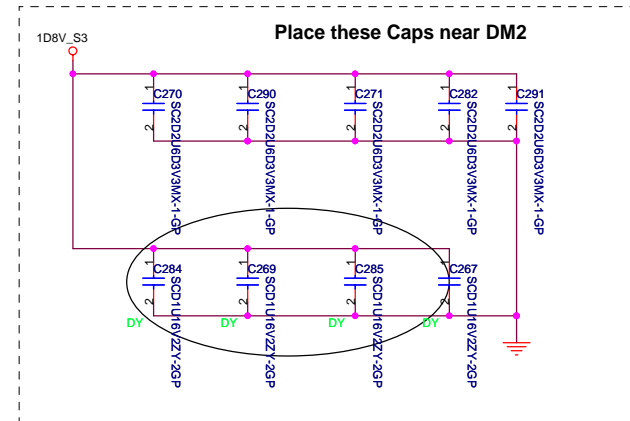
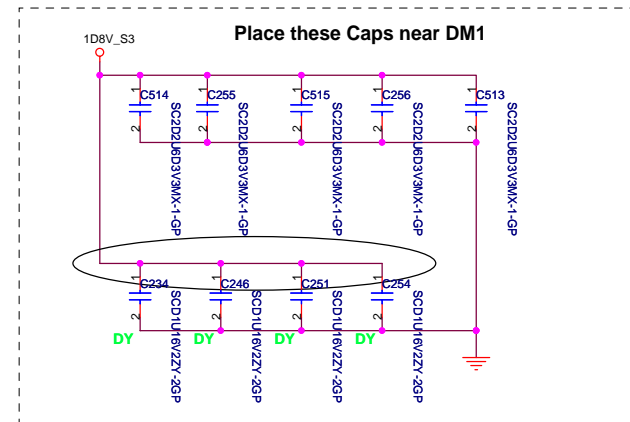
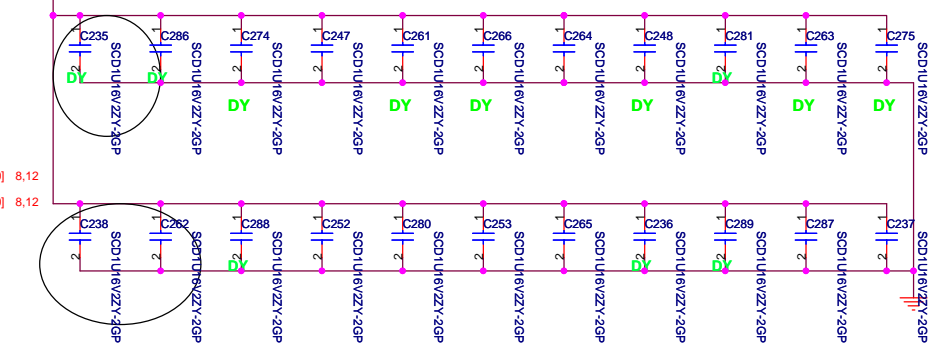


Put decap near power(0.9V) and pull-up resistor

M_A_A[14..0] <<< M_A_A[14..0] 8,12
 M_B_A[14..0] <<< M_B_A[14..0] 8,12

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

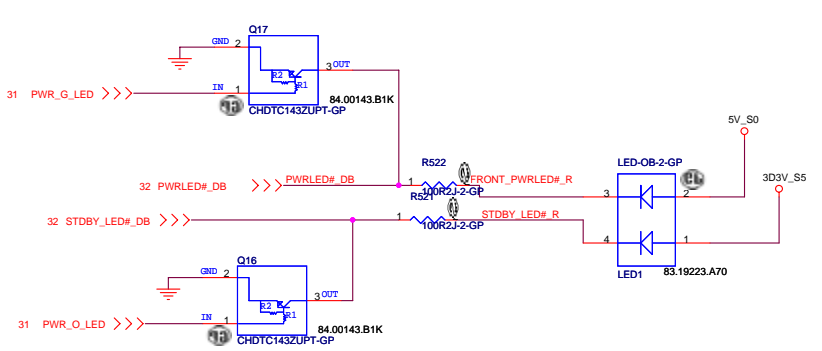
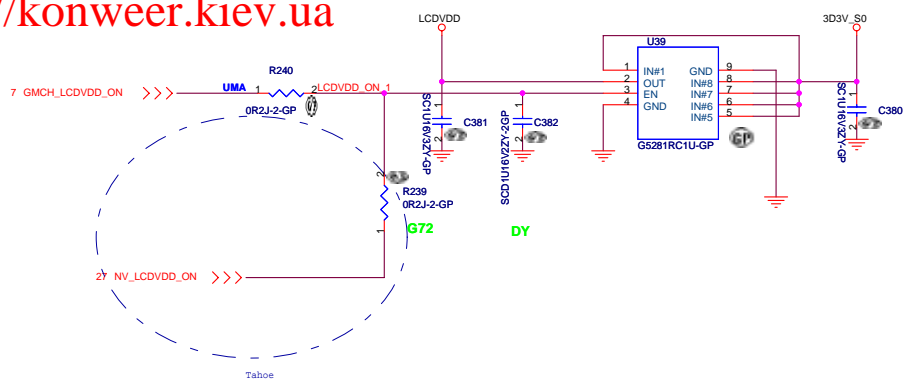


緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

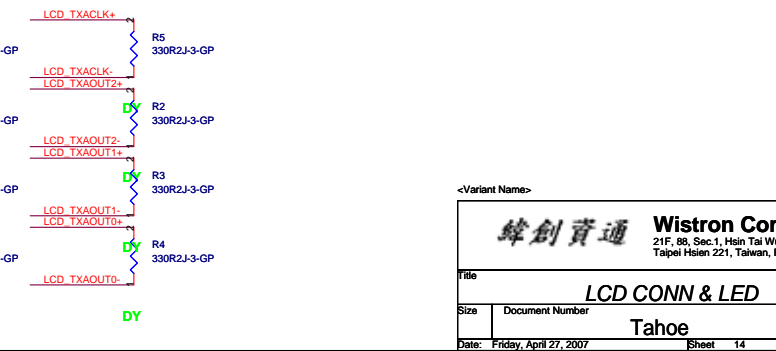
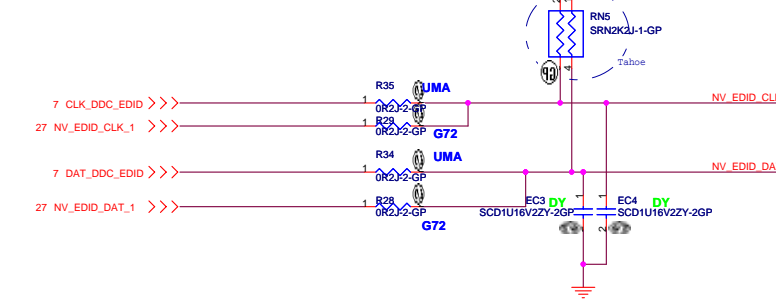
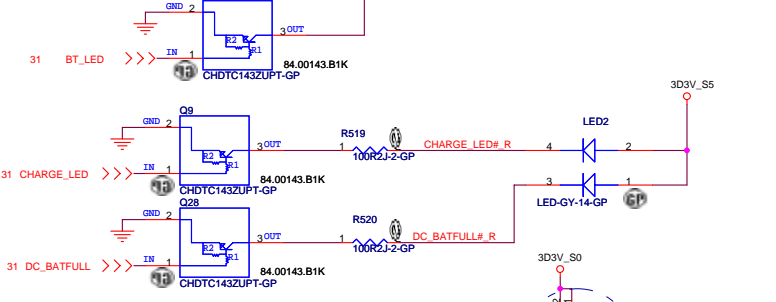
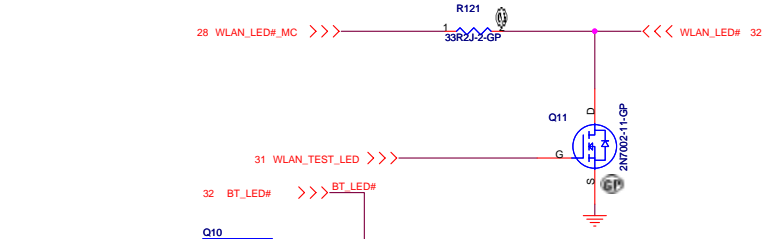
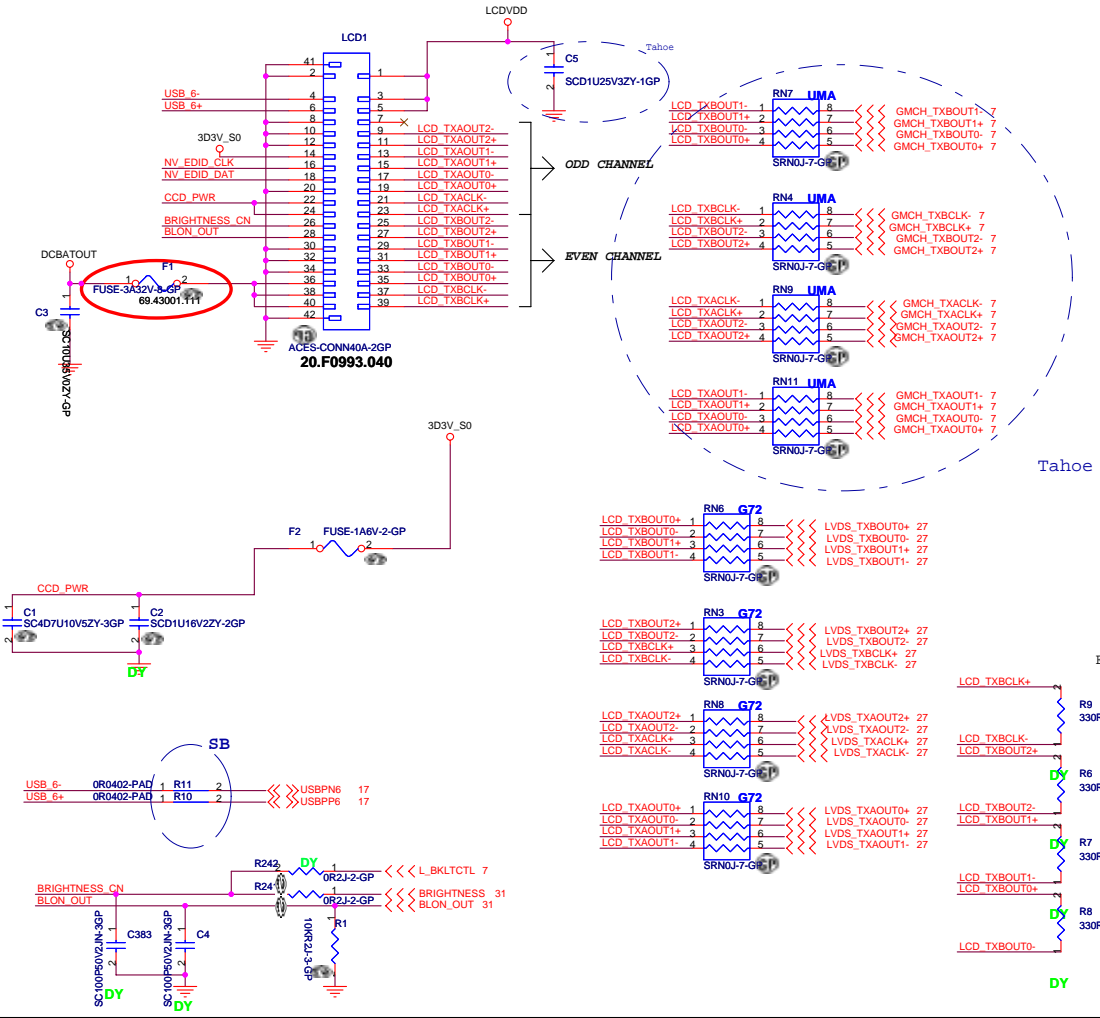
Title: **DDR2 Termination Resistor**

Size: Document Number: **Tahoe** Rev: **-1**

Date: Friday, April 27, 2007 Sheet 13 of 44



LCD/INVERTER CONN

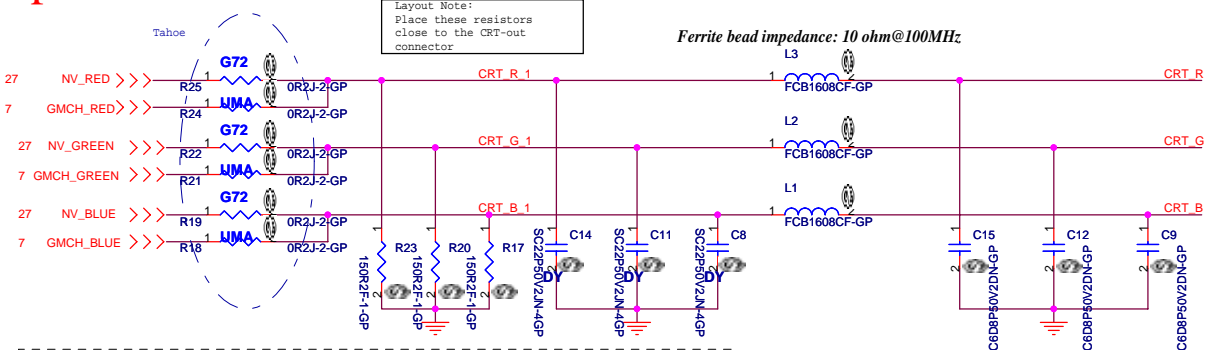


Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **LCD CONN & LED**

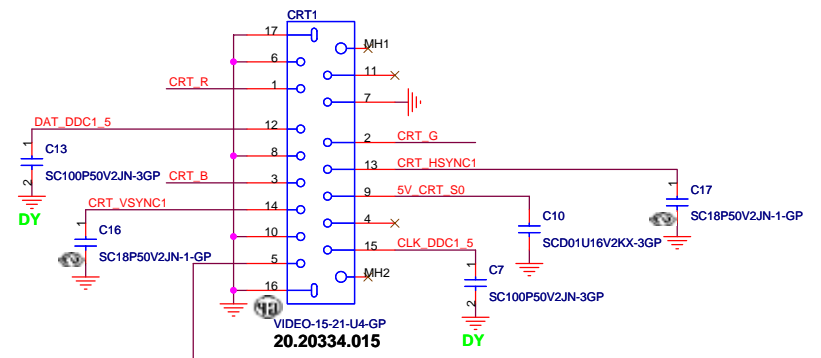
Size: Document Number **Tahoe** Rev: -1

Date: Friday, April 27, 2007 Sheet 14 of 44

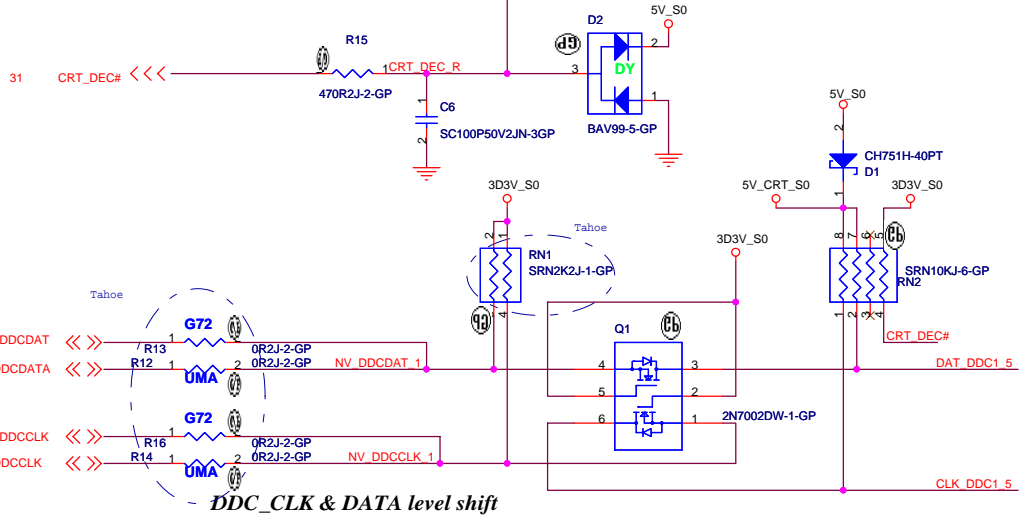
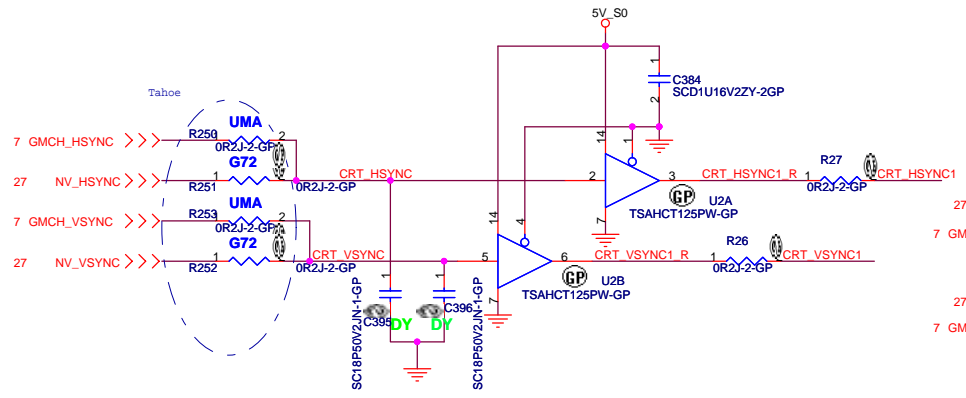


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

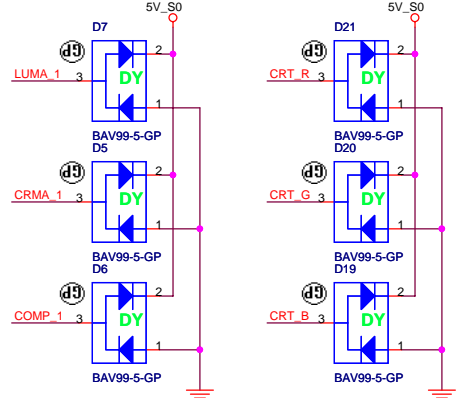
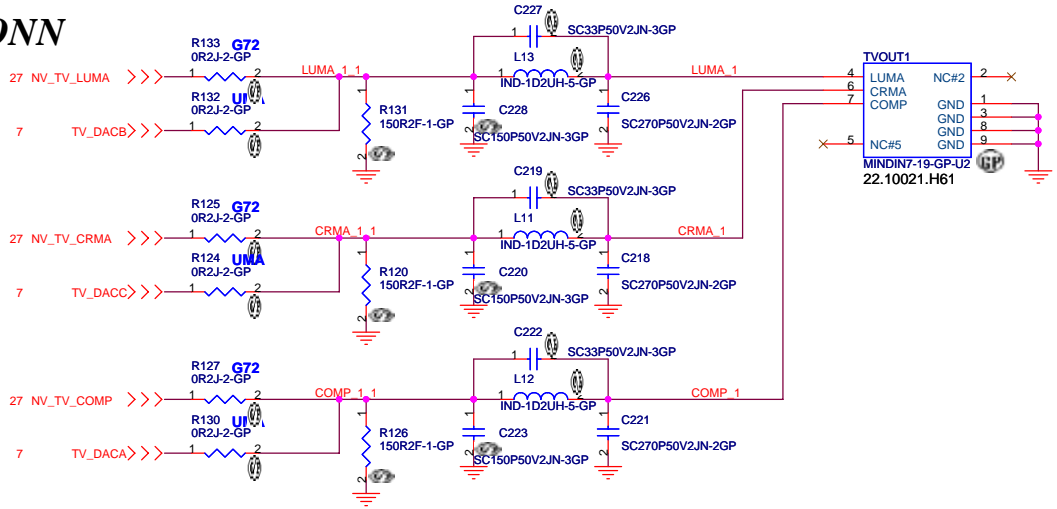
For DIS
C15---->78.15034.1FL
C12,C9---->78.18034.1FL



Hsync & Vsync level shift

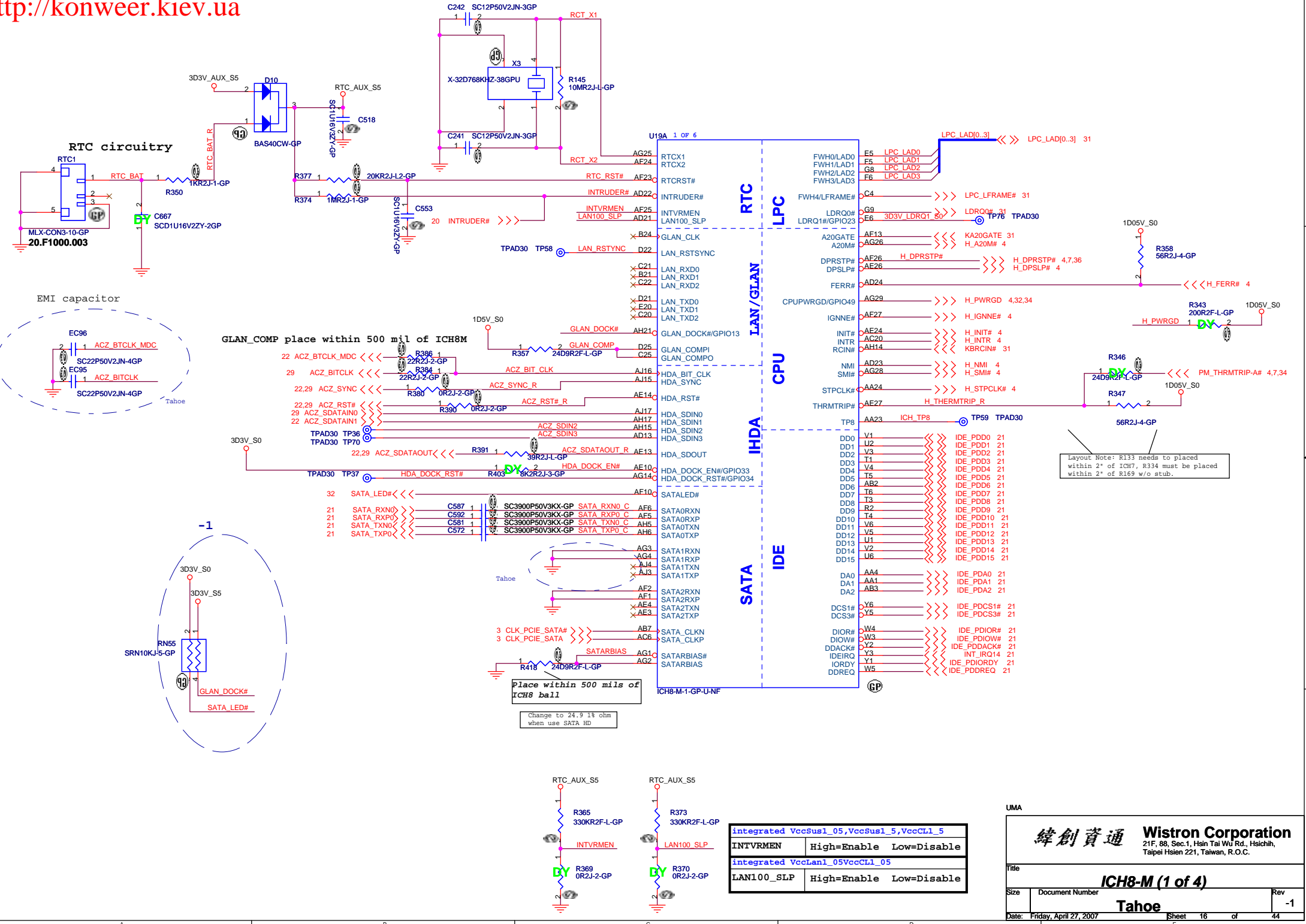


TV CONN



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title CRT/TV Connector		
Size	Document Number	Rev -1
Date: Friday, April 27, 2007	Sheet 15 of 44	



Layout Note: R133 needs to be placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.

Place within 500 mils of ICH8 ball

Change to 24.9 1% ohm when use SATA HD

integrated VccSus1_05,VccSus1_5,VccCLL_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCLL_05	
LAN100_SLP	High=Enable Low=Disable

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH8-M (1 of 4)**

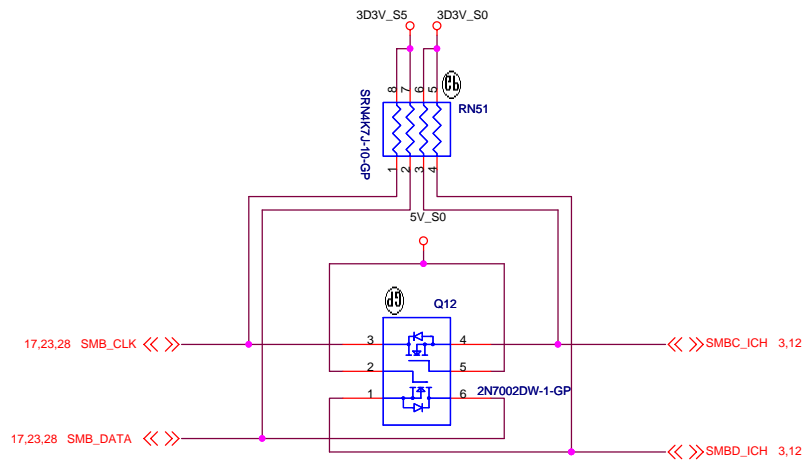
Size: Document Number: **Tahoe** Rev: -1

Date: Friday, April 27, 2007 Sheet 16 of 44

U19F 6 OF 6

A23	VSS	K7
A5	VSS	L1
AA2	VSS	L13
AA7	VSS	L15
A25	VSS	L26
AB1	VSS	L27
AB24	VSS	L4
AC11	VSS	L5
AC14	VSS	M12
AC25	VSS	M13
AC26	VSS	M14
AC27	VSS	M15
AD17	VSS	M16
AD20	VSS	M17
AD28	VSS	M23
AD29	VSS	M28
AD3	VSS	M29
AD4	VSS	M3
AD6	VSS	N1
AE1	VSS	N11
AE12	VSS	N12
AE2	VSS	N13
AE22	VSS	N14
AD1	VSS	N15
AE25	VSS	N16
AE5	VSS	N17
AE6	VSS	N18
AE9	VSS	N26
AF14	VSS	N27
AF16	VSS	N4
AF18	VSS	N5
AF3	VSS	N6
AF4	VSS	P12
AG5	VSS	P13
AG6	VSS	P14
AH10	VSS	P15
AH13	VSS	P16
AH16	VSS	P17
AH19	VSS	P23
AH2	VSS	P28
AE28	VSS	P29
AH22	VSS	R11
AH24	VSS	R12
AH26	VSS	R13
AH3	VSS	R14
AH4	VSS	R15
AH8	VSS	R16
AJ5	VSS	R17
B11	VSS	R18
B14	VSS	R28
B17	VSS	R4
B2	VSS	T12
B20	VSS	T13
B22	VSS	T14
B3	VSS	T15
C24	VSS	T16
C26	VSS	T17
C27	VSS	T2
C6	VSS	U12
D12	VSS	U13
D15	VSS	U14
D18	VSS	U15
D2	VSS	U16
D4	VSS	U17
E21	VSS	U23
E24	VSS	U26
E4	VSS	U27
E9	VSS	U3
F15	VSS	U5
E23	VSS	V13
F28	VSS	V15
F29	VSS	V28
F7	VSS	V29
G1	VSS	W2
F2	VSS	W26
G10	VSS	W27
G13	VSS	Y28
G19	VSS	Y29
G23	VSS	Y4
G25	VSS	AB4
G26	VSS	AB23
G27	VSS	AB5
H25	VSS	AB6
H28	VSS	AD5
H29	VSS	U4
H3	VSS	W24
H6	VSS	A1
J1	VSS	A2
J25	VSS_NCTF	A28
J26	VSS_NCTF	A29
J27	VSS_NCTF	AJ28
J4	VSS_NCTF	AH1
J5	VSS_NCTF	AH29
K23	VSS_NCTF	AJ1
K28	VSS_NCTF	AJ2
K29	VSS_NCTF	AJ29
K3	VSS_NCTF	B1
K6	VSS_NCTF	B29
	VSS_NCTF	A1
	VSS_NCTF	A2
	VSS_NCTF	A28
	VSS_NCTF	A29
	VSS_NCTF	AJ28
	VSS_NCTF	AH1
	VSS_NCTF	AH29
	VSS_NCTF	AJ1
	VSS_NCTF	AJ2
	VSS_NCTF	AJ29
	VSS_NCTF	B1
	VSS_NCTF	B29

ICH8-M-1-GP-U-NF

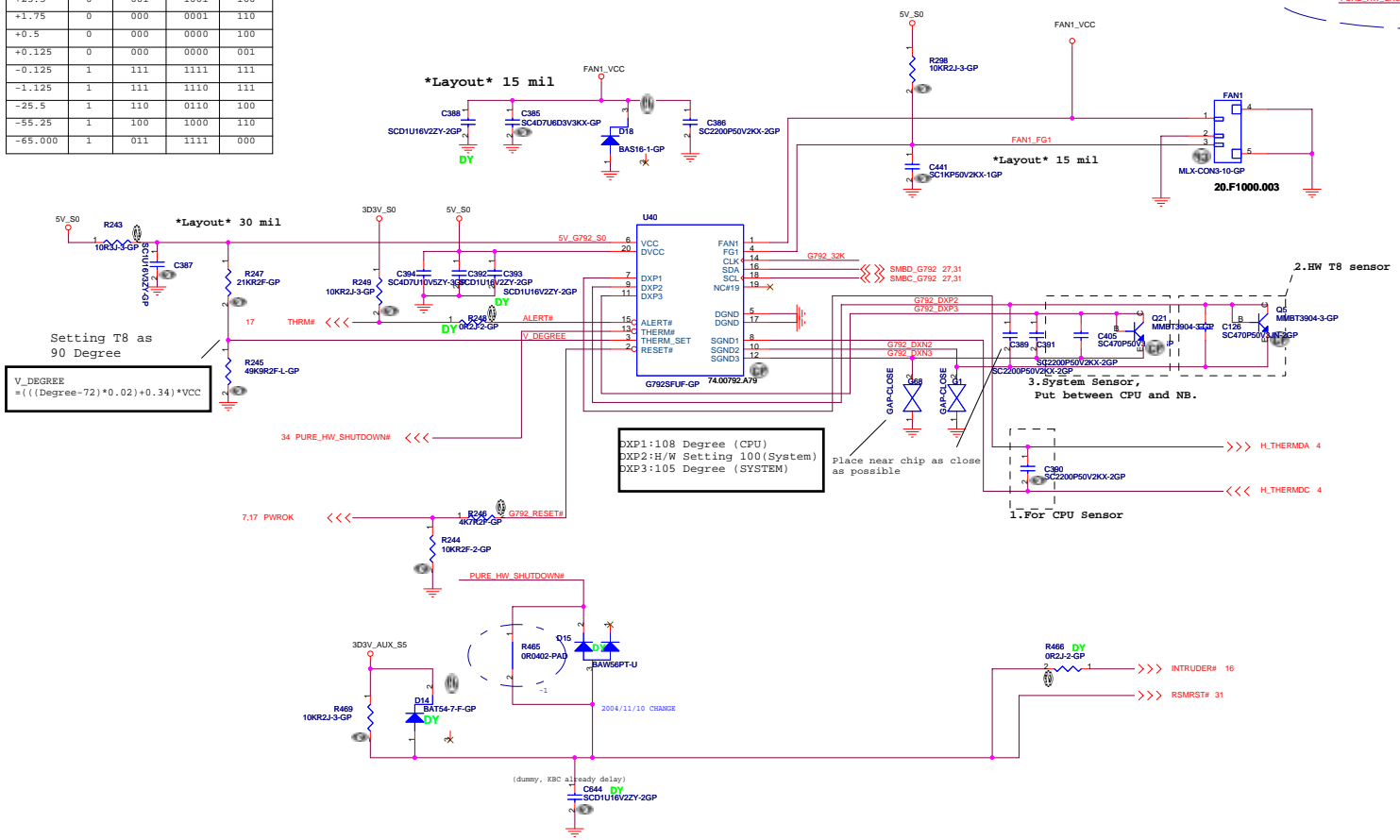
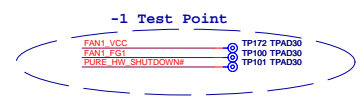


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBUS 2.0 compliance

SMBUS

<p>緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title: ICH8-M (4 of 4)</p>	
Size	Document Number
Date: Friday, April 27, 2007	Rev: -1
<p>Tahoe</p>	
Sheet 19	of 44

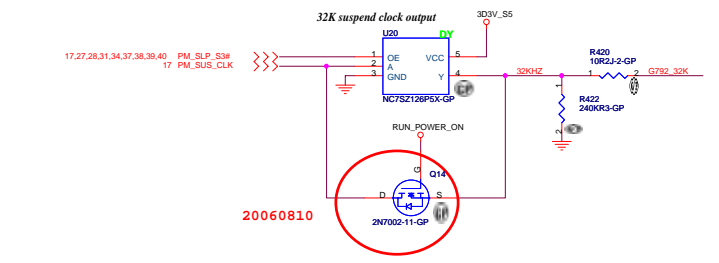
Temp	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	1111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

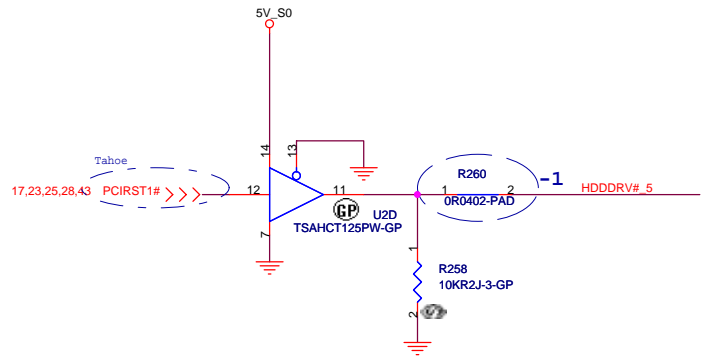
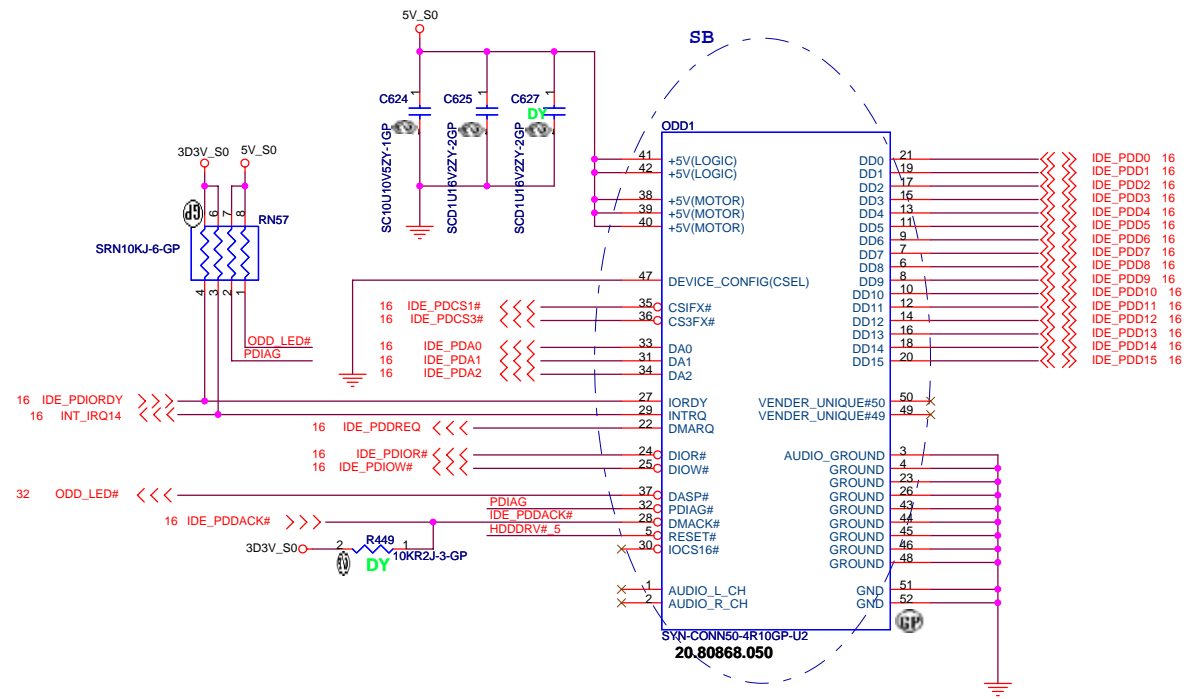
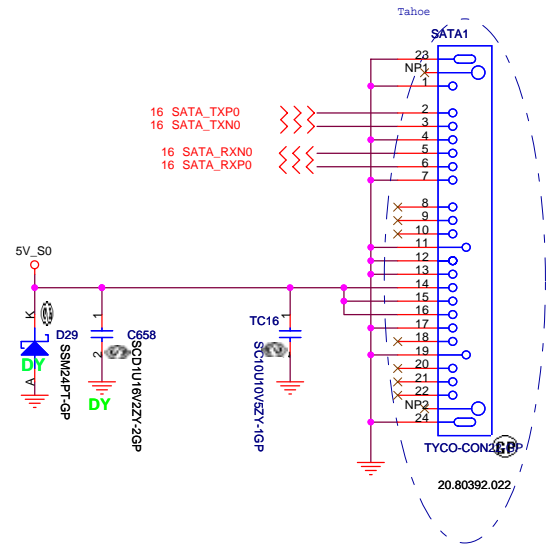


Setting T8 as 90 Degree
 $V_DEGREE = (((Degree-72)*0.02)+0.34)*VCC$

DXP1:108 Degree (CPU)
 DXP2:H/W Setting 100(System)
 DXP3:105 Degree (SYSTEM)

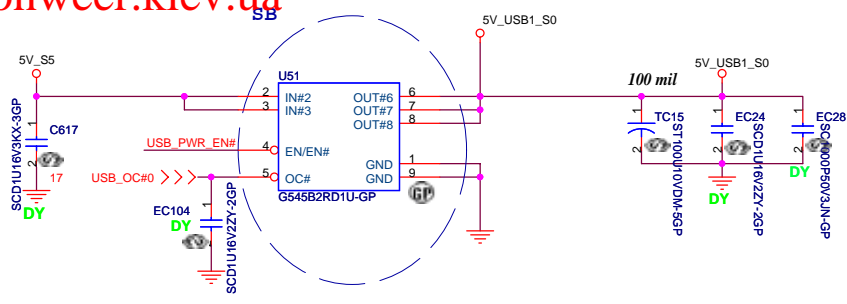
Place near chip as close as possible





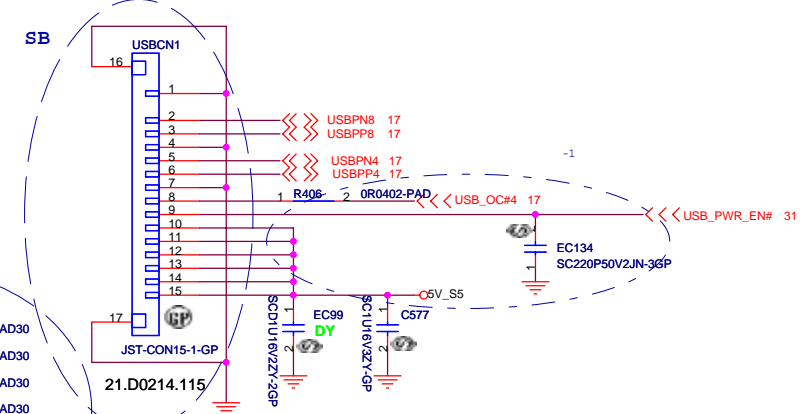
bom1

緯創資通		Wistron Corporation	
		21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
HDD and CDROM			
Title	Tahoe		Rev
Size	Document Number	Sheet	-1
Date: Friday, April 27, 2007		21	of 44

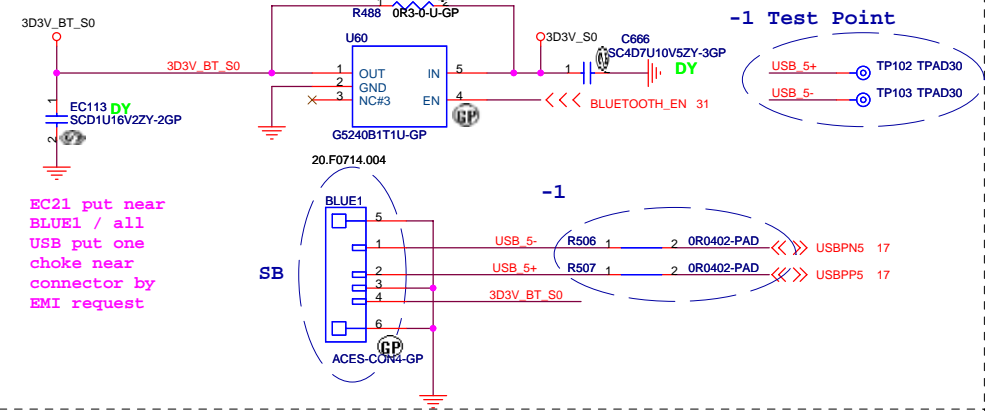


-1 Test Point

- 5V_S5 TP176 TPAD30
- 5V_S5 TP175 TPAD30
- USBPN8 TP104 TPAD30
- USBPP8 TP105 TPAD30
- USBPN4 TP106 TPAD30
- USBPP4 TP107 TPAD30
- USB_OC#4 TP108 TPAD30
- USB_PWR_EN# TP109 TPAD30

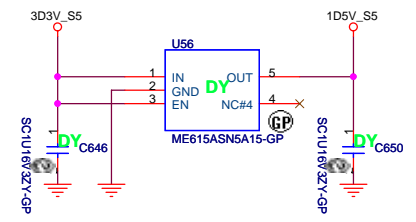
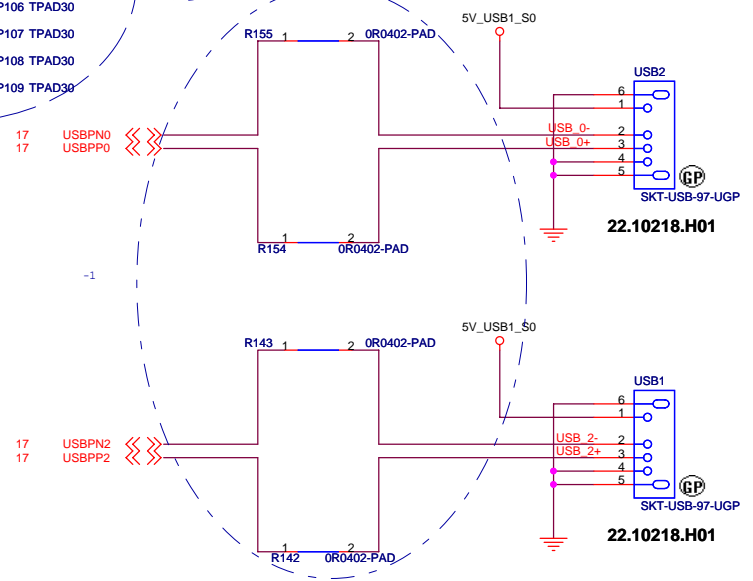
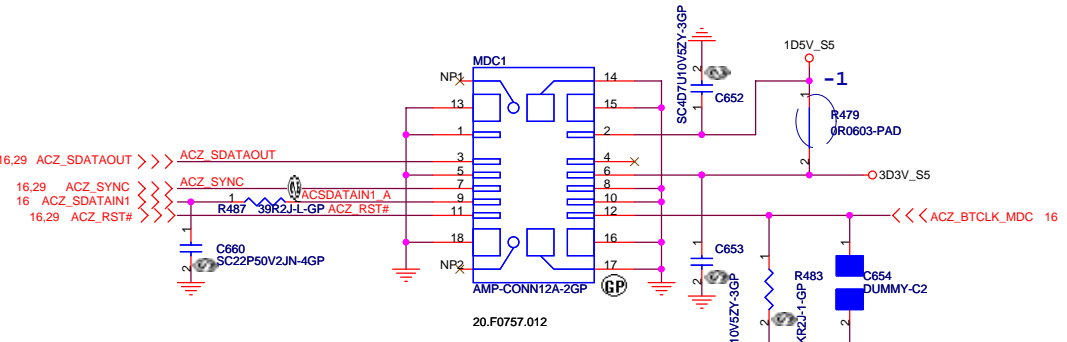


BLUETOOTH MODULE

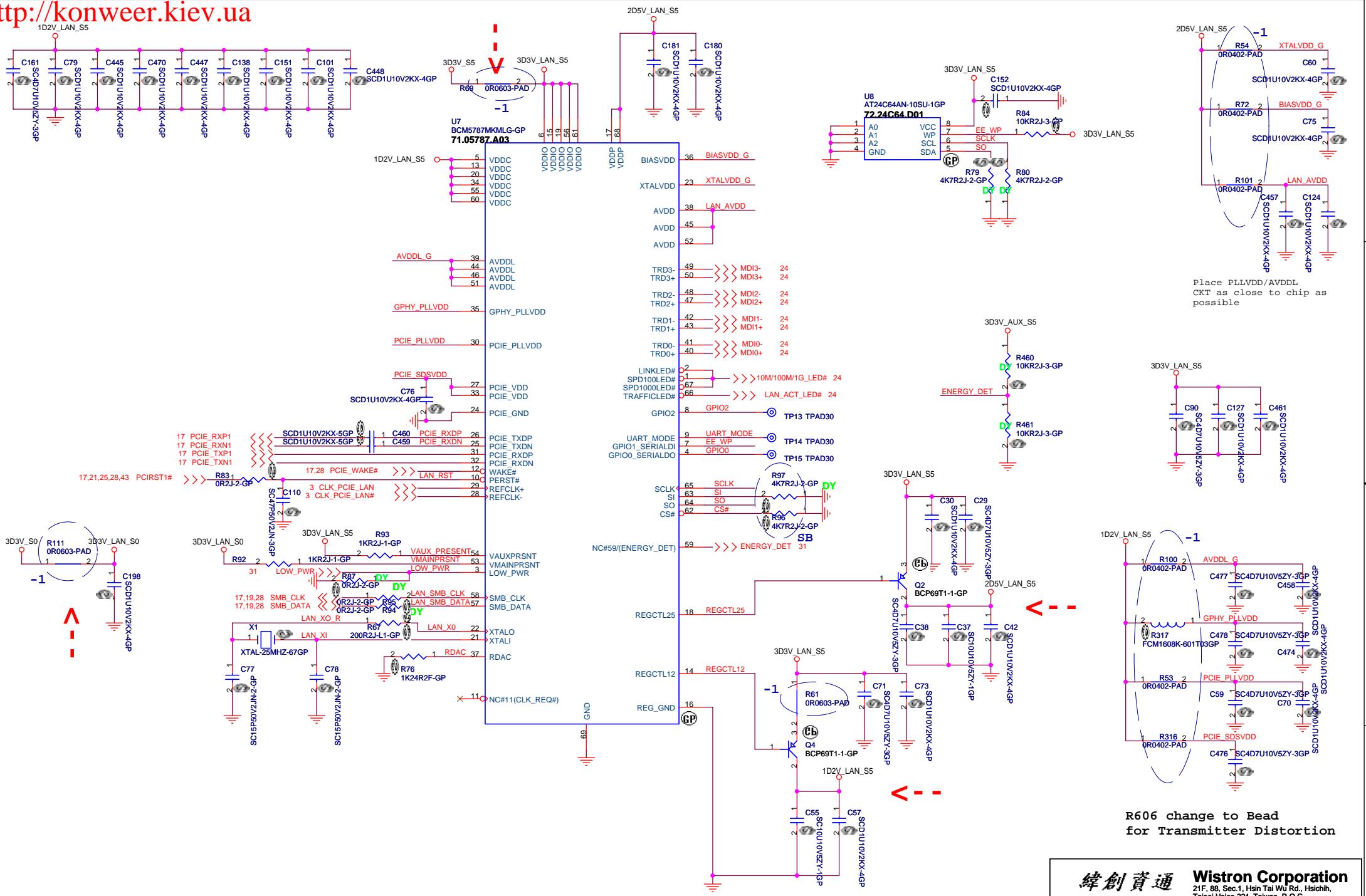


EC21 put near BLUE1 / all USB put one choke near connector by EMI request

MDC 1.5 CONN



		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB / MDC / BLUETOOTH			
File			
Size	Document Number	Rev	
		Tahoe	
Date:	Friday, April 27, 2007	Sheet	22 of 44



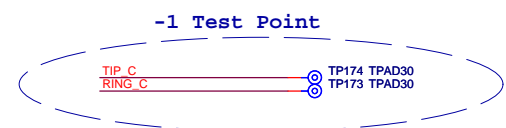
Place PLLVDD/AVDDL
CKT as close to chip as
possible

R606 change to Bead
for Transmitter Distortion

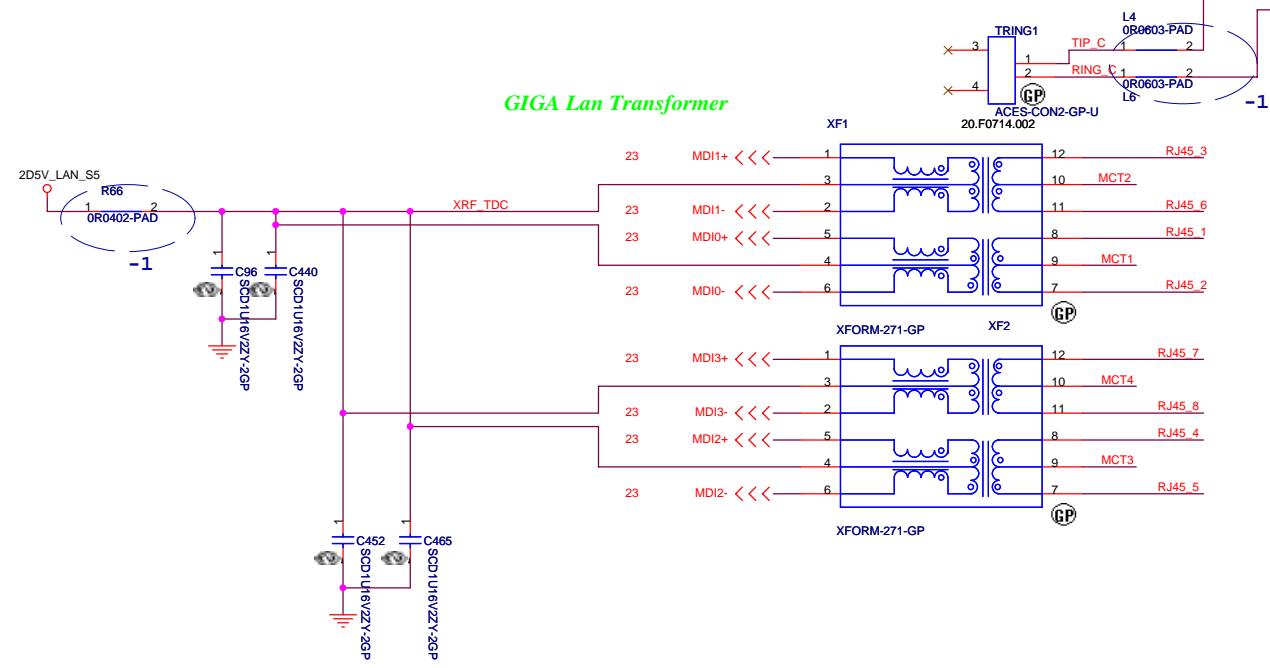
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	BCM5787MKMLG	
Size	Document Number	Rev
A3	Tahoe	-1
Date: Tuesday, May 08, 2007	Sheet 23	of 44

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector



GIGA Lan Transformer

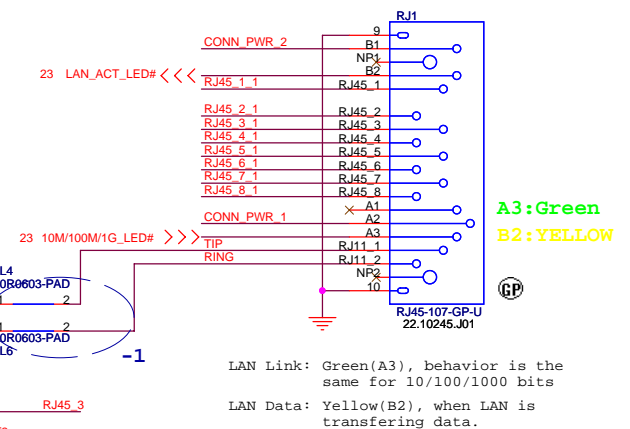
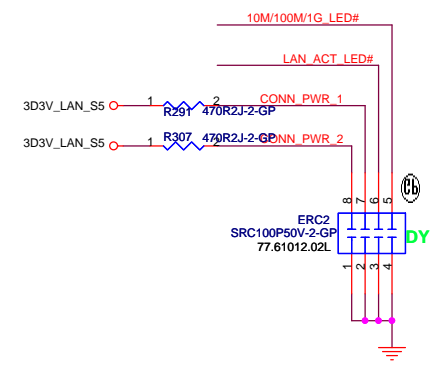
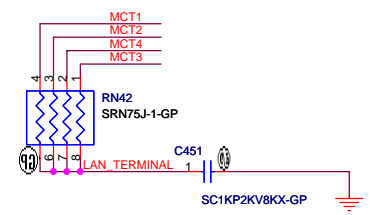


1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

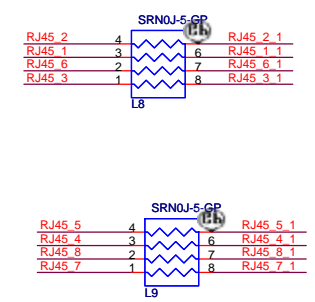
DOC_TIP, DOC_RING, TIP, RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

For EMI



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

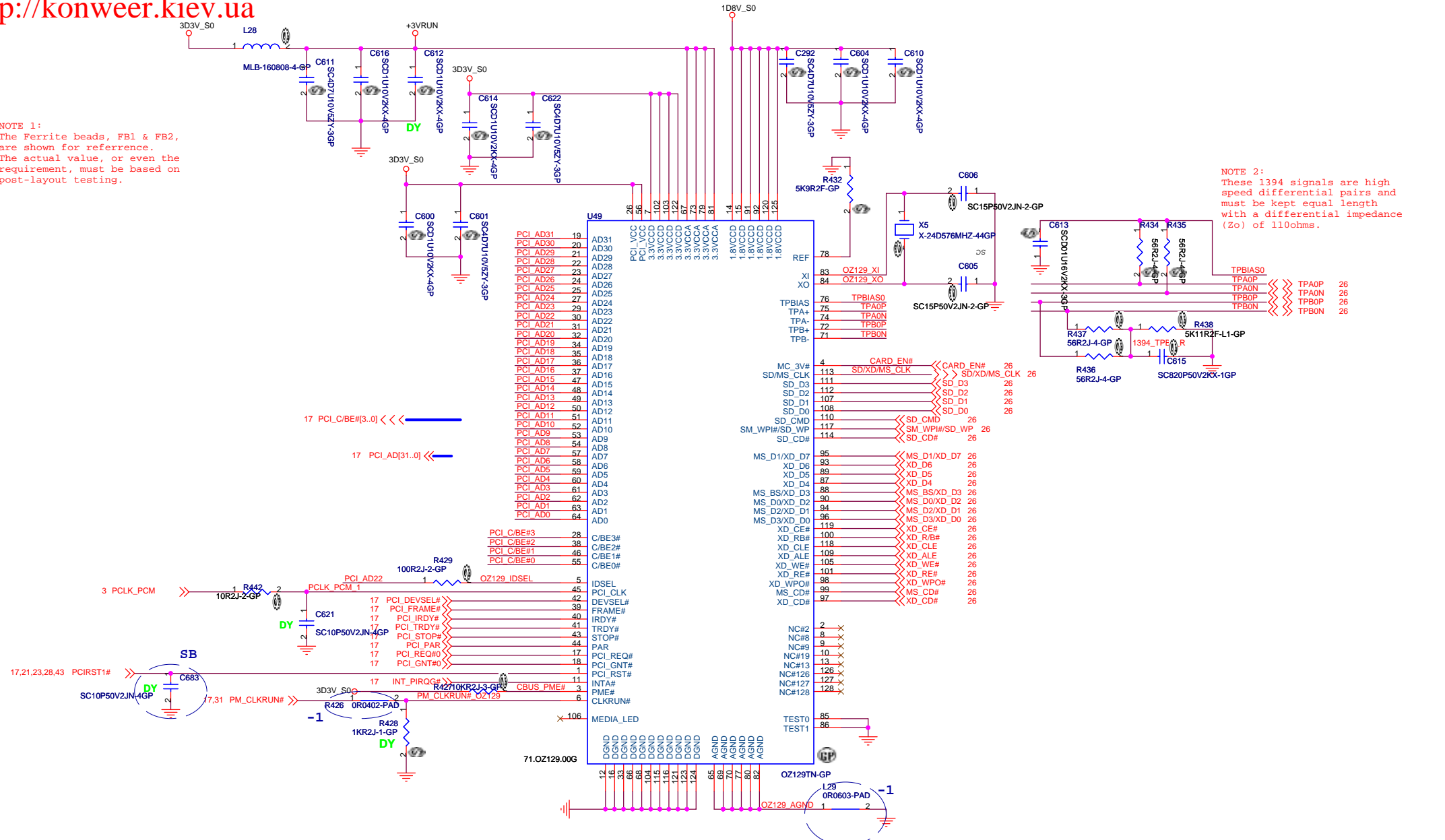
Title: **LAN Connector**

Size: A3 | Document Number: Tahoe | Rev: -1

Date: Friday, April 27, 2007 | Sheet: 24 of 44

NOTE 1:
The Ferrite beads, FB1 & FB2, are shown for reference. The actual value, or even the requirement, must be based on post-layout testing.

NOTE 2:
These I394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.



PCI_AD31	19	AD31
PCI_AD30	20	AD30
PCI_AD29	21	AD29
PCI_AD28	22	AD28
PCI_AD27	23	AD27
PCI_AD26	24	AD26
PCI_AD25	25	AD25
PCI_AD24	27	AD24
PCI_AD23	29	AD23
PCI_AD22	30	AD22
PCI_AD21	31	AD21
PCI_AD20	32	AD20
PCI_AD19	34	AD19
PCI_AD18	35	AD18
PCI_AD17	36	AD17
PCI_AD16	37	AD16
PCI_AD15	47	AD15
PCI_AD14	48	AD14
PCI_AD13	49	AD13
PCI_AD12	50	AD12
PCI_AD11	51	AD11
PCI_AD10	52	AD10
PCI_AD9	53	AD9
PCI_AD8	54	AD8
PCI_AD7	57	AD7
PCI_AD6	58	AD6
PCI_AD5	59	AD5
PCI_AD4	60	AD4
PCI_AD3	61	AD3
PCI_AD2	62	AD2
PCI_AD1	63	AD1
PCI_AD0	64	AD0
PCI_CBE#3	28	C/BE#3
PCI_CBE#2	38	C/BE#2
PCI_CBE#1	46	C/BE#1
PCI_CBE#0	55	C/BE#0
IDSEL	5	PCI_AD22
DEVSEL#	45	PCI_DEVSEL#
FRAME#	42	PCI_FRAME#
IRDY#	39	PCI_IRDY#
TRDY#	40	PCI_TRDY#
PAR	41	PCI_PAR
PCI_REQ#	43	PCI_STOP#
PCI_GNT#	44	PCI_REQ#
INTA#	17	INT_PIRQG#
INTB#	18	INT_PIRQG#
INTC#	19	INT_PIRQG#
INTD#	20	INT_PIRQG#
PMEN#	11	INT_PIRQG#
CLKRUN#	3	INT_PIRQG#
MEDIA_LED	6	INT_PIRQG#
DGND	12	AGND
DGND	13	AGND
DGND	14	AGND
DGND	15	AGND
DGND	16	AGND
DGND	17	AGND
DGND	18	AGND
DGND	19	AGND
DGND	20	AGND
DGND	21	AGND
DGND	22	AGND
DGND	23	AGND
DGND	24	AGND
DGND	25	AGND
DGND	26	AGND
DGND	27	AGND
DGND	28	AGND
DGND	29	AGND
DGND	30	AGND
DGND	31	AGND
DGND	32	AGND
DGND	33	AGND
DGND	34	AGND
DGND	35	AGND
DGND	36	AGND
DGND	37	AGND
DGND	38	AGND
DGND	39	AGND
DGND	40	AGND
DGND	41	AGND
DGND	42	AGND
DGND	43	AGND
DGND	44	AGND
DGND	45	AGND
DGND	46	AGND
DGND	47	AGND
DGND	48	AGND
DGND	49	AGND
DGND	50	AGND
DGND	51	AGND
DGND	52	AGND
DGND	53	AGND
DGND	54	AGND
DGND	55	AGND
DGND	56	AGND
DGND	57	AGND
DGND	58	AGND
DGND	59	AGND
DGND	60	AGND
DGND	61	AGND
DGND	62	AGND
DGND	63	AGND
DGND	64	AGND
DGND	65	AGND
DGND	66	AGND
DGND	67	AGND
DGND	68	AGND
DGND	69	AGND
DGND	70	AGND
DGND	71	AGND
DGND	72	AGND
DGND	73	AGND
DGND	74	AGND
DGND	75	AGND
DGND	76	AGND
DGND	77	AGND
DGND	78	AGND
DGND	79	AGND
DGND	80	AGND
DGND	81	AGND
DGND	82	AGND
DGND	83	AGND
DGND	84	AGND
DGND	85	AGND
DGND	86	AGND
DGND	87	AGND
DGND	88	AGND
DGND	89	AGND
DGND	90	AGND
DGND	91	AGND
DGND	92	AGND
DGND	93	AGND
DGND	94	AGND
DGND	95	AGND
DGND	96	AGND
DGND	97	AGND
DGND	98	AGND
DGND	99	AGND
DGND	100	AGND
DGND	101	AGND
DGND	102	AGND
DGND	103	AGND
DGND	104	AGND
DGND	105	AGND
DGND	106	AGND
DGND	107	AGND
DGND	108	AGND
DGND	109	AGND
DGND	110	AGND
DGND	111	AGND
DGND	112	AGND
DGND	113	AGND
DGND	114	AGND
DGND	115	AGND
DGND	116	AGND
DGND	117	AGND
DGND	118	AGND
DGND	119	AGND
DGND	120	AGND
DGND	121	AGND
DGND	122	AGND
DGND	123	AGND
DGND	124	AGND
DGND	125	AGND
DGND	126	AGND
DGND	127	AGND
DGND	128	AGND
DGND	129	AGND
DGND	130	AGND
DGND	131	AGND
DGND	132	AGND
DGND	133	AGND
DGND	134	AGND
DGND	135	AGND
DGND	136	AGND
DGND	137	AGND
DGND	138	AGND
DGND	139	AGND
DGND	140	AGND
DGND	141	AGND
DGND	142	AGND
DGND	143	AGND
DGND	144	AGND
DGND	145	AGND
DGND	146	AGND
DGND	147	AGND
DGND	148	AGND
DGND	149	AGND
DGND	150	AGND
DGND	151	AGND
DGND	152	AGND
DGND	153	AGND
DGND	154	AGND
DGND	155	AGND
DGND	156	AGND
DGND	157	AGND
DGND	158	AGND
DGND	159	AGND
DGND	160	AGND
DGND	161	AGND
DGND	162	AGND
DGND	163	AGND
DGND	164	AGND
DGND	165	AGND
DGND	166	AGND
DGND	167	AGND
DGND	168	AGND
DGND	169	AGND
DGND	170	AGND
DGND	171	AGND
DGND	172	AGND
DGND	173	AGND
DGND	174	AGND
DGND	175	AGND
DGND	176	AGND
DGND	177	AGND
DGND	178	AGND
DGND	179	AGND
DGND	180	AGND
DGND	181	AGND
DGND	182	AGND
DGND	183	AGND
DGND	184	AGND
DGND	185	AGND
DGND	186	AGND
DGND	187	AGND
DGND	188	AGND
DGND	189	AGND
DGND	190	AGND
DGND	191	AGND
DGND	192	AGND
DGND	193	AGND
DGND	194	AGND
DGND	195	AGND
DGND	196	AGND
DGND	197	AGND
DGND	198	AGND
DGND	199	AGND
DGND	200	AGND

IDSEL:AD22
INTA-->:INT_PIRQG#
GNT:PCI_GNT#0
REQ:PCI_REQ#0

<Variant Name>

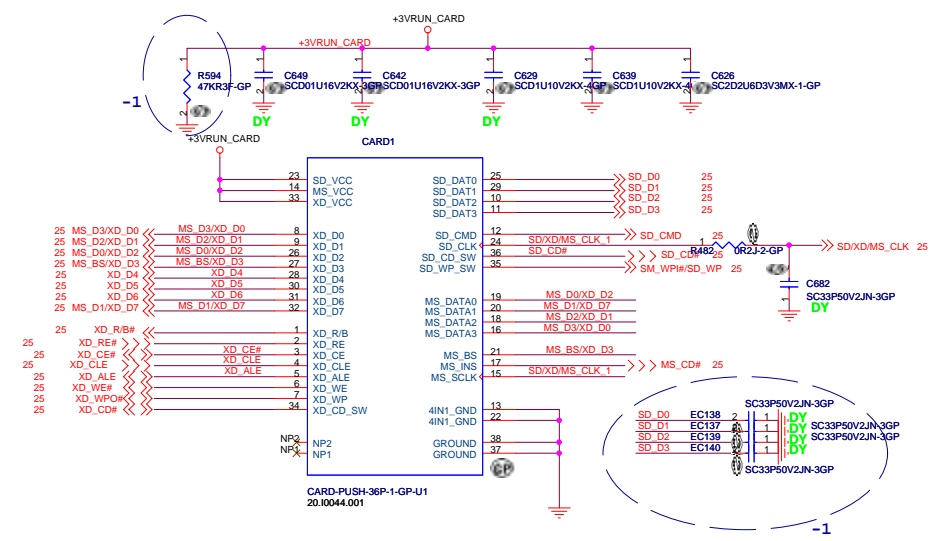
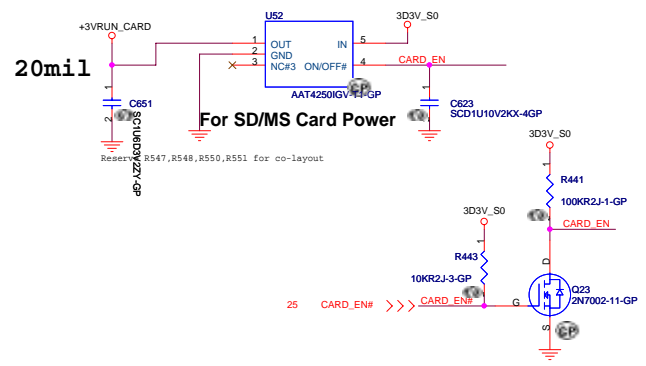
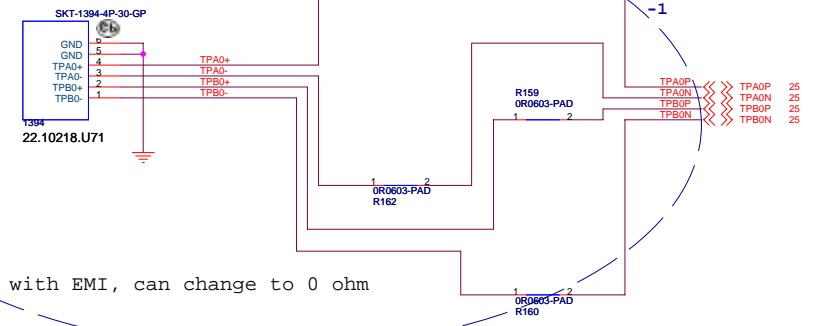
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **OZ129T**

Size: Document Number: Tahoe Rev: -1

Date: Friday, April 27, 2007 Sheet 25 of 44

1394 Connector



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

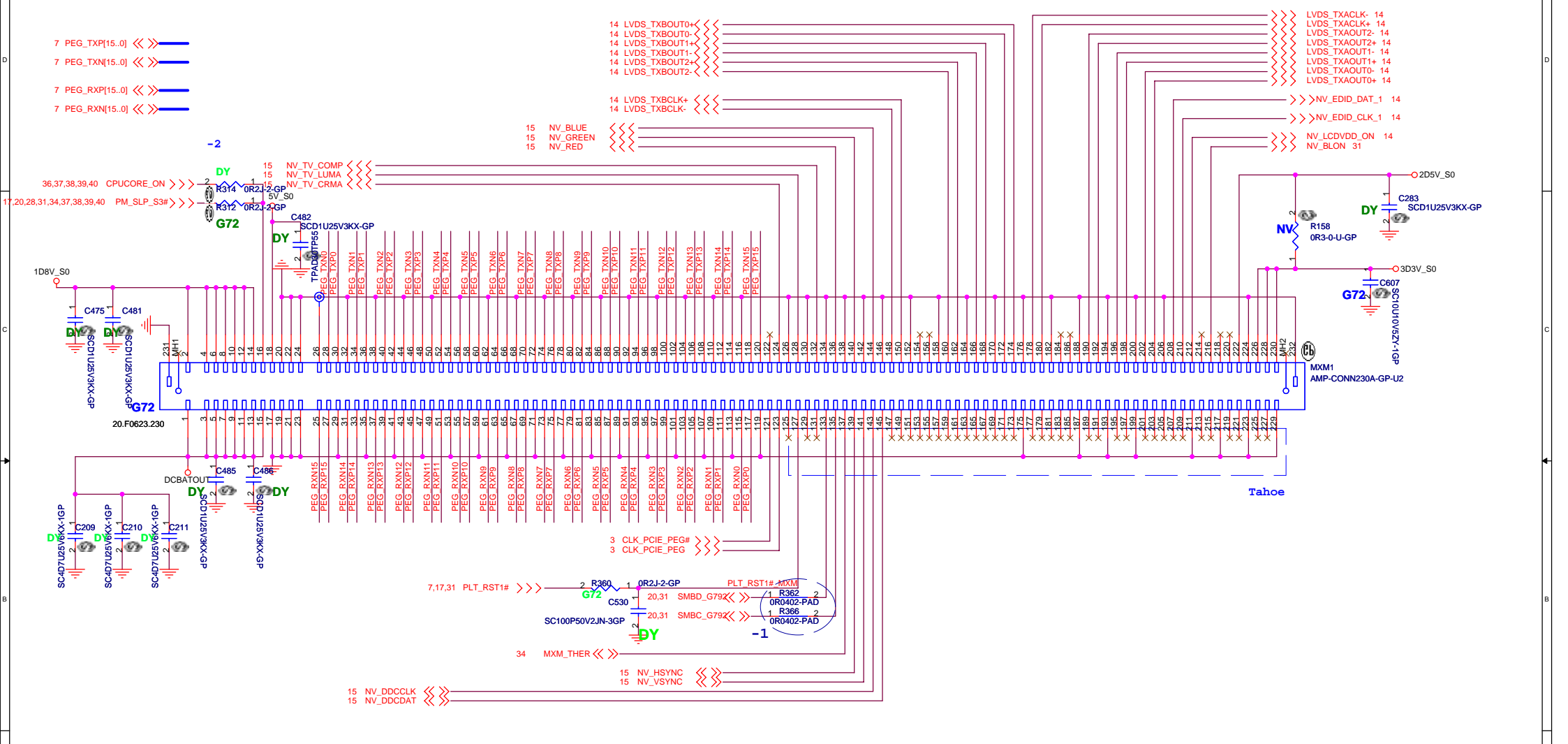
Title: **1394 / CARD READER**

Size: Document Number: Tahoe Rev: -1

Date: Friday, April 27, 2007 Sheet: 26 of 44

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector



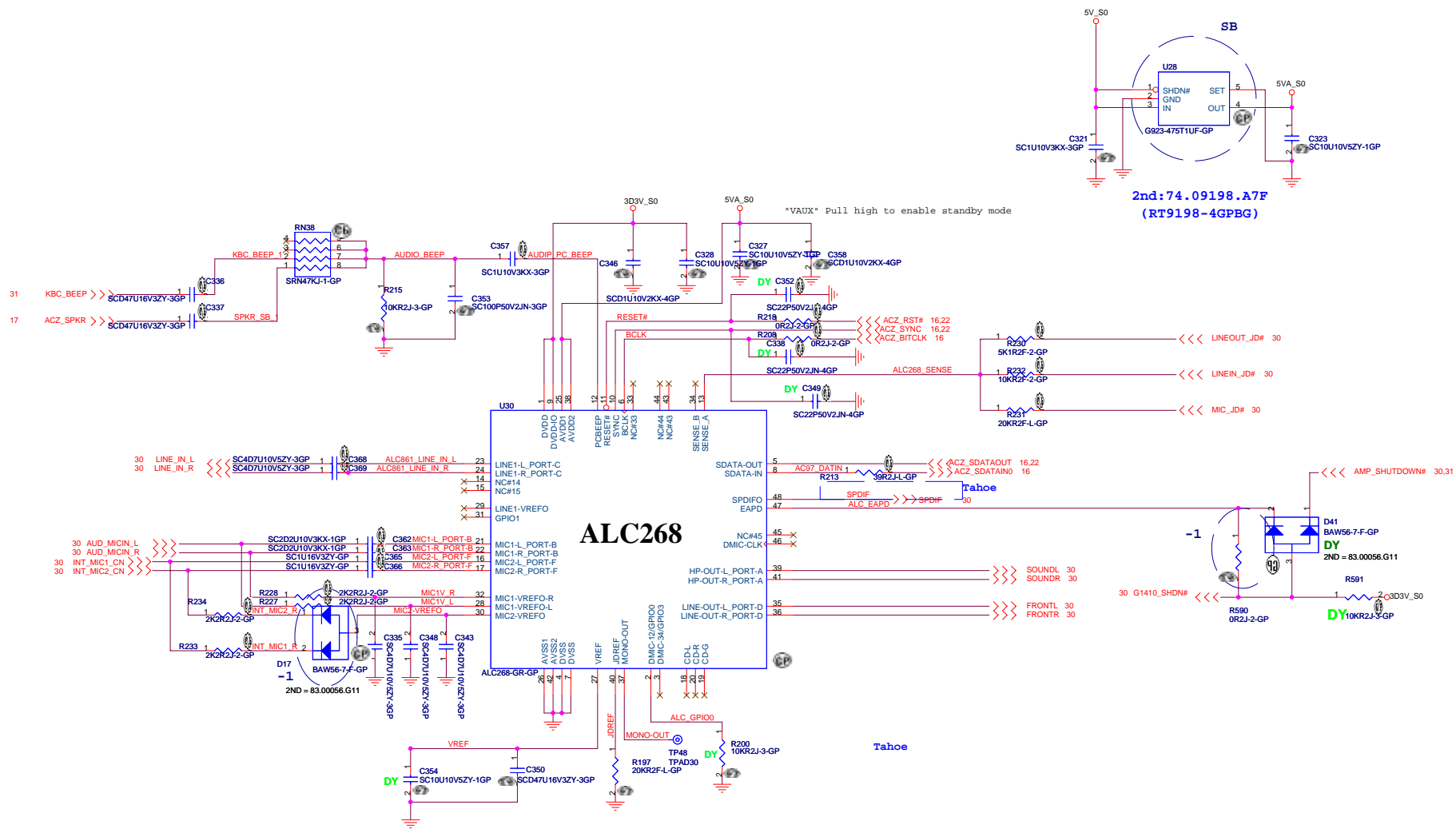
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Graphic MXM CONN**

Size: A3 Document Number: **Tahoe** Rev: **-1**

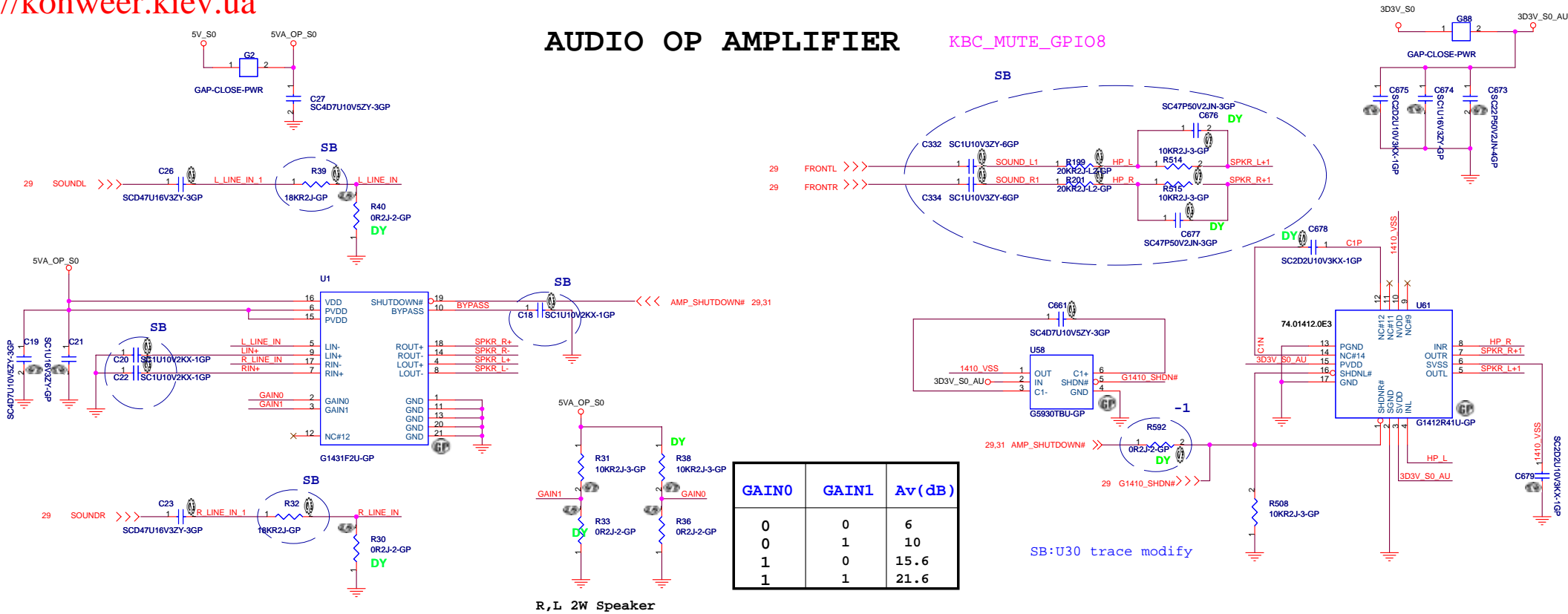
Date: Friday, April 27, 2007 Sheet 27 of 44



2nd: 74.09198.A7F (RT9198-4GPBG)

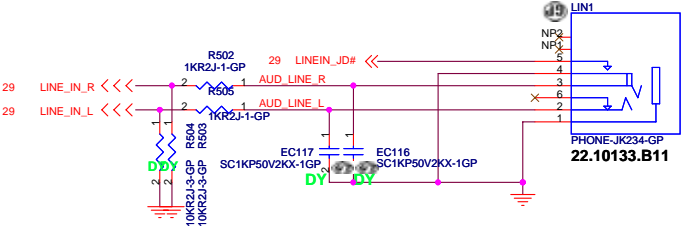
AUDIO OP AMPLIFIER

KBC_MUTE_GPIO8

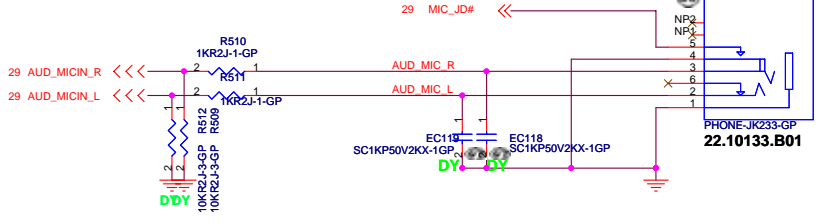


R,L 2W Speaker

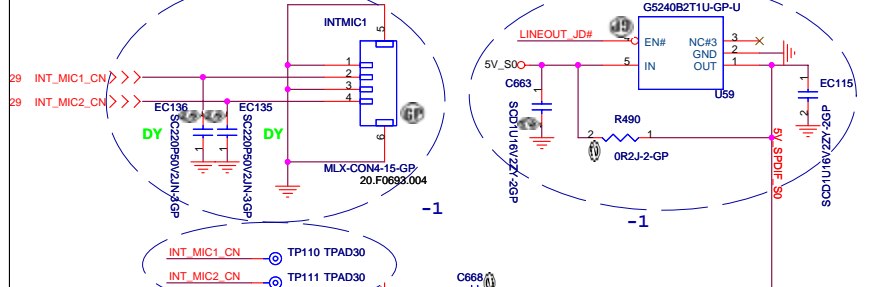
LINE IN



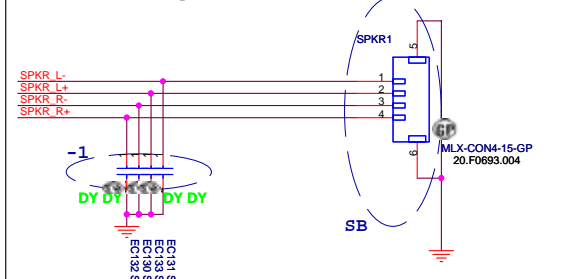
MIC IN



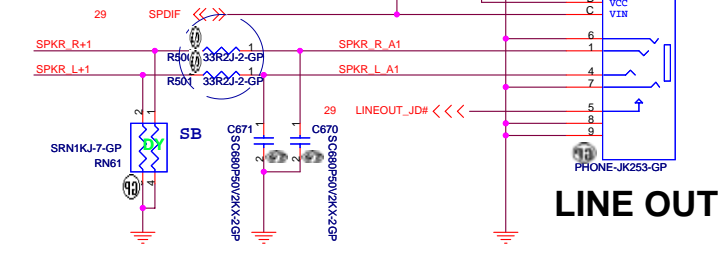
Internal Microphone



Internal Speaker



-1 Test Point



-1 Test Point



<Variant Name>

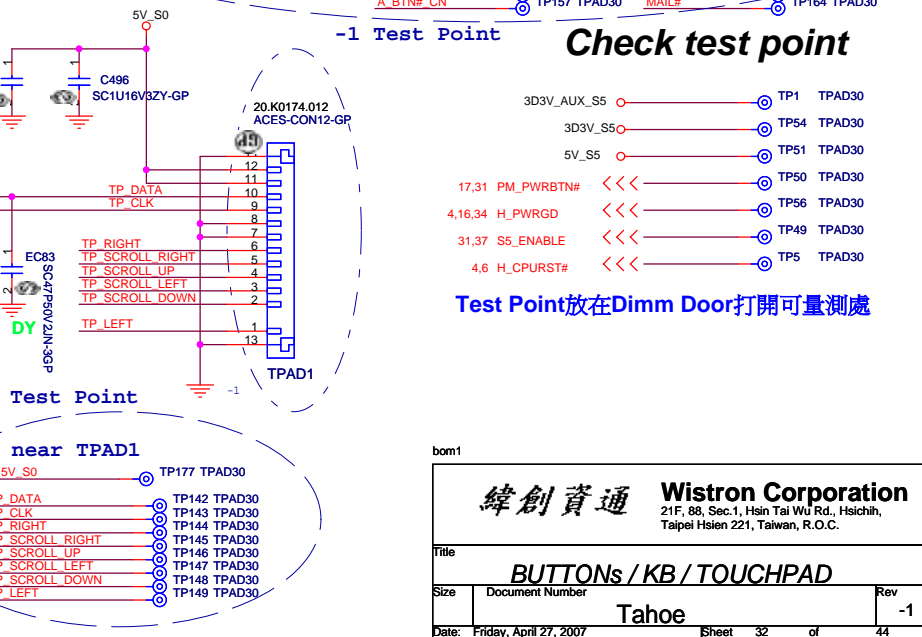
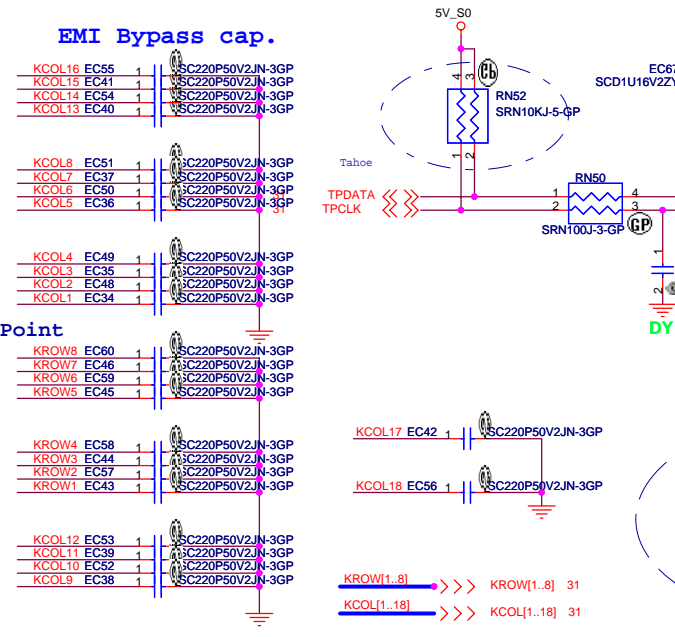
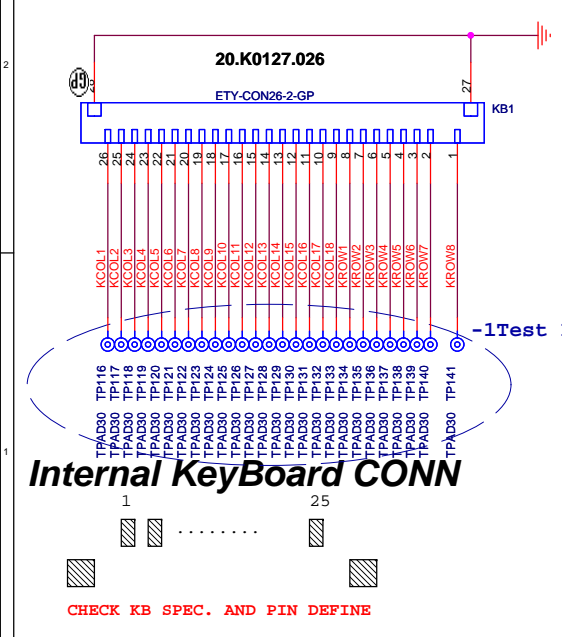
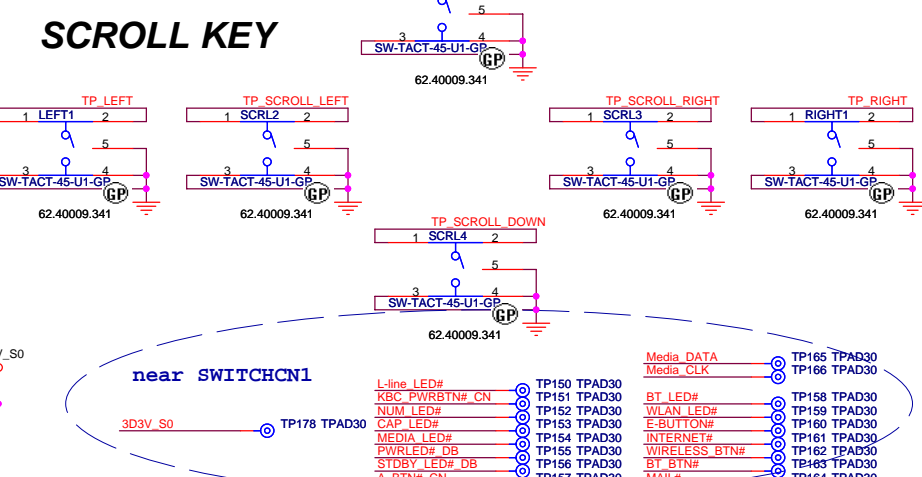
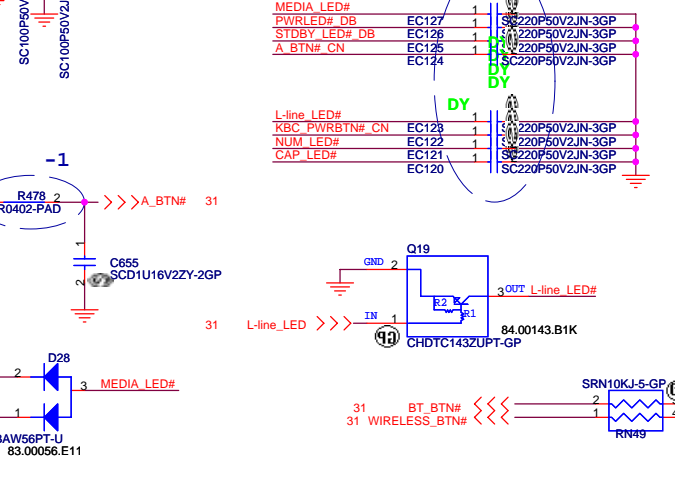
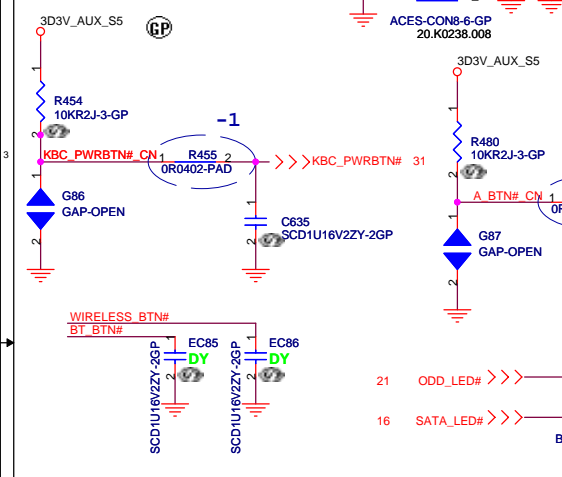
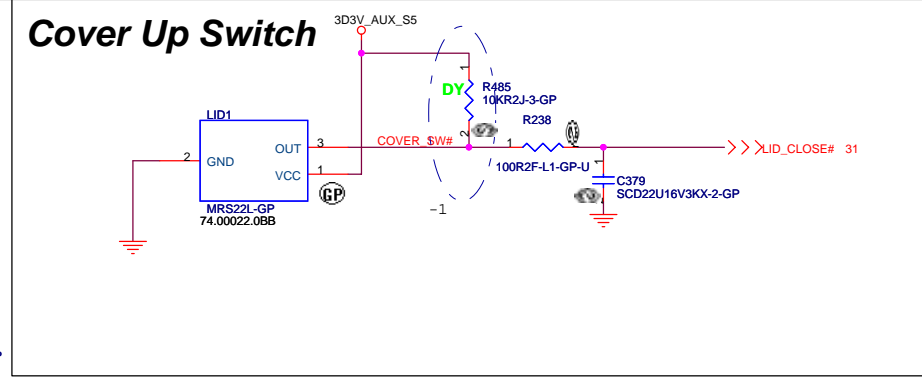
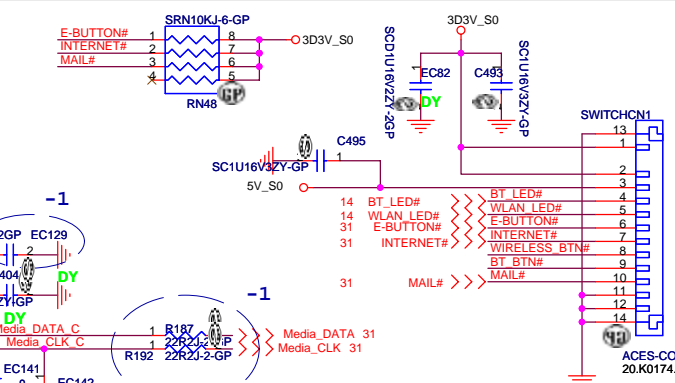
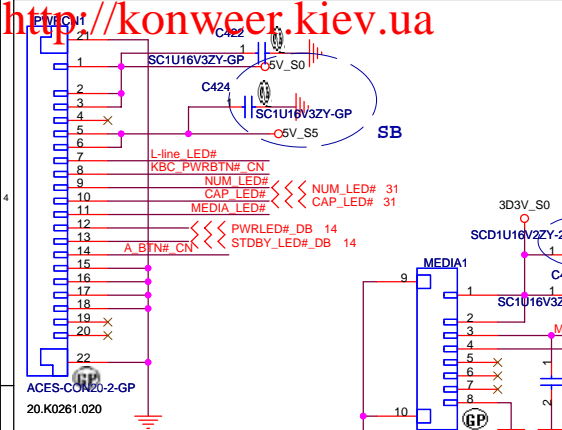
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP AND JACK**

Size: Document Number
Date: Friday, April 27, 2007

Sheet 30 of 44

Rev: -1



Check test point

3D3V_AUX_S5	TP1	TPAD30
3D3V_S5	TP54	TPAD30
5V_S5	TP51	TPAD30
17,31 PM_PWRBTN#	TP50	TPAD30
4,16,34 H_PWRGD	TP56	TPAD30
31,37 SS_ENABLE	TP49	TPAD30
4,6 H_CUPRST#	TP5	TPAD30

Test Point放在Dimm Door打開可量測處

20.K0174.012 ACES-CON12-GP

near TPAD1

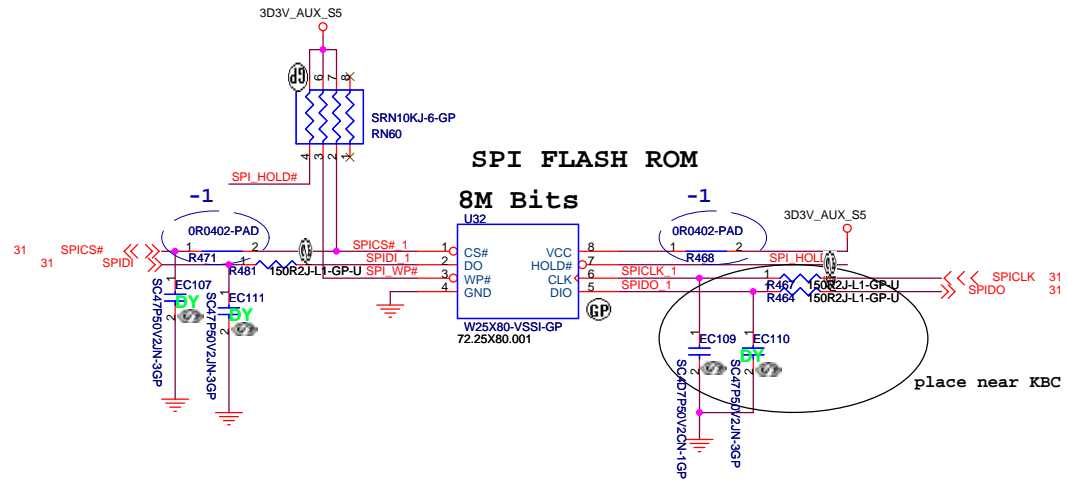
TP DATA	TP142	TPAD30
TP CLK	TP143	TPAD30
TP RIGHT	TP144	TPAD30
TP SCROLL_RIGHT	TP145	TPAD30
TP SCROLL_UP	TP146	TPAD30
TP SCROLL_LEFT	TP147	TPAD30
TP SCROLL_DOWN	TP148	TPAD30
TP LEFT	TP149	TPAD30

20.K0127.026 ETY-CON26-2-GP

Internal Keyboard CONN

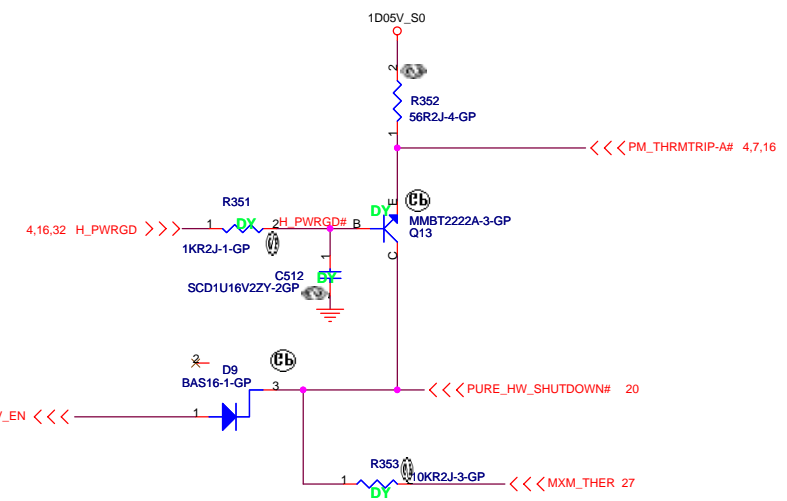
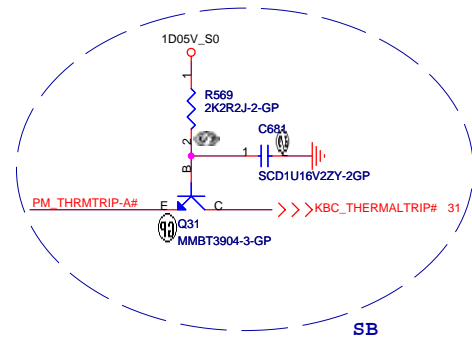
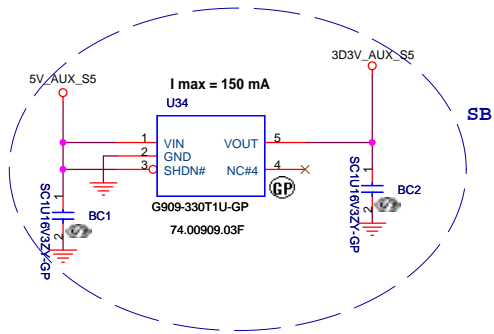
TPAD30	TP116	TPAD30
TPAD30	TP117	TPAD30
TPAD30	TP118	TPAD30
TPAD30	TP119	TPAD30
TPAD30	TP120	TPAD30
TPAD30	TP121	TPAD30
TPAD30	TP122	TPAD30
TPAD30	TP123	TPAD30
TPAD30	TP124	TPAD30
TPAD30	TP125	TPAD30
TPAD30	TP126	TPAD30
TPAD30	TP127	TPAD30
TPAD30	TP128	TPAD30
TPAD30	TP129	TPAD30
TPAD30	TP130	TPAD30
TPAD30	TP131	TPAD30
TPAD30	TP132	TPAD30
TPAD30	TP133	TPAD30
TPAD30	TP134	TPAD30
TPAD30	TP135	TPAD30
TPAD30	TP136	TPAD30
TPAD30	TP137	TPAD30
TPAD30	TP138	TPAD30
TPAD30	TP139	TPAD30
TPAD30	TP140	TPAD30
TPAD30	TP141	TPAD30

Check KB SPEC. AND PIN DEFINE

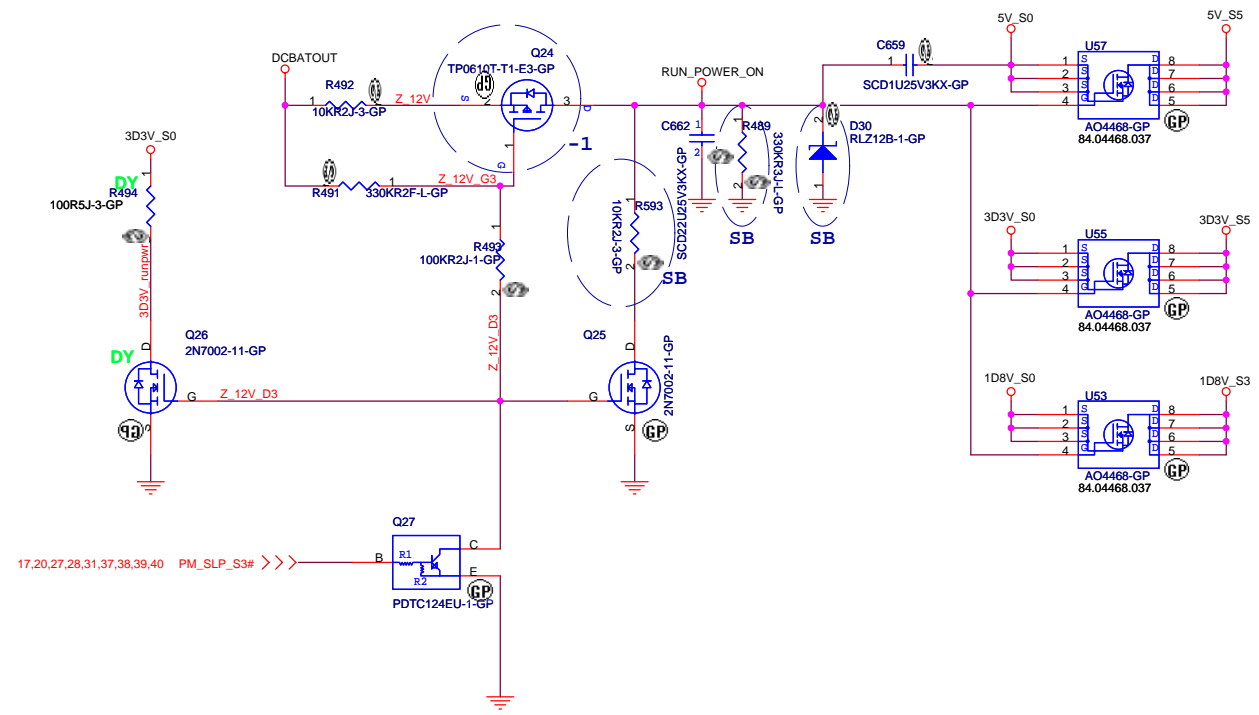


<Variant Name>

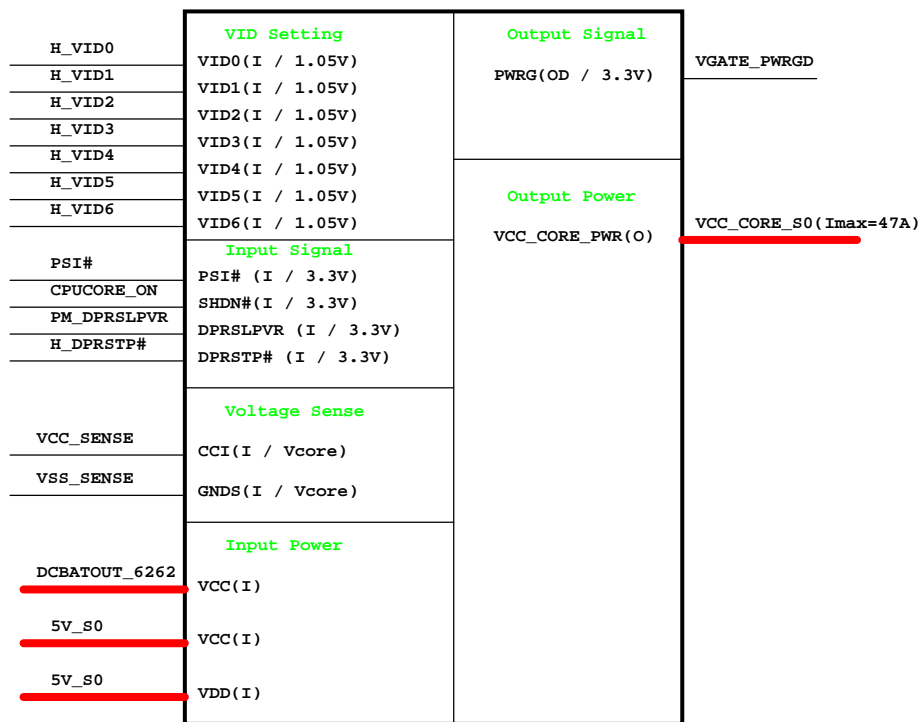
緯創資通		Wistron Corporation	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
BIOS			
Size	Document Number		Rev
A3	Tahoe		-1
Date: Friday, April 27, 2007		Sheet 33	of 44



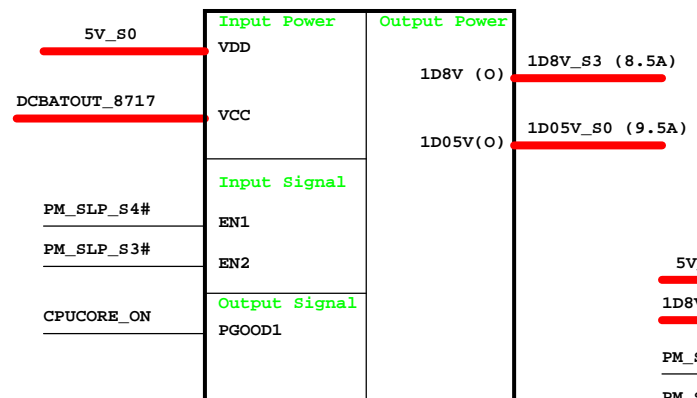
Run Power



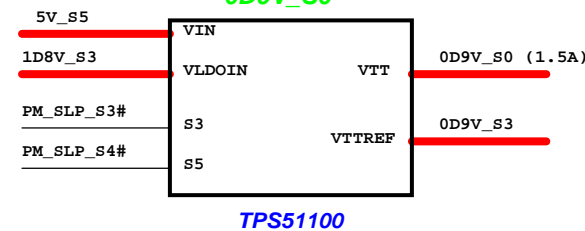
**CPU_CORE
MAX8770**



**MAX8717
1D8V/1D05V**

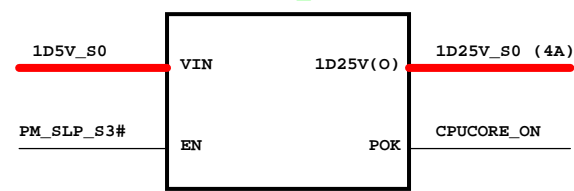


0D9V_S0



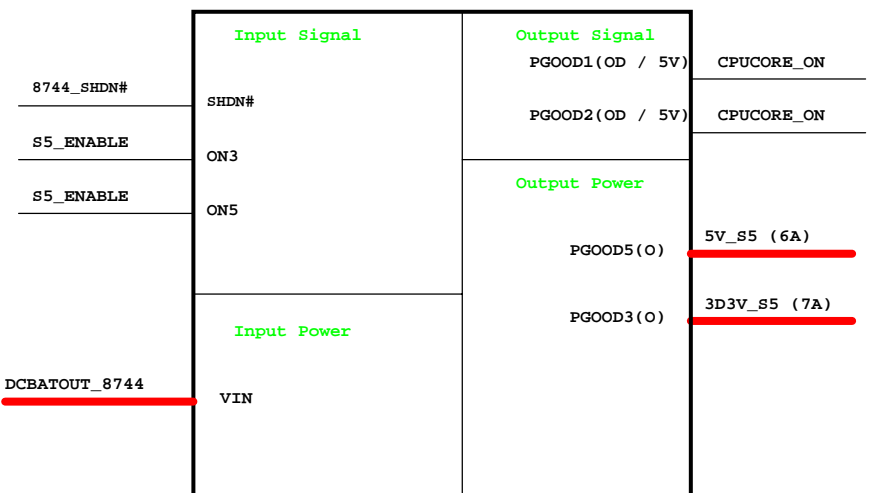
TPS51100

1D25V_S0

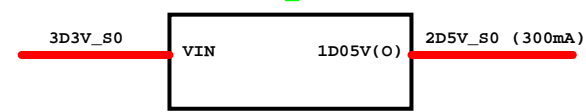


APL5915

**MAX8744
5V/3D3V**

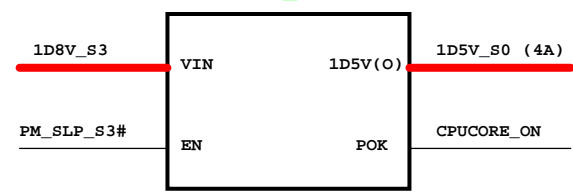


2D5V_S0



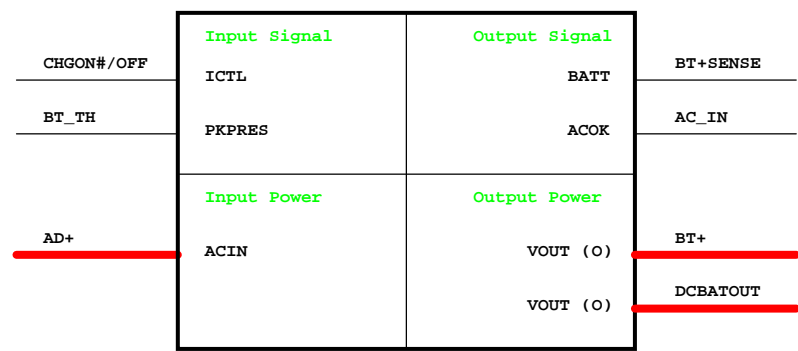
APL5308

1D5V_S0



APL5912

Charger ISL6255



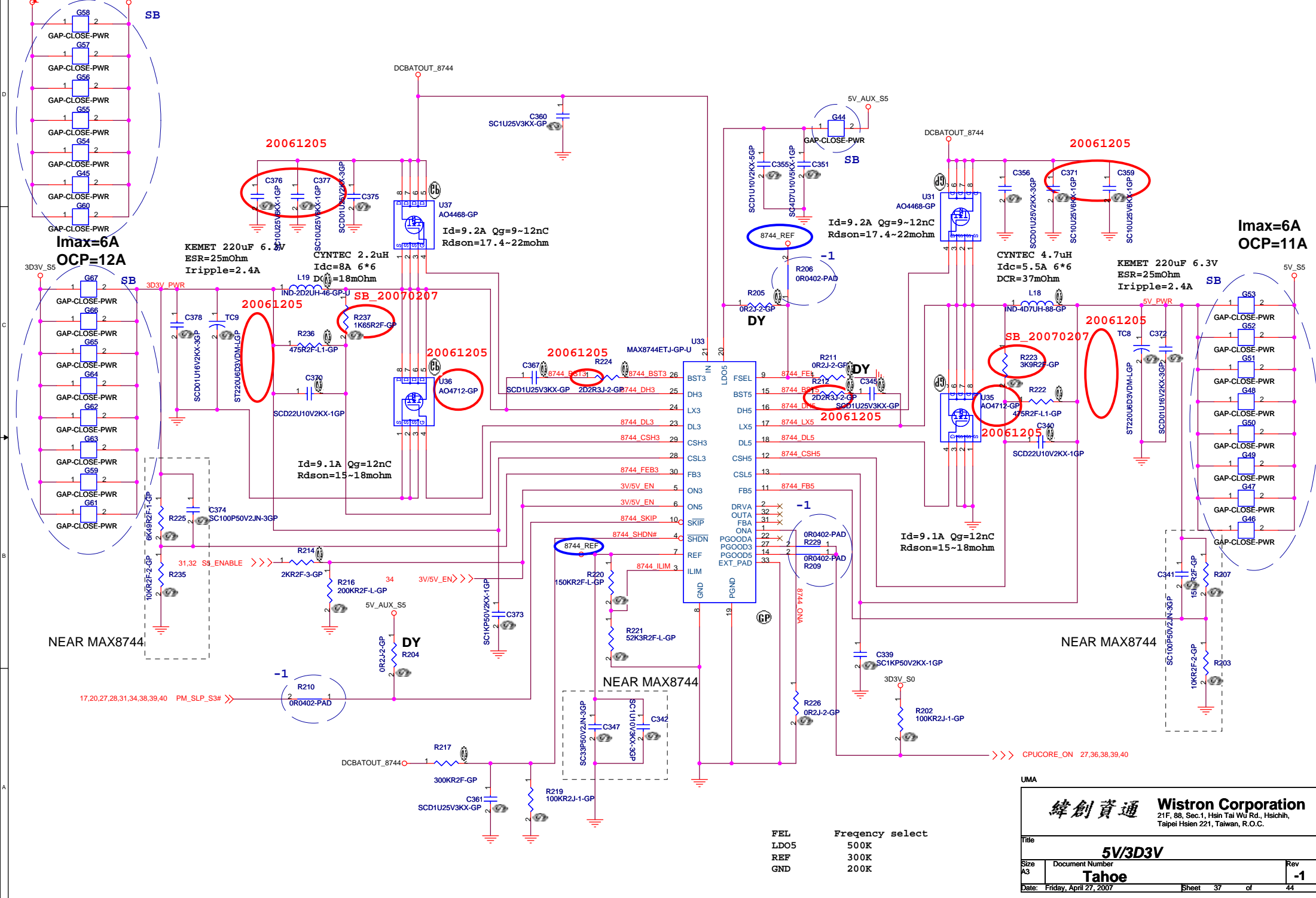
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size: A3 Document Number: **Tahoe** Rev: -1

Date: Friday, April 27, 2007 Sheet 35 of 44



I_{max}=6A
OCP=11A

FEL	Frequency select
LDO5	500K
REF	300K
GND	200K

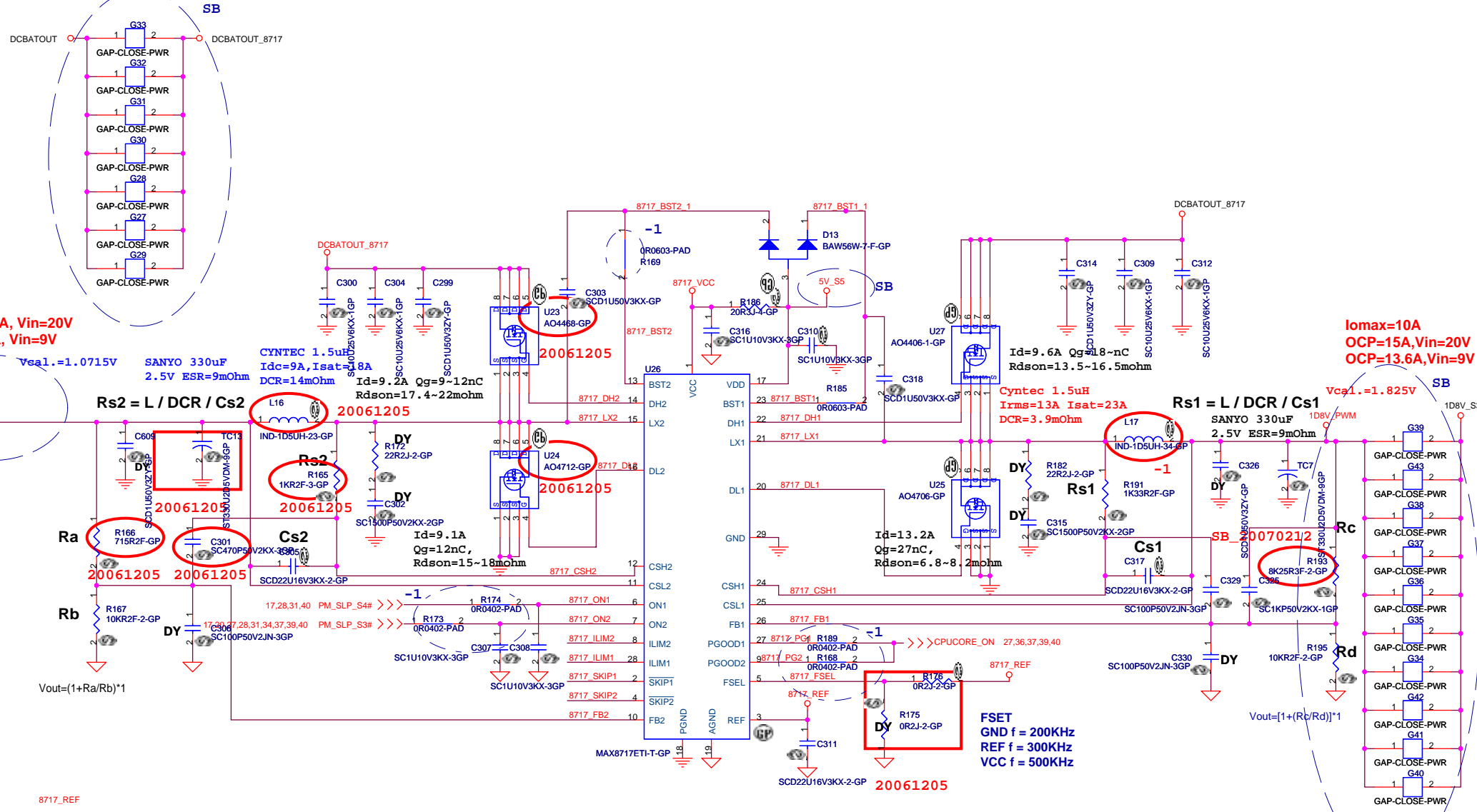
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **5V/3D3V**

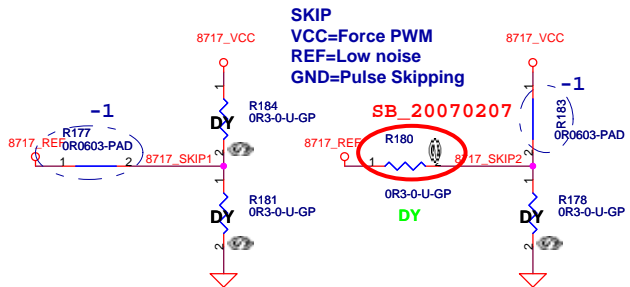
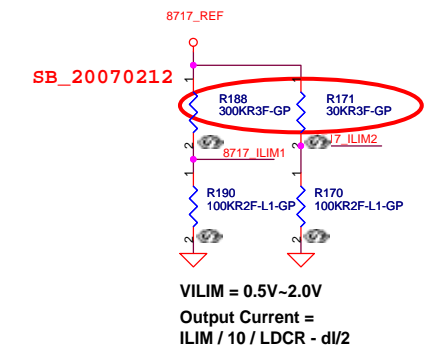
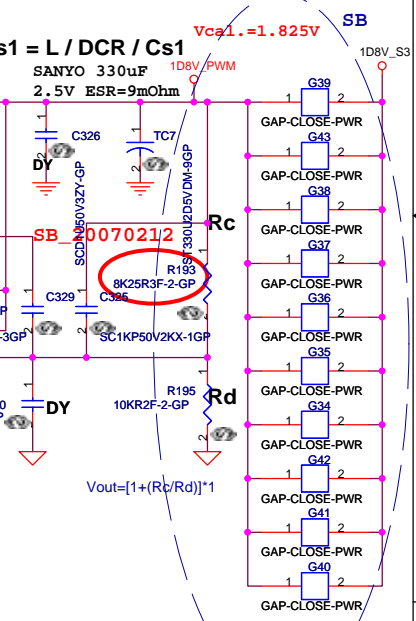
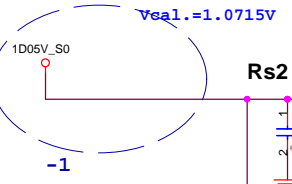
Size A3	Document Number	Rev
	Tahoe	-1

Date: Friday, April 27, 2007 Sheet 37 of 44

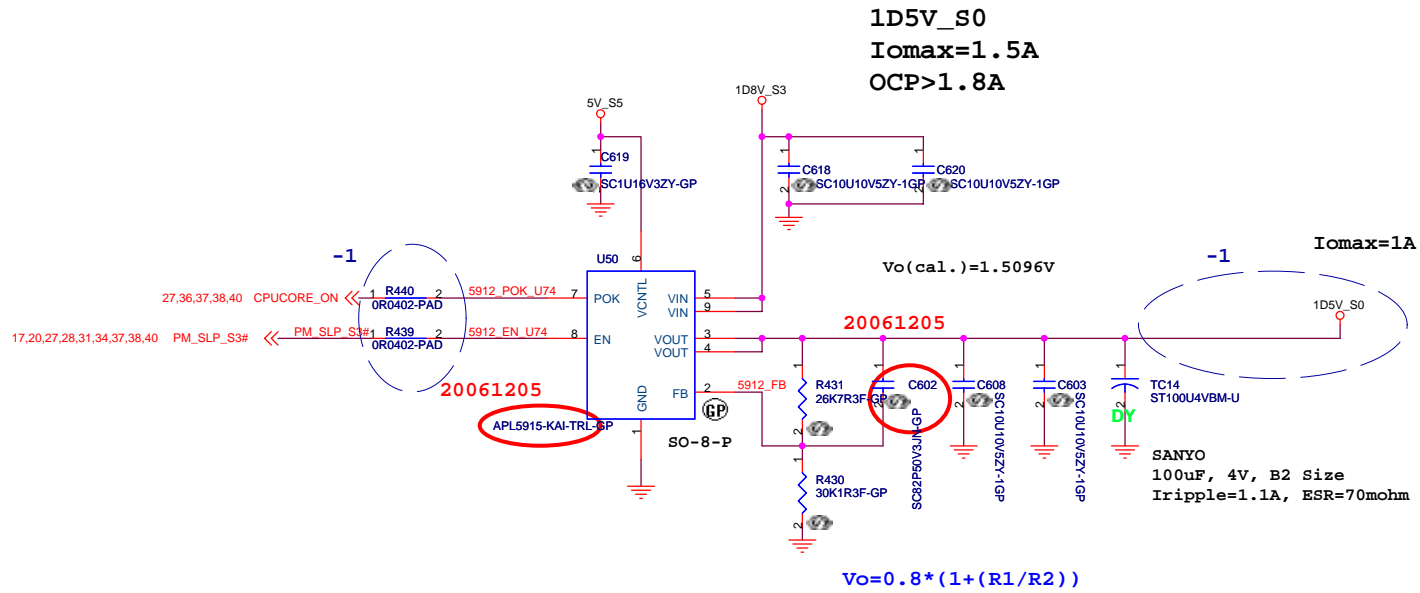


I_{omax}=6A
OCP=10.32A, Vin=20V
OCP=9.52A, Vin=9V

I_{omax}=10A
OCP=15A, Vin=20V
OCP=13.6A, Vin=9V



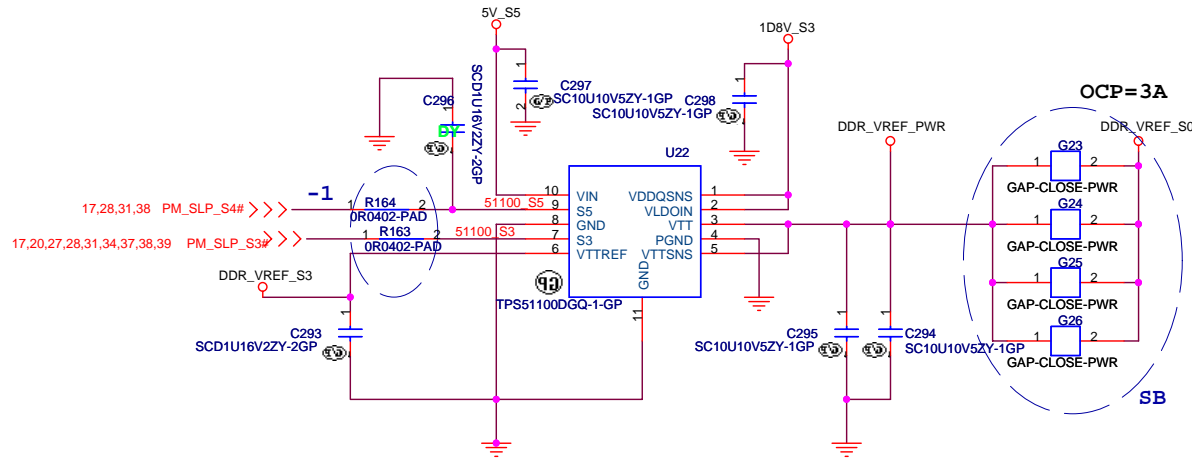
FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz



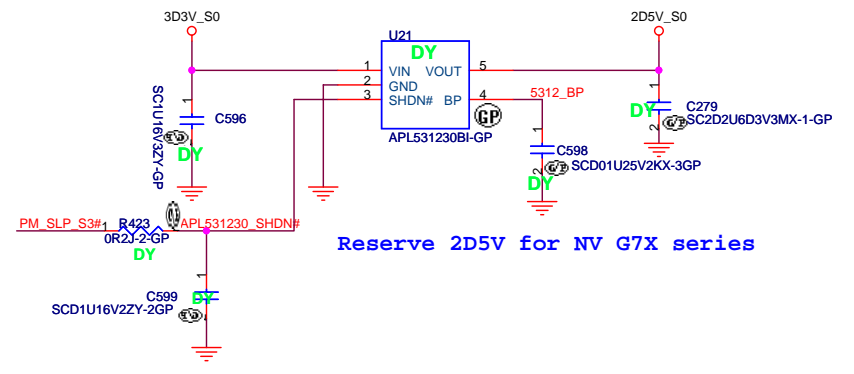
UMA

緯創資通 Wistron Corporation	
<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title APW5912_1D5V	
Size	Document Number
Tahoe	
Date: Friday, April 27, 2007	Rev -1
Sheet 39	of 44

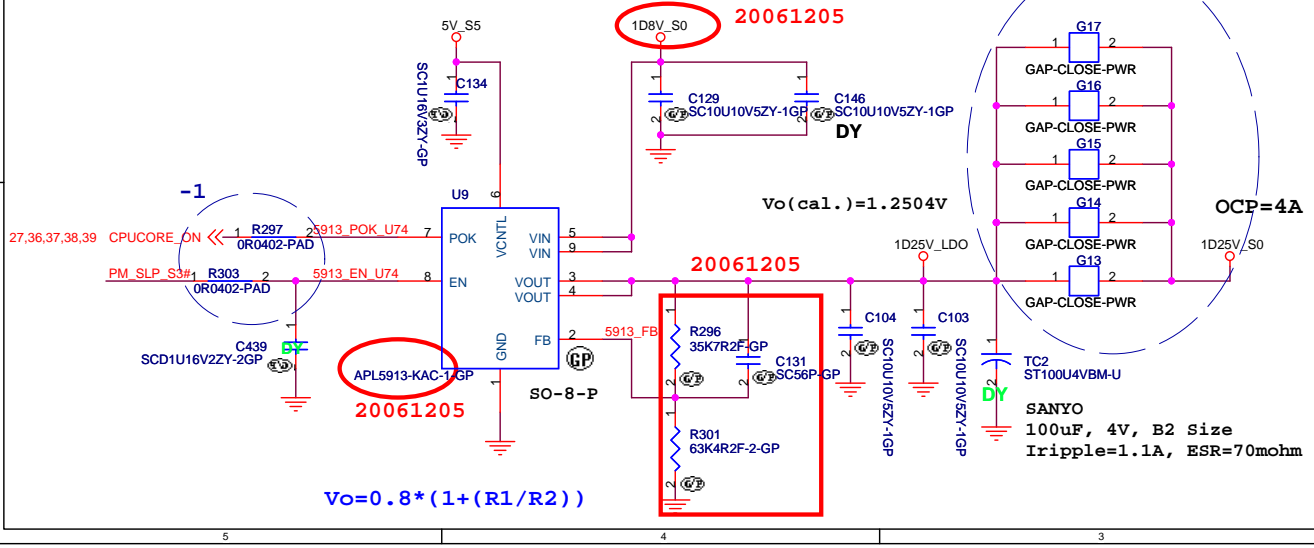
0D9V_S3
Iomax=0.5A



2D5V
Iomax=130mA

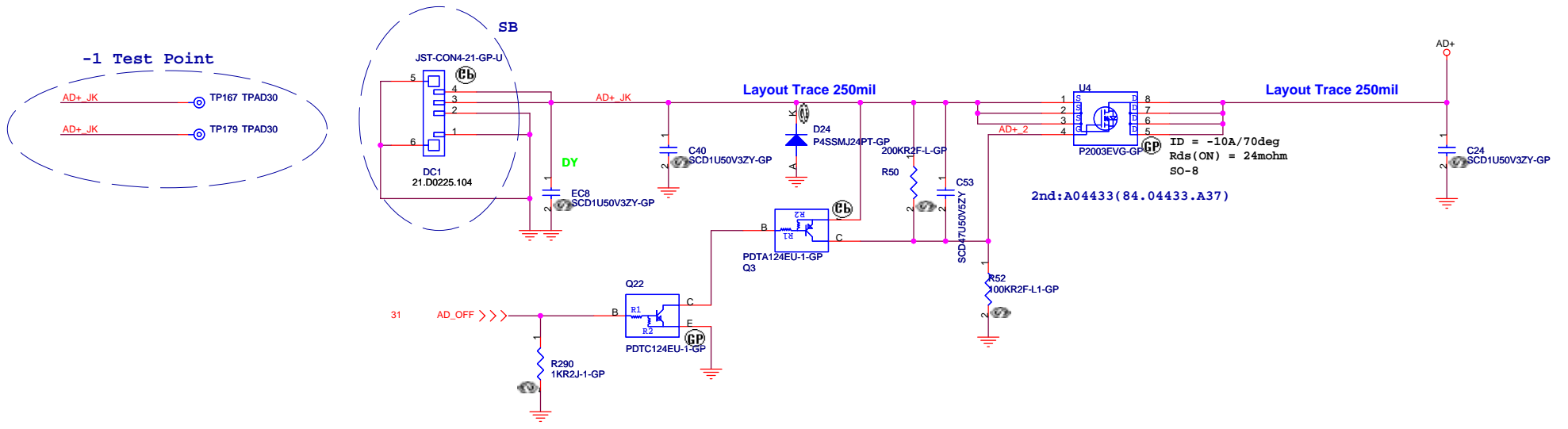


1D25V_S0
Iomax=2A

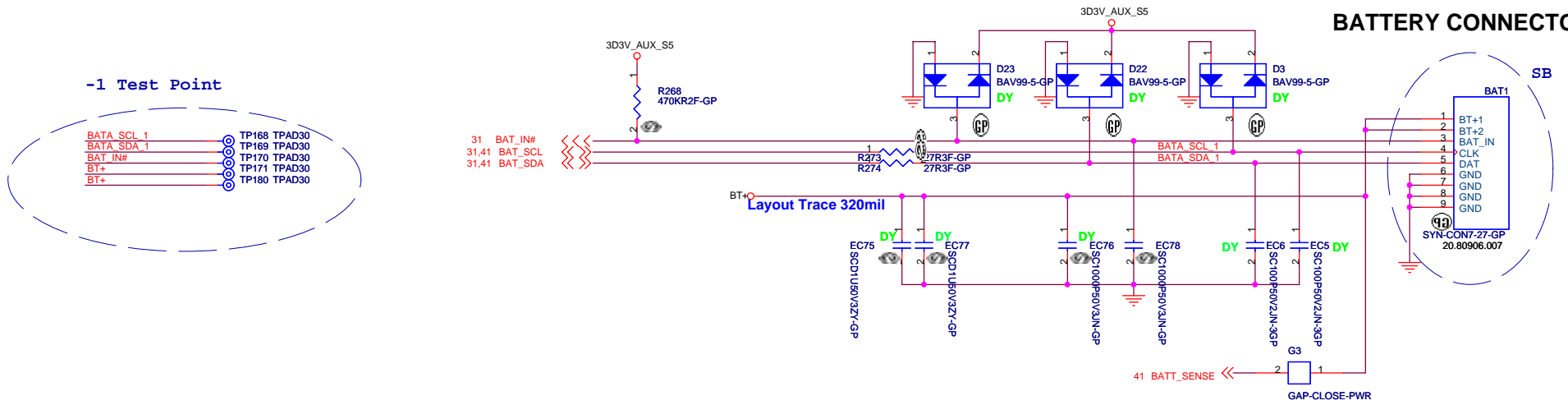


UMA	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title 1D25V/2D5V//1D05V/0D9V	
Size B	Document Number Tahoe
Date: Friday, April 27, 2007	Sheet 40 of 44
	Rev -1

Adaptor in to generate DCBATOUT

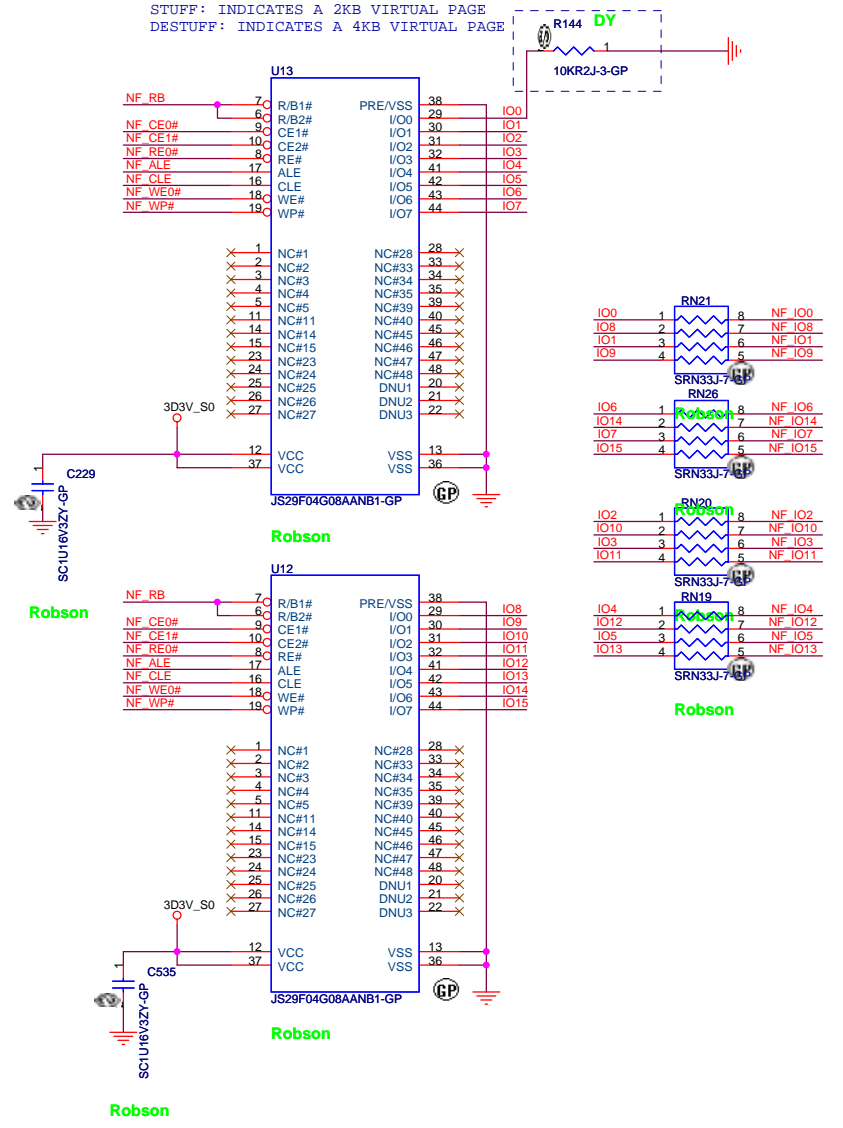
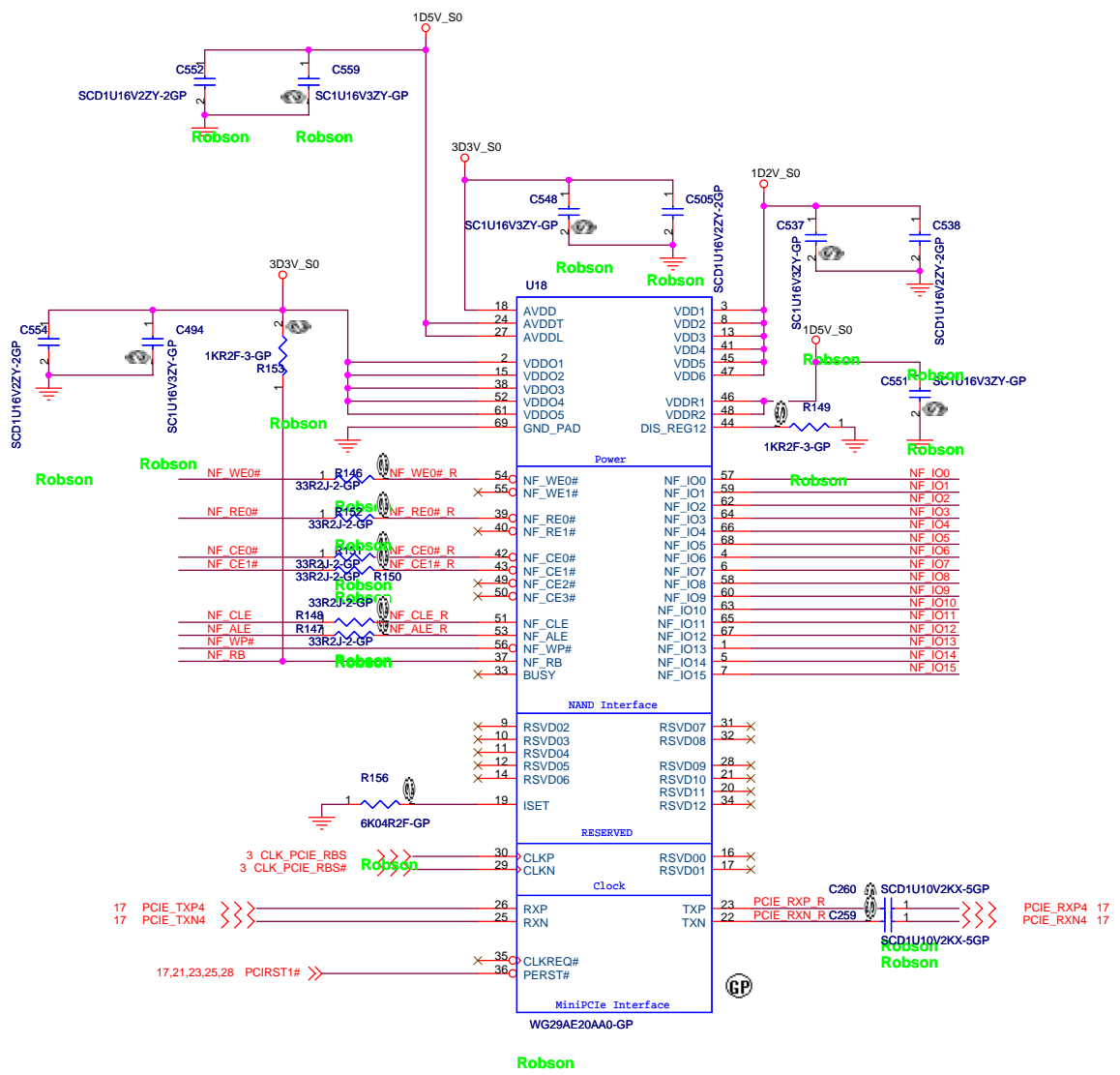


BATTERY CONNECTOR



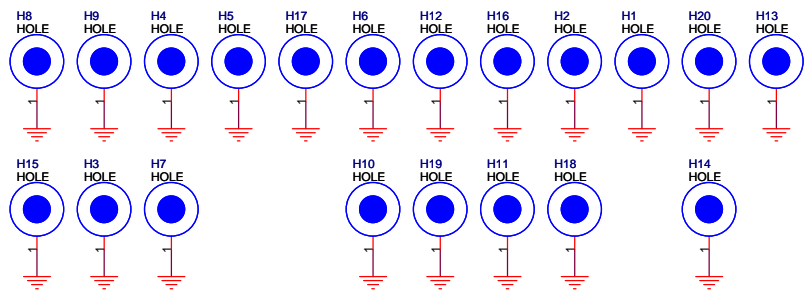
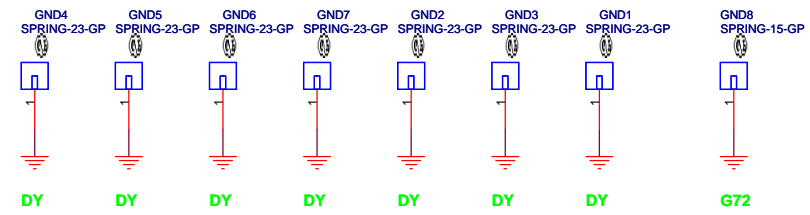
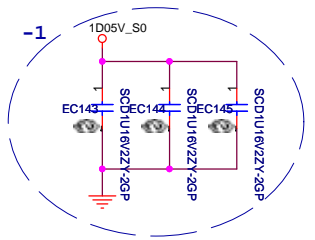
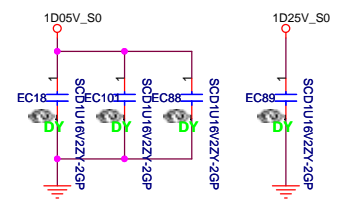
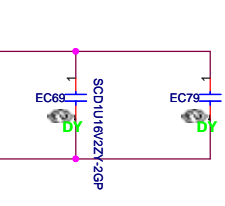
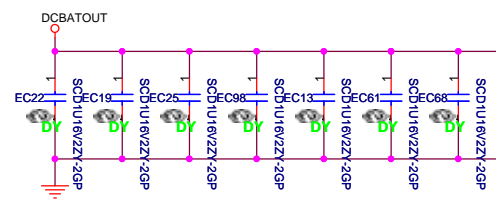
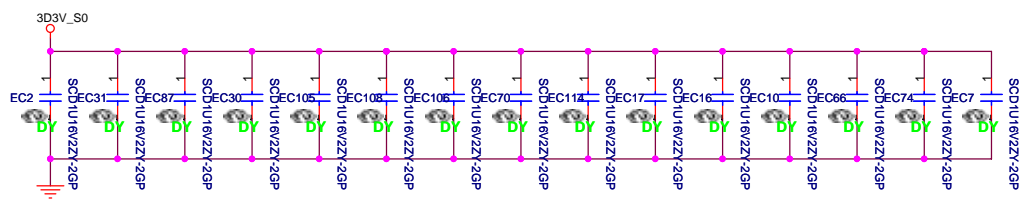
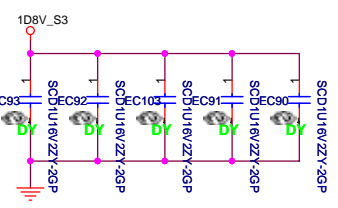
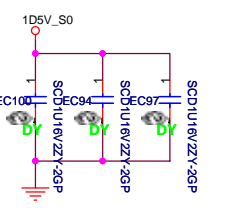
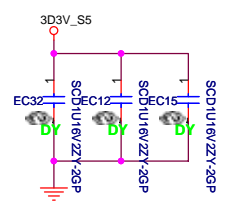
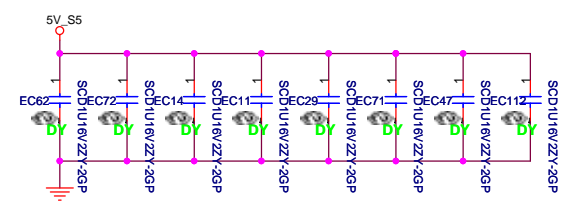
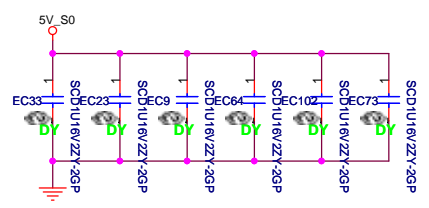
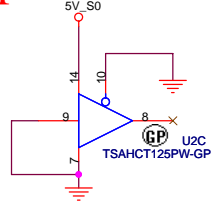
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
AD/BATT CONN	
Size	Document Number
A3	Tahoe
Date: Friday, April 27, 2007	Sheet 42 of 44
Rev -1	

R632
STUFF: INDICATES A 2KB VIRTUAL PAGE
DESTUFF: INDICATES A 4KB VIRTUAL PAGE



<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Robson			
Size A3		Document Number Tahoe	
		Rev -1	
Date: Thursday, May 17, 2007		Sheet 43 of 44	



bom1

Title EMI/Spring/Boss	
Size	Document Number
Date: Thursday, May 17, 2007	
Sheet 44 of 44	
Rev Tahoe -1	