

# Compal Confidential

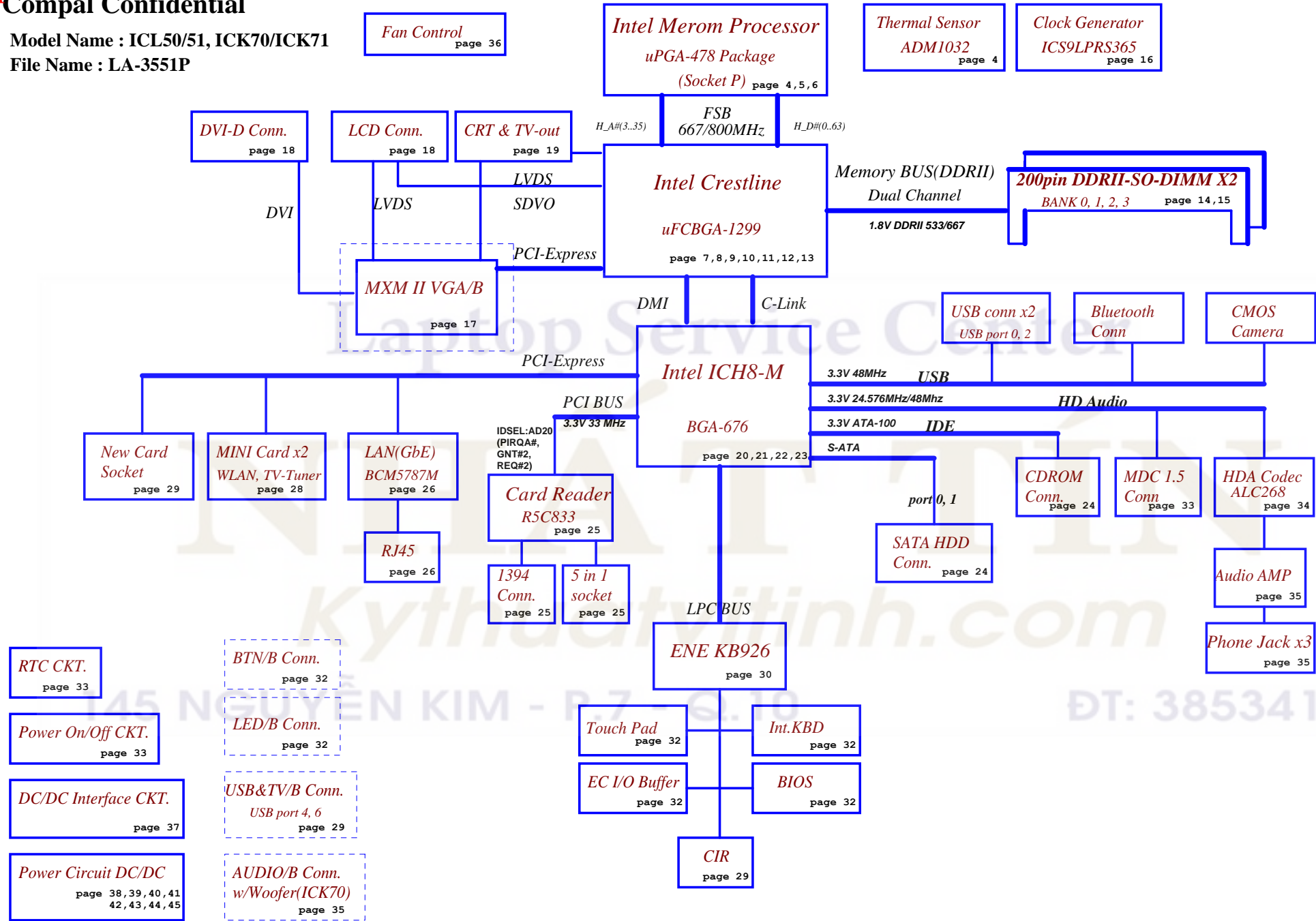
## ICL50/51, ICK70/71 Schematics Document

Intel Merom Processor with Crestline(PM965/GM965) + DDRII + ICH8M  
(With ATI MXM/B)

2007-8-15

REV: 2.0

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Block Diagrams		
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### Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

### External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394/Card Reader	AD16	0	PIRQE PIRQG

### EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

### EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b

### ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

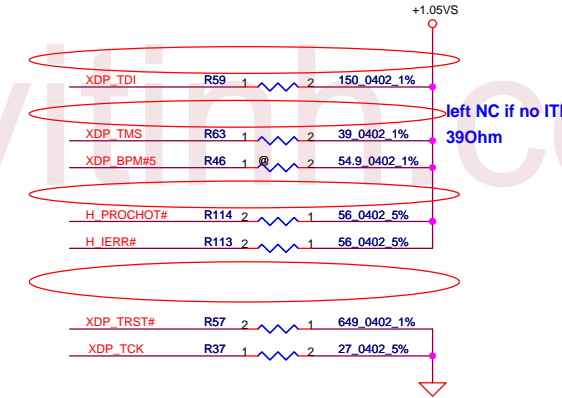
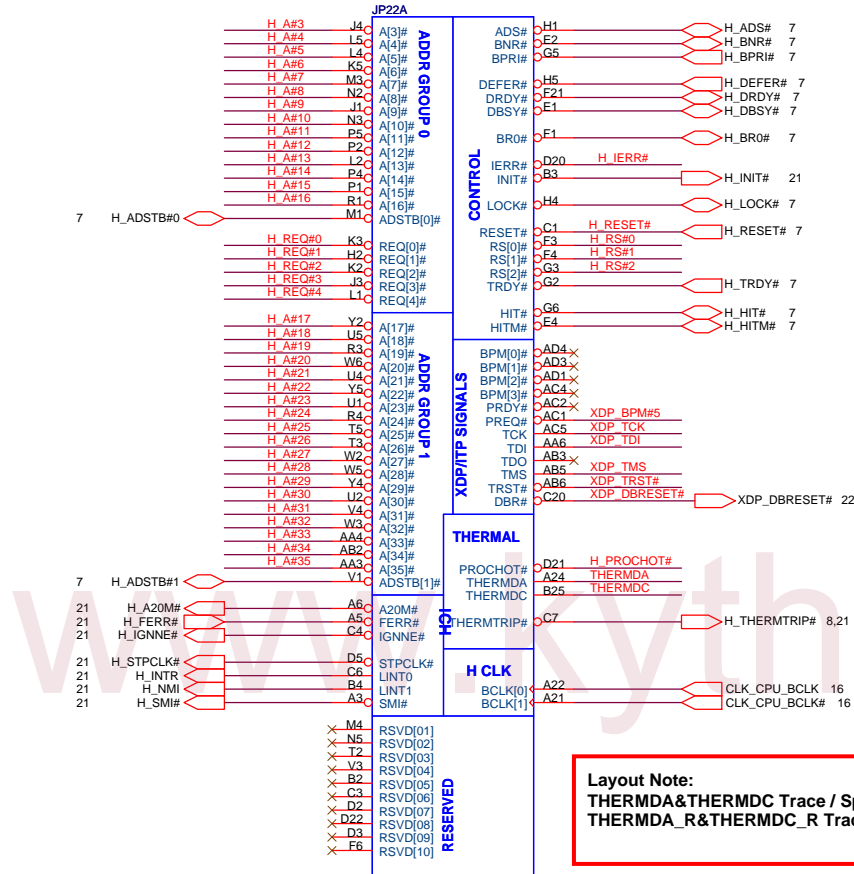
### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A(Nettiling)
5	1A(Acadia 960)
6	
7	

### BTO Option Table

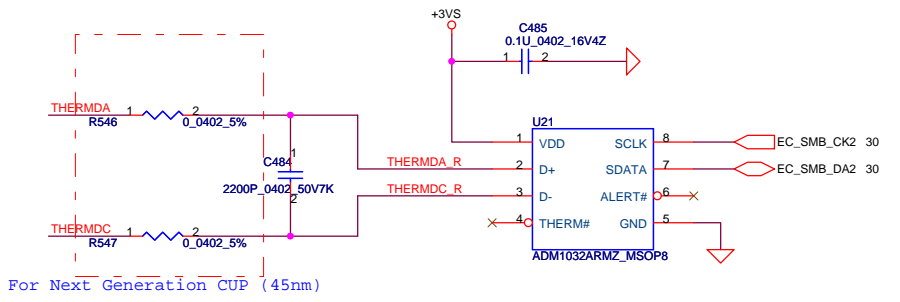
BTO Item	BOM Structure
Discrete	PM@
UMA	GM@

- 7 H\_A#[3..35] H\_A#[3..35]
- 7 H\_REQ#[0..4] H\_REQ#[0..4]
- 7 H\_RS#[0..2] H\_RS#[0..2]

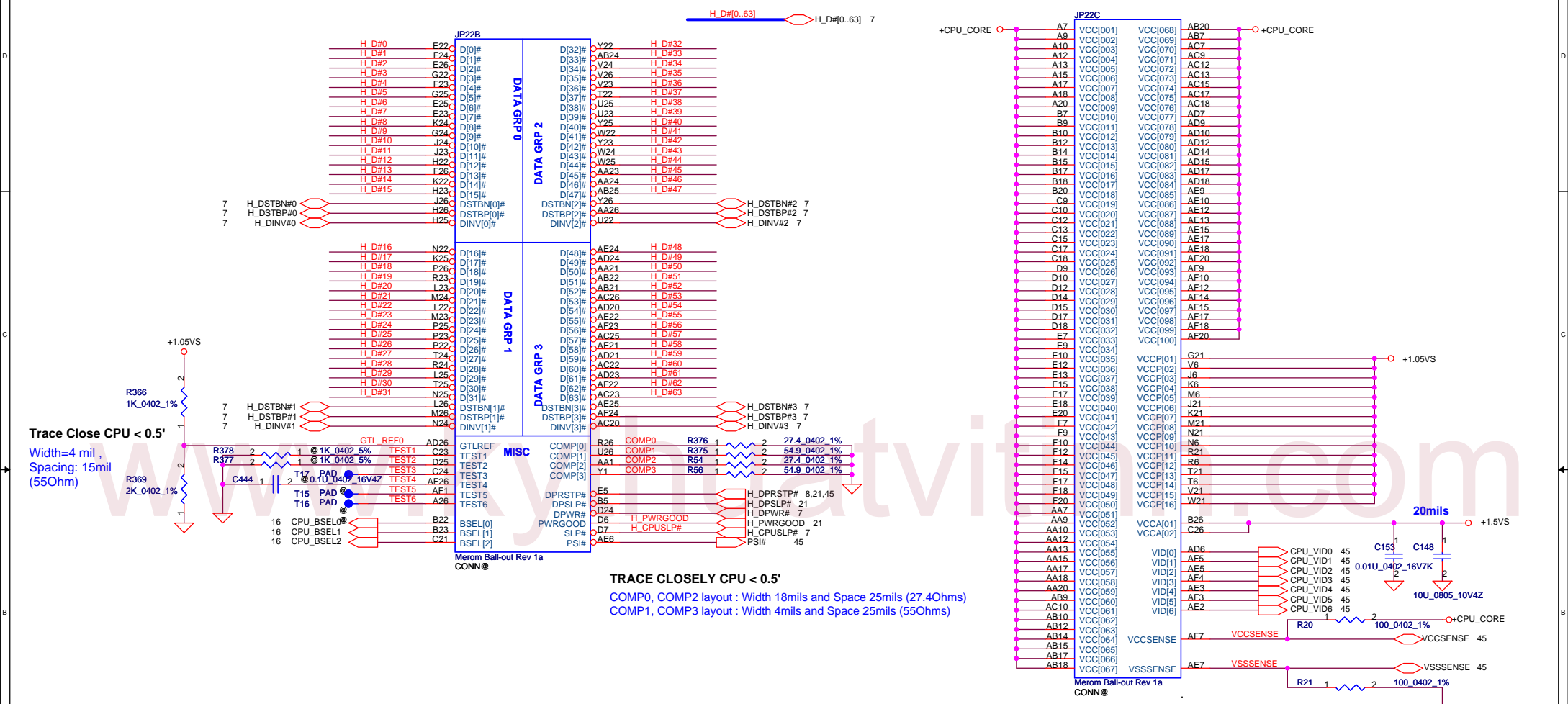


**Layout Note:**  
**THERMDA&THERMDC Trace / Space = 10 / 10 mil**  
**THERMDA\_R&THERMDC\_R Trace / Space = 10 / 10 mil**

BSEL2	BSEL1	BSEL0	BCLK
0	1	0	200
0	1	1	166



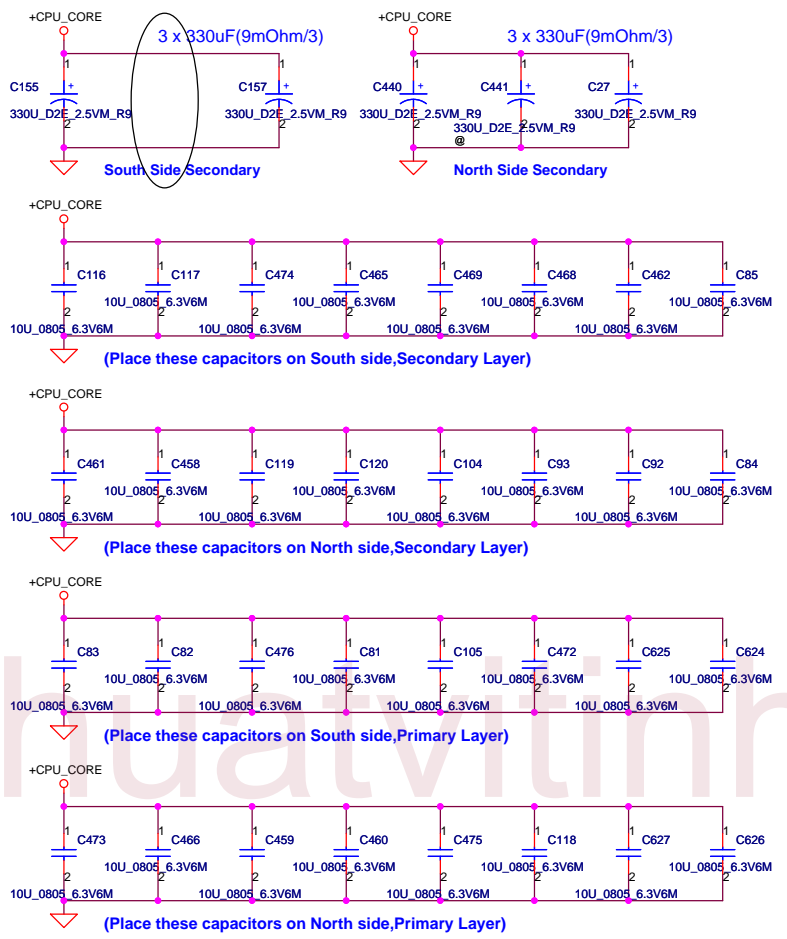
For Next Generation CUP (45nm)



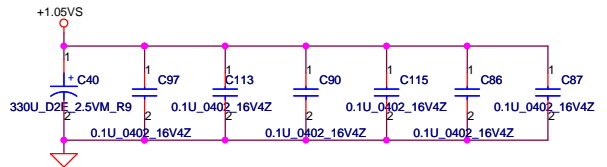
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				Merom (2/3)	
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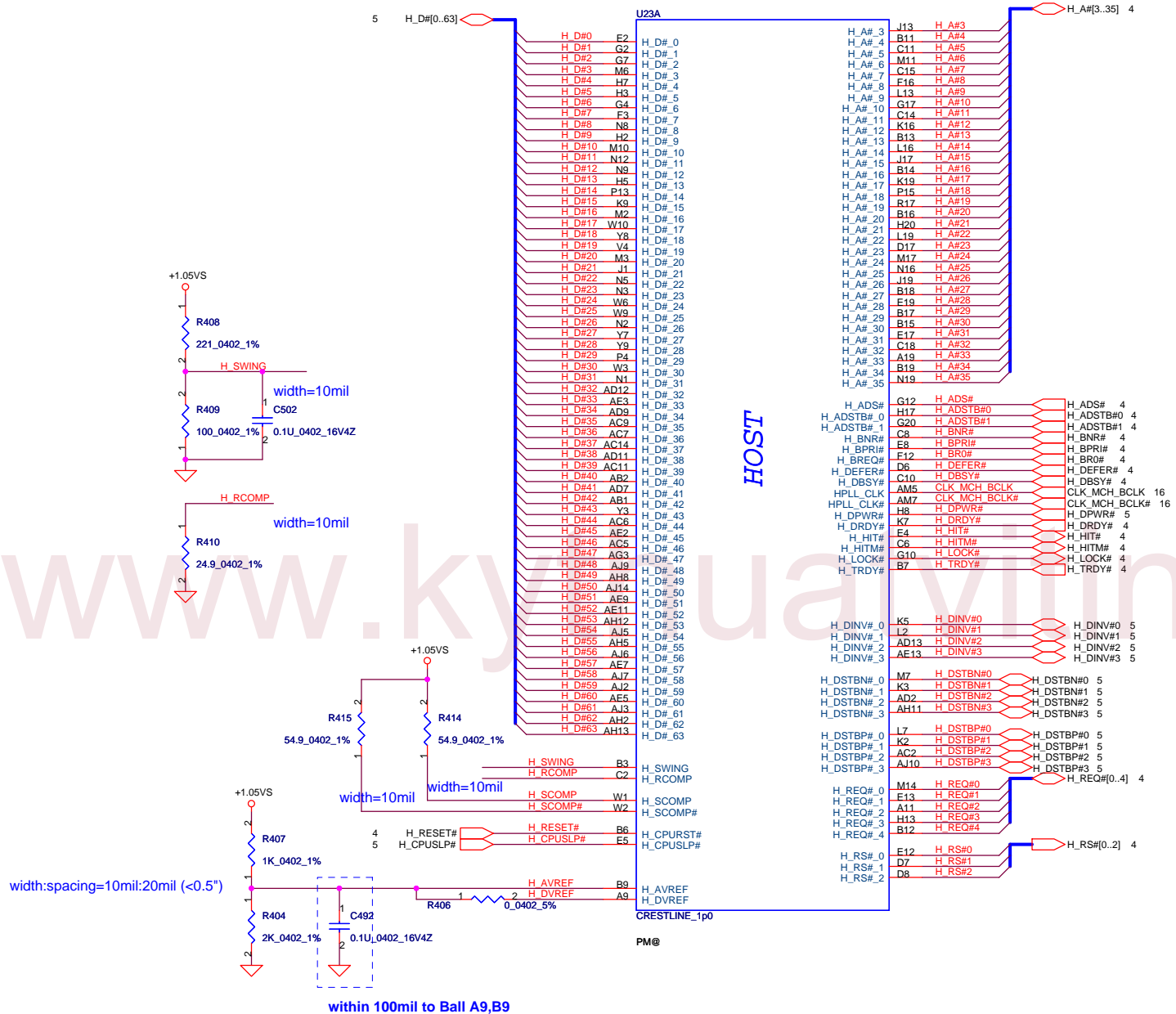
JP22D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
AF2	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C22	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F5	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F22	VSS[051]	VSS[132]
F25	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]
		VSS[163]

Merom Ball-out Rev 1a  
CONN@

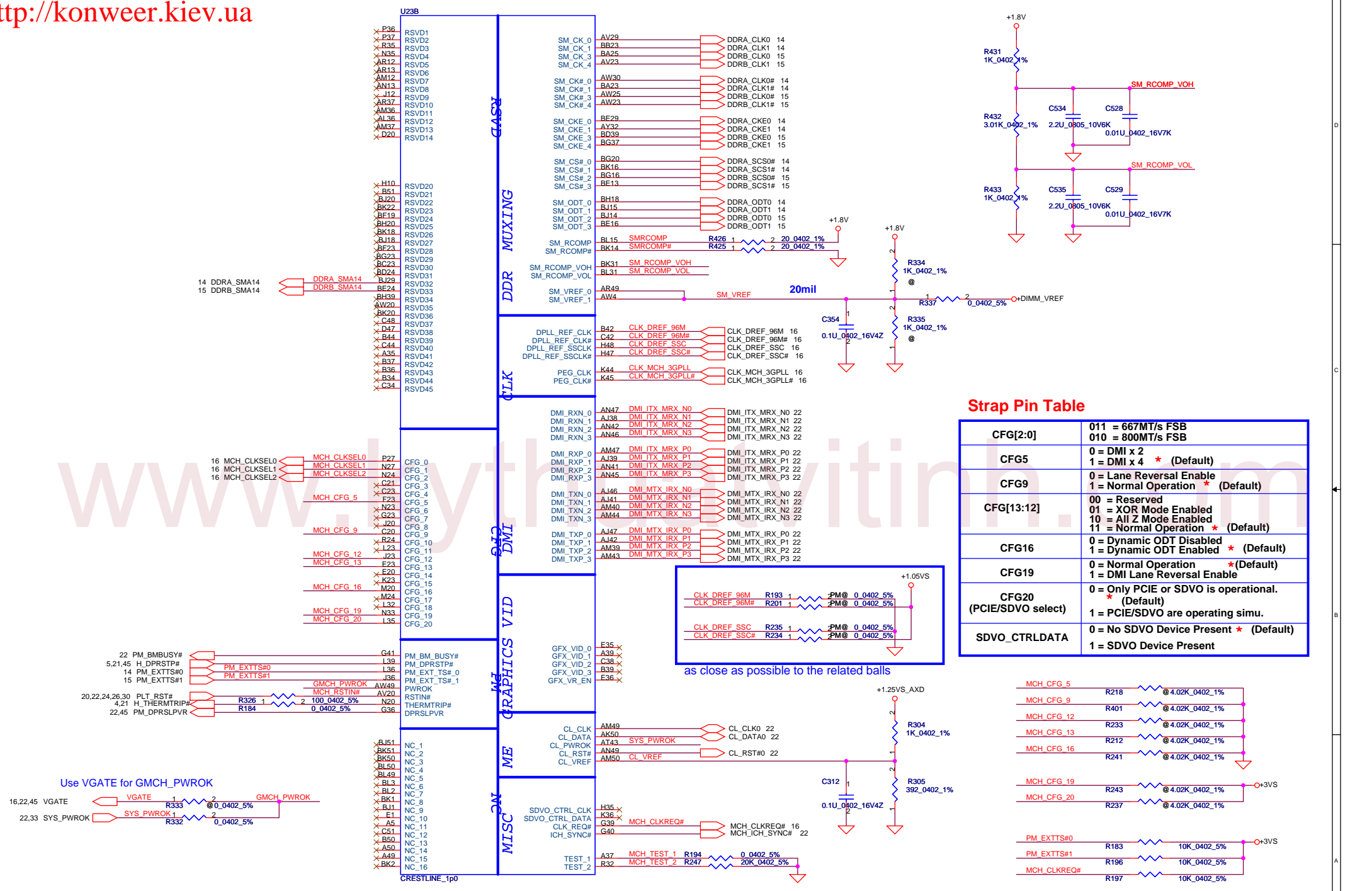


+CPU-CORE Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



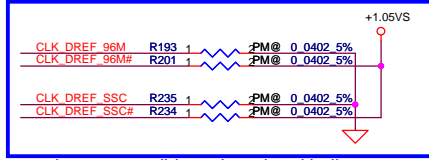
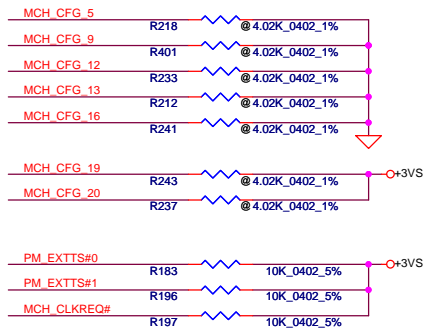


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**Strap Pin Table**

CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. * (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present



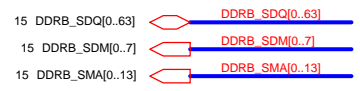
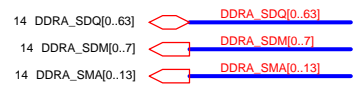
as close as possible to the related balls



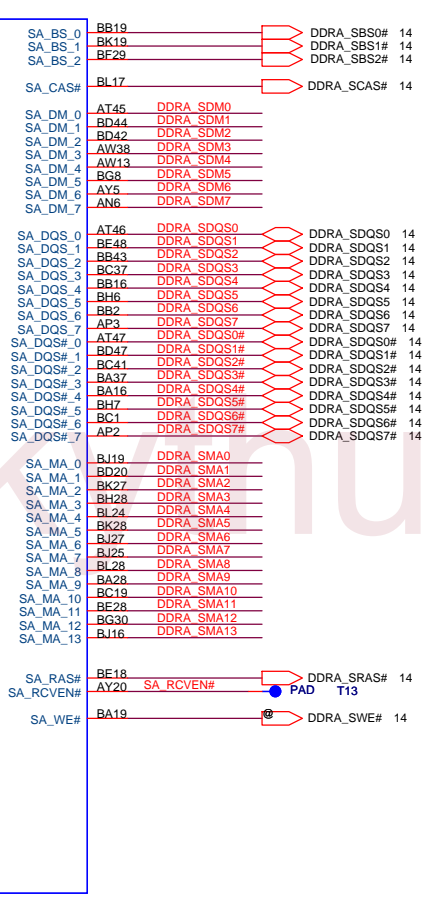
Use VGATE for GMCH\_PWROK

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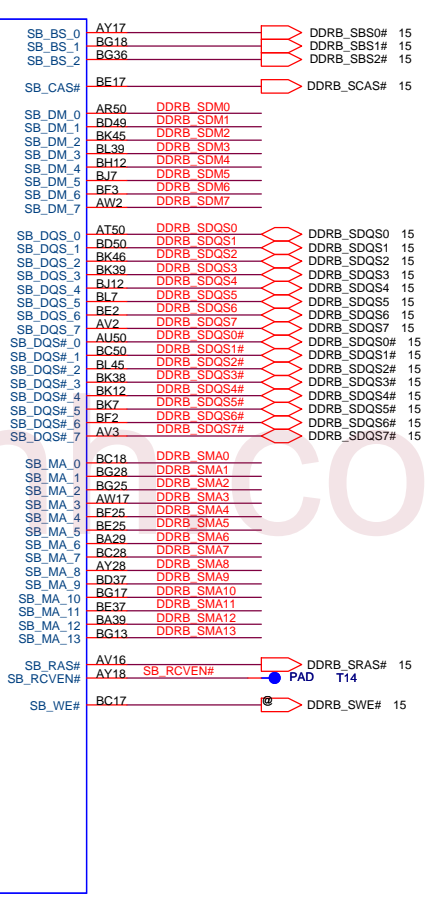
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DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B



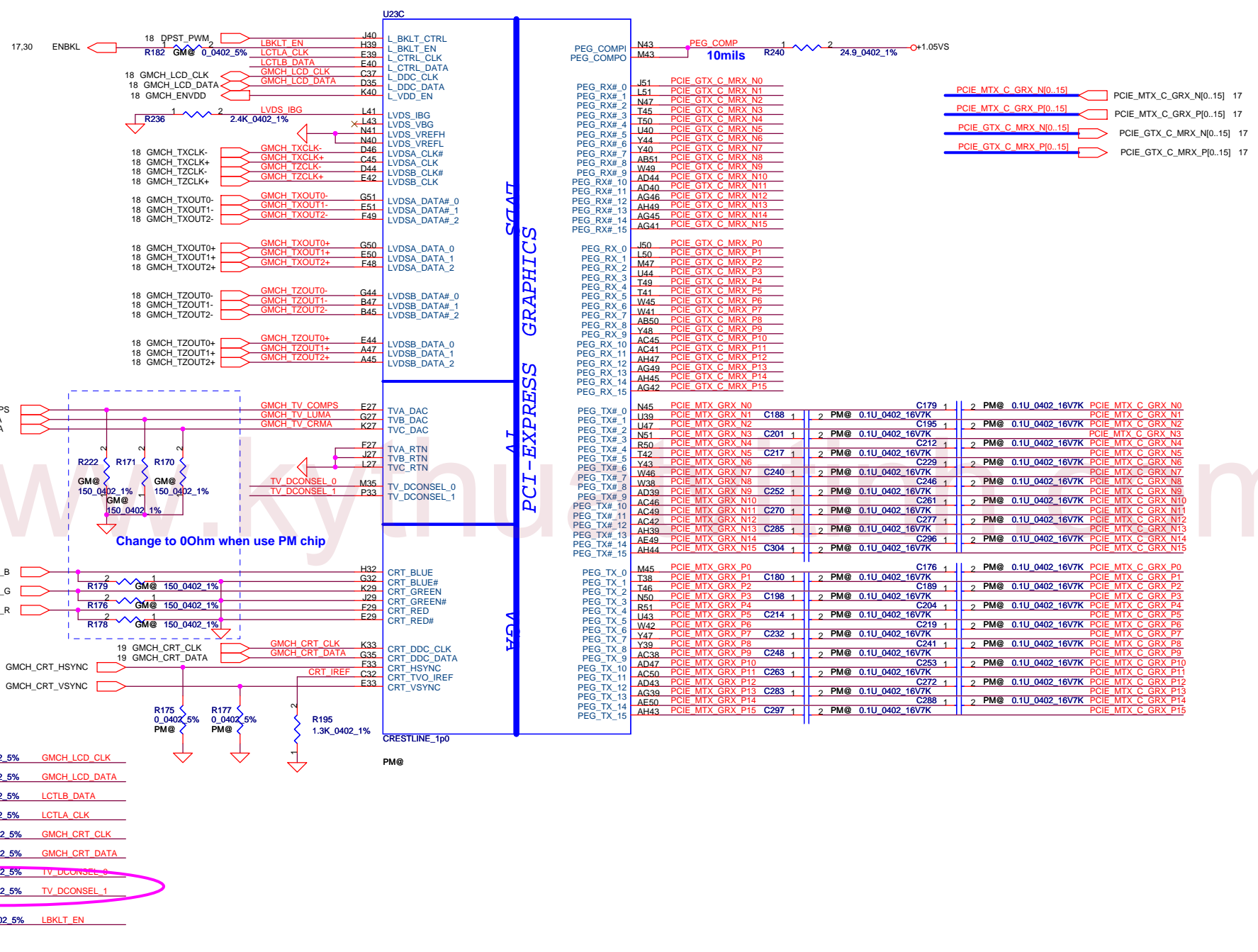
CRESTLINE\_1p0

CRESTLINE\_1p0

PM@

PM@

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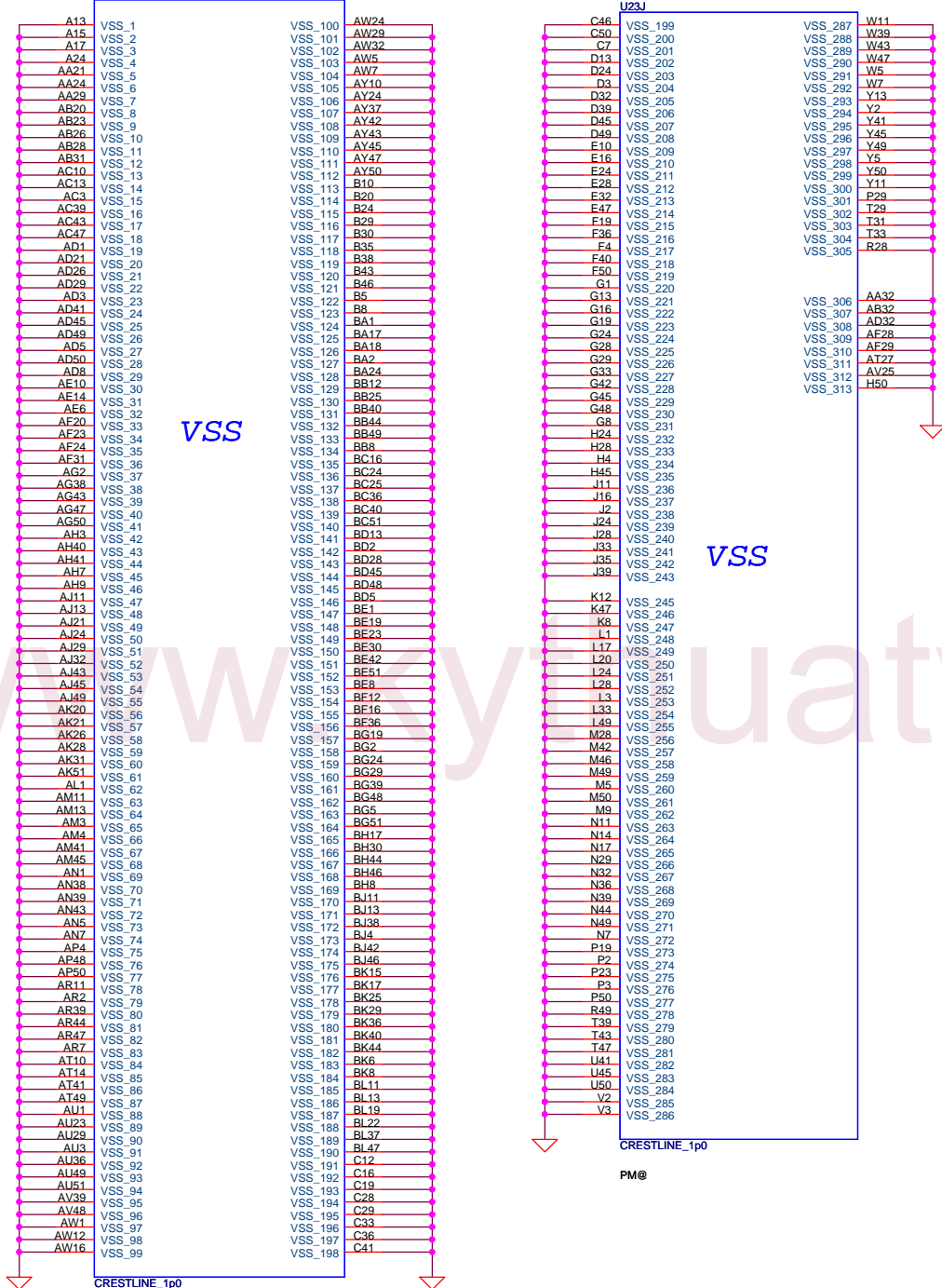


Change to 00hm when use PM chip

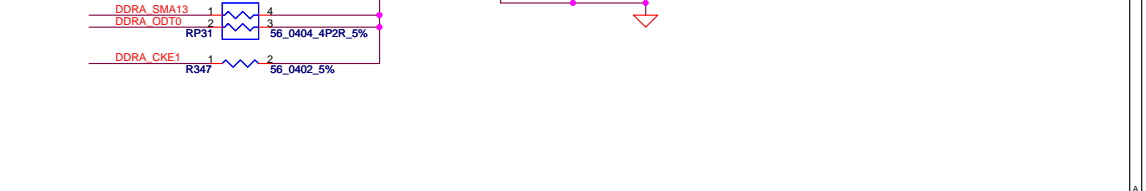
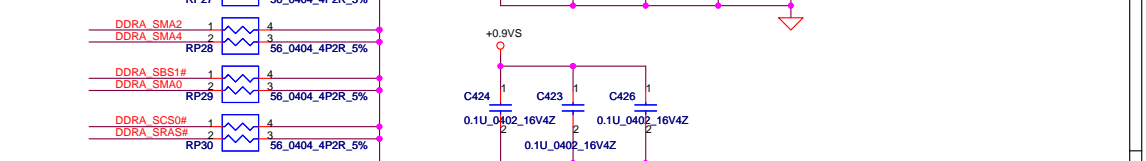
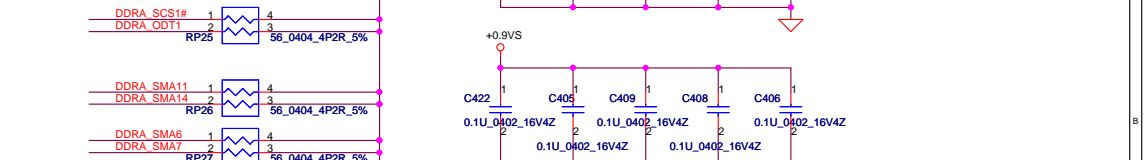
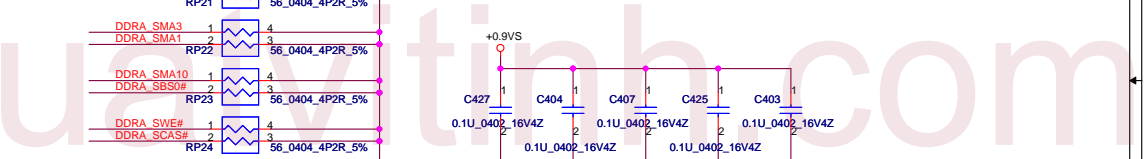
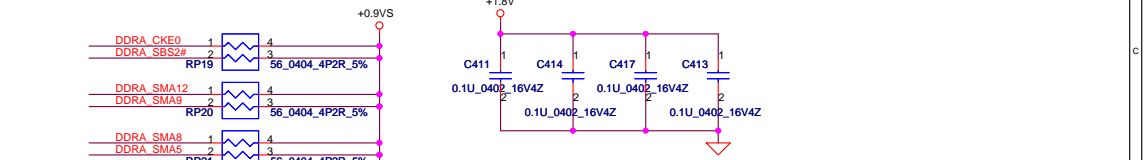
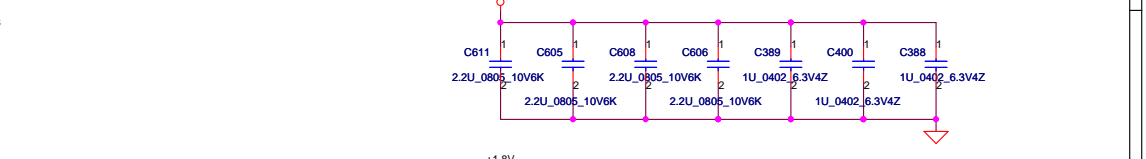
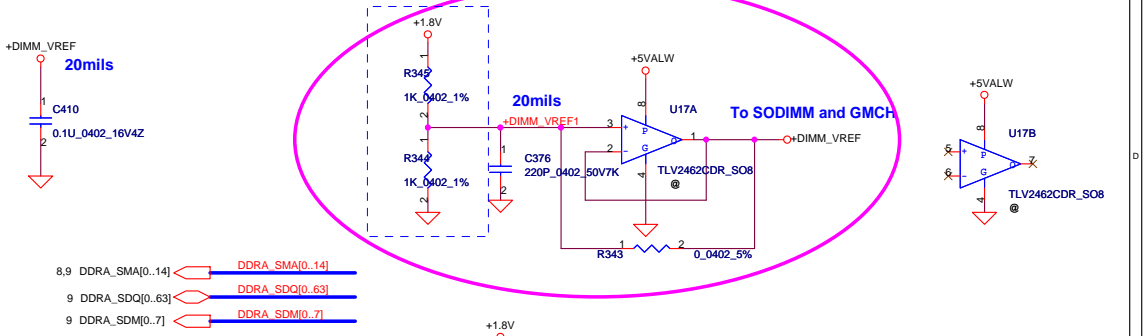
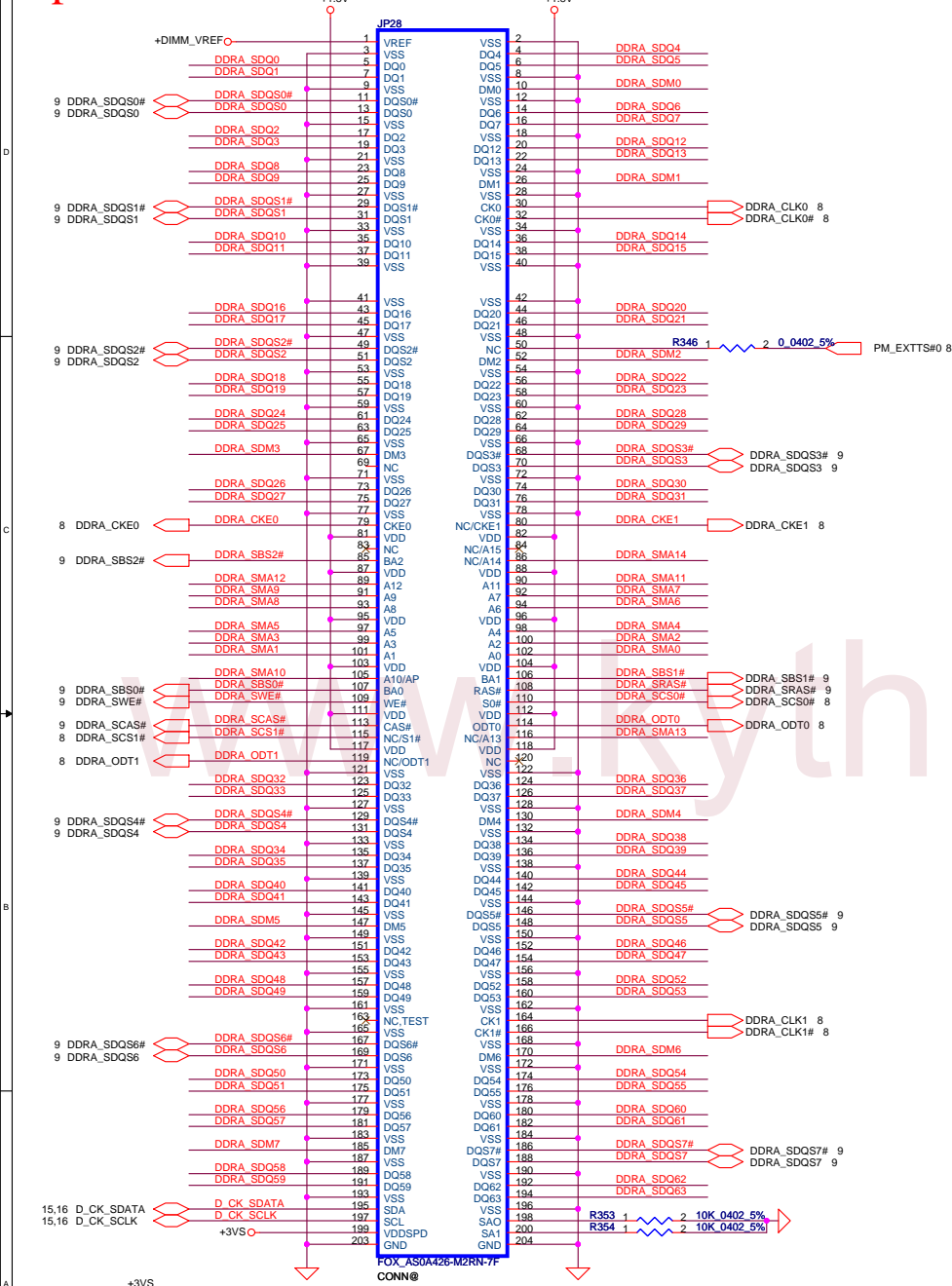
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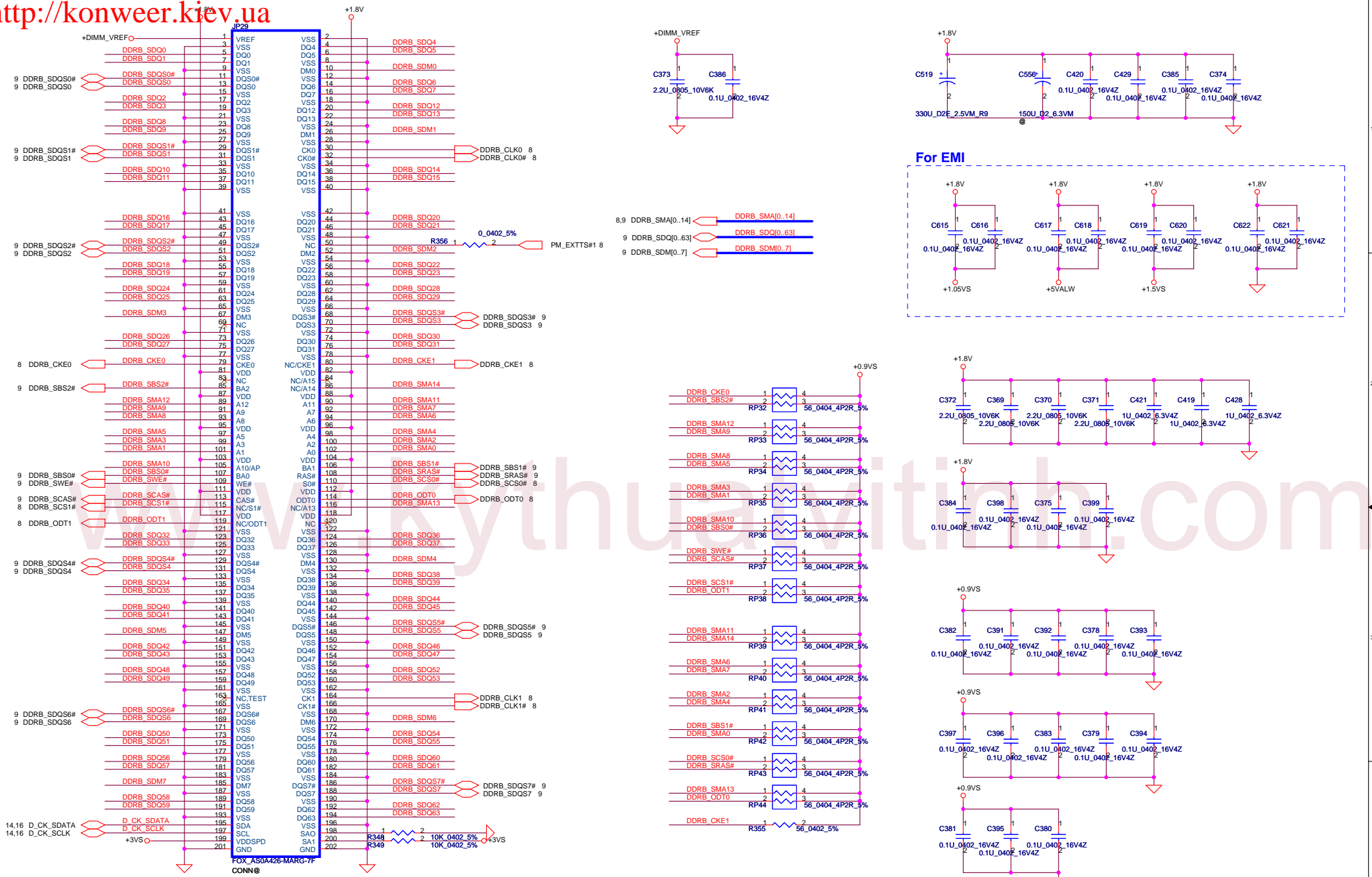




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				DDRII-SODIMMO		
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DIMM1 REV H:9.2mm (BOT)

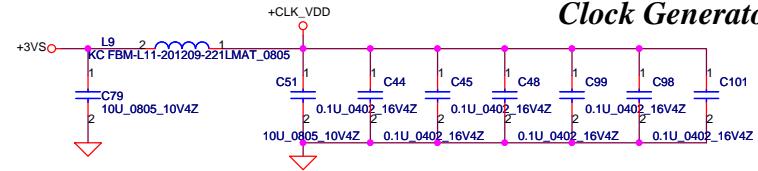
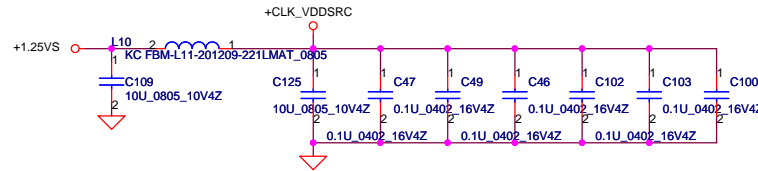
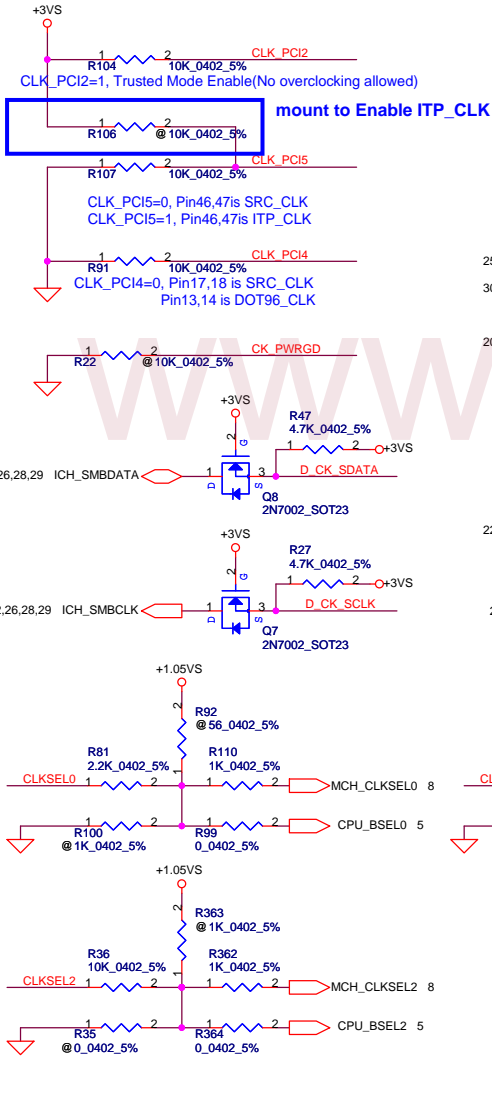
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FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR365

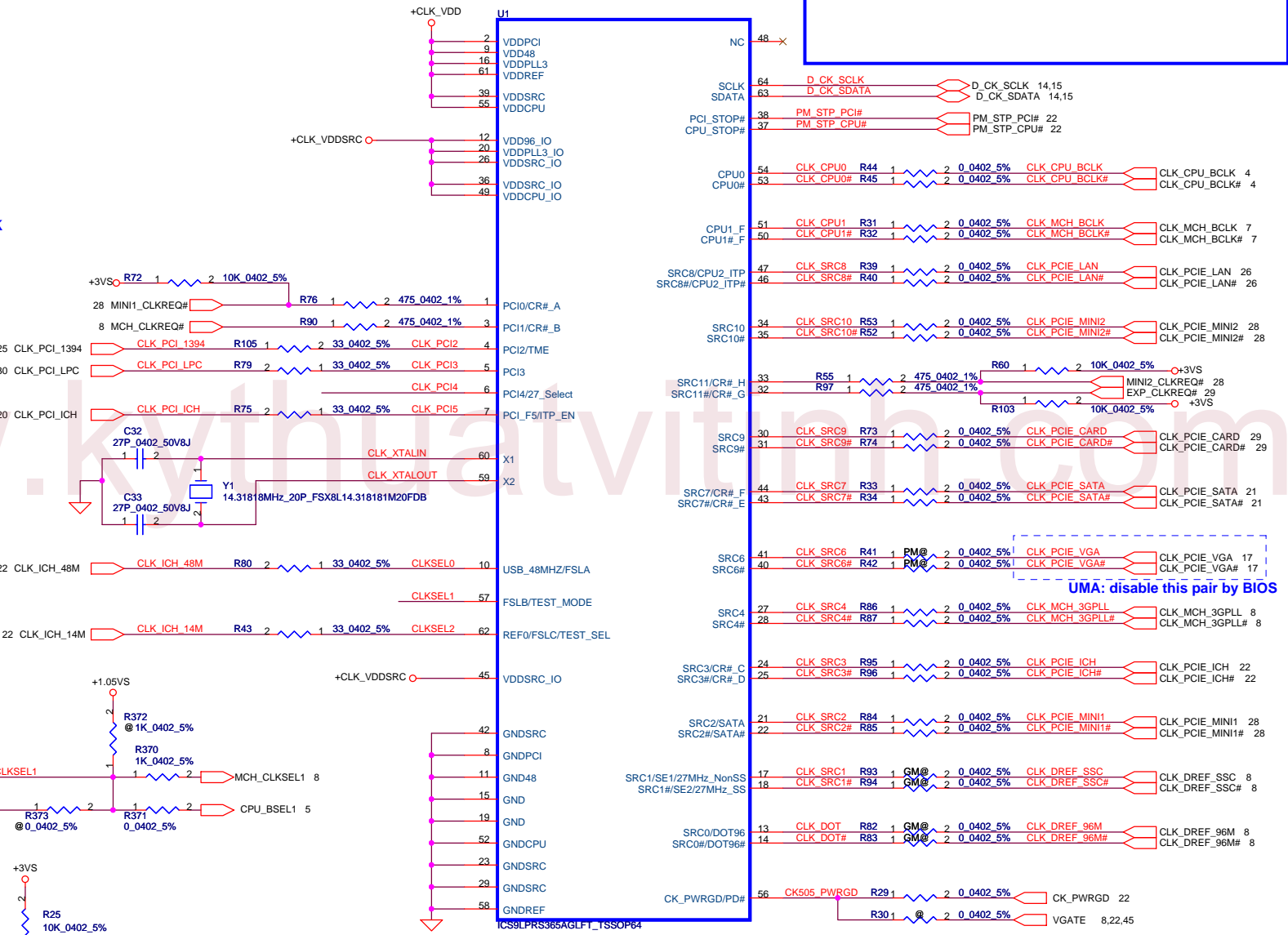
CLK_REQ#	Control	Free-Run
CR#_A(WLAN)	PCIEX2	PCIEX0
CR#_B(MCH)	PCIEX4	PCIEX1
CR#_G(NEW CARD)	PCIEX9	
CR#_H(MINI CARDII)	PCIEX10	

SRC6(VGA\_CLK): Discrete VGA[Enable] UMA[Disable]



### Clock Generator

mount to Enable ITP\_CLK

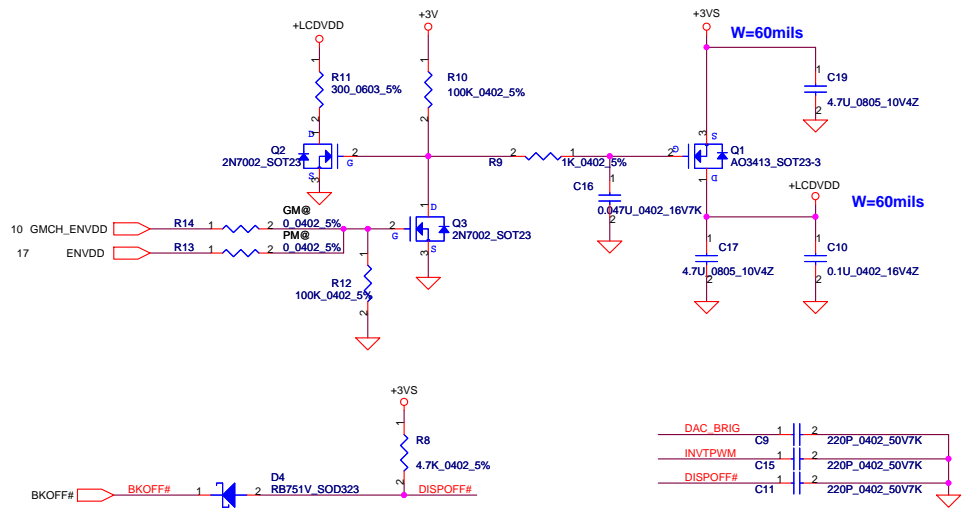


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Issued Date	2006/12/25	Deciphered Date	2007/12/25
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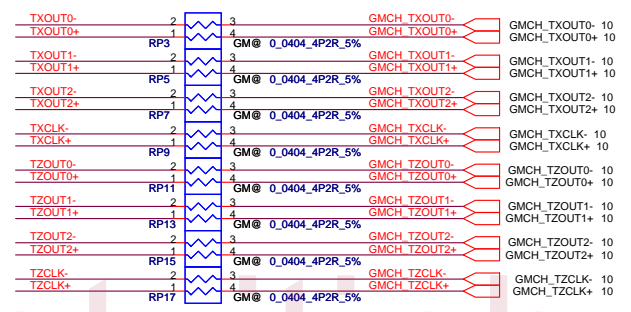
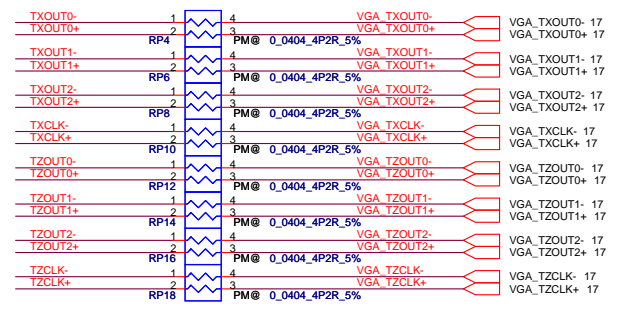
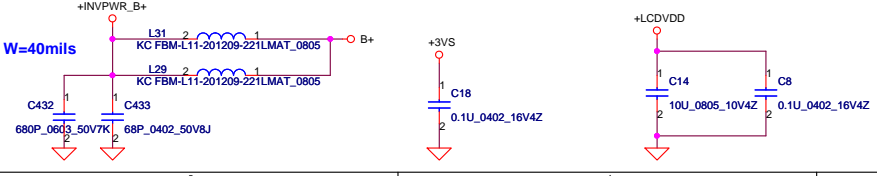
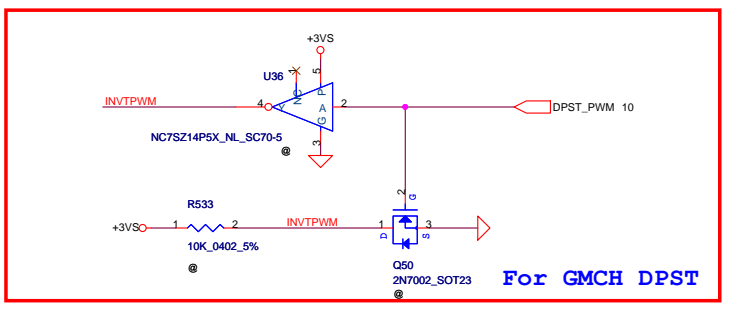
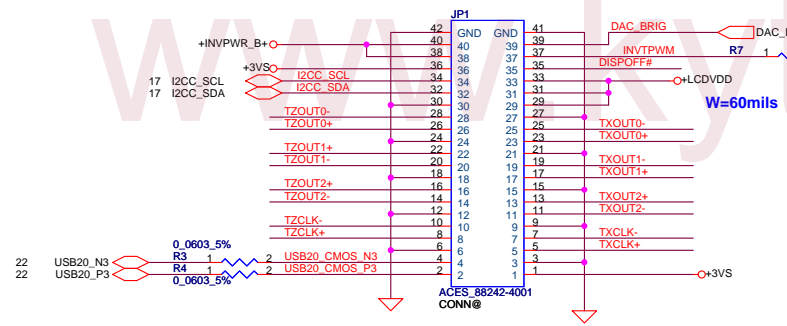
Compal Electronics, Inc.			
Title: Clock Generator (CK505)			
Size B	Document Number	Rev	
Date:	ICL50/ICK70 M/B LA-3551P Schmatf		
Wednesday, August 15, 2007	Sheet	16	of 49



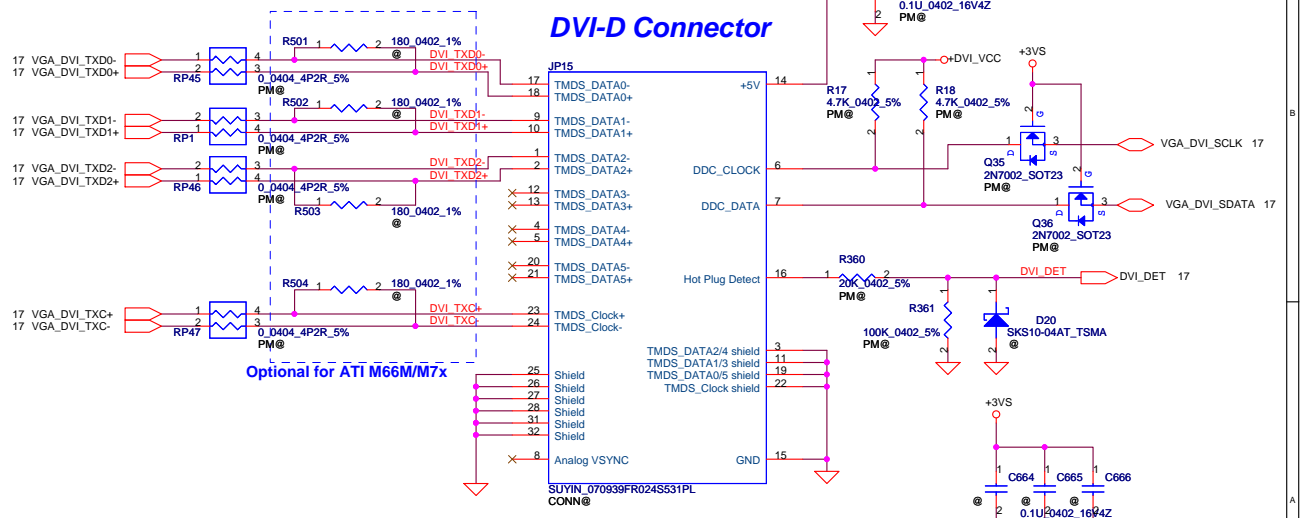
### LCD POWER CIRCUIT



### LCD/PANEL BD. Conn.



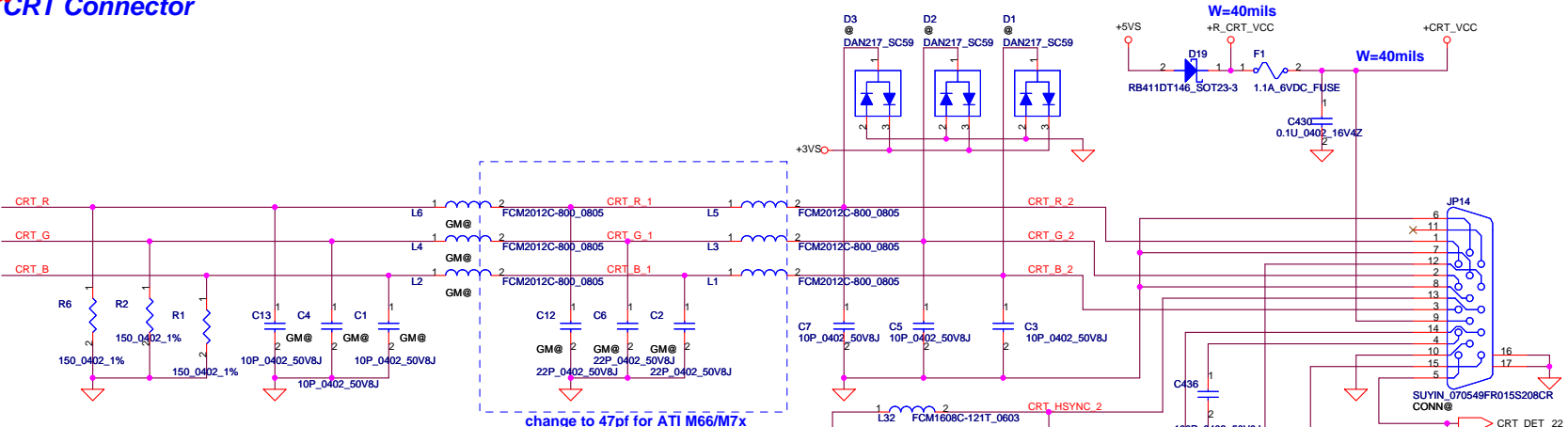
### DVI-D Connector



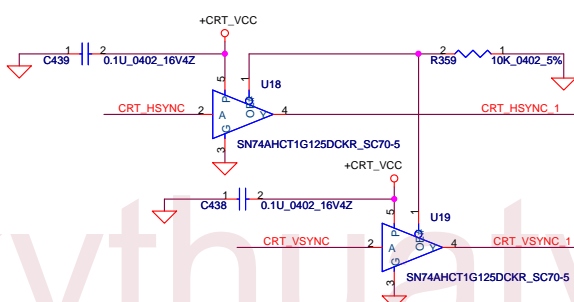
Security Classification	Compal Secret Data	
Issued Date	2006/12/25	Deciphered Date
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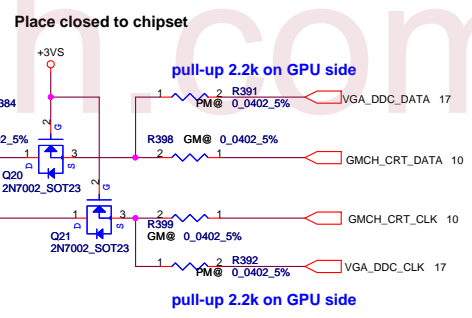
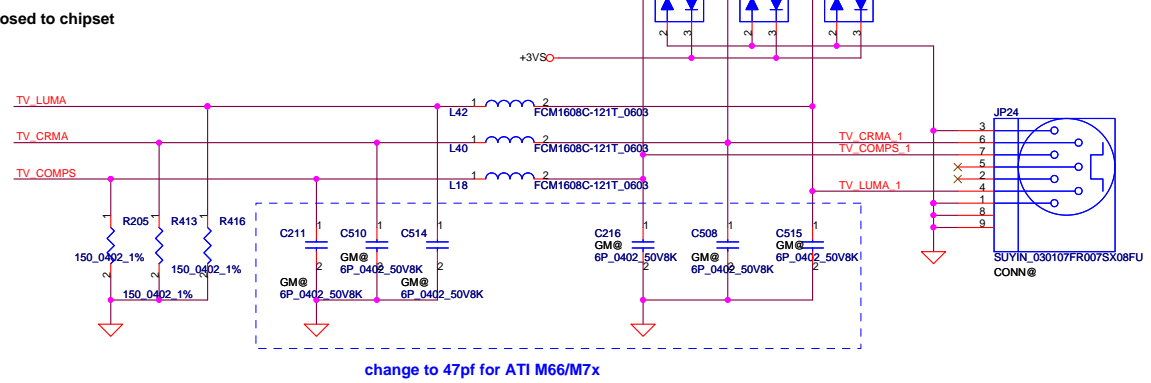
Compal Electronics, Inc.		
LVDS & DVI Connector		
Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematič	
Date:	Thursday, August 23, 2007	Sheet 18 of 49



- 10 GMCH\_CRT\_VSYNC 4 1 CRT\_VSYNC
- 10 GMCH\_CRT\_HSYNC 3 2 CRT\_HSYNC
- 10 GMCH\_CRT\_B 2 1 CRT\_B
- 10 GMCH\_CRT\_G 2 2 CRT\_G
- 10 GMCH\_CRT\_R 2 3 CRT\_R
- 10 GMCH\_TV\_COMPS 2 4 TV\_COMPS
- 10 GMCH\_TV\_LUMA 4 1 TV\_LUMA
- 10 GMCH\_TV\_CRMA 3 2 TV\_CRMA
- 17 VGA\_CRT\_VSYNC 1 4 CRT\_VSYNC
- 17 VGA\_CRT\_HSYNC 2 3 CRT\_HSYNC
- 17 VGA\_CRT\_B 2 1 CRT\_B
- 17 VGA\_CRT\_G 2 2 CRT\_G
- 17 VGA\_CRT\_R 2 3 CRT\_R
- 17 VGA\_TV\_COMPS 2 4 TV\_COMPS
- 17 VGA\_TV\_LUMA 1 1 TV\_LUMA
- 17 VGA\_TV\_CRMA 2 2 TV\_CRMA



TV-OUT Conn.



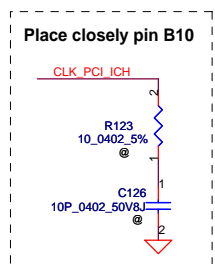
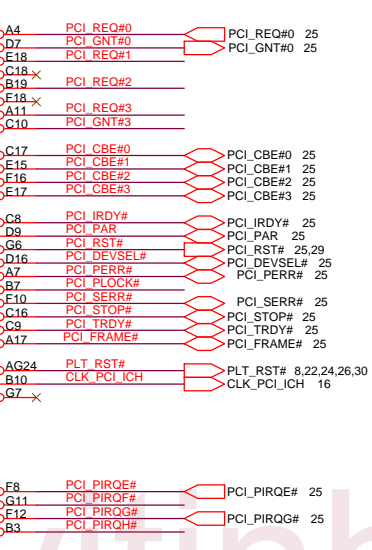
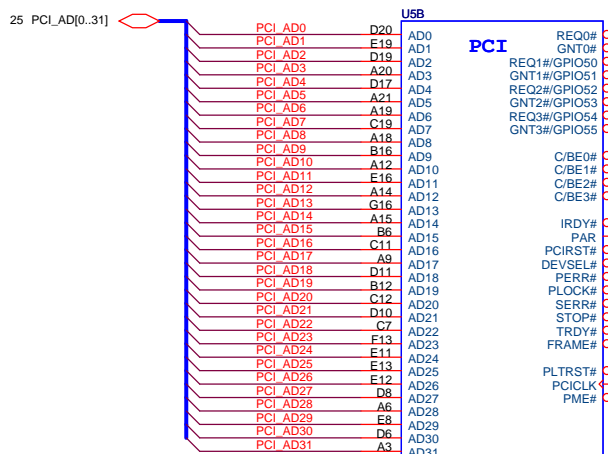
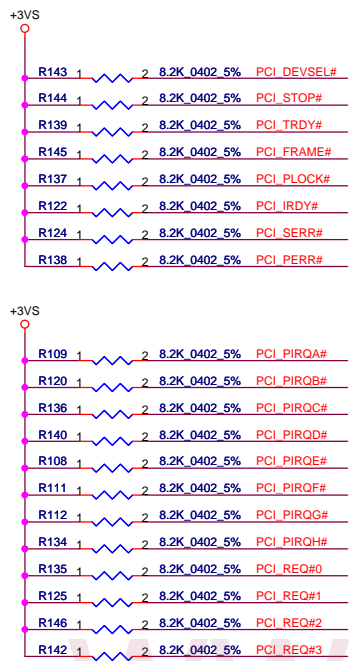
Place closed to chipset

Place closed to chipset

pull-up 2.2k on GPU side

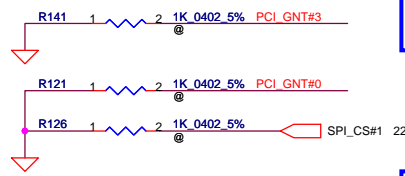
pull-up 2.2k on GPU side

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				ICL50/ICK70 M/B LA-3551P Schematič	
				Date:	Wednesday, August 15, 2007
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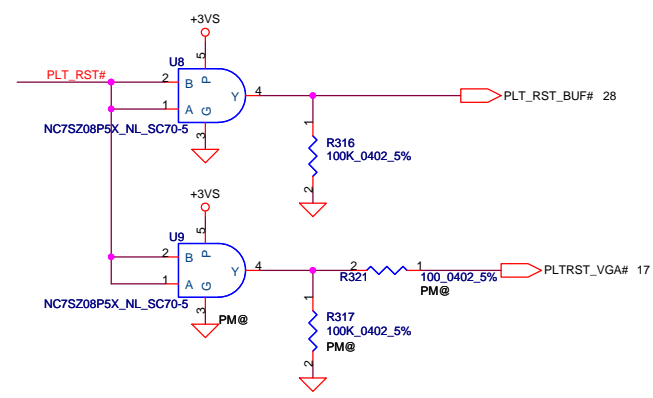


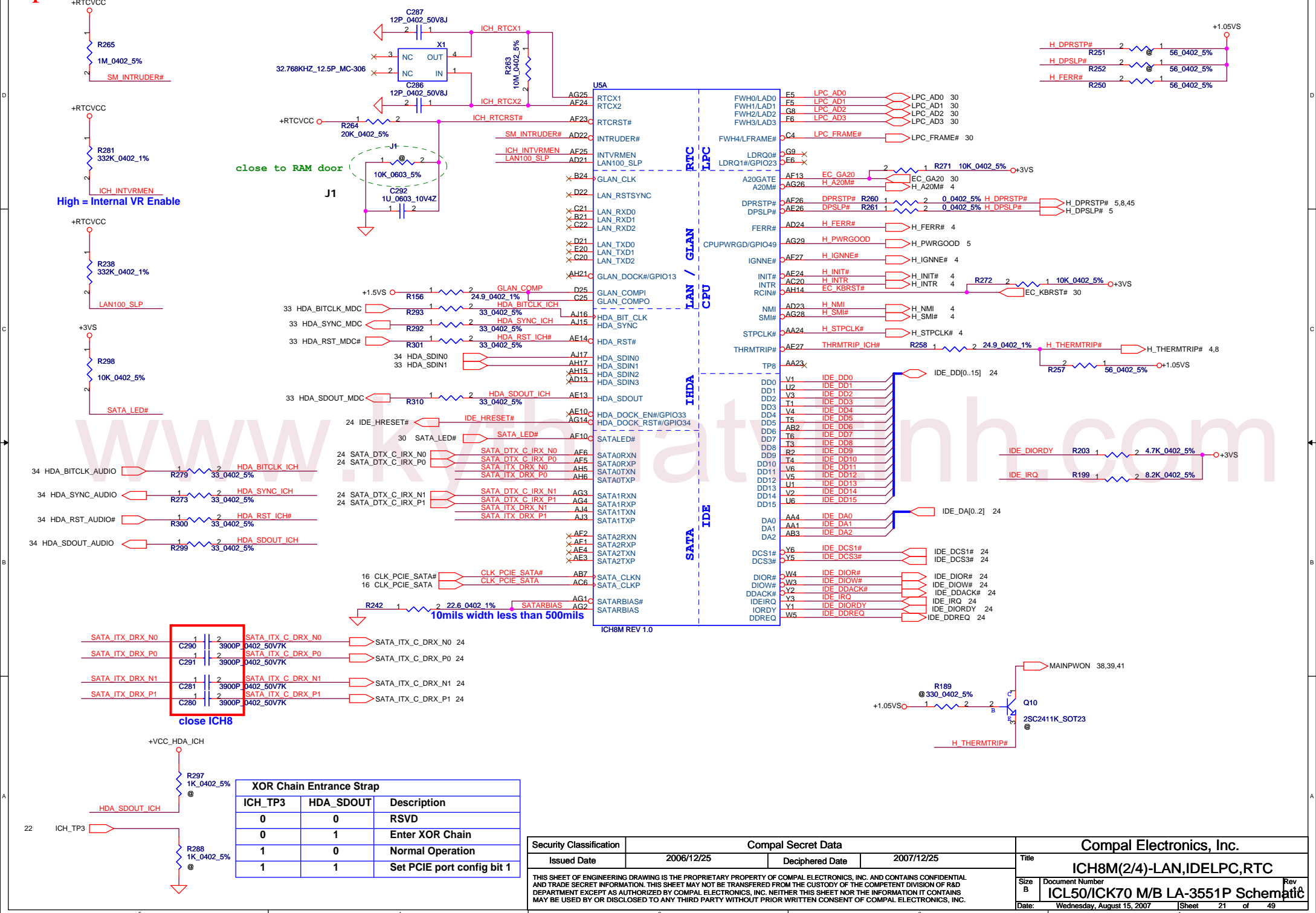
**A16 Swap Override Strap**  
 PCI\_GNT#3 Low= A16 swap override Enable  
 High= Default\*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



**Interrupt I/F**  
 ICH8M REV 1.0





close to RAM door

High = Internal VR Enable

J1

SATA LED#

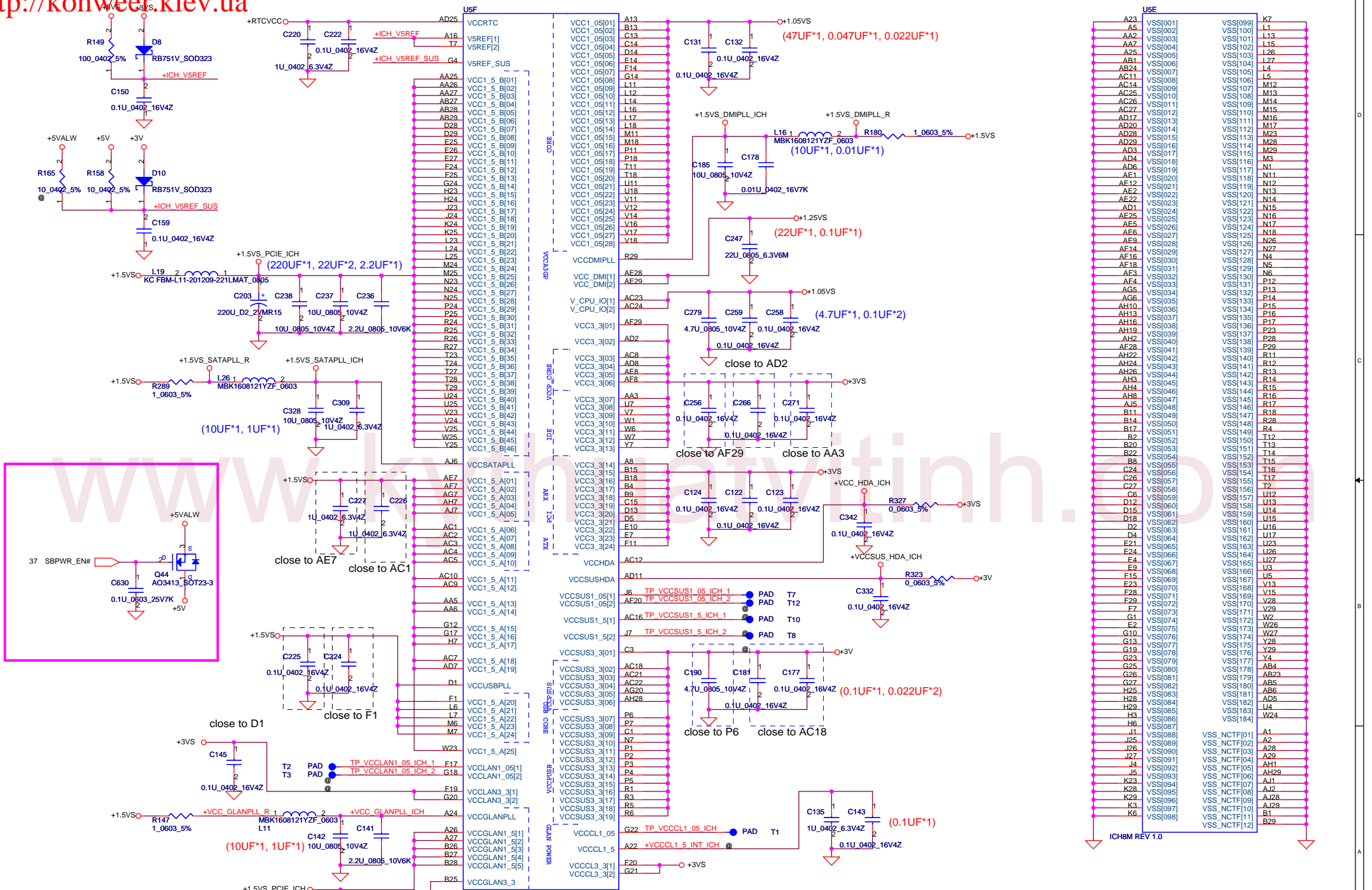
close ICH8

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

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Title		Compal Electronics, Inc.	
Document Number		ICL50/ICK70 M/B LA-3551P Schematic	
Date	Wednesday, August 15, 2007	Sheet	21 of 49

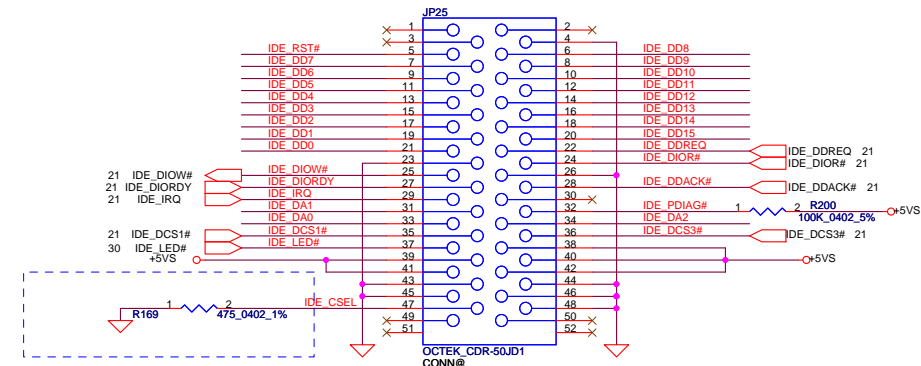
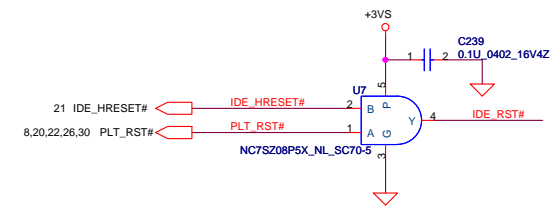
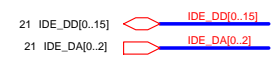
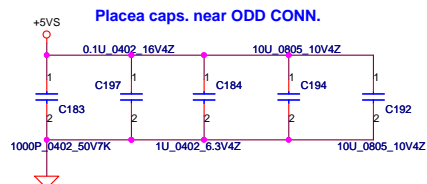




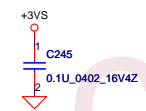
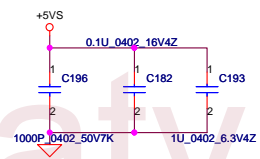
Security Classification	Compal Secret Data	
Issued Date	2006/12/25	Deciphered Date
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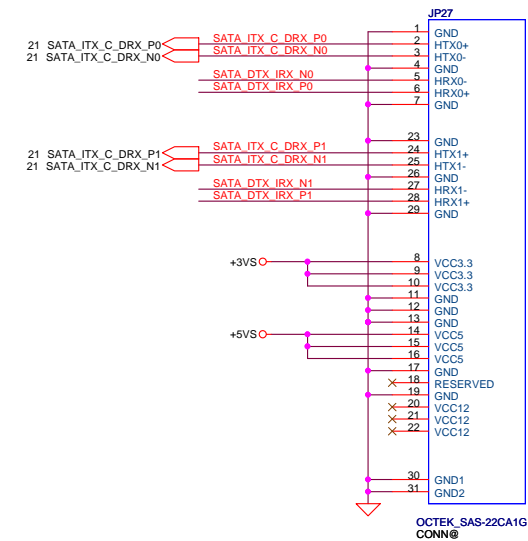
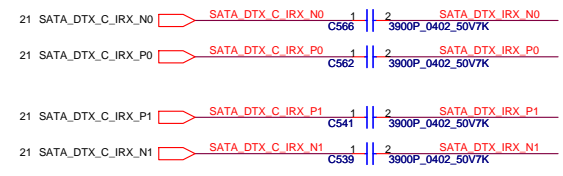
Compal Electronics, Inc.	
Title	
ICH8M(4/4)-POWER&GND	
Size	Document Number
Customer	ICL50/ICK70 M/B LA-3551P Schematic
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**IDE\_CSEL**  
 Grounding for Master (When use SATA HDD)  
 Open or High for Slaver (Normal)



**SATA HDD Conn.(SAS Connector)**

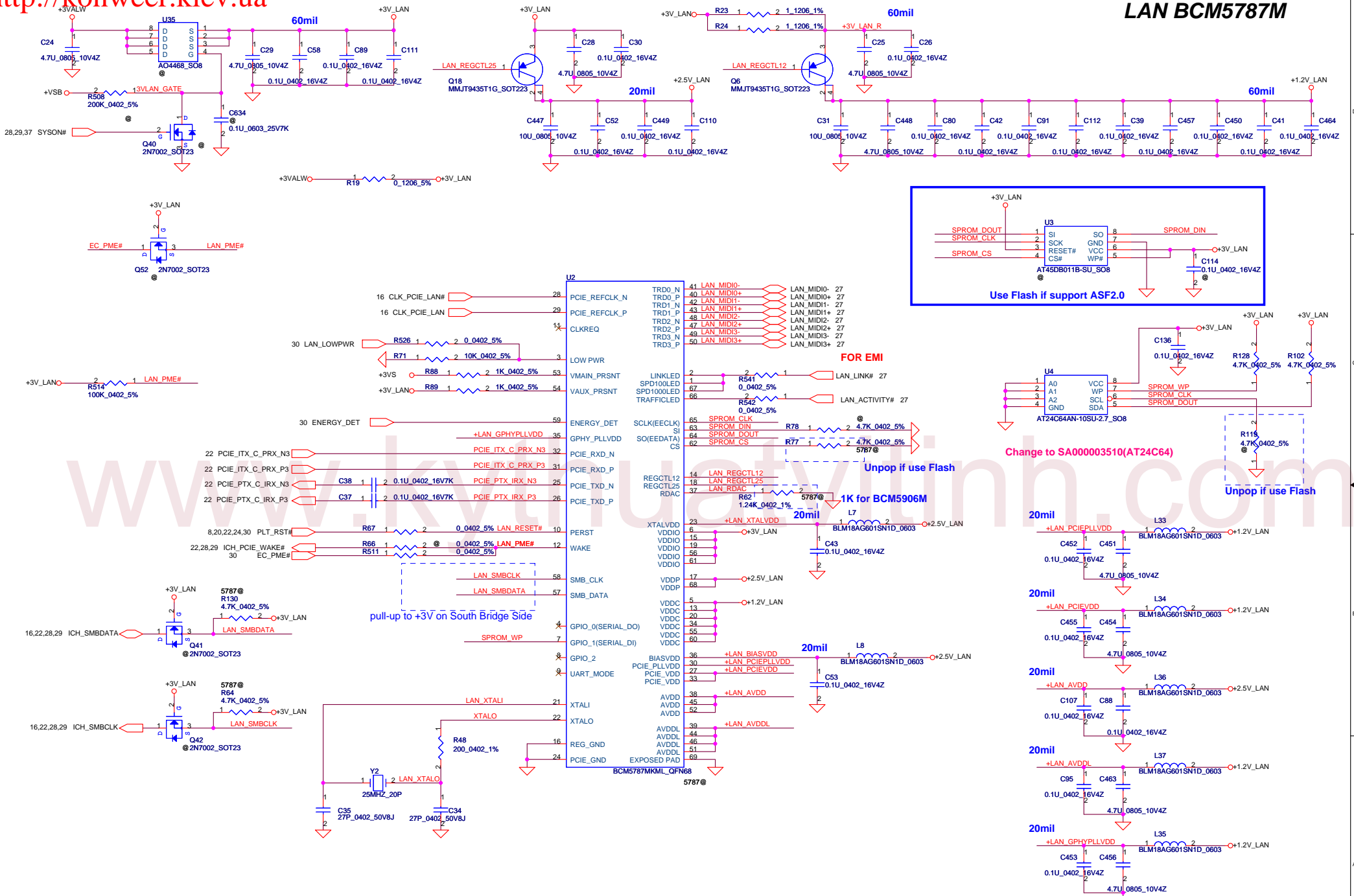


First HDD for 15.4"

2nd HDD for 17"

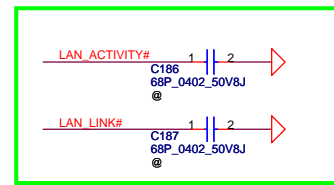
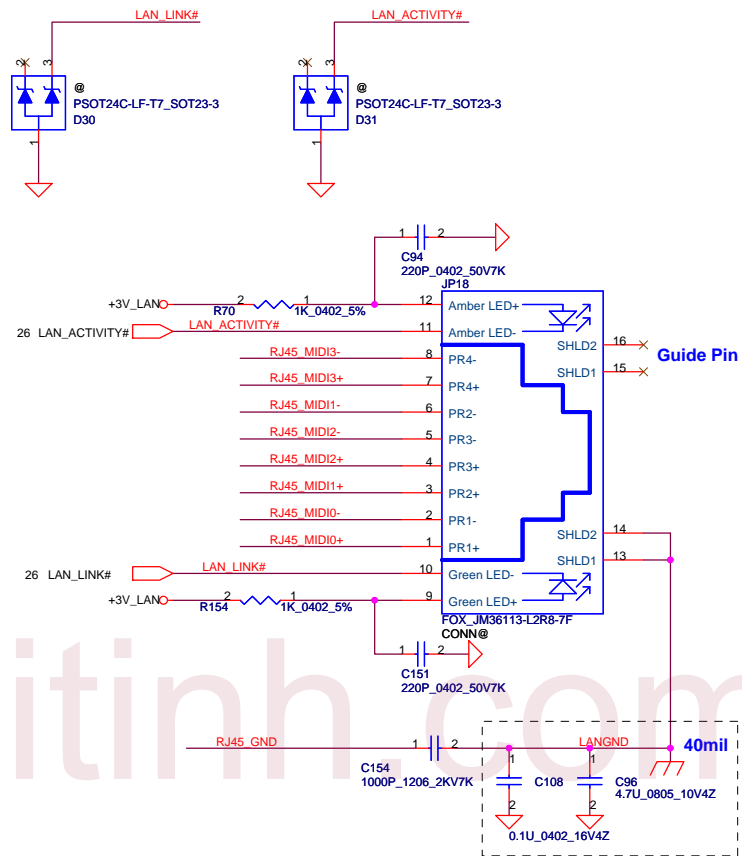
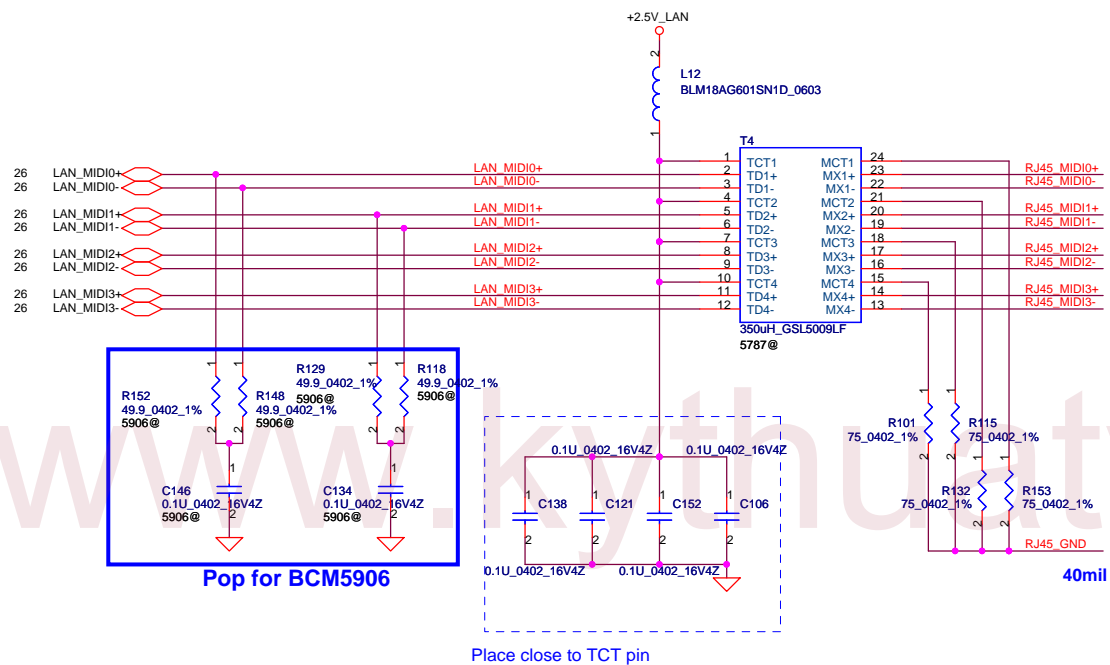
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Size	B	Document Number	ICL50/ICK70 M/B LA-3551P Schematié		Rev
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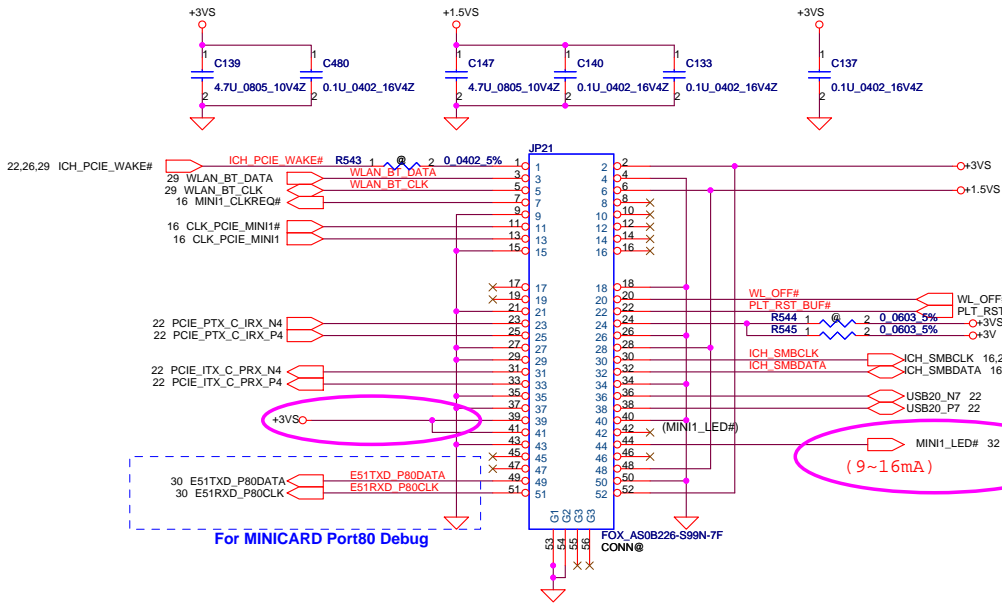
Security Classification	Compal Secret Data		Title	
Issued Date	2006/12/25	Deciphered Date	2007/12/25	LAN BCM5787M
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# LAN BCM5787M

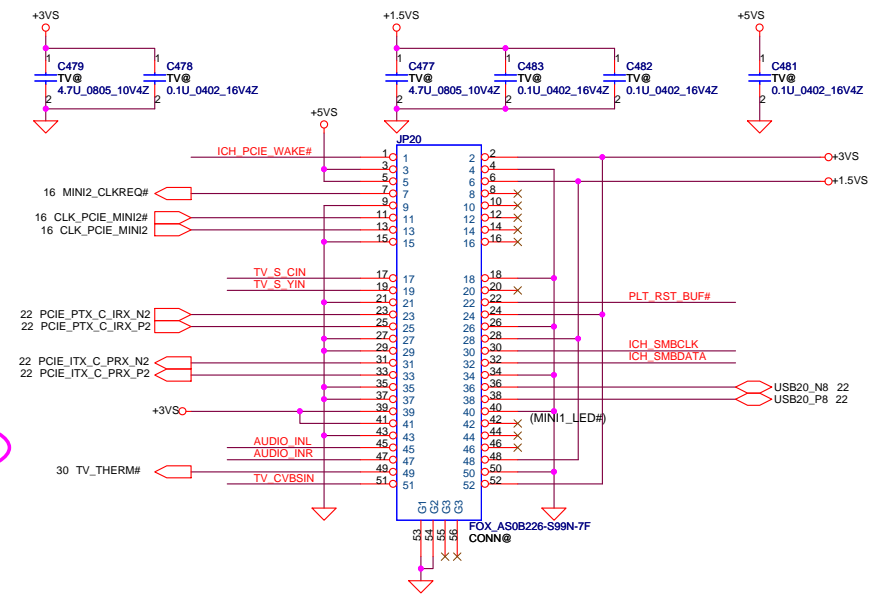


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Size B	Document Number	ICL50/ICK70 M/B LA-3551P Schematic		Rev	
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For Wireless LAN

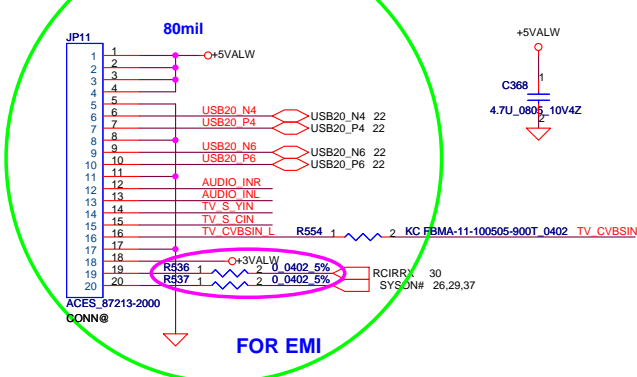


For TV-Tuner/HW MPEG



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

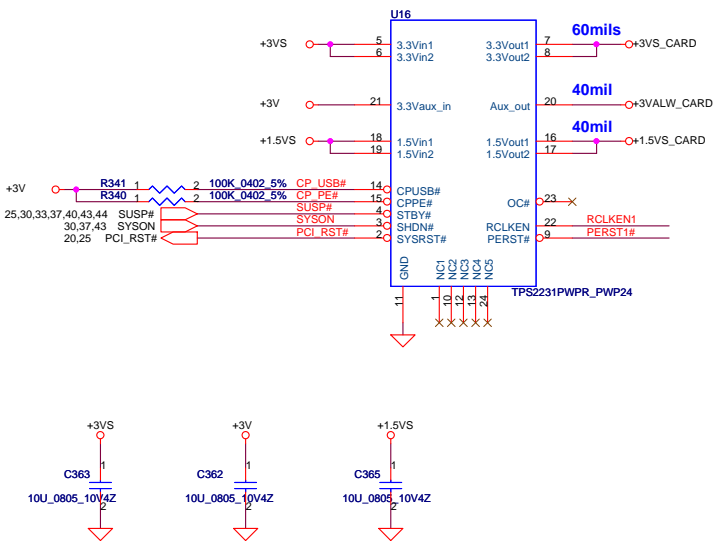
To USB/B Connector



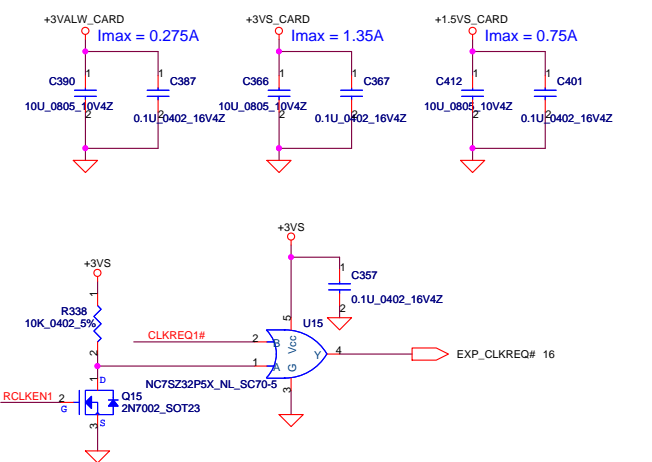
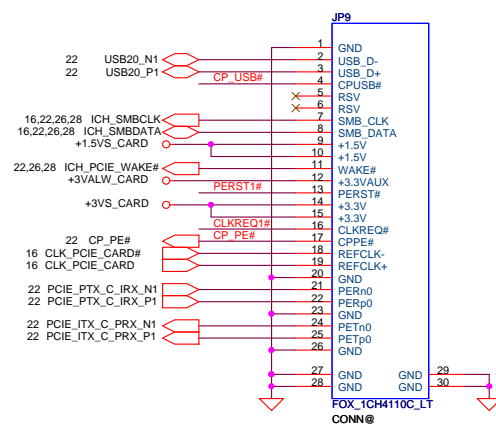
AV-IN Connector CIR

FOR EMI

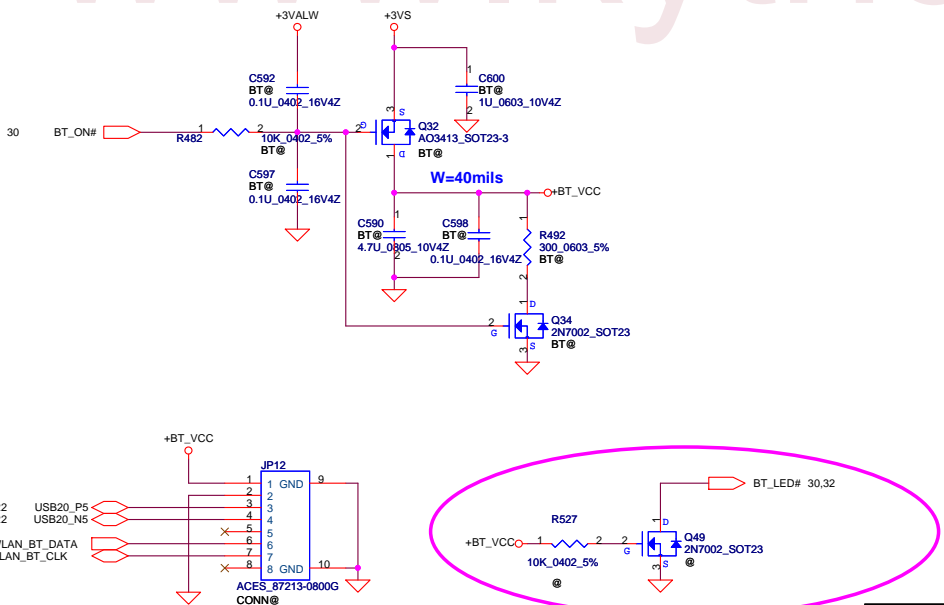
### New Card Power Switch



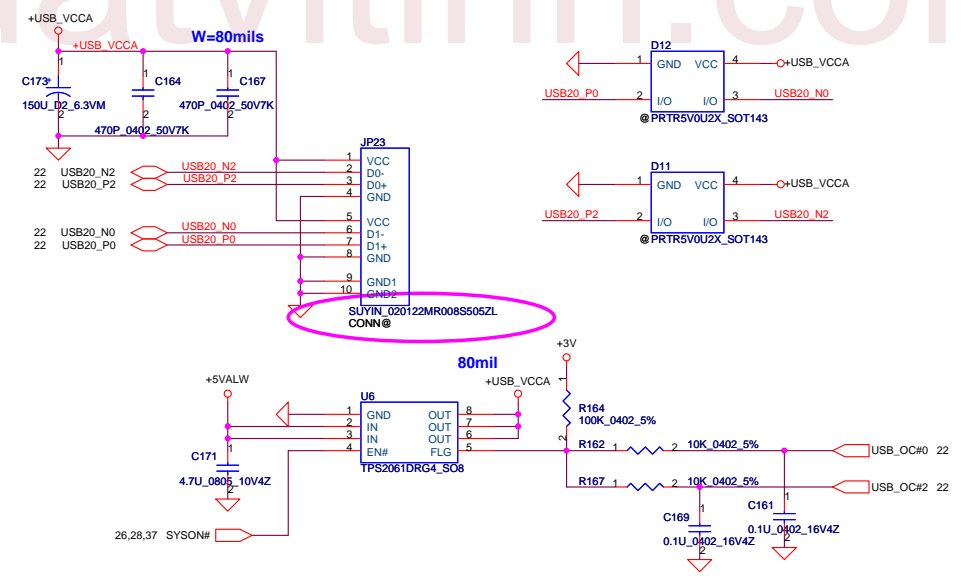
### New Card Socket (Left/TOP)



### Bluetooth Conn.



### USB CONN. (Stack-up Type)

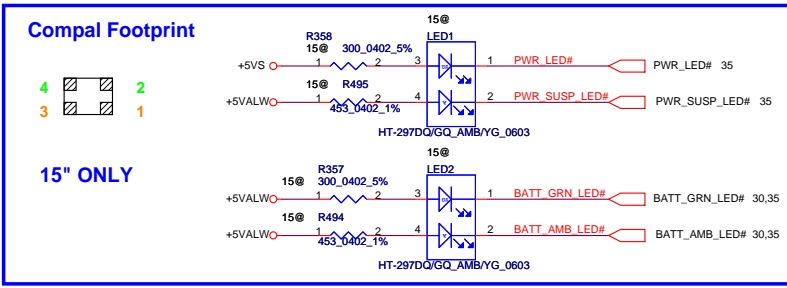
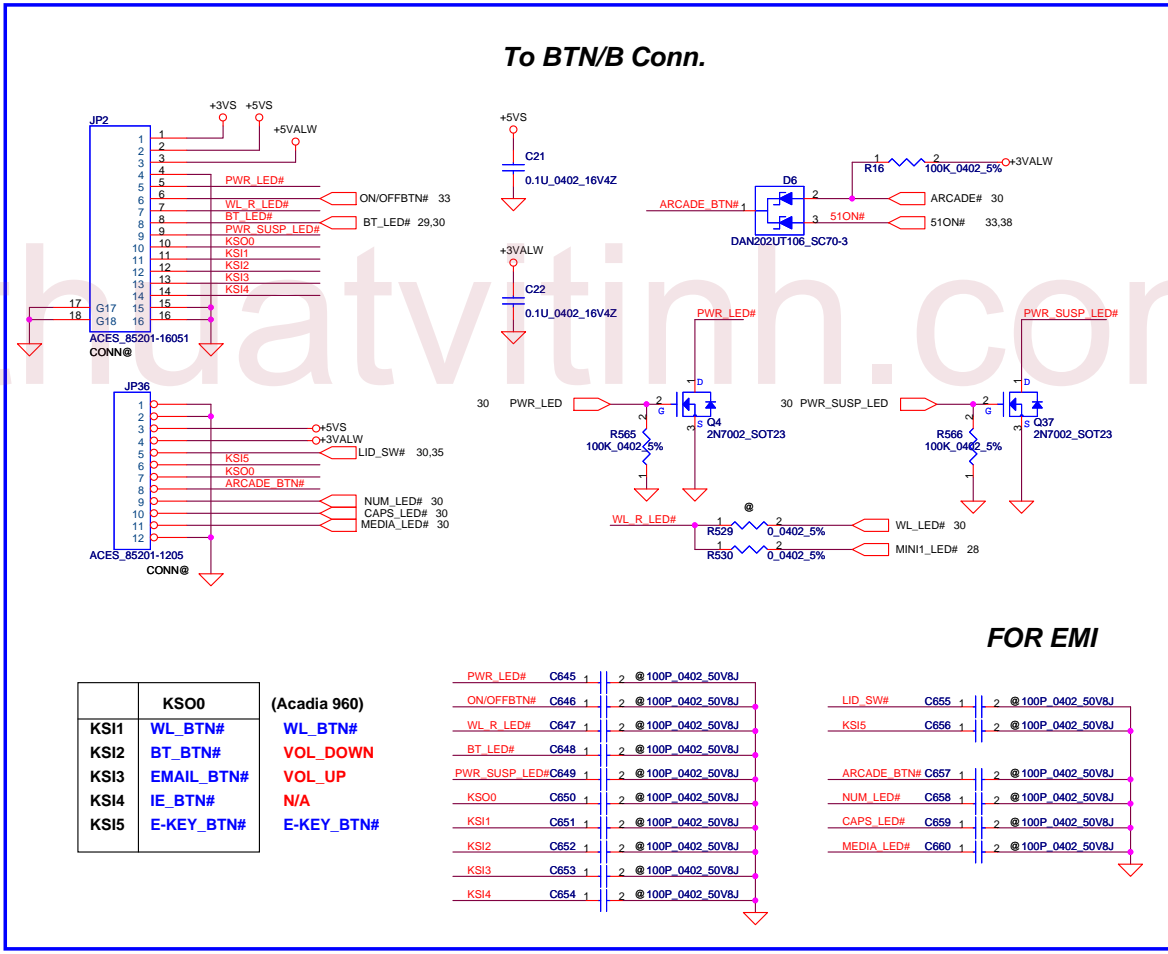
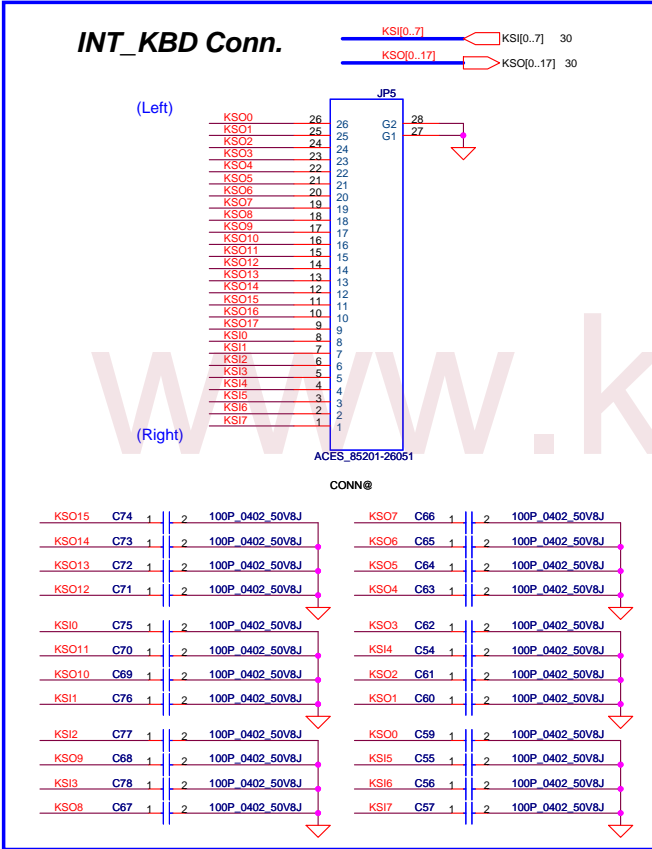
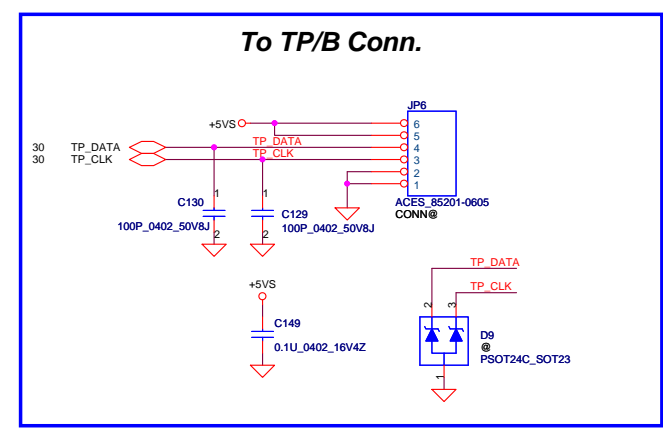
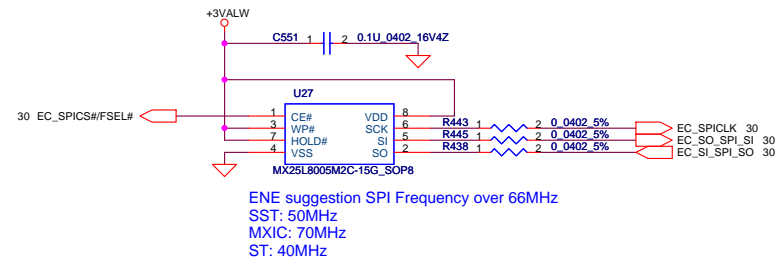
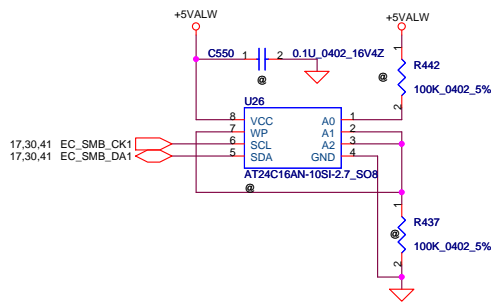


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				NEW CARD & USB Connector		
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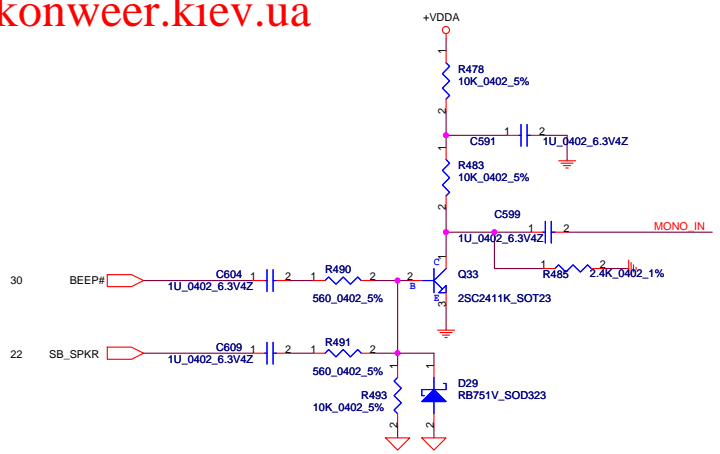


	KSO0	(Acadia 960)
KSI1	WL_BTN#	WL_BTN#
KSI2	BT_BTN#	VOL_DOWN
KSI3	EMAIL_BTN#	VOL_UP
KSI4	IE_BTN#	N/A
KSI5	E-KEY_BTN#	E-KEY_BTN#

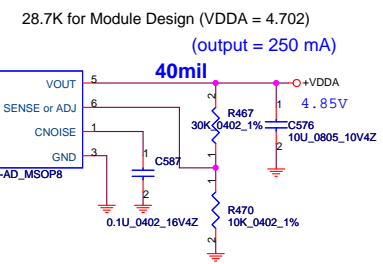
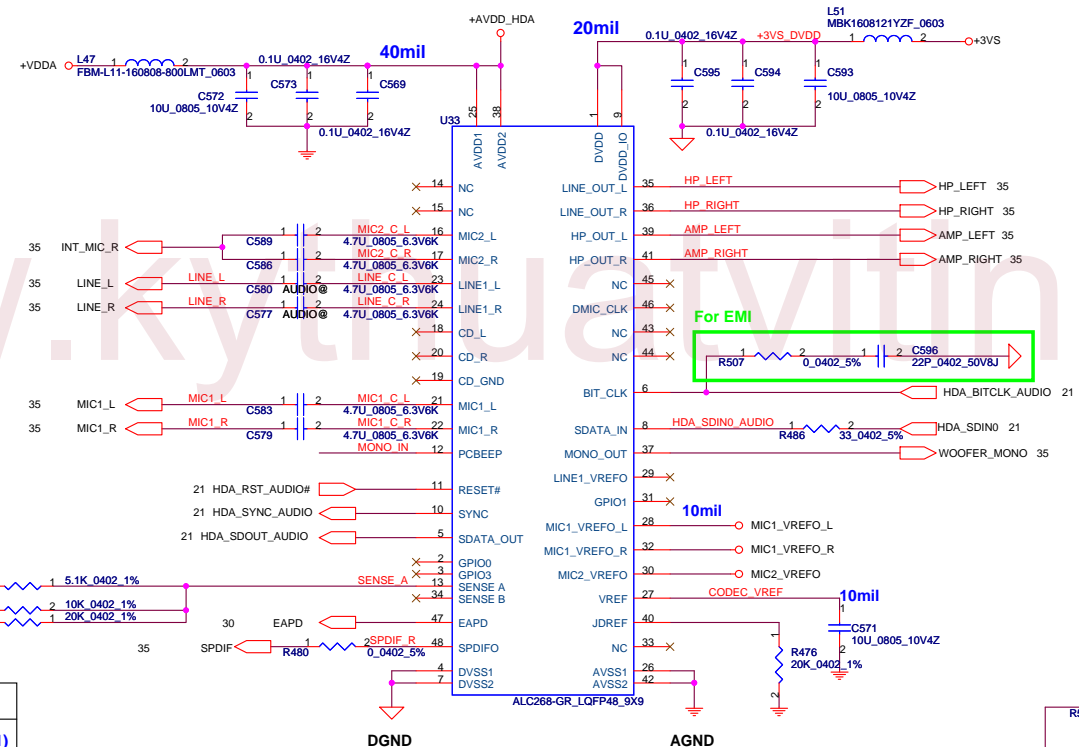
PWR_LED#	C645	1	2	@ 100P_0402_50V8J
ON/OFFBTN#	C646	1	2	@ 100P_0402_50V8J
WL_R_LED#	C647	1	2	@ 100P_0402_50V8J
BT_LED#	C648	1	2	@ 100P_0402_50V8J
PWR_SUSP_LED#	C649	1	2	@ 100P_0402_50V8J
KSO0	C650	1	2	@ 100P_0402_50V8J
KSI1	C651	1	2	@ 100P_0402_50V8J
KSI2	C652	1	2	@ 100P_0402_50V8J
KSI3	C653	1	2	@ 100P_0402_50V8J
KSI4	C654	1	2	@ 100P_0402_50V8J
LID_SW#	C655	1	2	@ 100P_0402_50V8J
KSI5	C656	1	2	@ 100P_0402_50V8J
ARCADIE_BTN#	C657	1	2	@ 100P_0402_50V8J
NUM_LED#	C658	1	2	@ 100P_0402_50V8J
CAPS_LED#	C659	1	2	@ 100P_0402_50V8J
MEDIA_LED#	C660	1	2	@ 100P_0402_50V8J

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Size	Document Number	Rev		Date	
B	ICL50/ICK70 M/B LA-3551P Schematic	Rev		Monday, August 20, 2007	
				Sheet	32 of 49

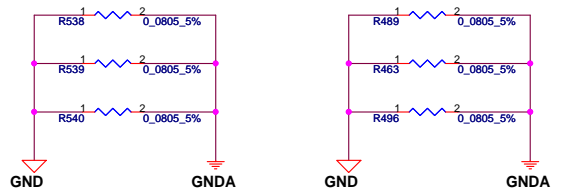




### HD Audio Codec



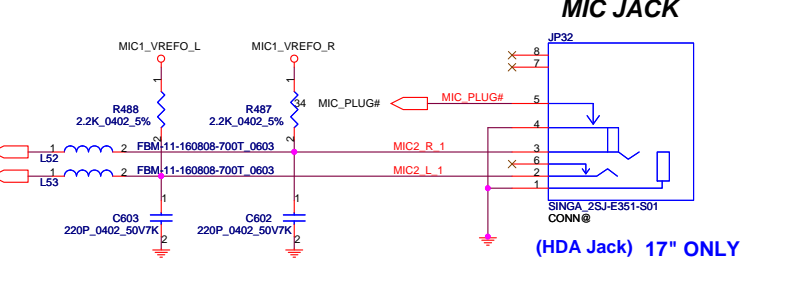
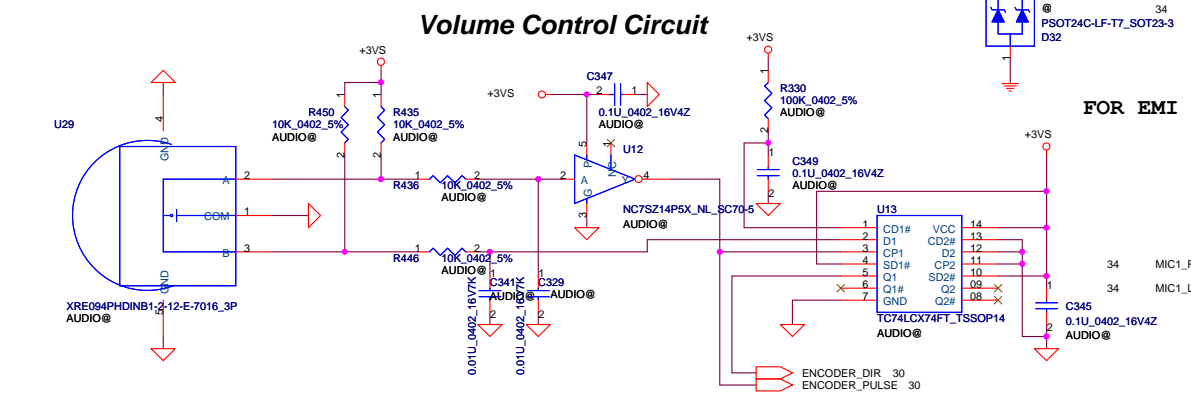
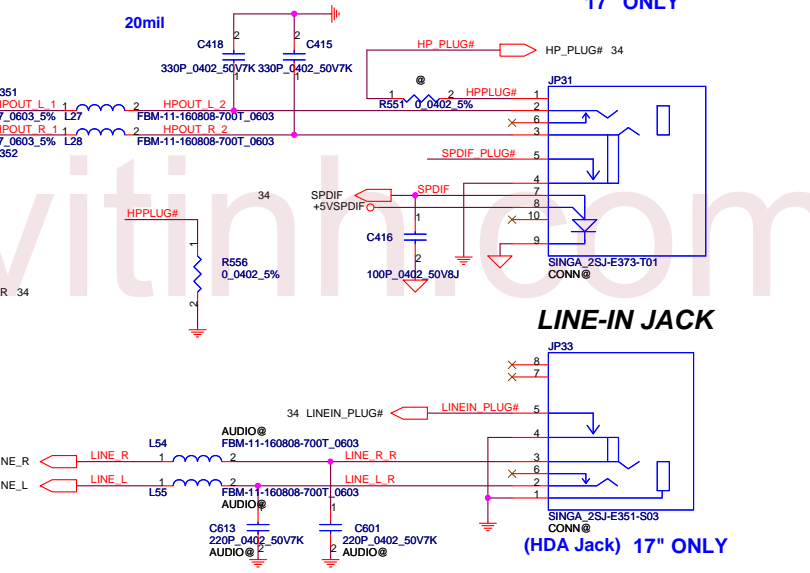
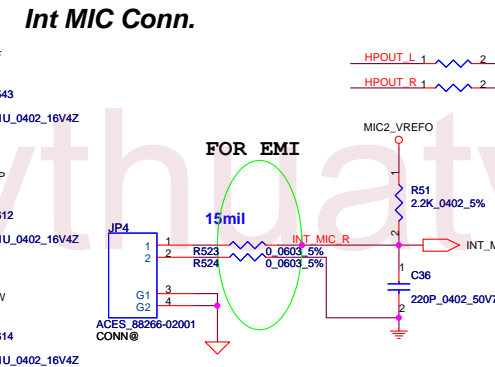
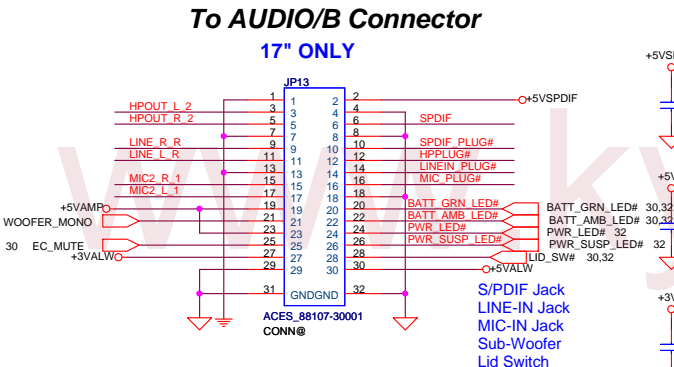
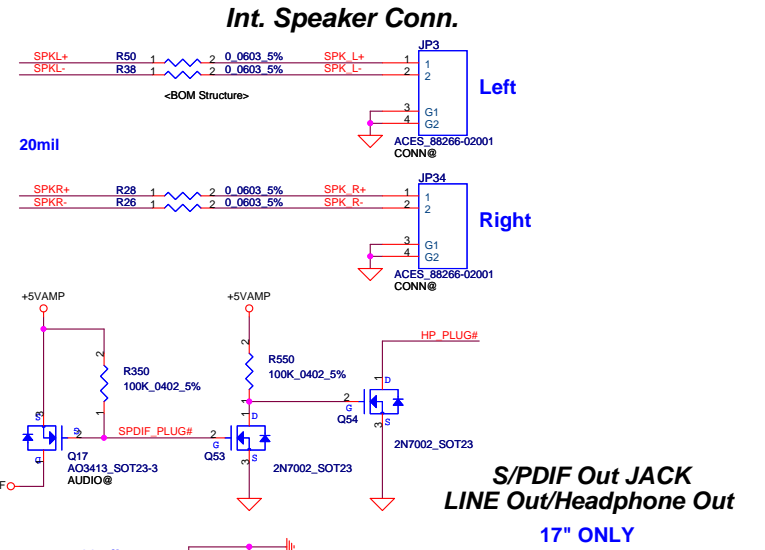
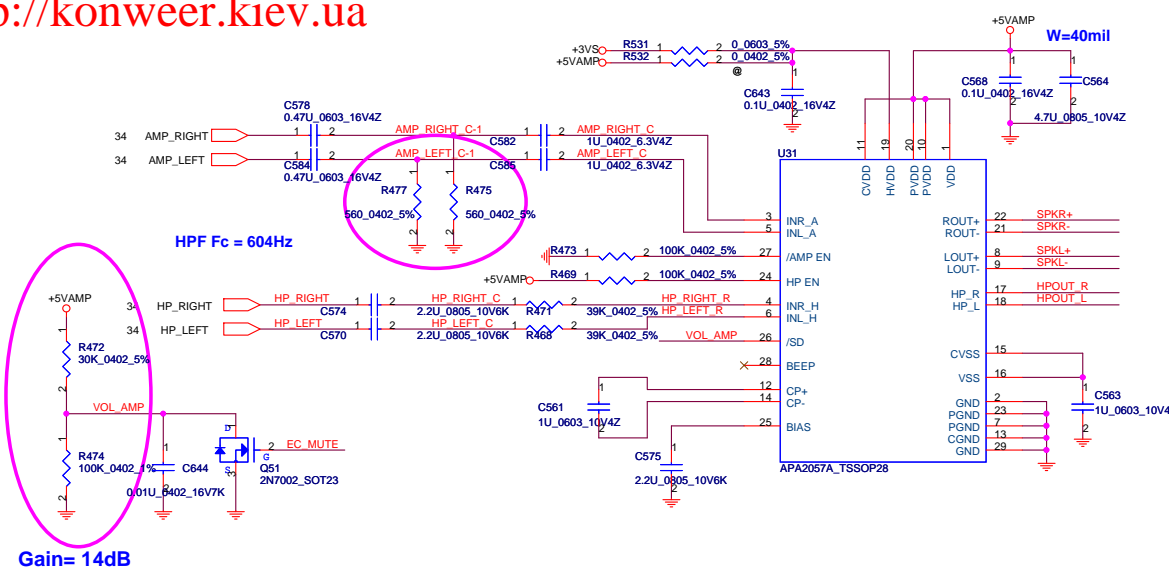
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



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Issued Date	2006/12/25	Deciphered Date
		2007/12/25

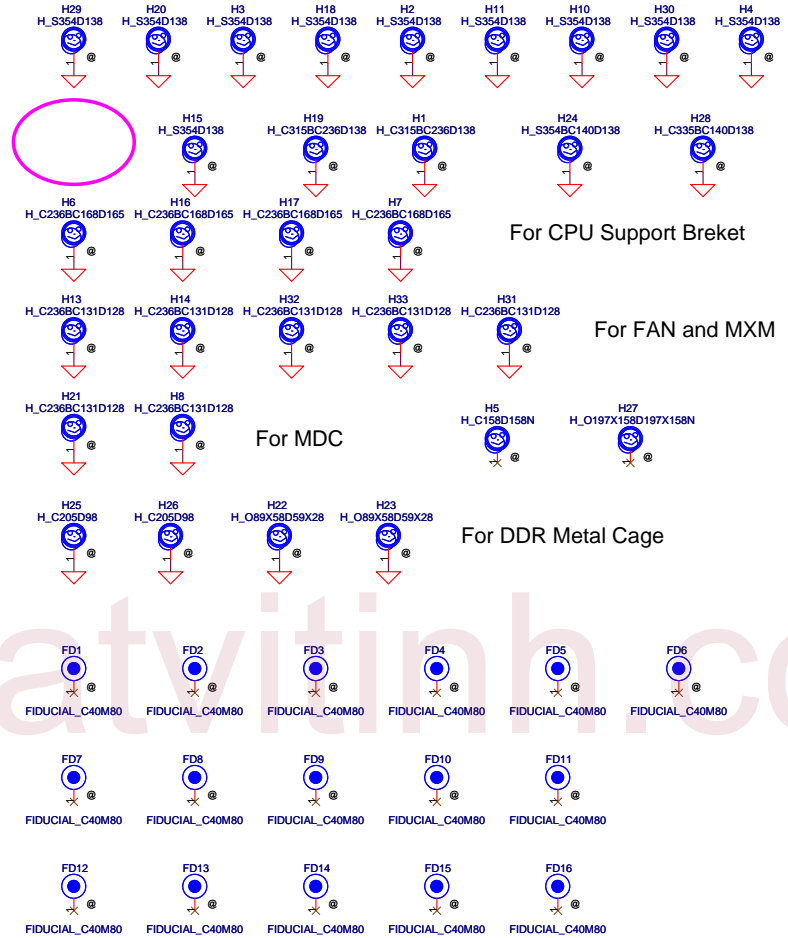
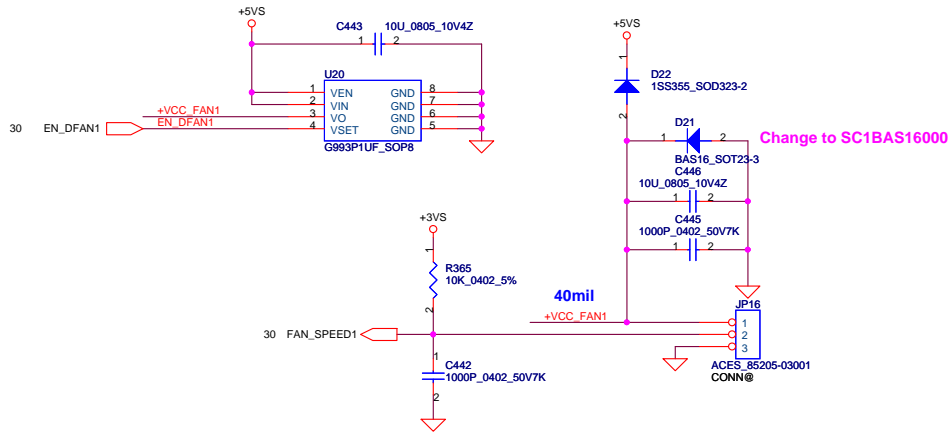
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Compal Electronics, Inc.		
Title		
HD Audio Codec ALC268		
Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematič	
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Security Classification		Compal Secret Data		Title	
Issued Date	2006/12/25	Deciphered Date	2007/12/25	Compal Electronics, Inc.	
				Amplifier & Audio Jack	
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				ICL50/ICK70 M/B LA-3551P Schematic	
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FAN1 Conn



For CPU Support Bracket

For FAN and MXM

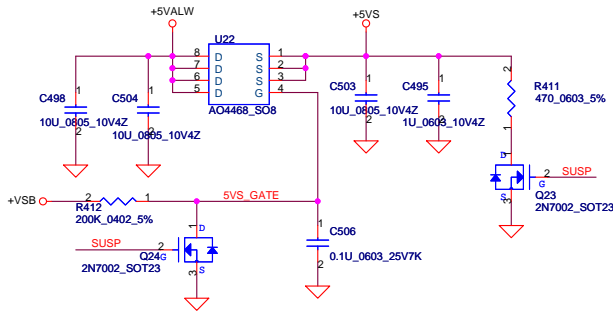
For MDC

For DDR Metal Cage

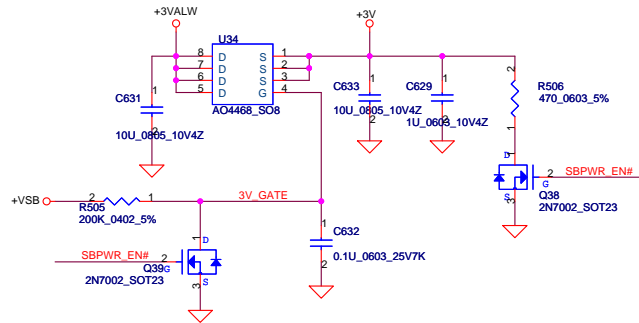
www.kythuativitinh.com

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Size	Document Number	Rev		
B	ICL50/ICK70 M/B LA-3551P Schematic			
Date:	Wednesday, August 15, 2007	Sheet	36	of 49

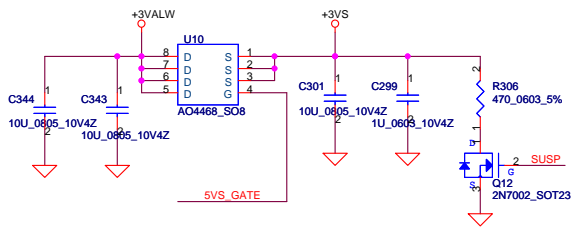
**+5VALW TO +5VS**



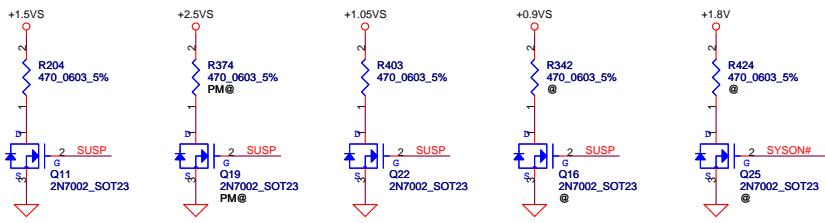
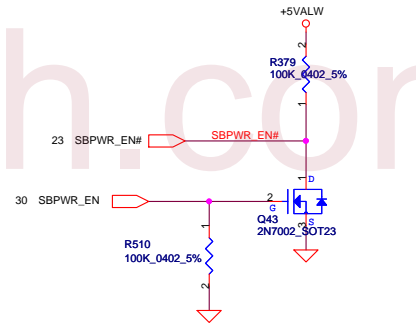
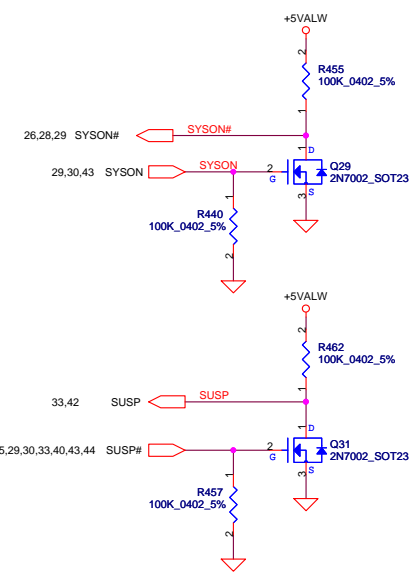
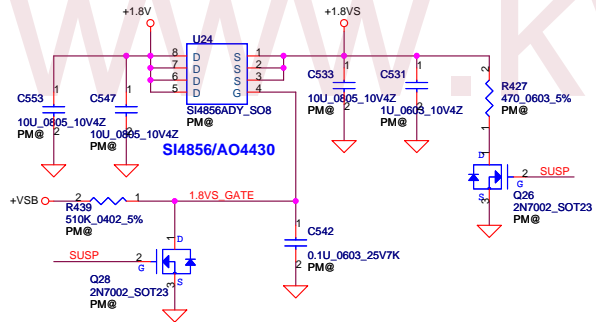
**+3VALW TO +3V\_SB(ICH8M AUX Power)**



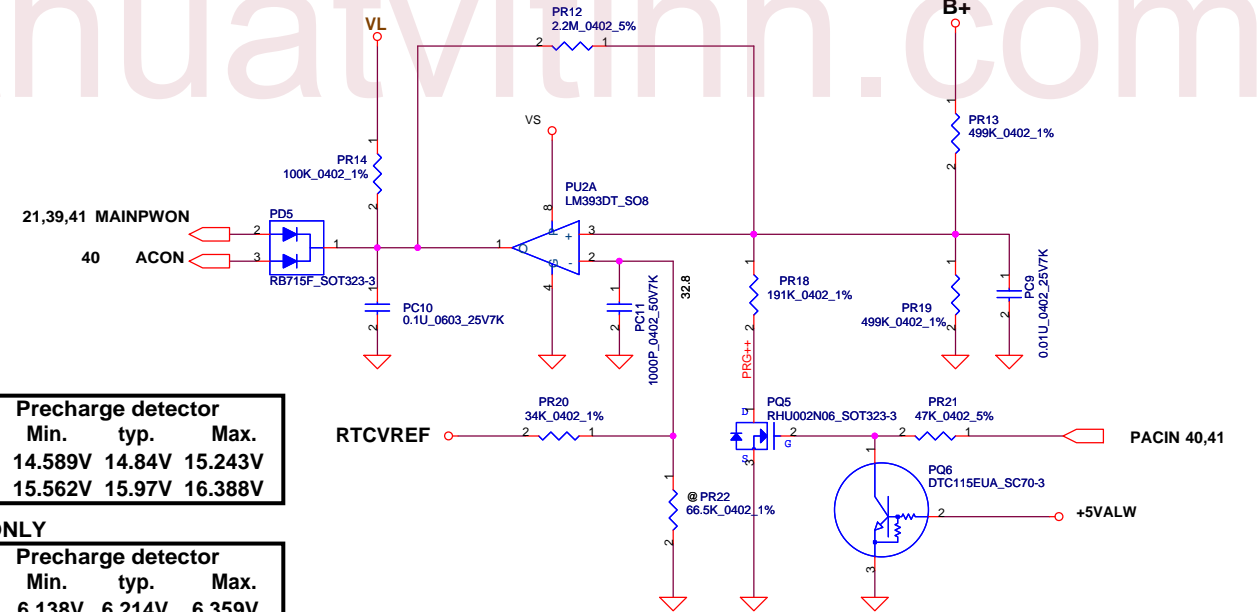
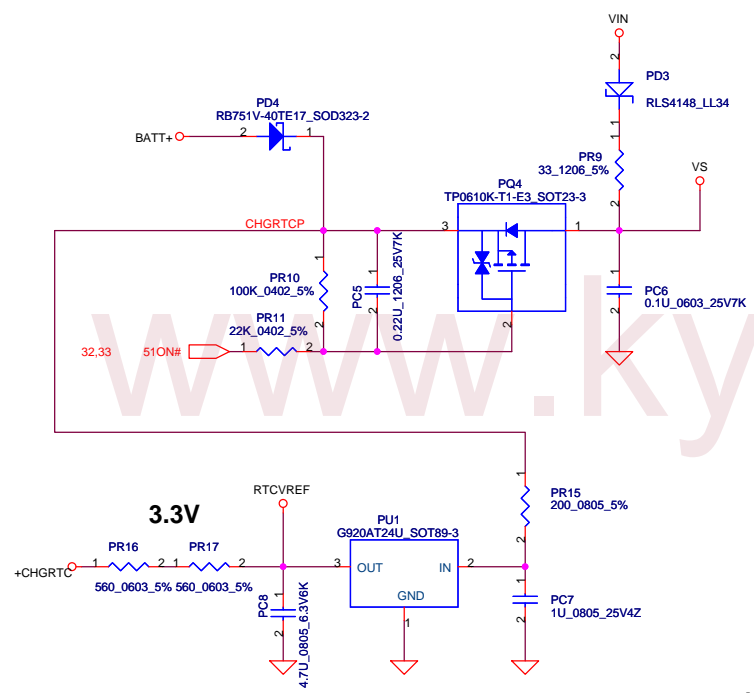
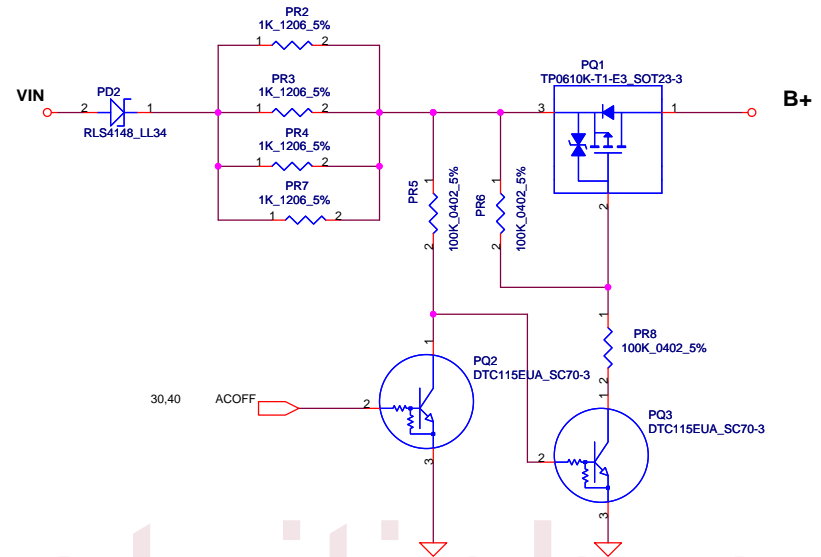
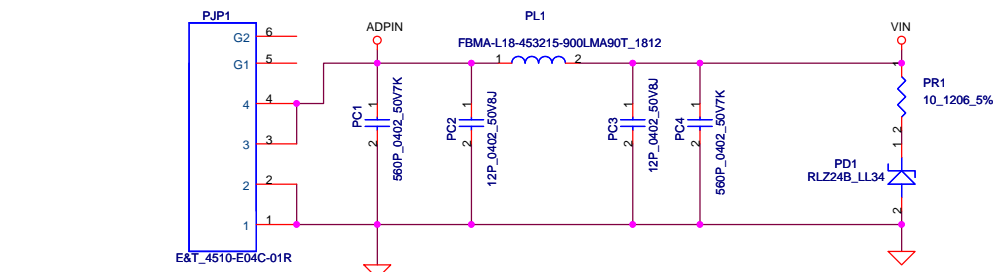
**+3VALW TO +3VS**



**+1.8V to +1.8VS**



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Size	Document Number	Date:		Rev	
B	ICL50/ICK70 M/B LA-3551P Schematic	Wednesday, August 15, 2007		37 of 49	

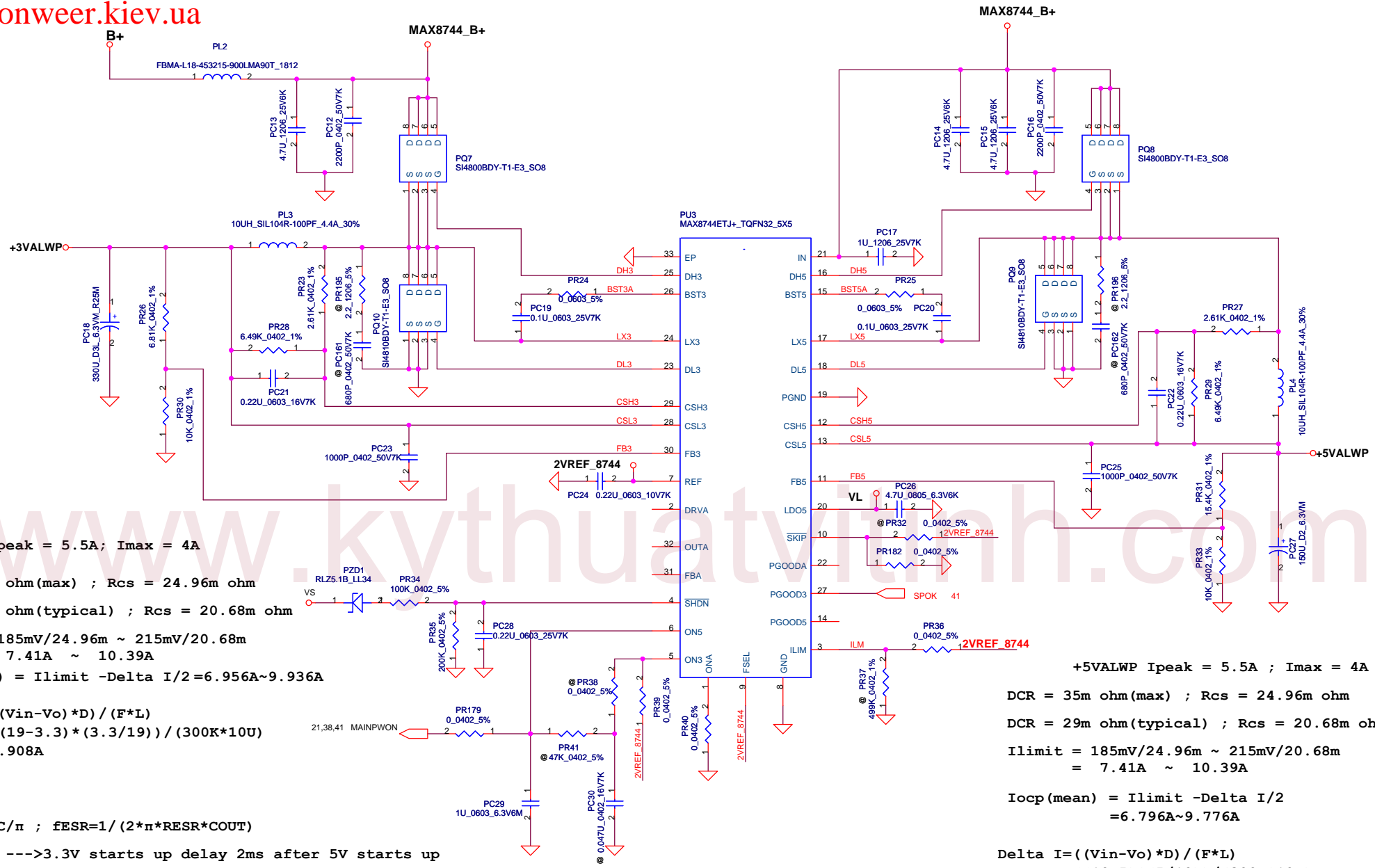


ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

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Title	DCIN/DECTOR			
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**+3VALWP Ipeak = 5.5A; Imax = 4A**  
 DCR = 35m ohm(max) ; Rcs = 24.96m ohm  
 DCR = 29m ohm(typical) ; Rcs = 20.68m ohm  
 Ilimit = 185mV/24.96m ~ 215mV/20.68m  
 = 7.41A ~ 10.39A  
 Iocp(mean) = Ilimit -Delta I/2=6.956A~9.936A

Delta I=((Vin-Vo)\*D)/(F\*L)  
 =((19-3.3)\*(3.3/19))/(300K\*10U)  
 =0.908A

Notes :  
 fESR<=fOSC/n ; fESR=1/(2\*pi\*RESR\*COU)  
 ON3 = REF --->3.3V starts up delay 2ms after 5V starts up

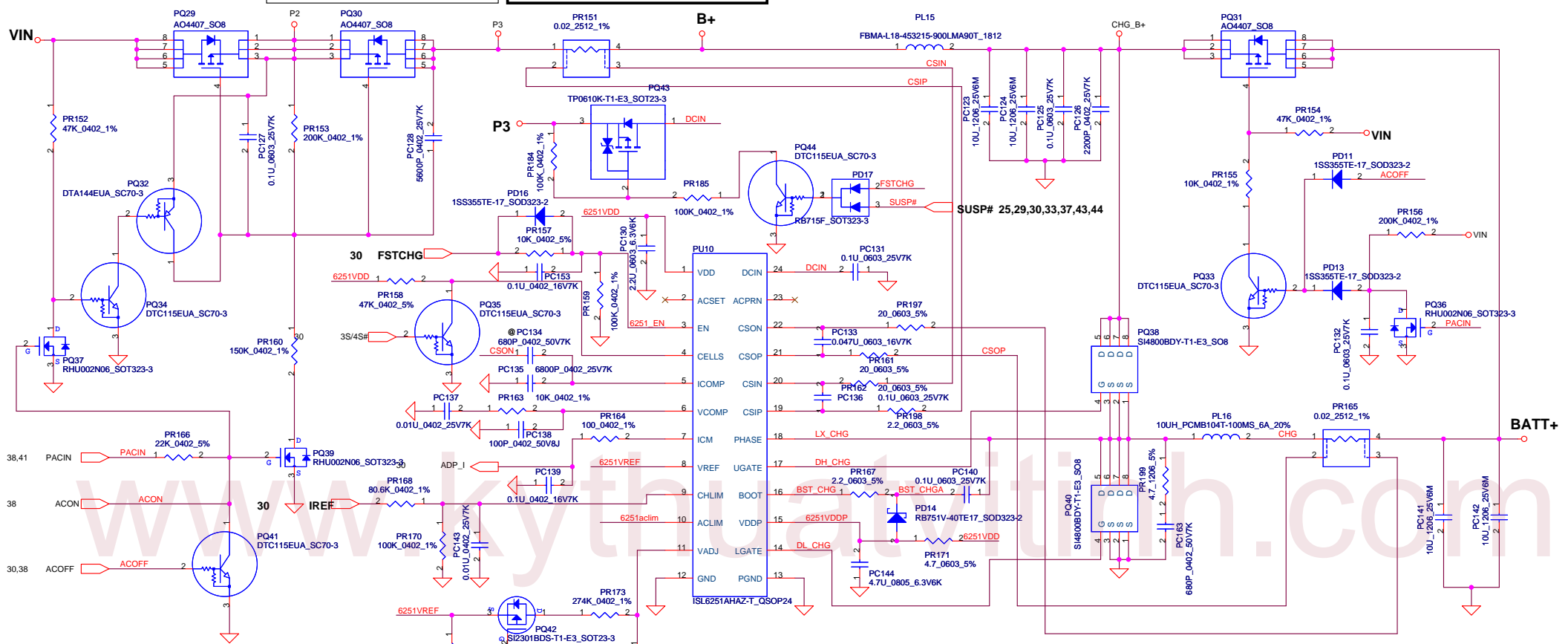
**+5VALWP Ipeak = 5.5A ; Imax = 4A**  
 DCR = 35m ohm(max) ; Rcs = 24.96m ohm  
 DCR = 29m ohm(typical) ; Rcs = 20.68m ohm  
 Ilimit = 185mV/24.96m ~ 215mV/20.68m  
 = 7.41A ~ 10.39A  
 Iocp(mean) = Ilimit -Delta I/2  
 =6.796A~9.776A  
 Delta I=((Vin-Vo)\*D)/(F\*L)  
 =((19-5)\*(5/19))/(300K\*10U)  
 1.228A

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Iada=0~4.74A (90W)

$ADP\_I = 19.9 * I_{adapter} * R_{sense}$

$CP = 85\% * I_{ada} ; CP = 4.07A$

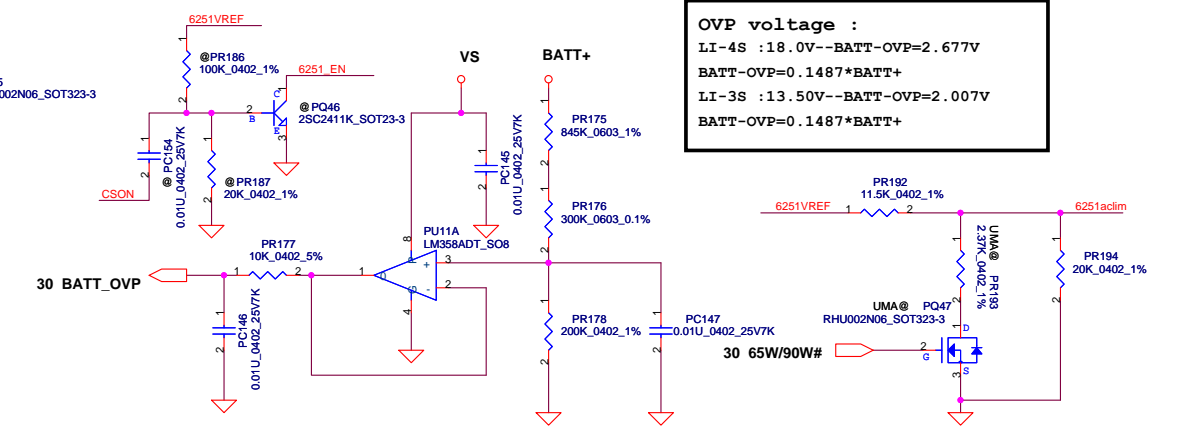
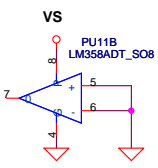


CP mode  
 $I_{input} = (1/0.02) * ((0.05 * Vaclim) / 2.39 + 0.05)$   
 where  $Vaclim = 1.502V$ ,  $I_{input} = 4.07A$   
 $Vaclim = 2.39 * ((10K // 152K) / ((5.76K // 152K) + (10K // 152K))) = 1.502V$

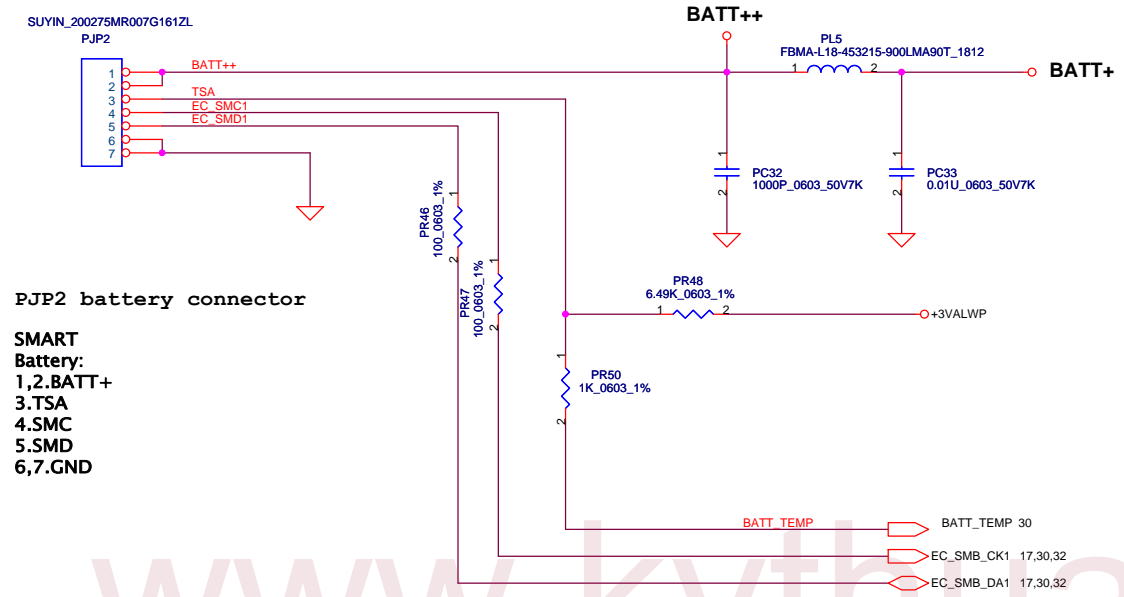
CC=0.6~4.48A  
 $I_{REF} = 0.7224 * I_{charge}$   
 $I_{REF} = 0.43V \sim 3.24V$

BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V

OVP voltage :  
 LI-4S : 18.0V -- BATT-OVP = 2.677V  
 BATT-OVP = 0.1487 \* BATT+  
 LI-3S : 13.50V -- BATT-OVP = 2.007V  
 BATT-OVP = 0.1487 \* BATT+

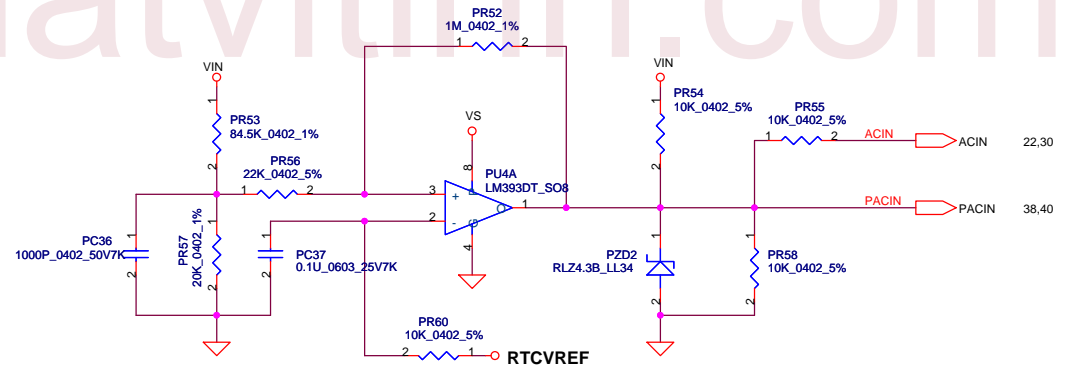
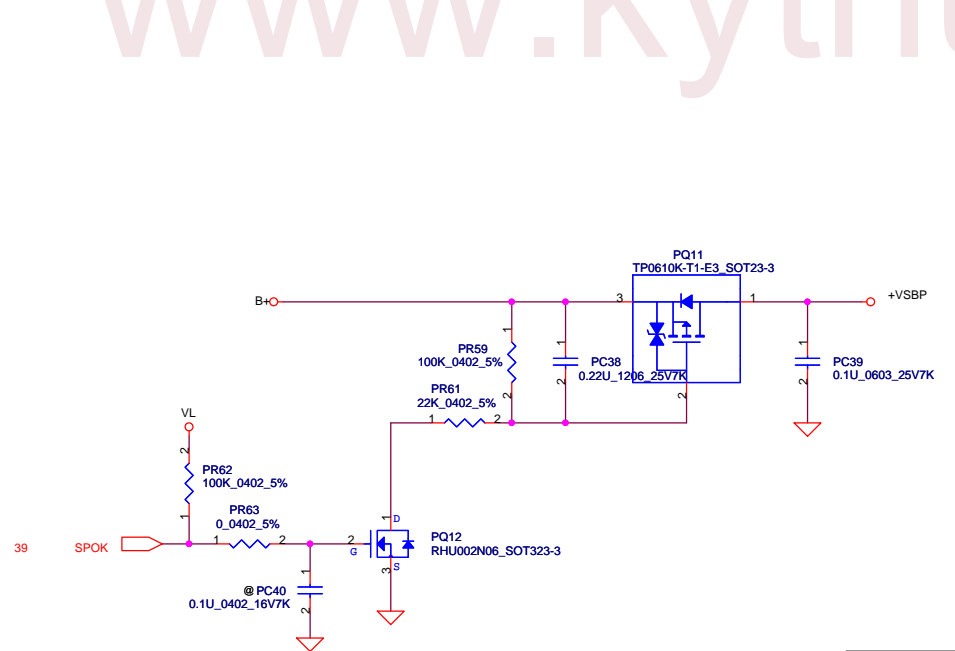
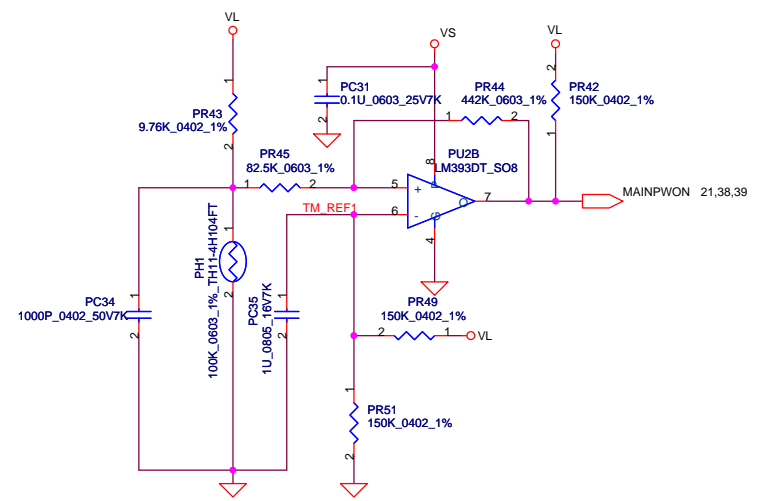


PH1 under CPU botten side :  
 CPU thermal protection at 90 degree C  
 Recovery at 70 degree C



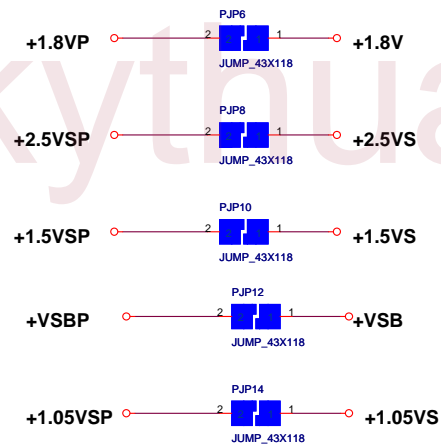
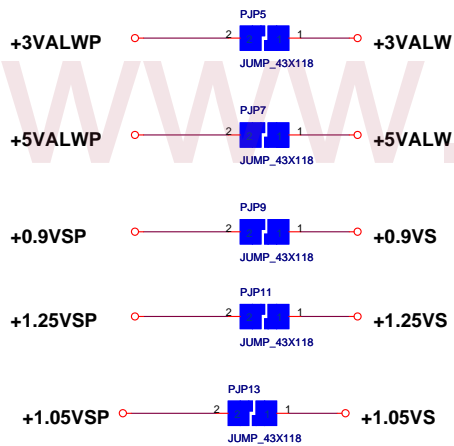
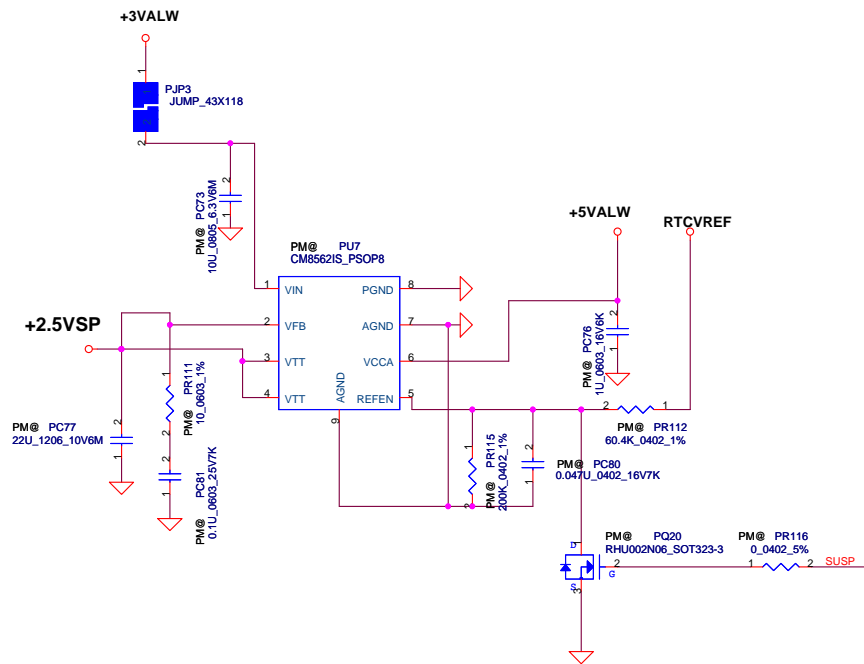
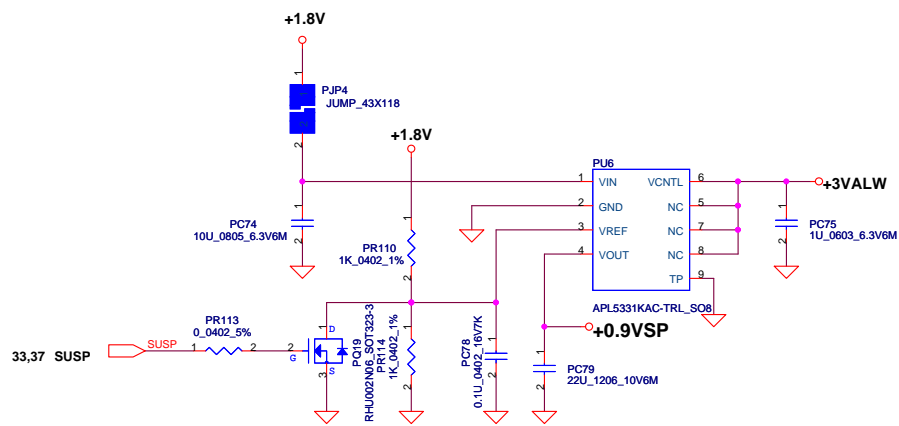
PJP2 battery connector

SMART Battery:  
 1,2.BATT+  
 3.TSA  
 4.SMC  
 5.SMD  
 6,7.GND

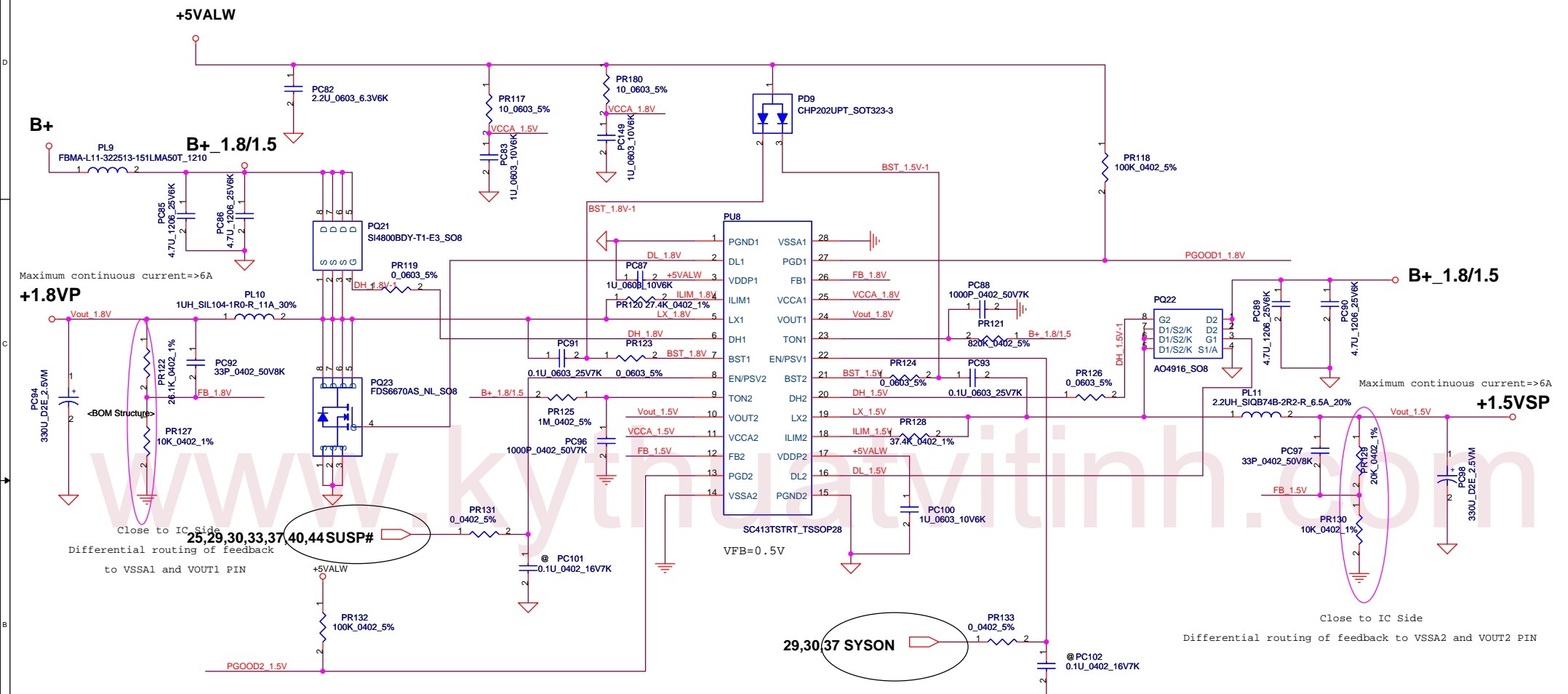


Vin Detector			
Min.	typ.	Max.	
H-->L	16.976V	17.257V	17.728V
L-->H	17.430V	17.901V	18.384V

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Size		Document Number	Rev	
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Date:	Wednesday, August 15, 2007	Sheet	42	of 49



Maximum continuous current=>6A

Maximum continuous current=>6A

Close to IC Side  
Differential routing of feedback  
to VSSA1 and VOUT1 PIN

Close to IC Side  
Differential routing of feedback to VSSA2 and VOUT2 PIN

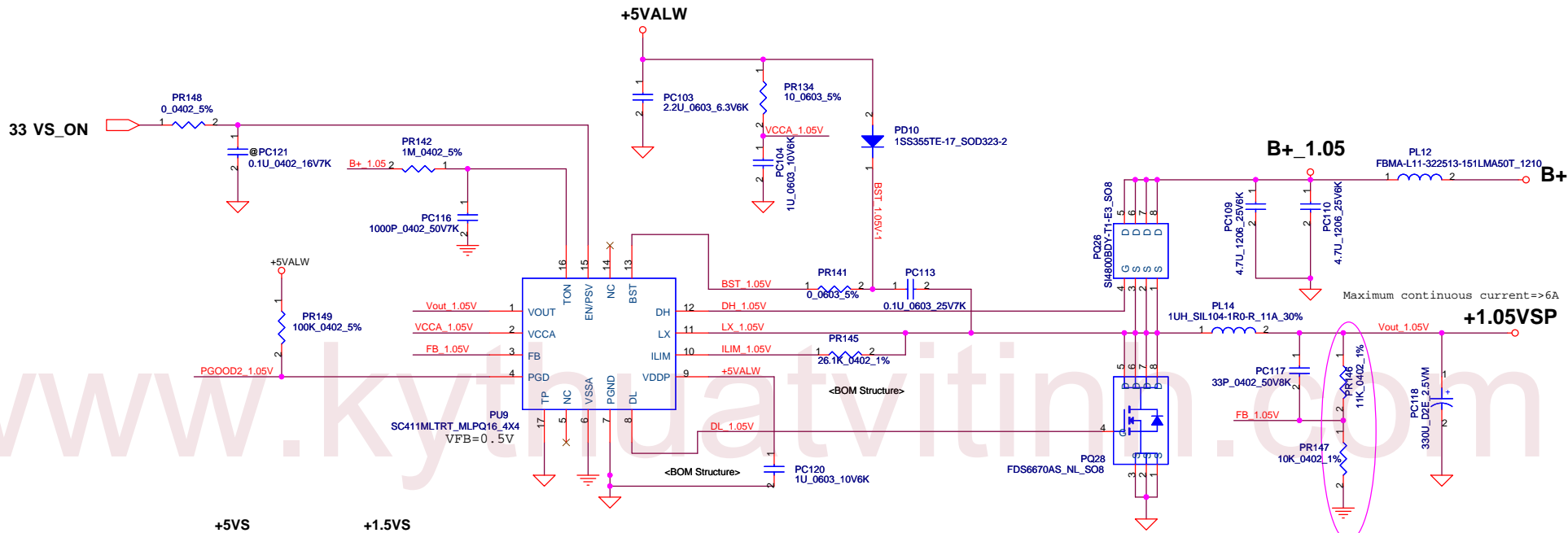
VFB=0.5V  
 $V_o = VFB * (1 + PR122 / PR127) = 1.805V$   
**Ipeak=11.73A, Imax=8.211A**  
 $Ton = (3.3E-12 * (PR121 + 37K) * (Vout / VBat)) + 50ns$   
 $= 3.3 * 10e-12 * (820K + 37K) * (1.8 / 19) + 50ns = 0.3179us$   
 FDS6670AS:Rds(on) => Typ: 9 mOhm  
 Max: 11.5 mOhm  
 $Iocp = Ivalley + Iripple / 2$   
 $Iripple = (vin - vout) * (Ton / L) = 5.467A, 1/2 Iripple = 2.734A$   
 $Ivalleymin = 10E-6 * (PR120 / Rds(ON)max * 1.5)$   
 $= 9 * 10e-6 * (27.4K / 0.0115 * 1.5) = 14.295A > 11.73 * 1.2 = 14.076A$   
 $Ivalleymax = 10E-6 * (PR120 / Rds(ON)typ * 1.2)$   
 $= 11 * 10e-6 * (27.4K / 0.009 * 1.2) = 27.907A$   
 OCP ==> 17.029A ~ 30.641A

VFB=0.5V  
 $V_o = VFB * (1 + PR129 / PR130) = 1.5V$   
**Ipeak=4.39A+2.91A=7.3A, Imax=7.3\*0.7=5.11A**  
 $Ton = (3.3E-12 * (PR125 + 37K) * (Vout / VBat)) + 50ns$   
 $= 0.3201us$   
 AO4916 Rds(on) => Typ: 21 mOhm  
 Max: 27 mOhm  
 $Ivalleymin = 9 * E-6 * (37.4K / 0.027 * 1.4) = 8.904A > 7.3 * 1.2 = 8.76A$   
 $Ivalleymax = 11 * E-6 * (37.4K / 0.021 * 1.1) = 17.809A$   
 $Iripple = (vin - vout) * (Ton / L) = 2.546A, 1/2 Iripple = 1.273A$   
 $Iocp = Ivalley + Iripple / 2$   
 OCP ==> 10.177A ~ 19.082A



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Compal Electronics, Inc.



Maximum continuous current=>6A

Close to IC Side  
Differential routing of feedback to VSSA2 and VOUT2 PIN

**VFB=0.5V, Ipeak=14.02A, Imax=9.814A**

The current rating of +1.05VSP include +VCC\_GFX current.

$V_o = VFB * (1 + PR146 / PR147) = 1.05V$

$Ton = (3.3E-12 * (PR142 + 37K) * (Vout / VBat)) + 50ns = 0.2391us$

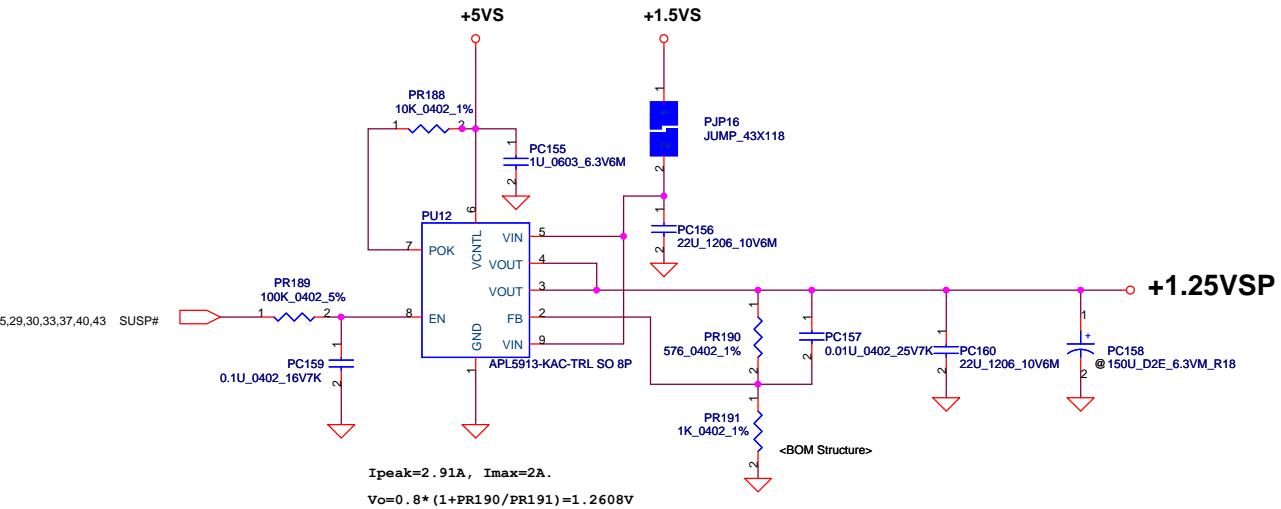
SI4810BDY:Rds(on) => Typ: 9mOhm  
Max: 11.5 mOhm

$Ivalleymin = 9 * 10E-6 * (PR145 / Rds(ON))max * 1.5$   
 $= 9 * 10E-6 * (26.1K / (0.0115 * 1.5)) = 13.617A$

$Ivalleymax = 11 * 10E-6 * (PR145 / Rds(ON))min * 1.2$   
 $= 11 * 10E-6 * (26.1K / (0.009 * 1.3)) = 20.076A$

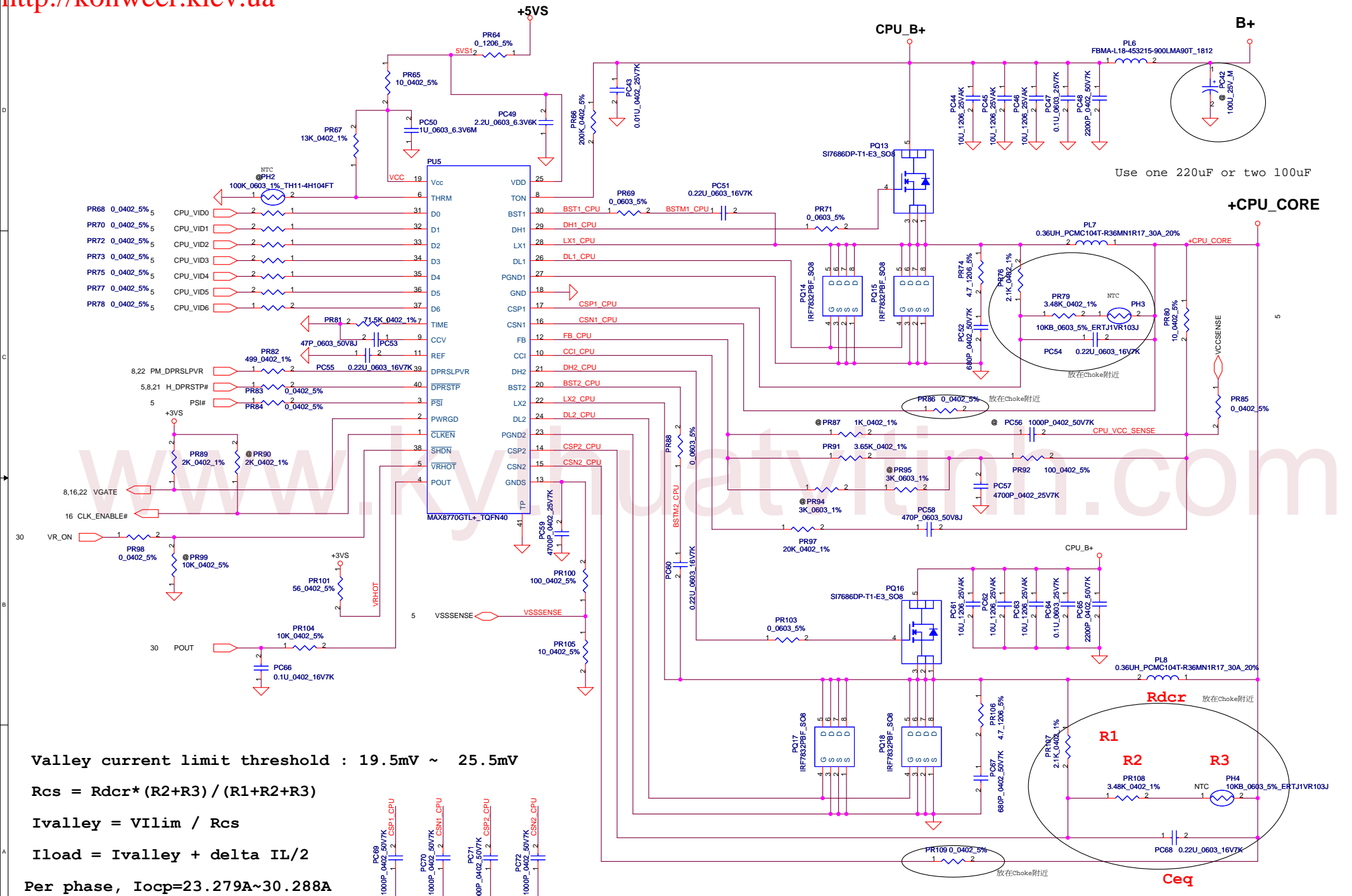
$Iripple = (vin - vout) * (Ton / L) = 4.292A, 1/2 Iripple = 2.146A$

$Iocp = Ivalley + Iripple / 2$   
**OCP => 15.763A ~ 22.222A**



Ipeak=2.91A, Imax=2A.  
Vo=0.8 \* (1+PR190/PR191)=1.2608V

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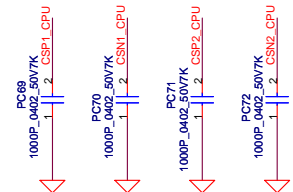
Valley current limit threshold : 19.5mV ~ 25.5mV

$$R_{cs} = R_{dcr} * (R2 + R3) / (R1 + R2 + R3)$$

$$I_{valley} = V_{lim} / R_{cs}$$

$$I_{load} = I_{valley} + \Delta I_L / 2$$

Per phase,  $I_{ocp} = 23.279A \sim 30.288A$



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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	CPU_CORE high side MOS desine change	In order to prevent EOL of SI7840, change to SI7686.	0.1	45	Change PQ13 and PQ16 form SB578400080(S TR SI7840DP-T1-E3 1N S08) to SB000008L80(S TR SI7686DP-T1-E3 1N S08).	10/30/06	EVT
2	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ43 SB906100210( S TR TP0610K)	12/21/06	DVT
3	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ44 SB301150000(S TR DTC115EUA)	12/21/06	DVT
4	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD16 SC1SS355010( S DIO 1SS355) Delete PD12 SC1SS355010( S DIO 1SS355)	12/21/06	DVT
5	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD17 SCSB715F000(S DIO RB715F)	12/21/06	DVT
6	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR184,PR185 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
7	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC153 SE076104K80(S CER CAP 0.1U 0402 16V K X7R)	12/21/06	DVT
8	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ45 SB502060000(S TR RHU002N06)	12/21/06	DVT
9	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ46 SB324110010(S TR 2SC411K)	12/21/06	DVT
10	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR183 SD034274380(S RES 1/16W 274K 0402 1%)	12/21/06	DVT
11	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR186 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
12	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR187 SD034200280(S RES 1/16W 20K 0402 1%)	12/21/06	DVT
13	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC154 and PC146 SE075103K80(S CER CAP 0.01U K 25V X7R 0402)	12/21/06	DVT
14	Noise issue in S3 mode and idle mode.	In order to prevent noise issue in S3 mode and idle mode.	0.2	40	Add PC42 SF22004M210(S CAP 220U_25V_M)	12/21/06	DVT
15	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Change PR157 from SD028000080(s res 1/16w 0 0402 5%) TO SD0281000280(S RES 1/16W 10K 0402 5%)	12/21/06	DVT
16	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR34 from SD028470280(S RES 1/16w 47K 0402 5%) to SD028100380(S RES 1/16W 100K 0402 5%)	12/21/06	DVT
17	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR35 SD028100380( S RES 1/16W 100K 0402 5%) to SD028200380(S RES 1/16W 200K 0402 5%)	12/21/06	DVT
18	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PC28 from SE042104K80(S CER CAP 0.1U 25V K X7R 0603) to SE000005ZM8(S CER CAP 0.22U 25V K X7R 0603)	12/21/06	DVT
19	CPU MOSFET switching has interference.	Improve CPU switching interference.	0.2	45	Change PC69,PC70,PC71,PC72 from SE082221J80 to SE068102J80(S CER CAP 1000P 25V J NPO 0402)	12/21/06	DVT
20	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PU7 SA085620080 from X63470BOL01.	12/21/06	DVT
21	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PQ20 SB502060000 from X63470BOL01.	12/21/06	DVT
22	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR111 SD014100A80 from X63470BOL01.	12/21/06	DVT
23	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR112 SD034604280 from X63470BOL01.	12/21/06	DVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR115 SD034200380 from X63470BOL01.	10/30/06	EVT
2	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR116 SD028000080 from X63470BOL01.	12/21/06	DVT
3	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC73 SE142475K80 from X63470BOL01.	12/21/06	DVT
4	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC76 SE135105K80 from X63470BOL01.	12/21/06	DVT
5	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC77 SE116226M80 from X63470BOL01.	12/21/06	DVT
6	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC80 SE076473K80 from X63470BOL01.	12/21/06	DVT
7	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC81 SE042104K80 from X63470BOL01.	12/21/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ25 SB548000310(S TR SI4800BDY) .	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ27 SB548100020(S TR 4810BDY)	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PD10 from SC1P202U010 to SC1SS355010.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR135 SD034100380.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR140,SD013000080, PR150 SD028000080.	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR181 SD013100A80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR139 SD034150280.	12/27/06	DVT
15	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR144 SD034100280	12/27/06	DVT
16	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR137 SD034105280.	12/27/06	DVT
17	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR138 SD028100480.	12/27/06	DVT
18	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC105,PC106 SE142475K80.	12/27/06	DVT
19	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC107,PC151 SE080105K80.	12/27/06	DVT
20	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC108 SE074102K80.	12/27/06	DVT
21	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC111 SE042104K80.	12/27/06	DVT
22	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC112 SE068330K80	12/27/06	DVT
24	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PL13 SH000008Y80.	12/27/06	DVT

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1	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC114 SGA20221D30	12/27/06	DVT
2	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PU9 from SA00001FD80 to SA00001FB80	12/27/06	DVT
3	For SMT BOM convenient.	For SMT BOM convenient.	0.3	40	Change PD14 from SC1H751H010 to SC1B751V010.	12/27/06	DVT
4	Increase _1.5VSP OCP point	Increase _1.5VSP OCP point for +1.25VSP new solution.'	0.3	43	Change PR128 from SD034154280 to SD034374380.	12/27/06	DVT
5	Decrease +1.05VSP OCP point.	Decrease +1.05VSP OCP point.	0.3	44	Change PR145 from SD034324280 to SD034261280		DVT
6	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PU12 SA000015410.	12/27/06	DVT
7	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR188 SD034100280.	12/27/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR189 SD034100380.	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR191 SD034100180.	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR190 SD034576080.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC155 SE107105M80.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC156, PC160 SE116226M80	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC157 SE075103K80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC159 SE076104K80.	12/27/06	DVT
15	Increase +1.5VSP output capacitor.	Increase +1.5VSP output capacitor.	0.3	43	Change PC98 from SGA20221D30 to SGA19331D00	12/27/06	DVT
16	Cost issue.	Cost issue.	0.3	44	Change PC118 from SGA20471D00 to SGA19331D00.	12/30/06	DVT
17	BOM issue.	BOM issue.	0.3	45	Change PH3, PH4 from SL210021F20 to SL200000200	12/30/06	DVT
18	Assembly issue.	Due to assembly hard, delete PC42.	0.3	45	Delete PC42 SM22004M210.	12/30/06	DVT
19	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE142475K80 to SE093106M80	01/04/06	DVT
20	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE153106K80 to SE093106M80	01/04/06	DVT
21	Add pull high resistor for VAGTE.	Add pull high resistor for VAGTE.	0.4	45	Add PR89 SD034200180 (S RES 1/16W 2K 0402 1%)	01/04/06	DVT
22	Delete PQ46	PQ46 has potential risk to cause system battery OVP.	0.4	40	Delete PQ46 SB324110010 (S TR 2SC411K)	01/04/06	DVT
23	Material shipping issue.	Material shipping issue.	0.4	45	Change PC69, PC70, PC71, PC72 from SE068102J80 to SE074102K80	01/04/06	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Cost down	Cost down	0.5	40	Change PQ38 from SB548100020 to SB548000310.	03/09/07	FVT
2	Cost down	Cost down	0.5	40	Change PQ40 from SB548100020 to SB548000310.	03/09/07	FVT
3	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PR199 SD001470B80(S RES 1/4W 4.7 1206 +-5%)	04/01/07	Pre-MP
4	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PC163 SE074681K80 ( S CER CAP 680P 50V K X7R)	04/01/07	Pre-MP
5	For battery life issue.	For battery life issue.	0.6	42	Add PR113 SD028000080.		
6	For battery life issue.	For battery life issue.	0.6	42	Add PQ19 SB502060000.		
7	PC28 change to LF PN.	PC28 change to LF PN.	0.7	39	Change PC28 from SE000005ZM8 to SE000005Z80.	04/18/07	MP
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