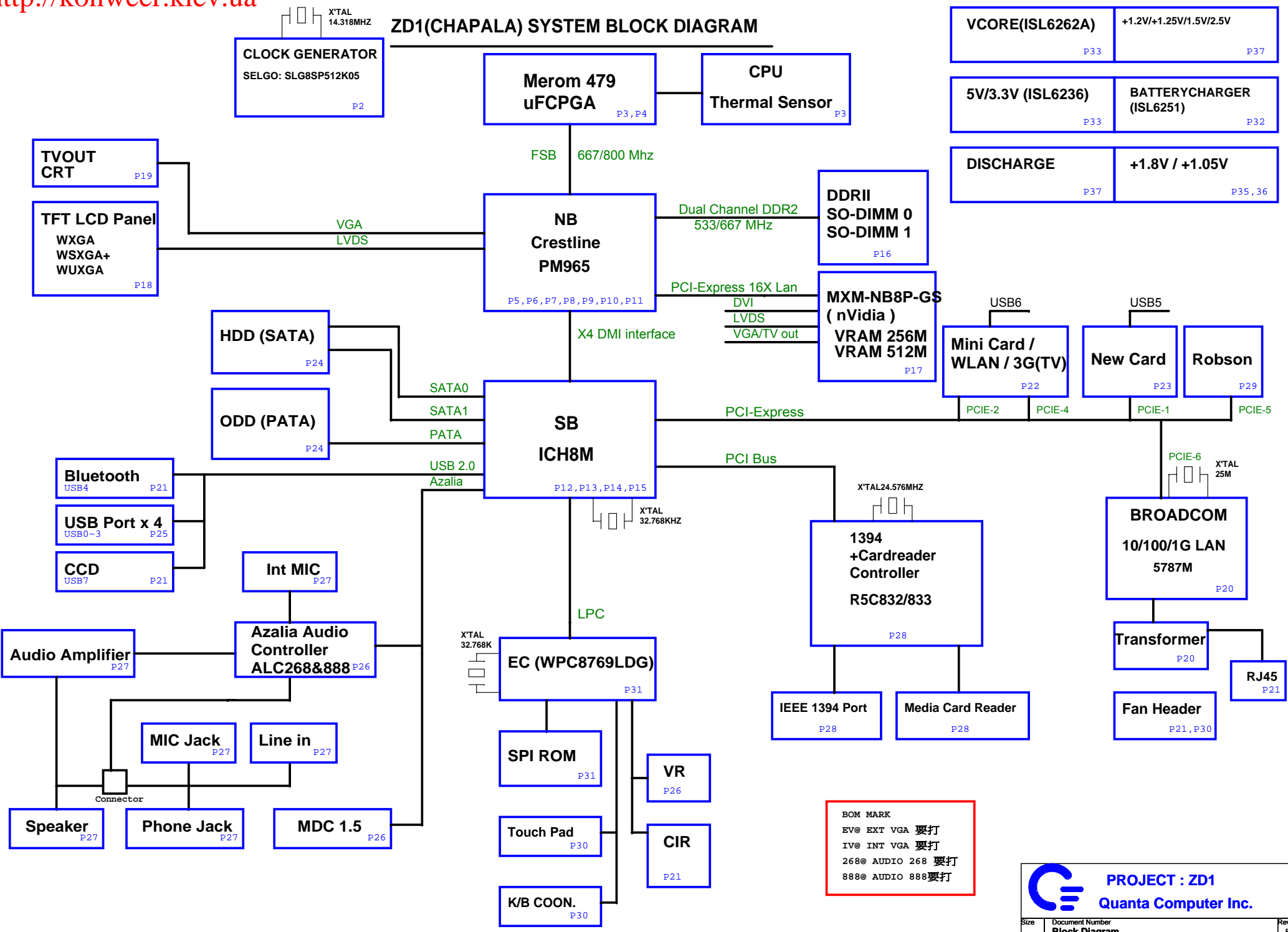
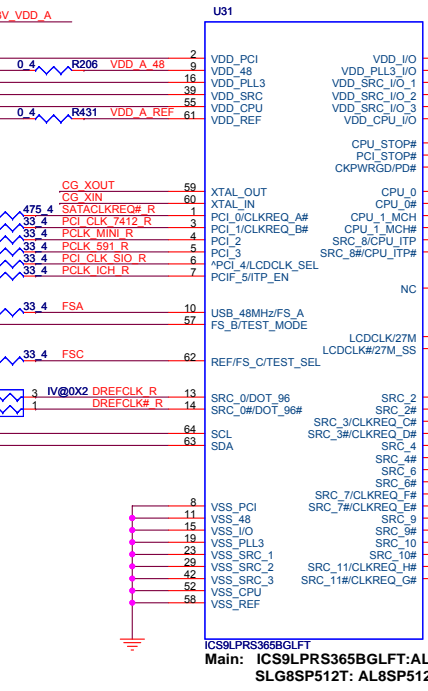
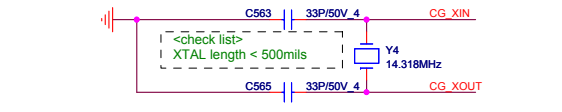
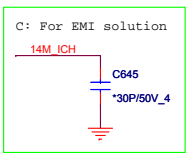
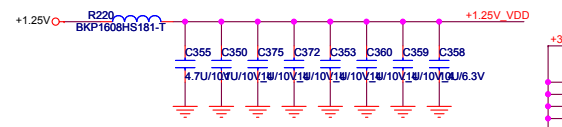
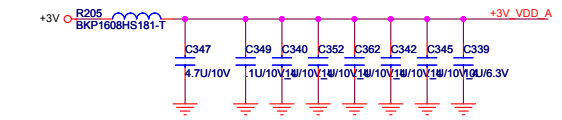


### ZD1(CHAPALA) SYSTEM BLOCK DIAGRAM

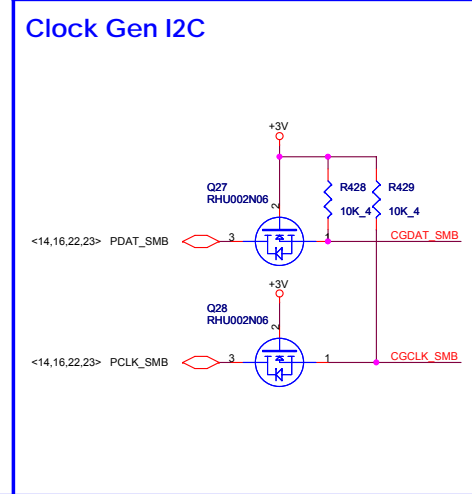
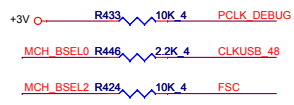
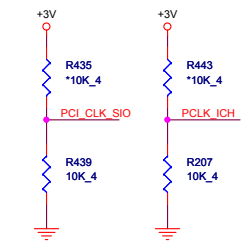


BOM MARK  
 EV@ EXT VGA 要打  
 IV@ INT VGA 要打  
 268@ AUDIO 268 要打  
 888@ AUDIO 888 要打

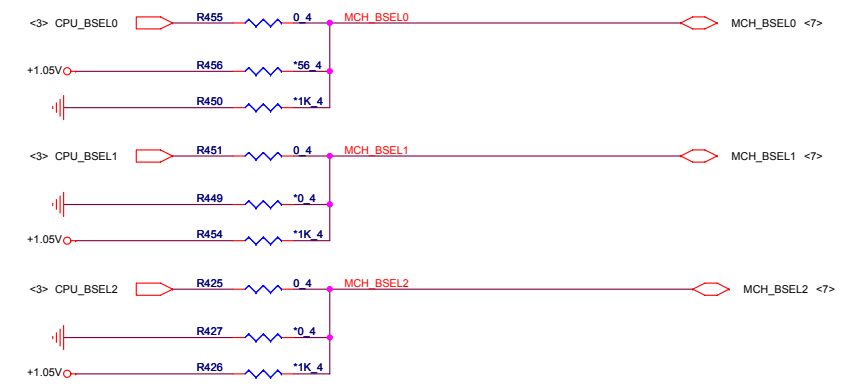
Change list:  
 B-test  
 1.Change U31 P/N to ALPRS365K13 (ICS)



Main: ICS9LPRS365BGLFT:ALPRS365K13  
 SLG8SP512T: AL8SP512K05



CPU Clock select



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	1.33Mhz
0	1	1	1.66Mhz
0	1	0	2.00Mhz
1	1	0	4.00Mhz
1	1	1	Reserved
1	0	1	1.00Mhz
1	0	0	3.33Mhz

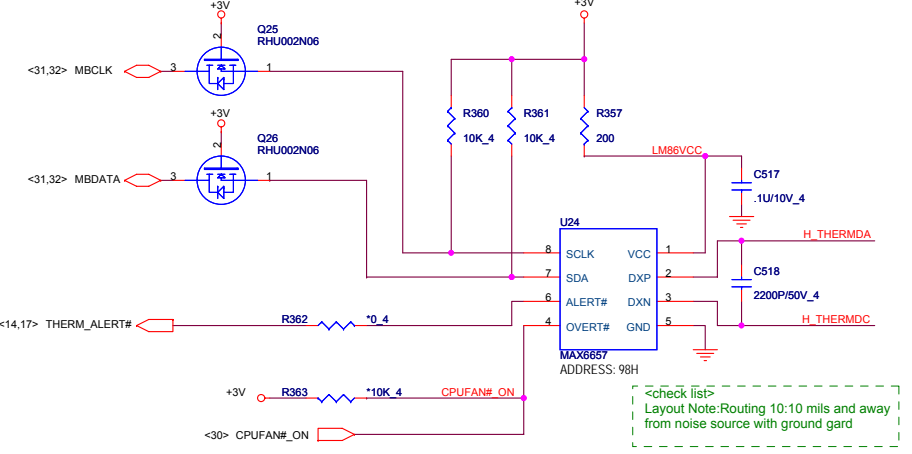
**PROJECT : ZD1**  
**Quanta Computer Inc.**

Size: Document Number: **CLOCK GENERATOR CK505 W/REGULATOR** Rev: E

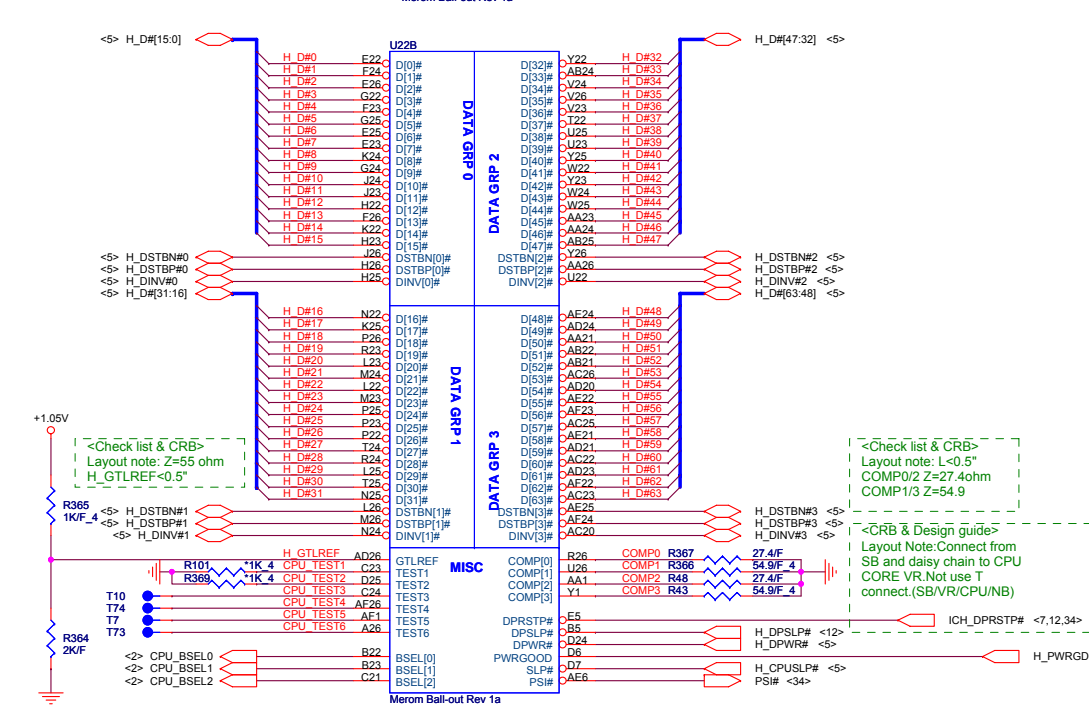
Date: Monday, May 07, 2007 Sheet 2 of 38



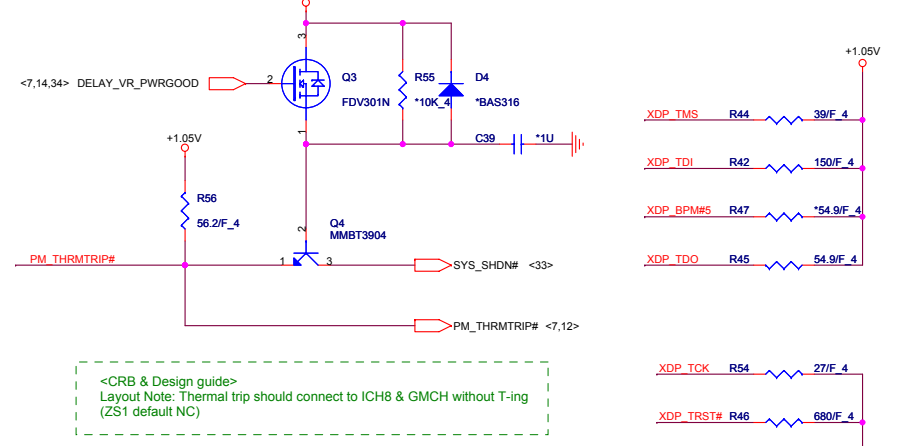
### CPU Thermal monitor



<check list>  
Layout Note: Routing 10:10 mils and away from noise source with ground guard



### Thermal Trip

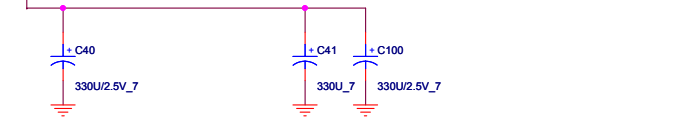
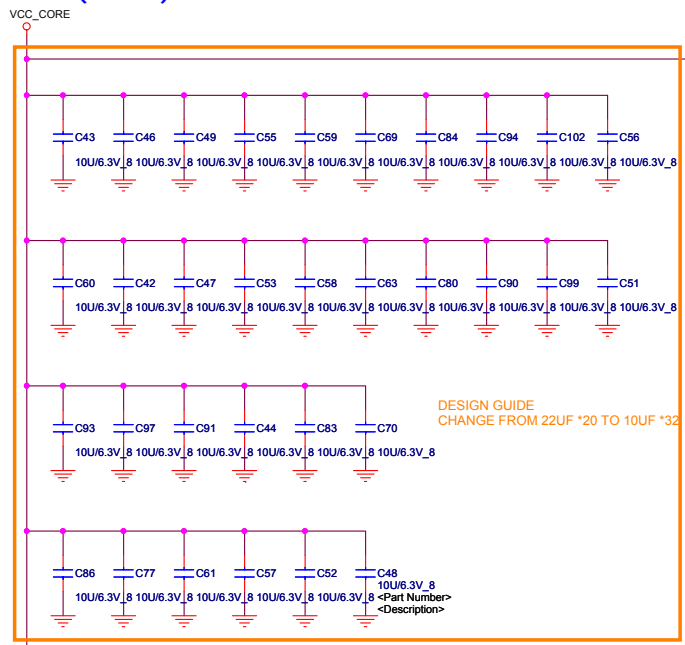


<CRB & Design guide>  
Layout Note: Thermal trip should connect to ICH8 & GMCH without T-ing (ZS1 default NC)

**PROJECT : ZD1**  
**Quanta Computer Inc.**

Size Document Number  
**CPU(1 of 2)/FAN/Thermal**

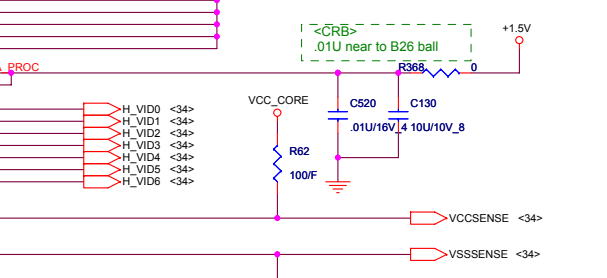
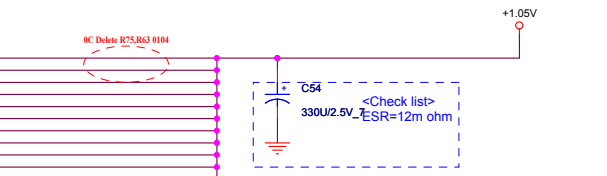
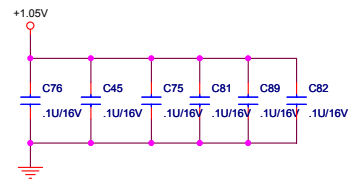
Date: Monday, May 07, 2007 Sheet 3 of 38



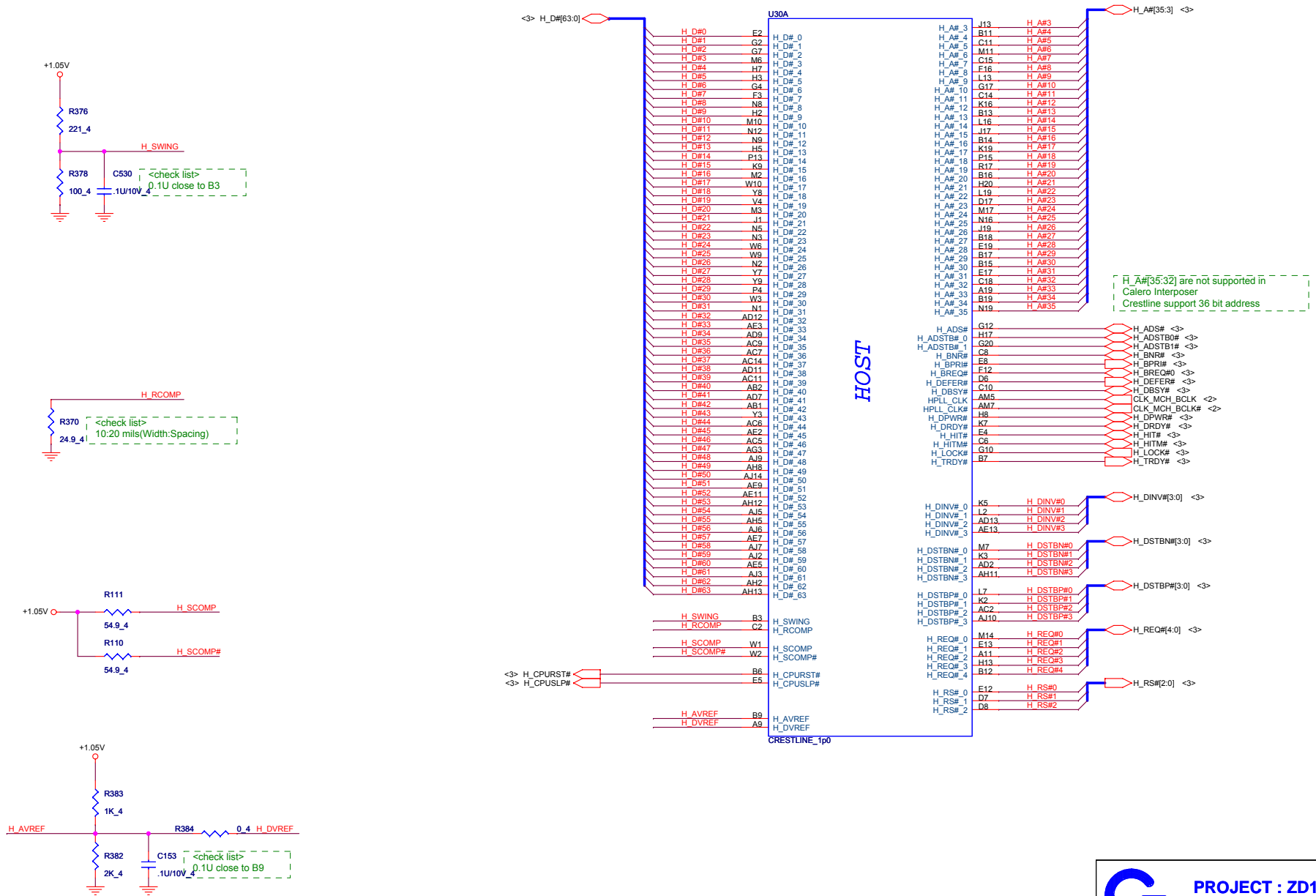
<Check list>  
Option1:330U\*6(ESR=1.5m ohm aggregate , ESL=0.8nH/6) and 22U\*20(ESR=3mohm typ/20 , ESL=0.6nH/20)  
Option2:330U\*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U\*32(ESR=3mohm typ/32 , ESL=0.6nH/32)

U22C		
A7	VCC[001]	VCC[068]
A8	VCC[002]	VCC[069]
A9	VCC[003]	VCC[070]
A10	VCC[004]	VCC[071]
A11	VCC[005]	VCC[072]
A12	VCC[006]	VCC[073]
A13	VCC[007]	VCC[074]
A14	VCC[008]	VCC[075]
A15	VCC[009]	VCC[076]
A16	VCC[010]	VCC[077]
A17	VCC[011]	VCC[078]
A18	VCC[012]	VCC[079]
A19	VCC[013]	VCC[080]
A20	VCC[014]	VCC[081]
B7	VCC[015]	VCC[082]
B8	VCC[016]	VCC[083]
B9	VCC[017]	VCC[084]
B10	VCC[018]	VCC[085]
B11	VCC[019]	VCC[086]
B12	VCC[020]	VCC[087]
B13	VCC[021]	VCC[088]
B14	VCC[022]	VCC[089]
B15	VCC[023]	VCC[090]
B16	VCC[024]	VCC[091]
B17	VCC[025]	VCC[092]
B18	VCC[026]	VCC[093]
B19	VCC[027]	VCC[094]
B20	VCC[028]	VCC[095]
C9	VCC[029]	VCC[096]
C10	VCC[030]	VCC[097]
C11	VCC[031]	VCC[098]
C12	VCC[032]	VCC[099]
C13	VCC[033]	VCC[100]
C14	VCC[034]	VCC[001]
C15	VCC[035]	VCC[002]
C16	VCC[036]	VCC[003]
C17	VCC[037]	VCC[004]
C18	VCC[038]	VCC[005]
C19	VCC[039]	VCC[006]
C20	VCC[040]	VCC[007]
C21	VCC[041]	VCC[008]
C22	VCC[042]	VCC[009]
C23	VCC[043]	VCC[010]
C24	VCC[044]	VCC[011]
C25	VCC[045]	VCC[012]
C26	VCC[046]	VCC[013]
C27	VCC[047]	VCC[014]
C28	VCC[048]	VCC[015]
C29	VCC[049]	VCC[016]
C30	VCC[050]	VCC[017]
C31	VCC[051]	VCC[018]
C32	VCC[052]	VCC[019]
C33	VCC[053]	VCC[020]
C34	VCC[054]	VCC[021]
C35	VCC[055]	VCC[022]
C36	VCC[056]	VCC[023]
C37	VCC[057]	VCC[024]
C38	VCC[058]	VCC[025]
C39	VCC[059]	VCC[026]
C40	VCC[060]	VCC[027]
C41	VCC[061]	VCC[028]
C42	VCC[062]	VCC[029]
C43	VCC[063]	VCC[030]
C44	VCC[064]	VCC[031]
C45	VCC[065]	VCC[032]
C46	VCC[066]	VCC[033]
C47	VCC[067]	VCC[034]

<REV.NO. 0.5/REF.NO.19343>  
Ivcc Max 52A  
Ivccp Max 6A(VCCP supply before Vcc stable)  
Max 2A(VCCP supply after Vcc stable)  
Ivcca Max 130mA



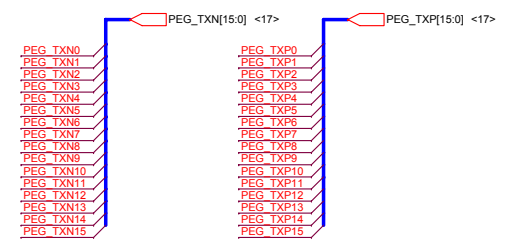
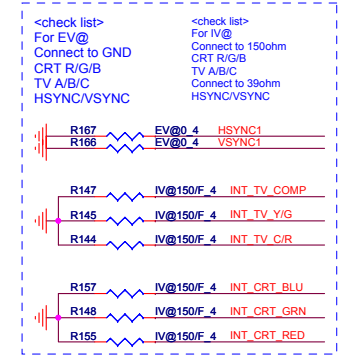
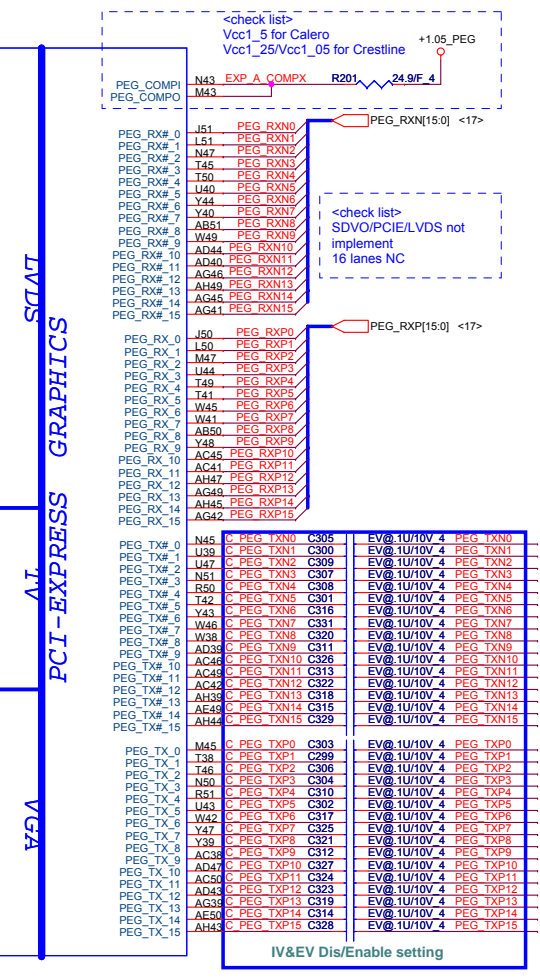
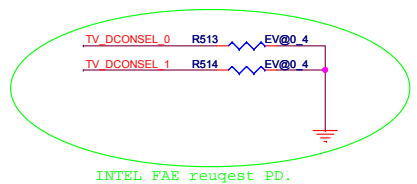
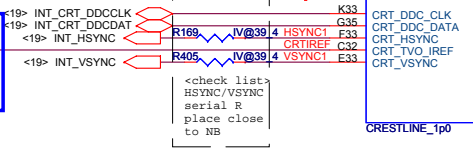
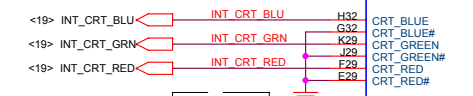
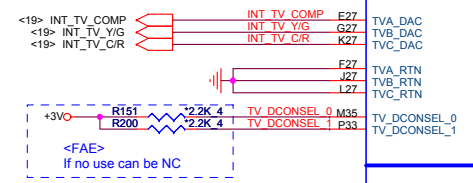
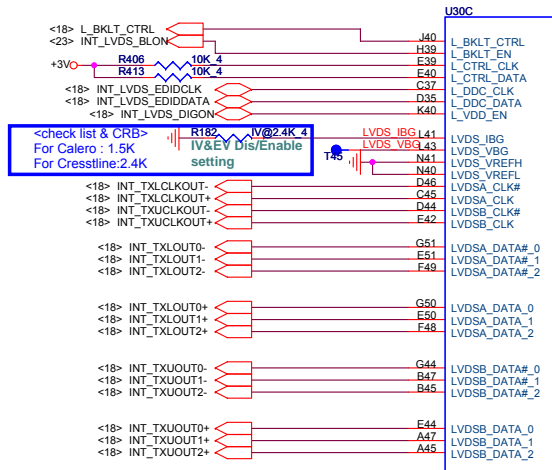
U22D		
A4	VSS[001]	VSS[082]
A5	VSS[002]	VSS[083]
A6	VSS[003]	VSS[084]
A7	VSS[004]	VSS[085]
A8	VSS[005]	VSS[086]
A9	VSS[006]	VSS[087]
A10	VSS[007]	VSS[088]
A11	VSS[008]	VSS[089]
A12	VSS[009]	VSS[090]
A13	VSS[010]	VSS[091]
A14	VSS[011]	VSS[092]
A15	VSS[012]	VSS[093]
A16	VSS[013]	VSS[094]
A17	VSS[014]	VSS[095]
A18	VSS[015]	VSS[096]
A19	VSS[016]	VSS[097]
A20	VSS[017]	VSS[098]
B6	VSS[018]	VSS[099]
B7	VSS[019]	VSS[100]
B8	VSS[020]	VSS[101]
B9	VSS[021]	VSS[102]
B10	VSS[022]	VSS[103]
B11	VSS[023]	VSS[104]
B12	VSS[024]	VSS[105]
B13	VSS[025]	VSS[106]
B14	VSS[026]	VSS[107]
B15	VSS[027]	VSS[108]
B16	VSS[028]	VSS[109]
B17	VSS[029]	VSS[110]
B18	VSS[030]	VSS[111]
B19	VSS[031]	VSS[112]
B20	VSS[032]	VSS[113]
C1	VSS[033]	VSS[114]
C2	VSS[034]	VSS[115]
C3	VSS[035]	VSS[116]
C4	VSS[036]	VSS[117]
C5	VSS[037]	VSS[118]
C6	VSS[038]	VSS[119]
C7	VSS[039]	VSS[120]
C8	VSS[040]	VSS[121]
C9	VSS[041]	VSS[122]
C10	VSS[042]	VSS[123]
C11	VSS[043]	VSS[124]
C12	VSS[044]	VSS[125]
C13	VSS[045]	VSS[126]
C14	VSS[046]	VSS[127]
C15	VSS[047]	VSS[128]
C16	VSS[048]	VSS[129]
C17	VSS[049]	VSS[130]
C18	VSS[050]	VSS[131]
C19	VSS[051]	VSS[132]
C20	VSS[052]	VSS[133]
C21	VSS[053]	VSS[134]
C22	VSS[054]	VSS[135]
C23	VSS[055]	VSS[136]
C24	VSS[056]	VSS[137]
C25	VSS[057]	VSS[138]
C26	VSS[058]	VSS[139]
C27	VSS[059]	VSS[140]
C28	VSS[060]	VSS[141]
C29	VSS[061]	VSS[142]
C30	VSS[062]	VSS[143]
C31	VSS[063]	VSS[144]
C32	VSS[064]	VSS[145]
C33	VSS[065]	VSS[146]
C34	VSS[066]	VSS[147]
C35	VSS[067]	VSS[148]
C36	VSS[068]	VSS[149]
C37	VSS[069]	VSS[150]
C38	VSS[070]	VSS[151]
C39	VSS[071]	VSS[152]
C40	VSS[072]	VSS[153]
C41	VSS[073]	VSS[154]
C42	VSS[074]	VSS[155]
C43	VSS[075]	VSS[156]
C44	VSS[076]	VSS[157]
C45	VSS[077]	VSS[158]
C46	VSS[078]	VSS[159]
C47	VSS[079]	VSS[160]
C48	VSS[080]	VSS[161]
C49	VSS[081]	VSS[162]
C50	VSS[081]	VSS[163]



H\_A#(35:32) are not supported in Calero Interposer  
Crestline support 36 bit address

**PROJECT : ZD1**  
**Quanta Computer Inc.**

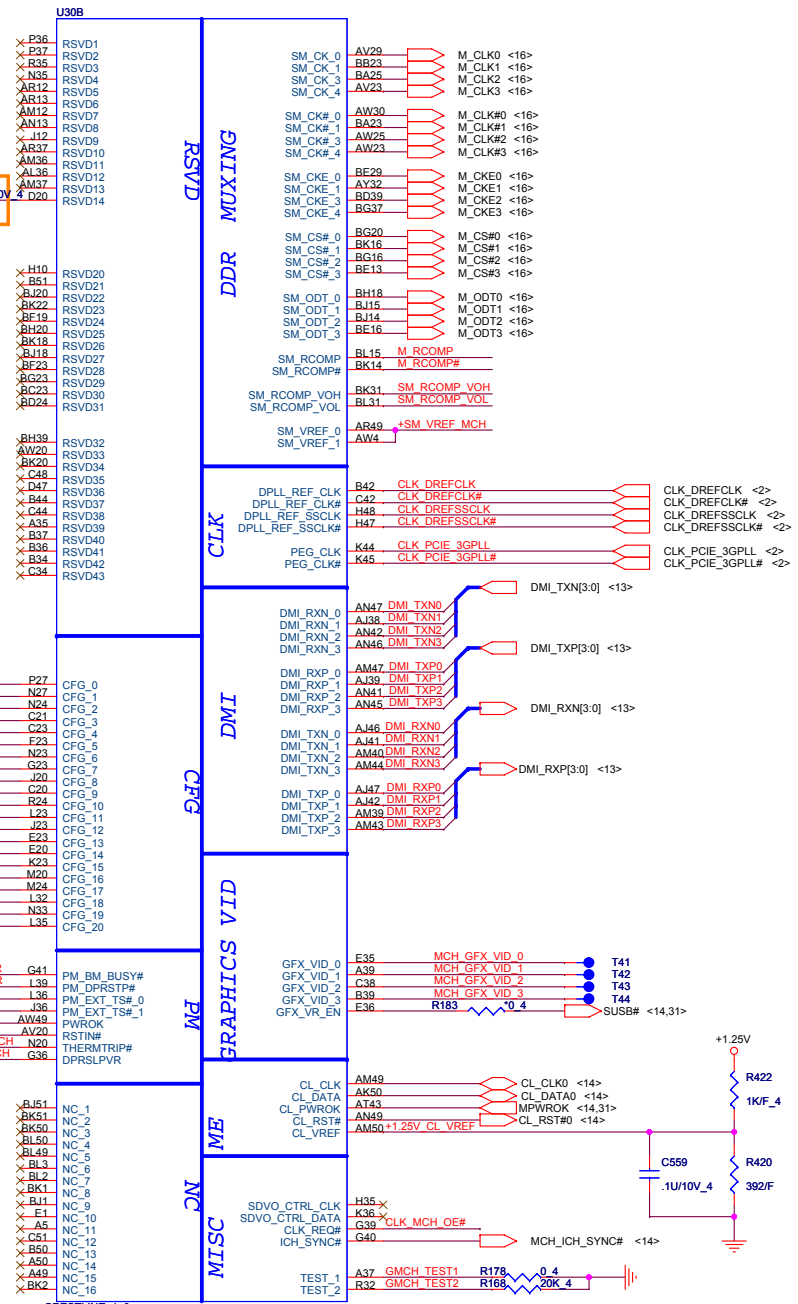
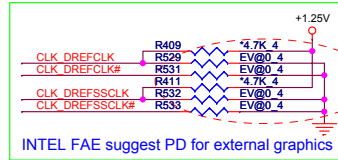
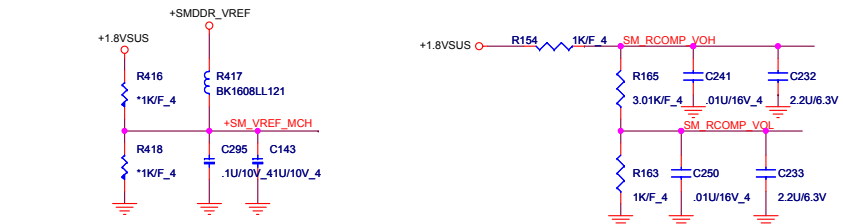
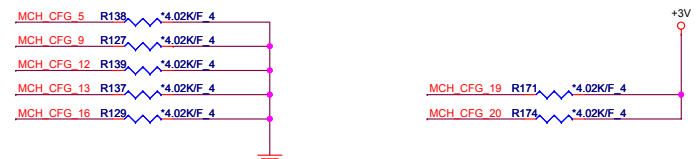
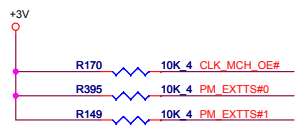
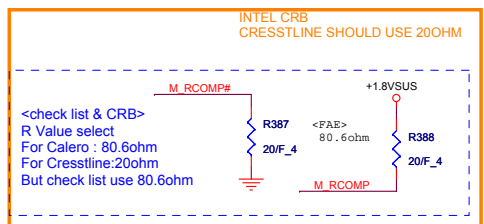
Size	Document Number	Rev
	<b>GMCH HOST(1/7)</b>	E
Date:	Monday, May 07, 2007	Sheet 5 of 38



Strapping table

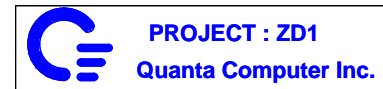
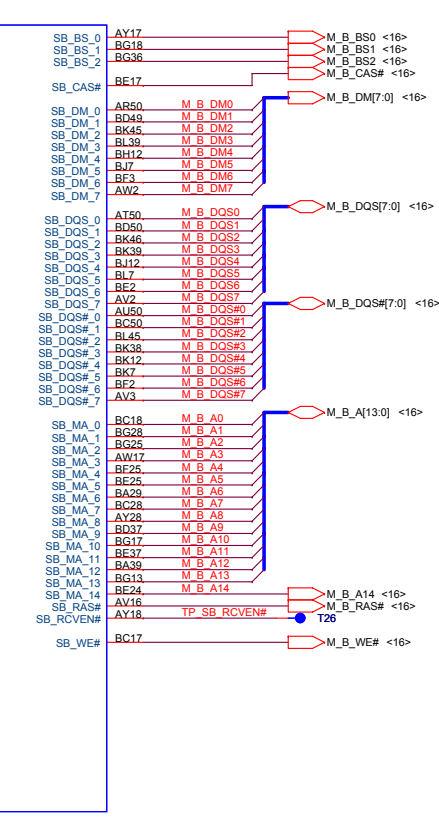
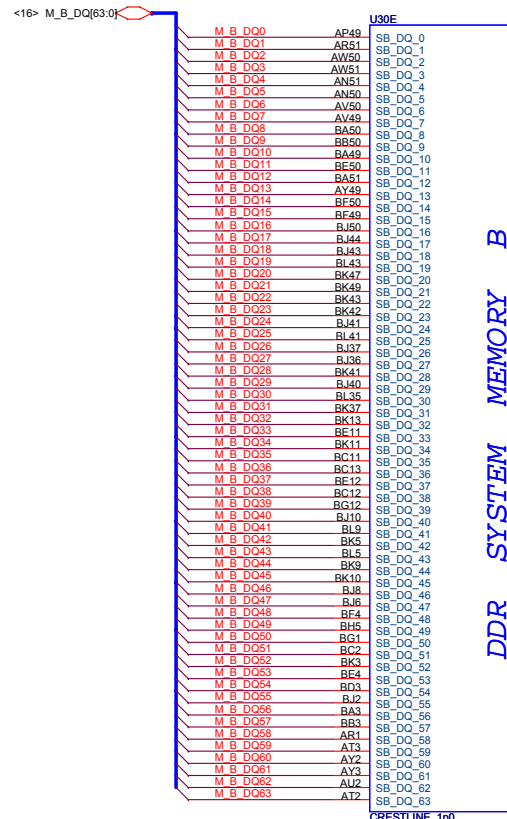
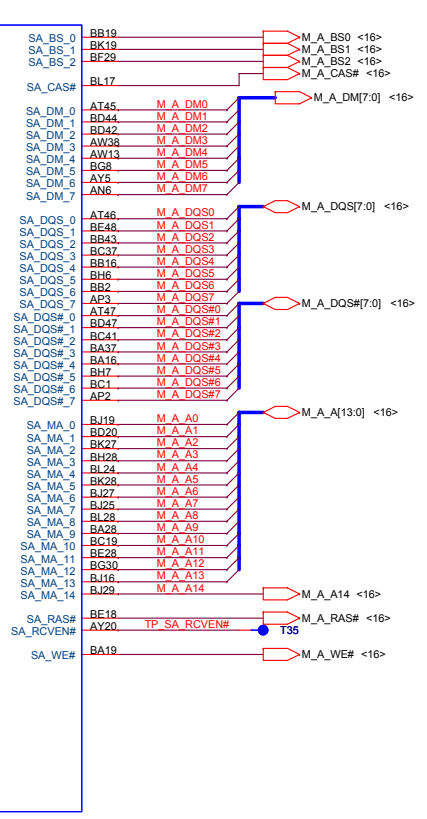
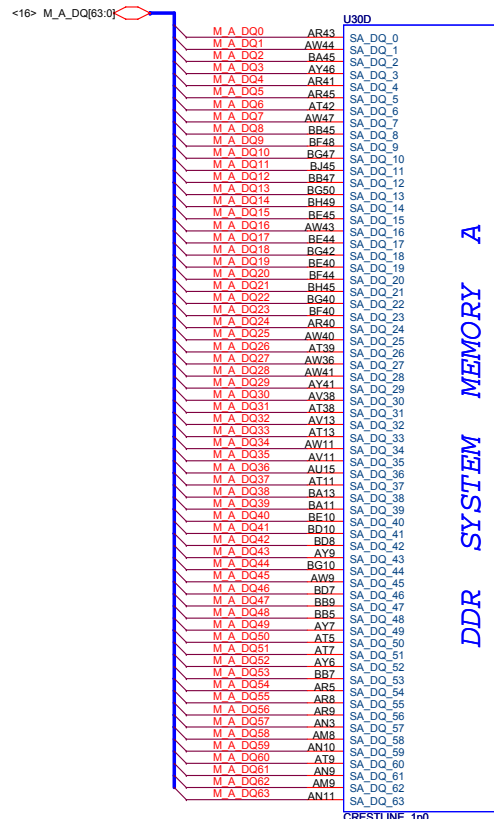
All strap are sampled with respect to the leading edge of the GMCH power ok signal  
 CFG[17:3] have internal pull-up  
 CFG[18:19] have internal pull-down  
 Any CFG signal strapping option not list below should be left NC pin

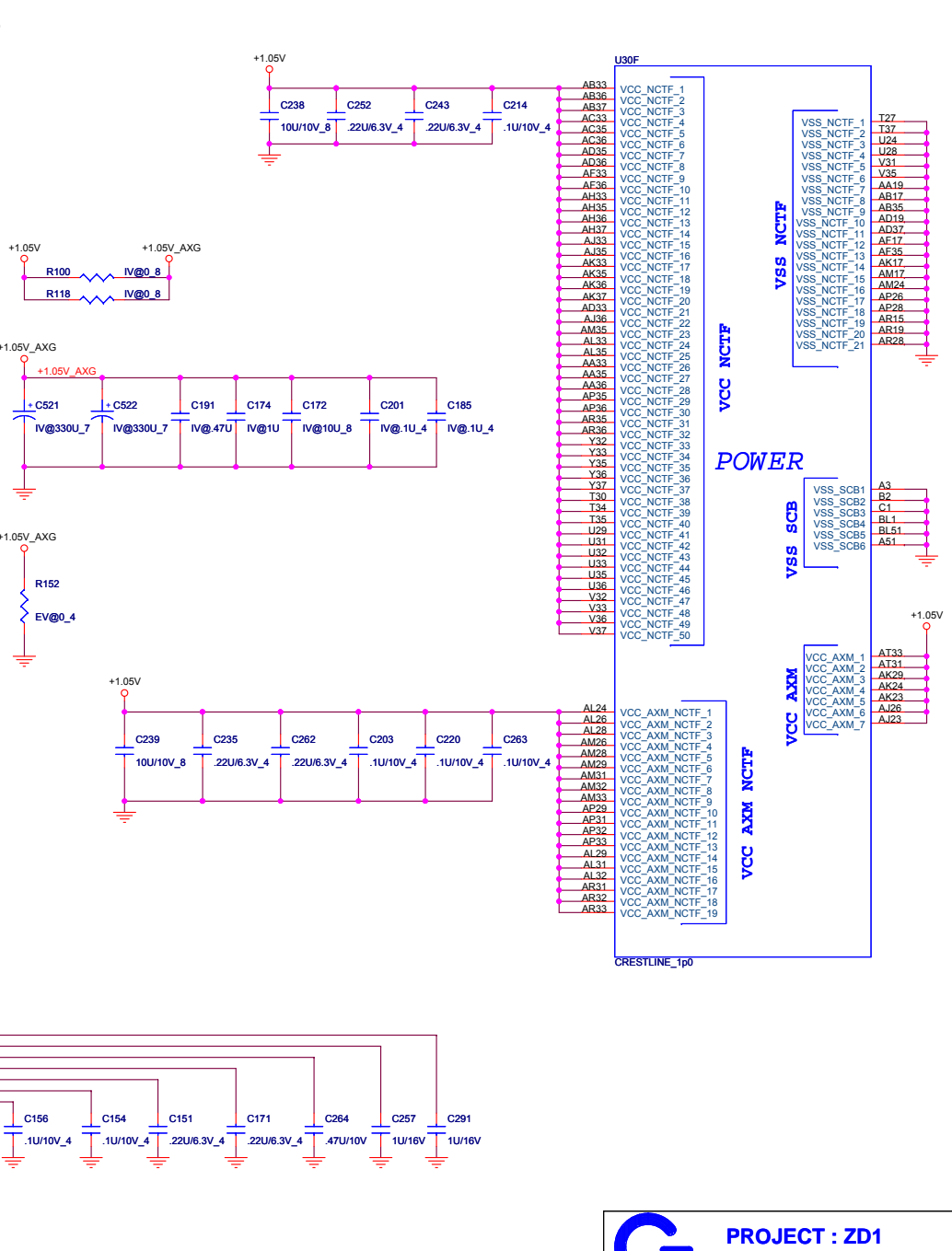
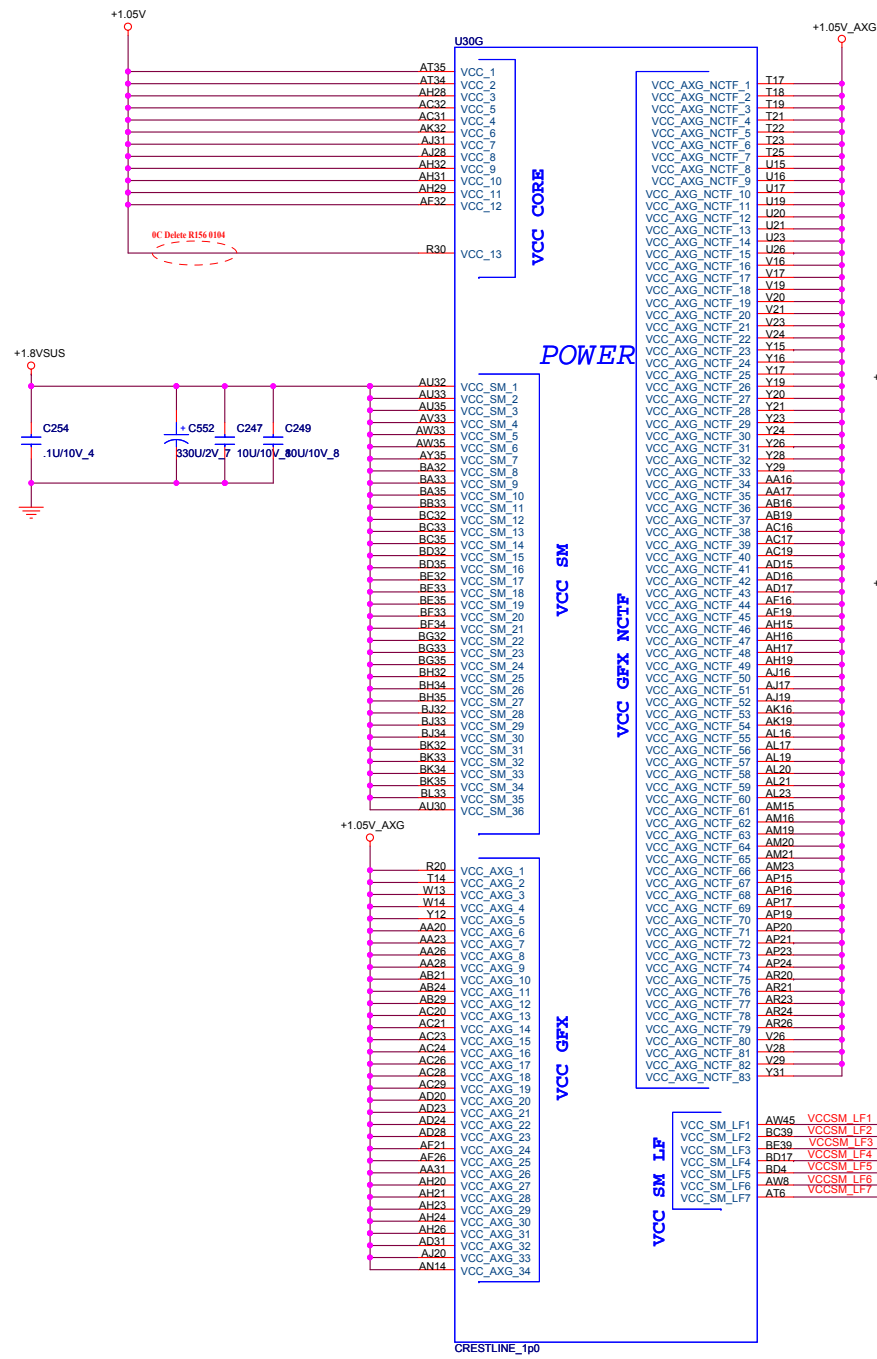
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CEG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Mobile CPU (Default) 1 = Low Power mode
CFG8	Low Power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reserved Lanes 1 = Normal operation (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ ALLZ/ Clock Un gating	00 = Clock gating disable 01 = ALL-Z Mode Enable 10 = XOR Mode Enable 11 = Normal C operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation 1 = Reverse Lanes (Default)
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIe x1 is operation (Default) 1 = SDVO and PCIe x1 are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card Present



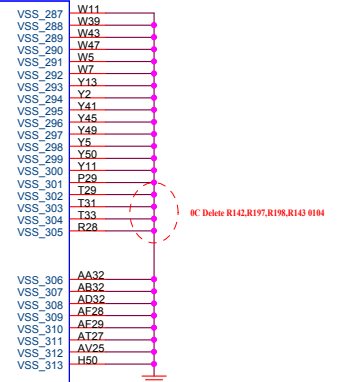
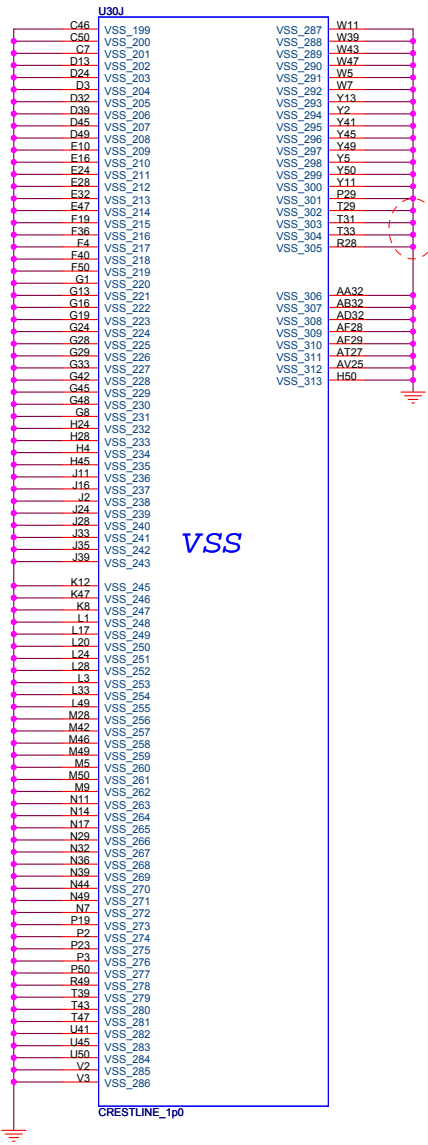
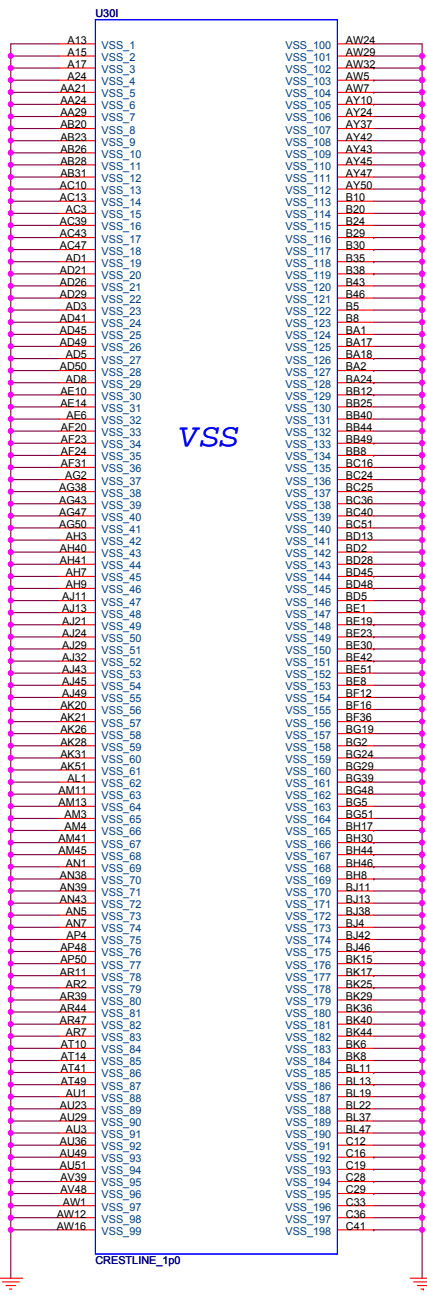
**PROJECT : ZD1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>GMCH (STRAPPING/OTHER 3/7)</b>	E
Date:	Monday, May 07, 2007	Sheet 7 of 38

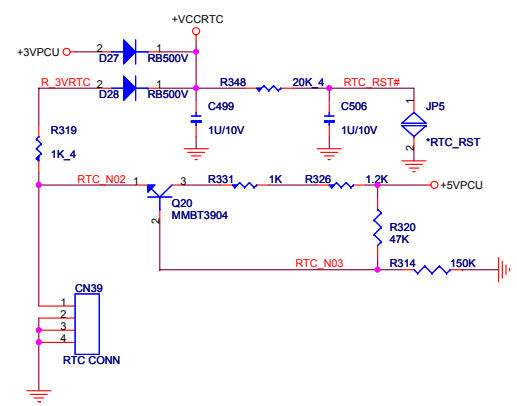






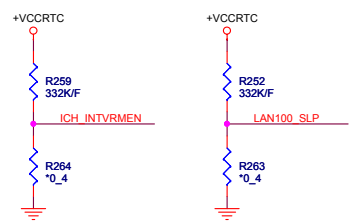


### RTC

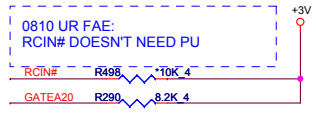
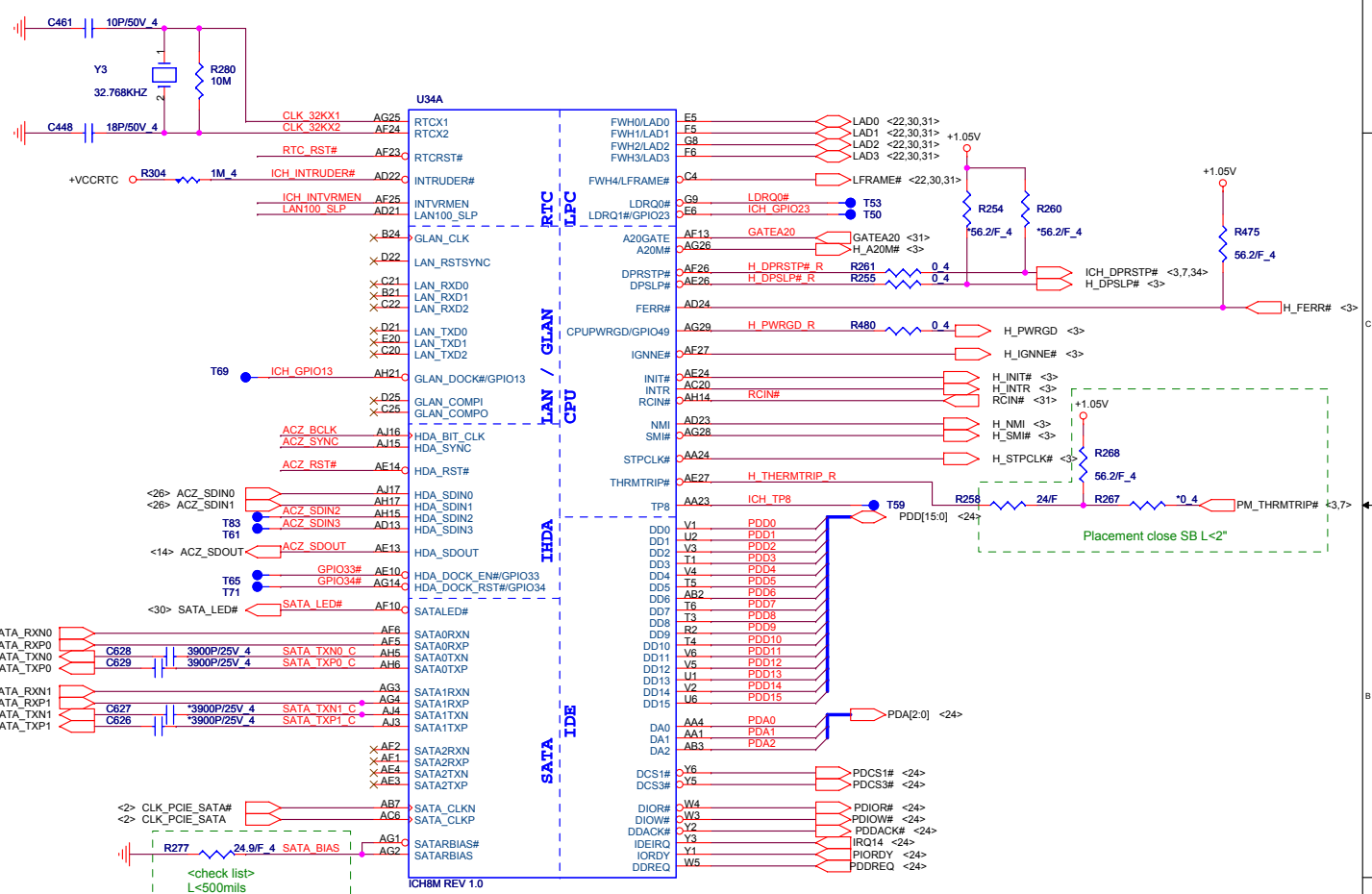
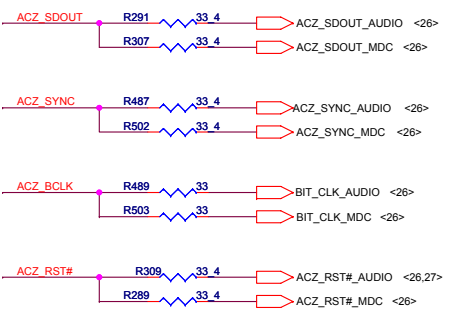


### SB Strap

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



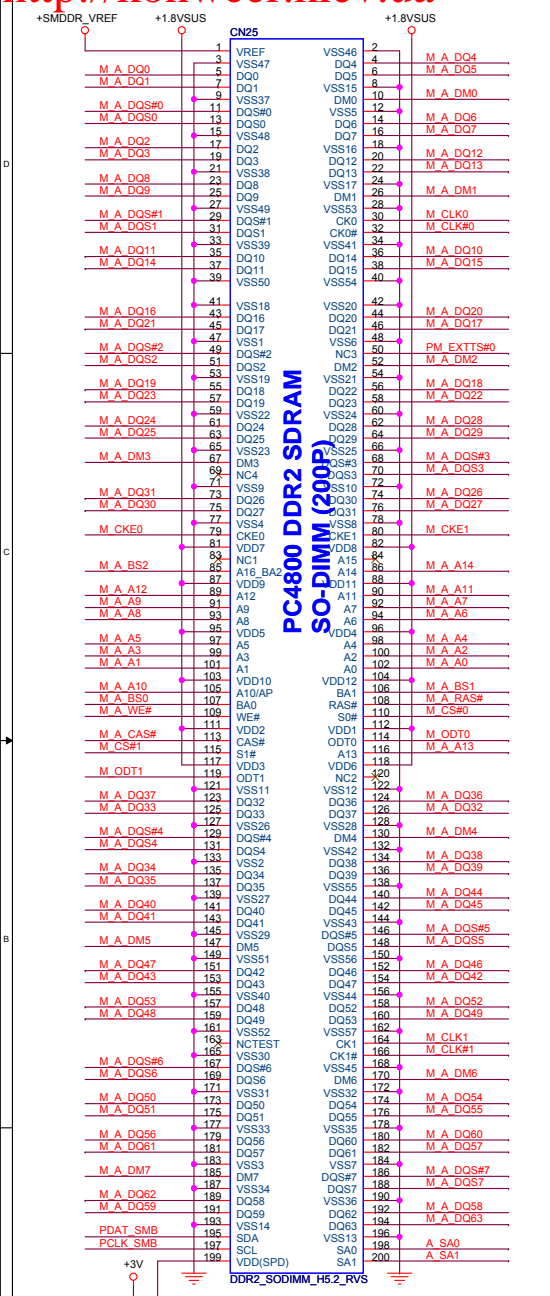
### HDA



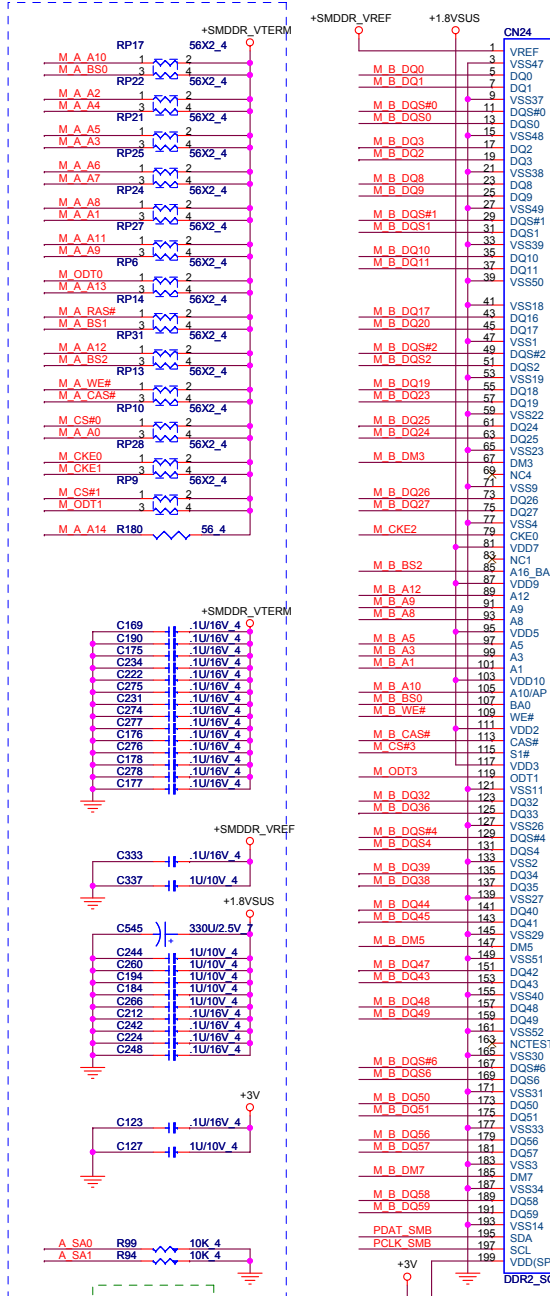




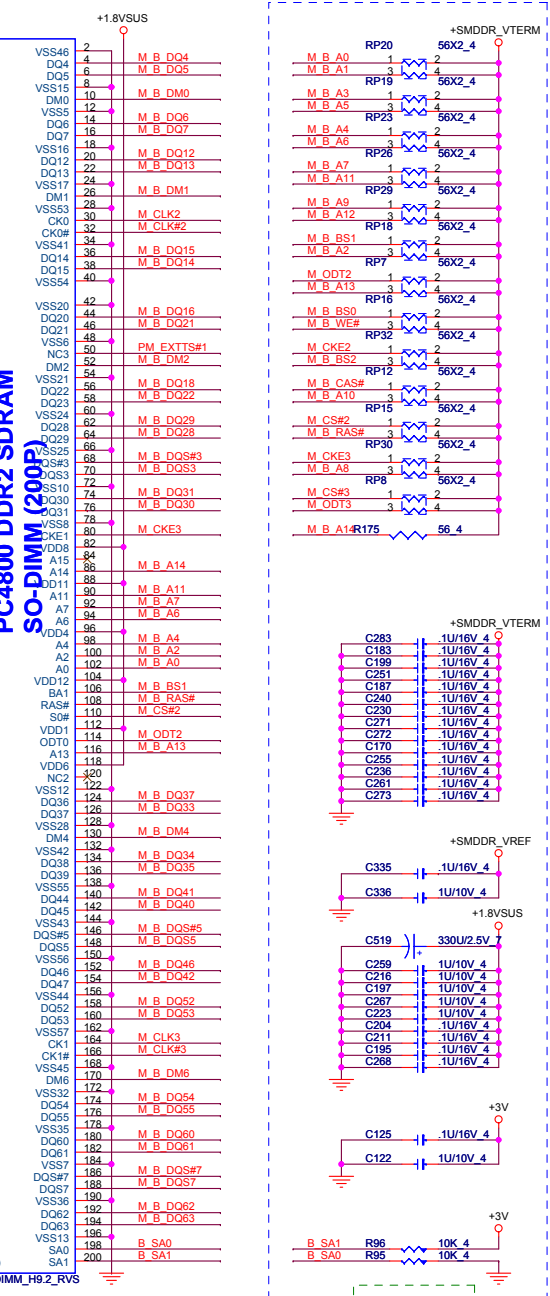




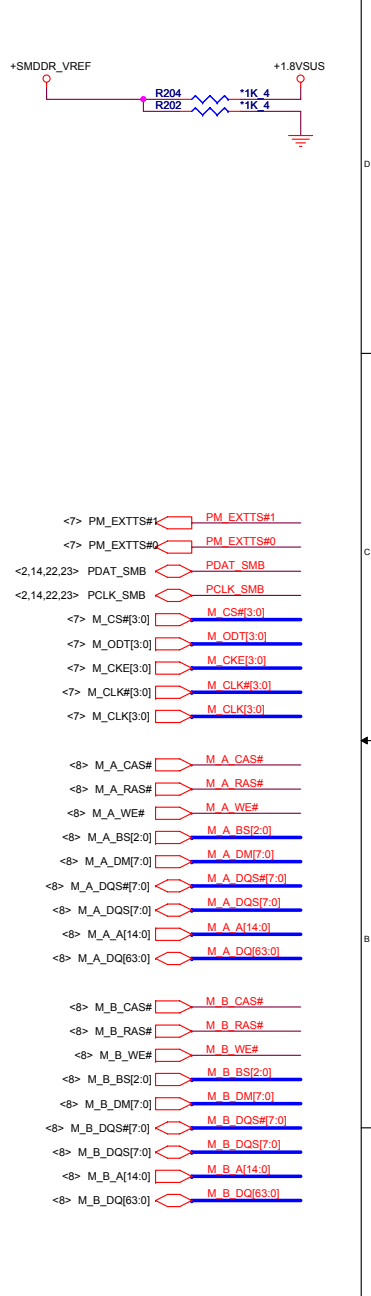
SO-DIMM0 SMbus address A0



SO-DIMM1 SMbus address A2

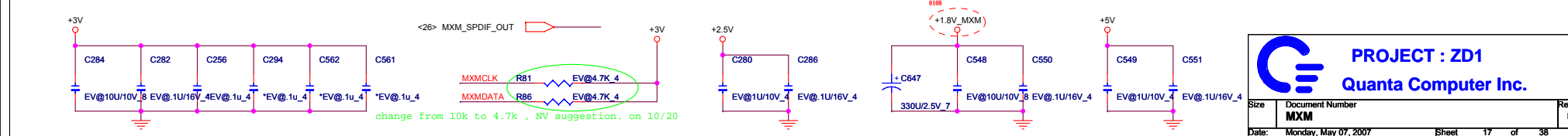
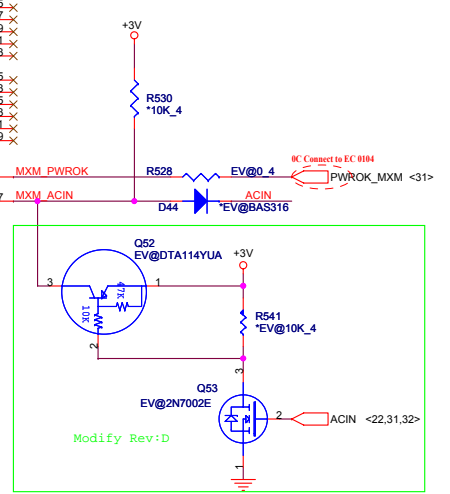
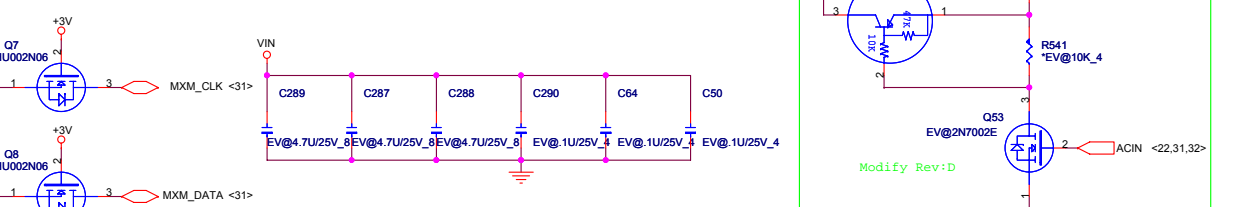
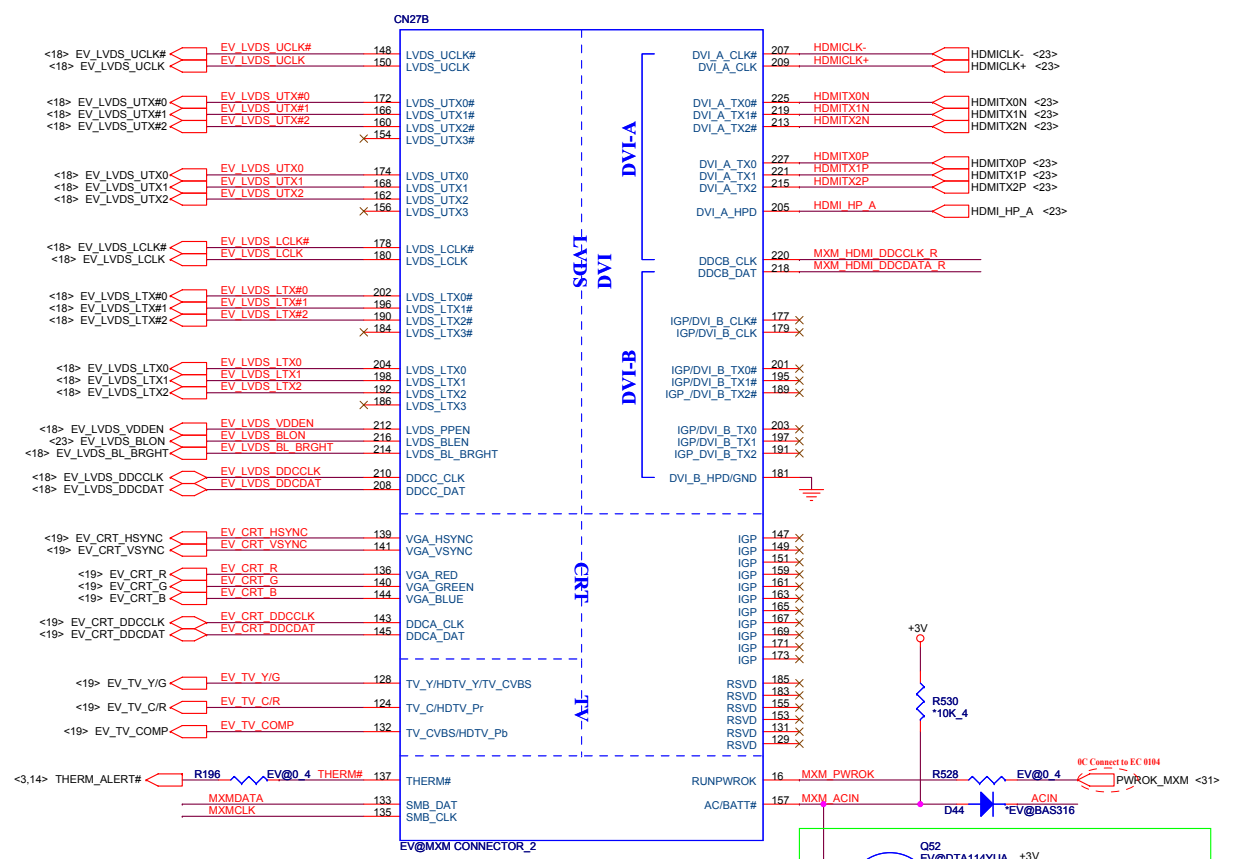
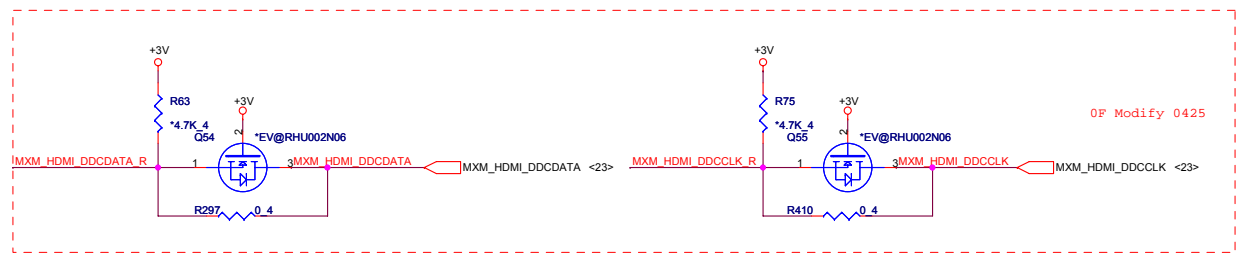
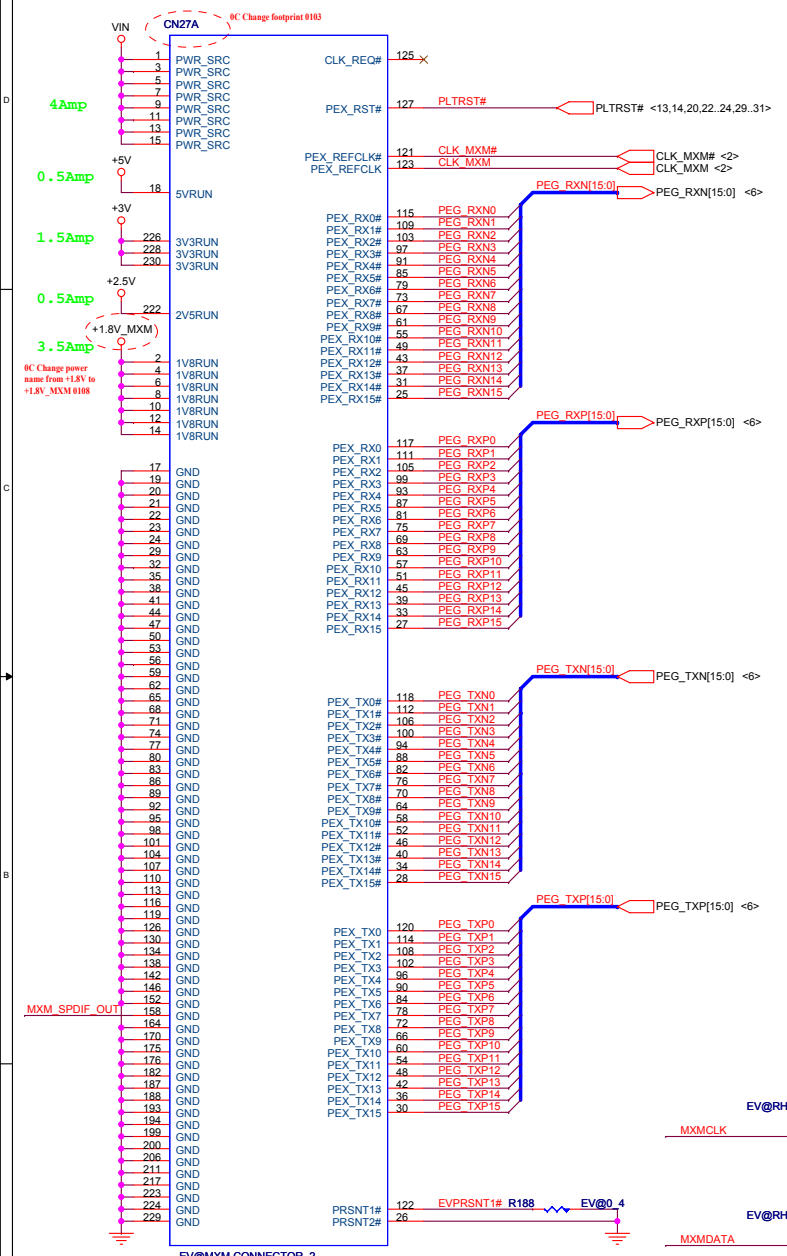


SO-DIMM2 SMbus address A2



**PROJECT : ZD1**  
**Quanta Computer Inc.**

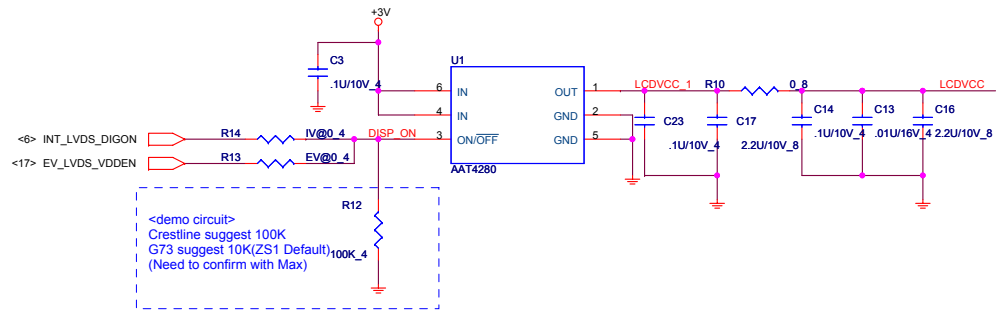
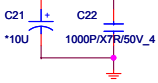
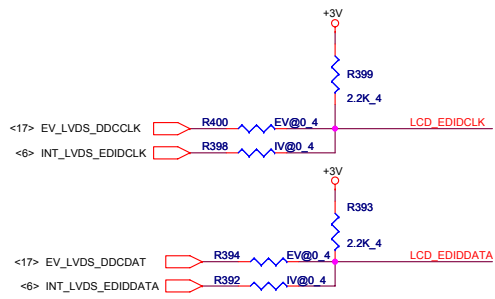
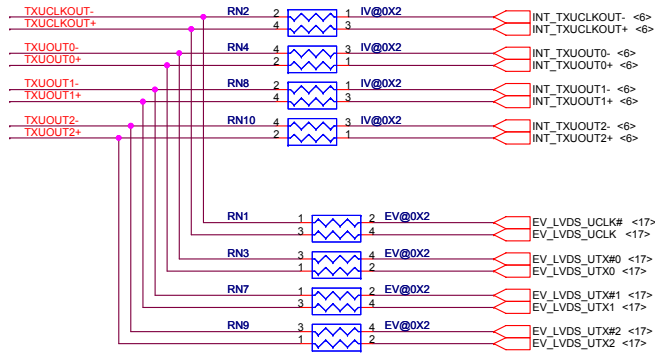
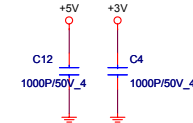
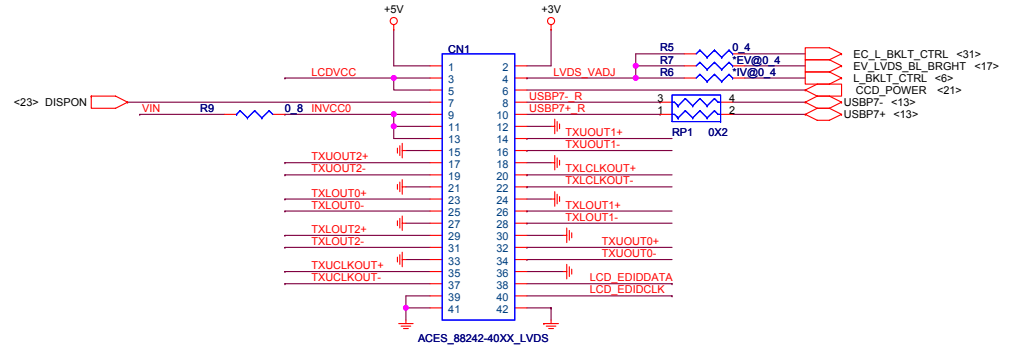
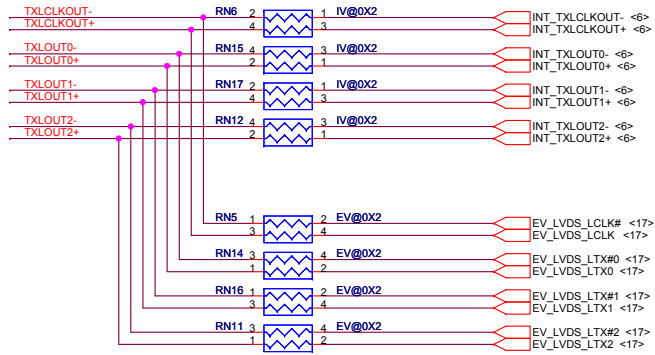
Size	Document Number	Rev
	<b>DDR11 SO-DIMM</b>	E
Date:	Monday, May 07, 2007	Sheet 16 of 38



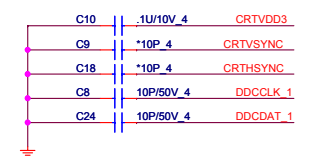
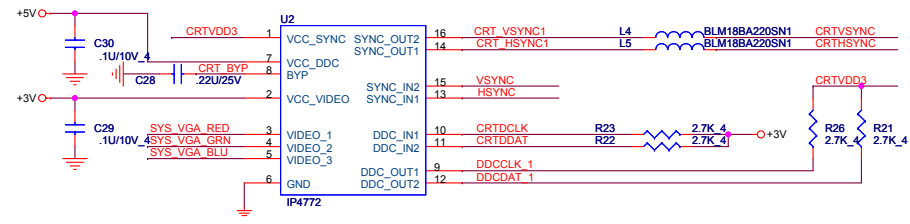
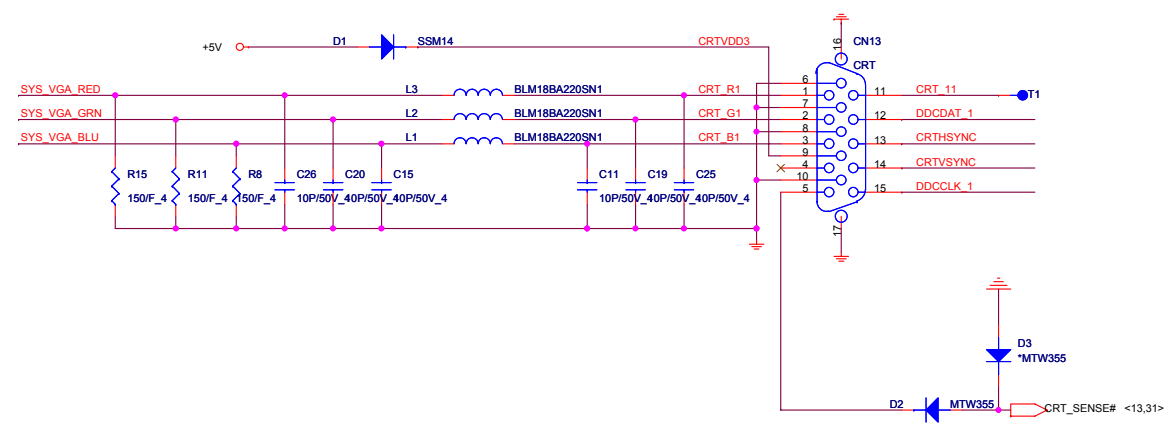
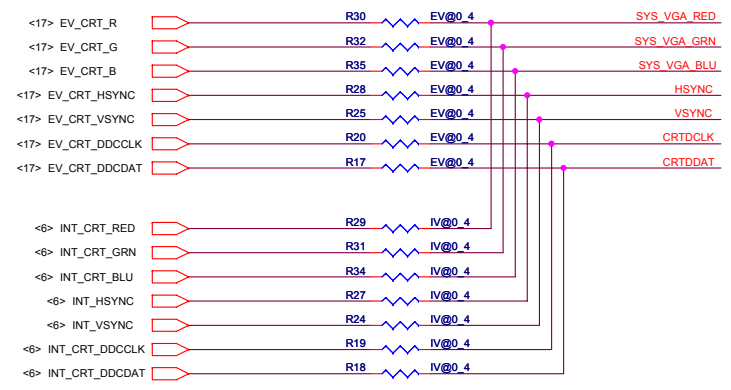
**PROJECT : ZD1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>MXM</b>	E

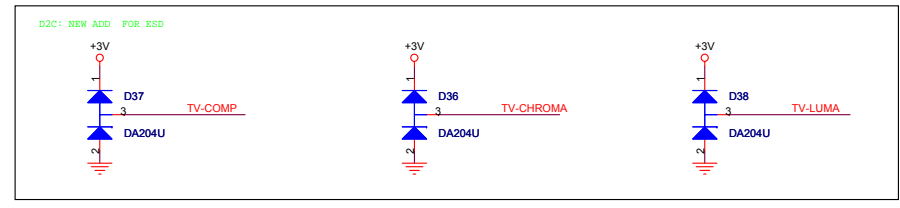
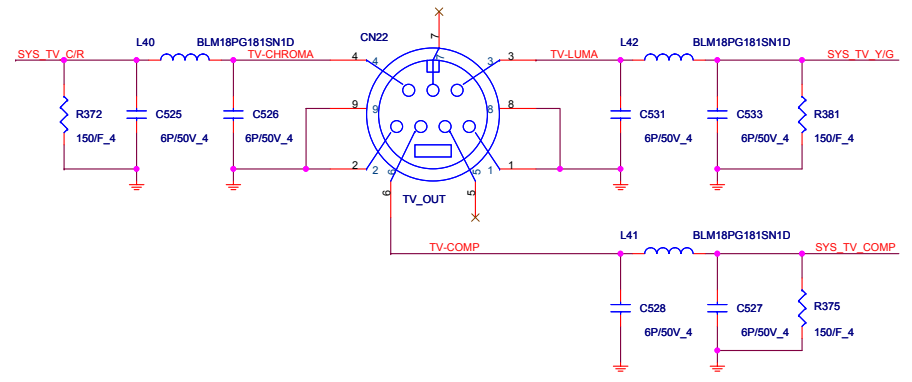
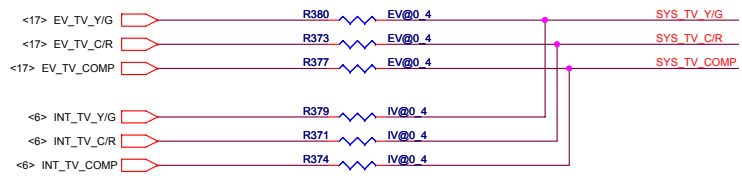
Date: Monday, May 07, 2007 Sheet 17 of 38



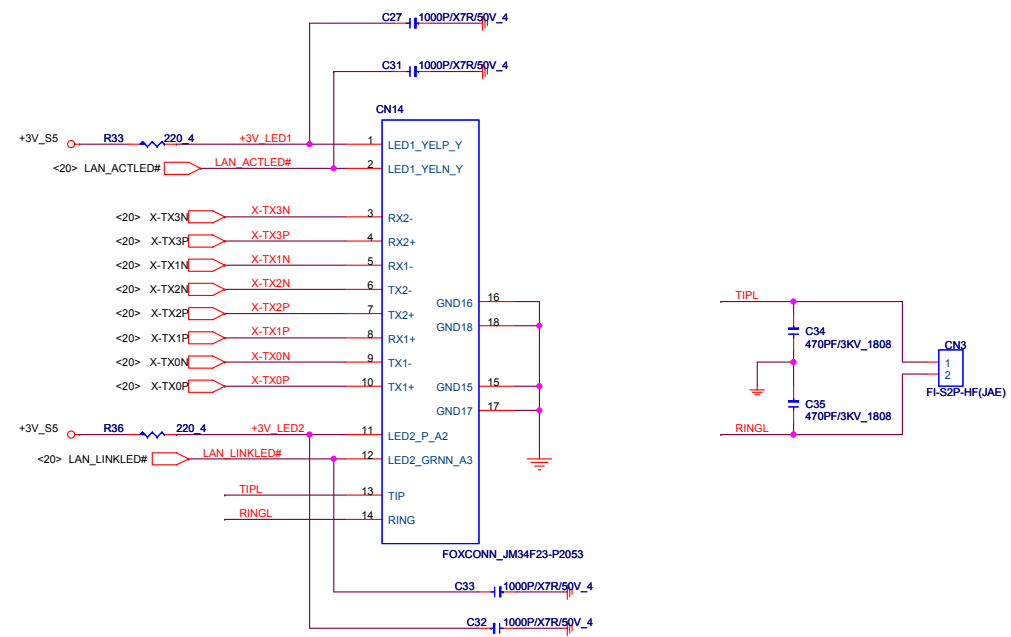
CRT CONNECTOR AND ESD



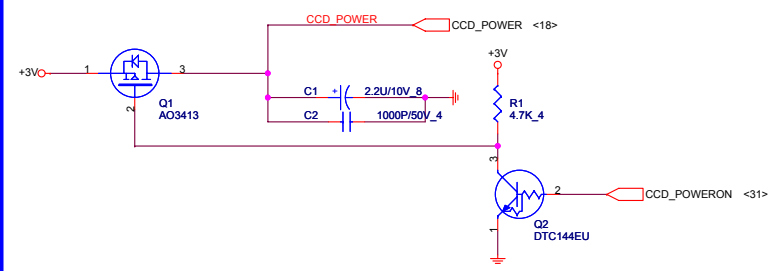
TV Out (SVHS) MiniDIN 7-pin



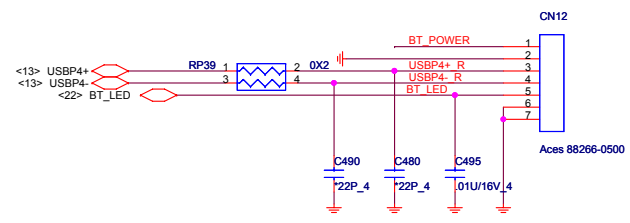
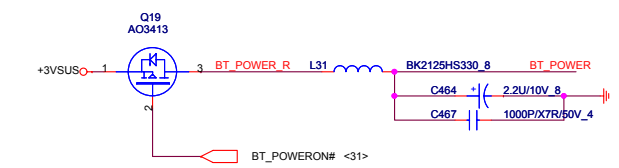




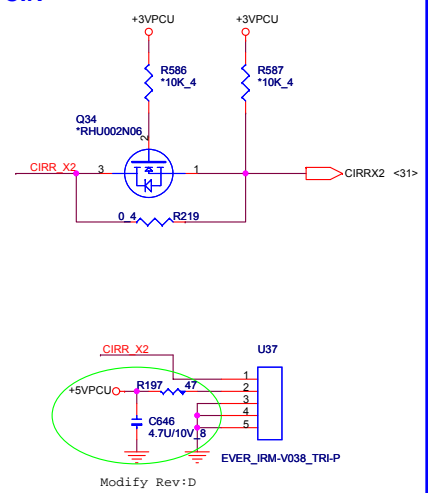
### CAMERA MODULE CONNECTOR



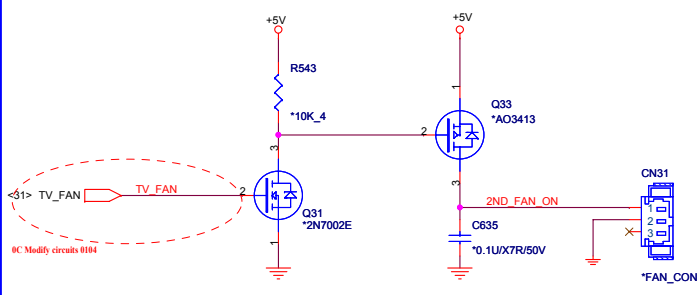
### BLUETOOTH MODULE CONNECTOR

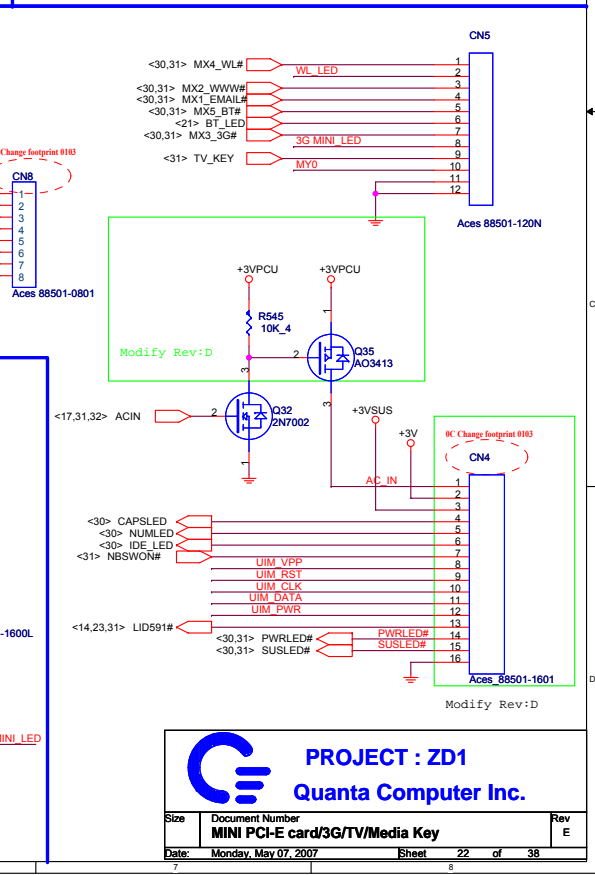
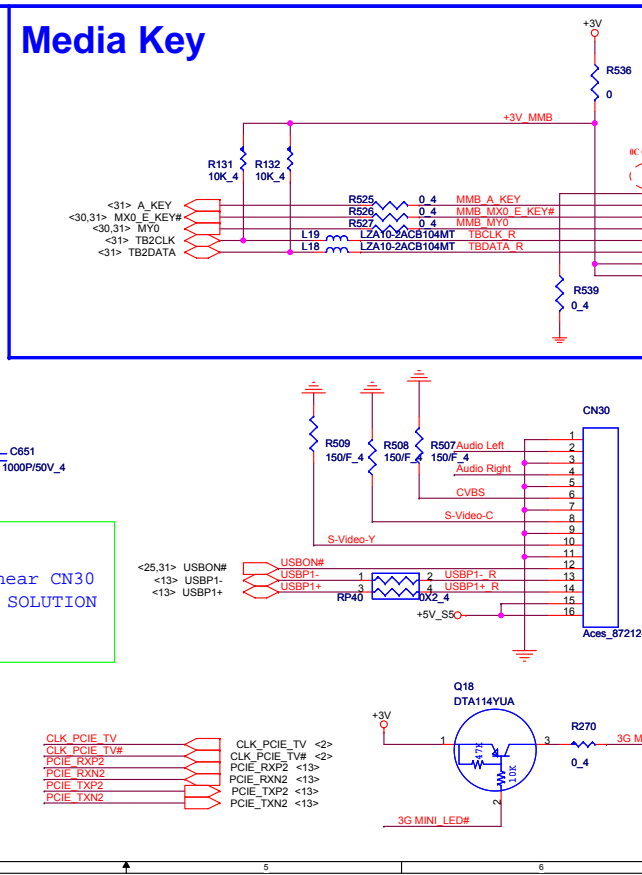
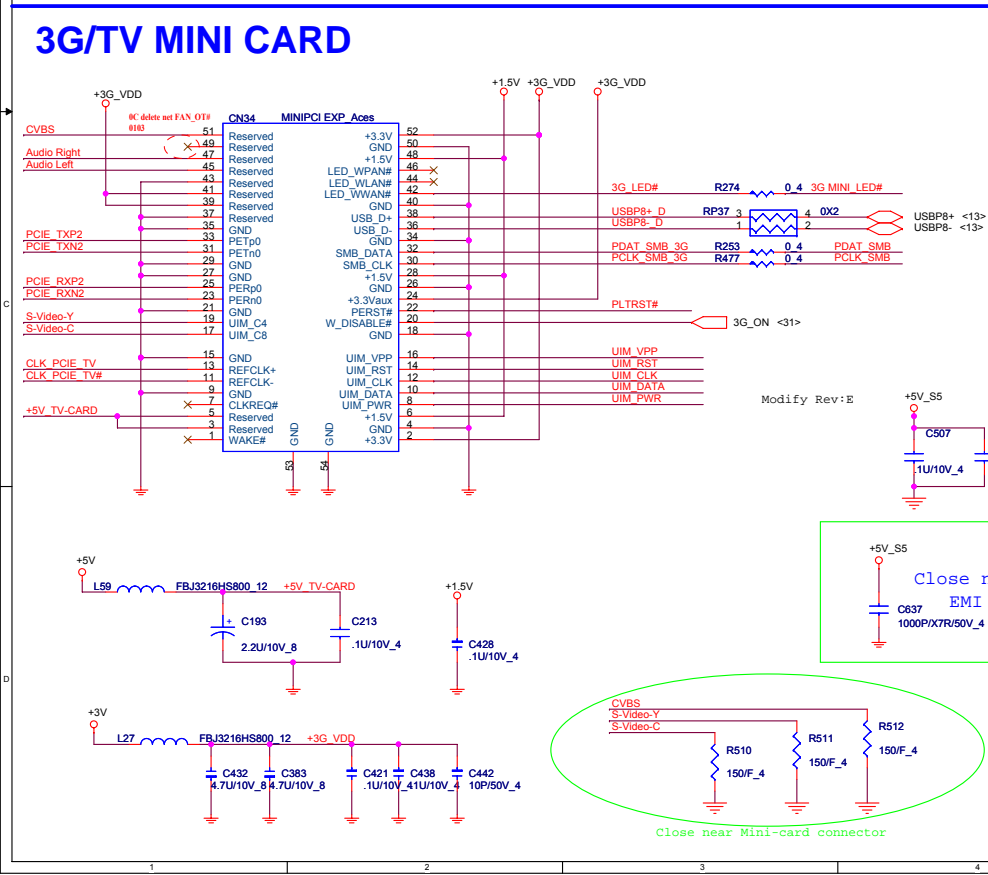
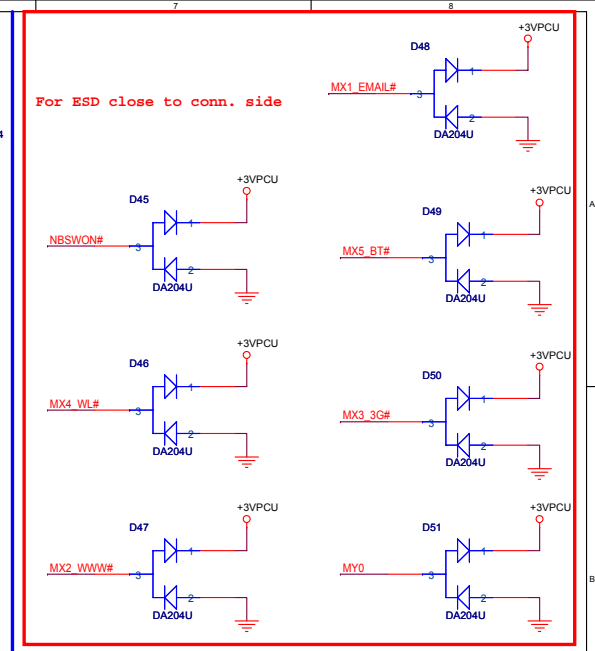
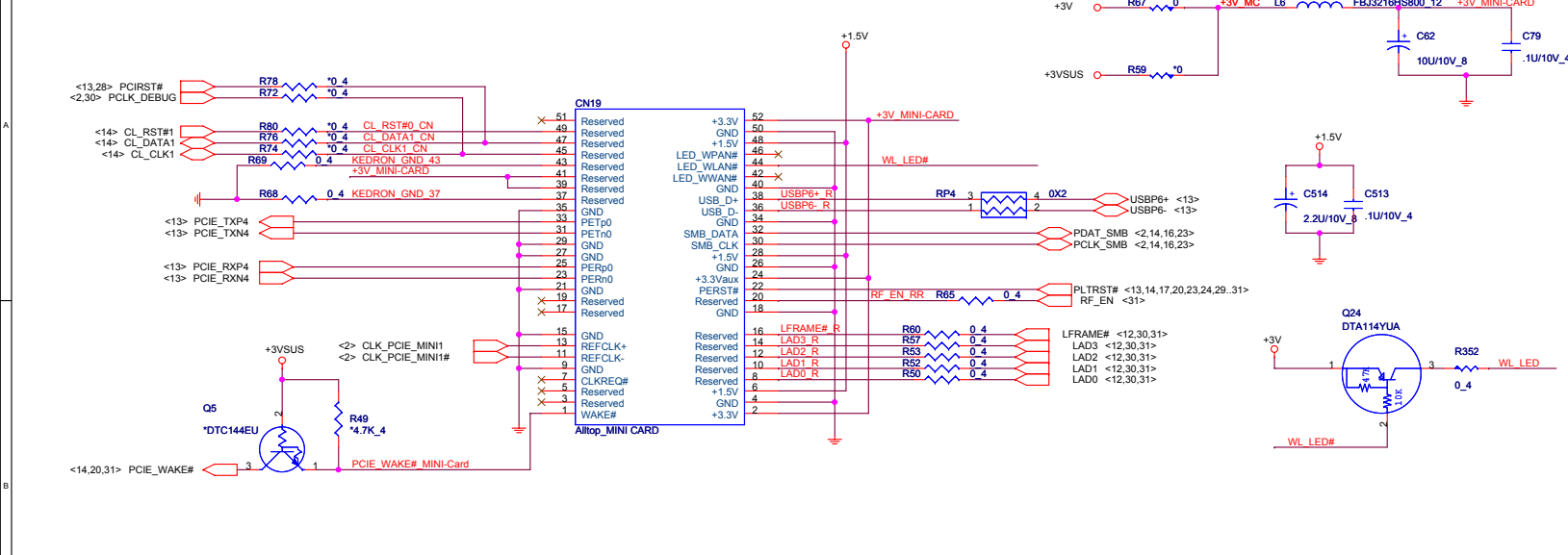


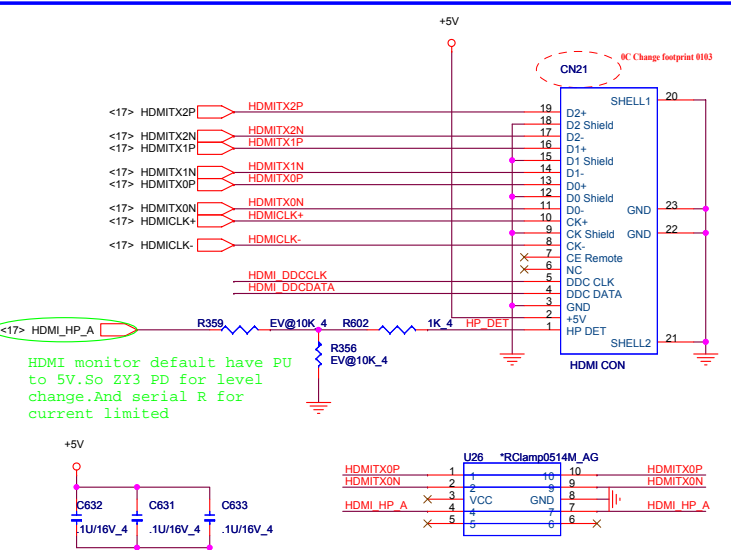
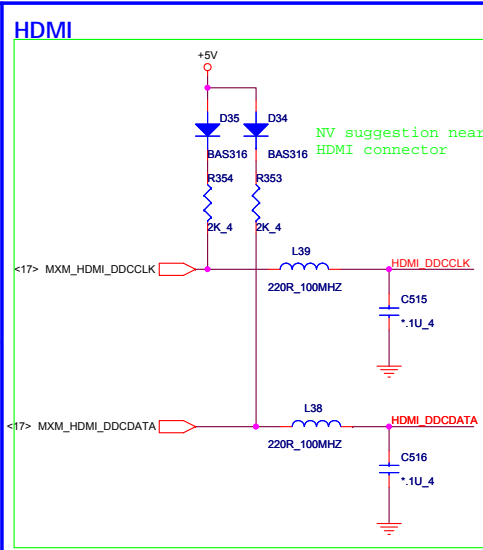
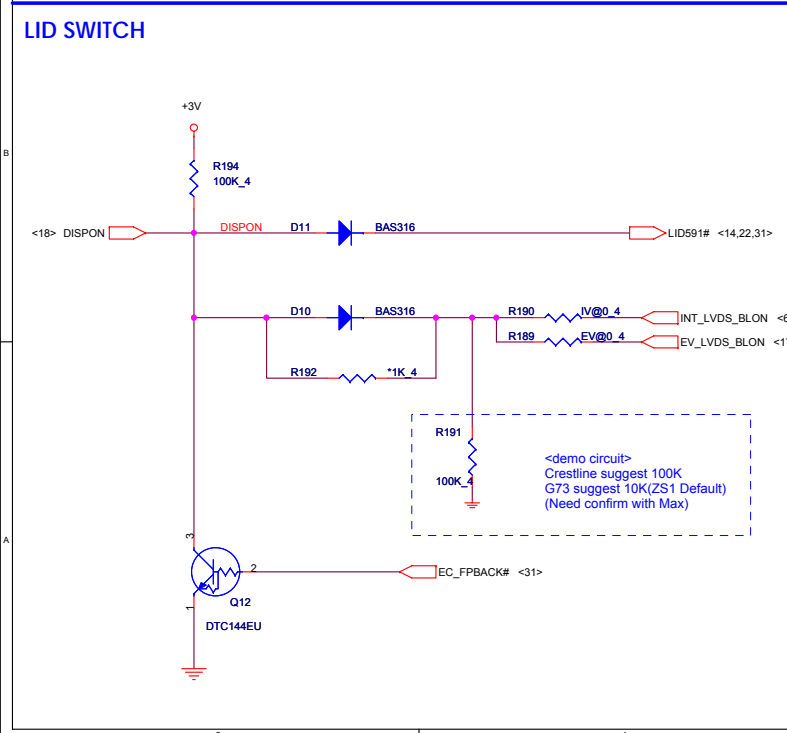
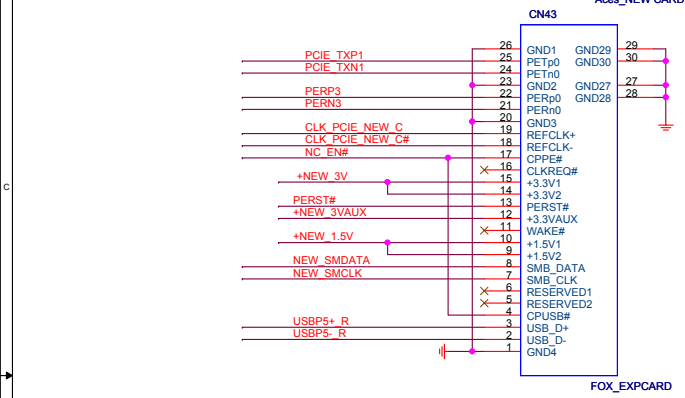
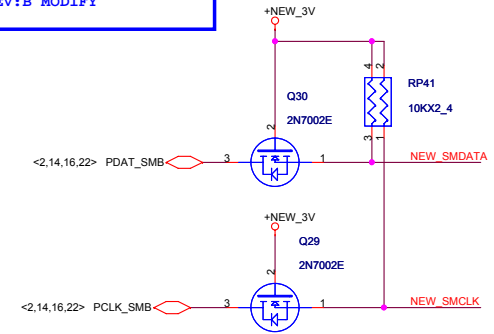
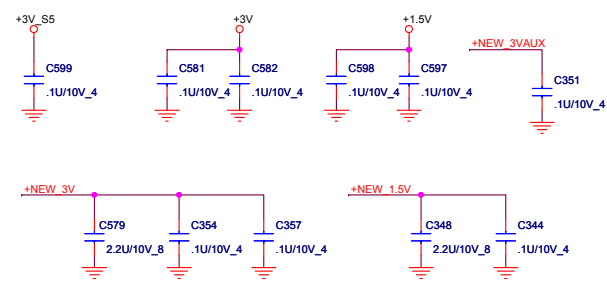
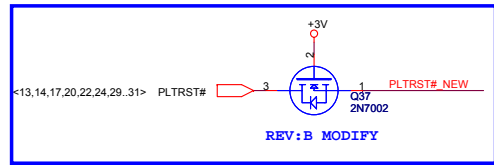
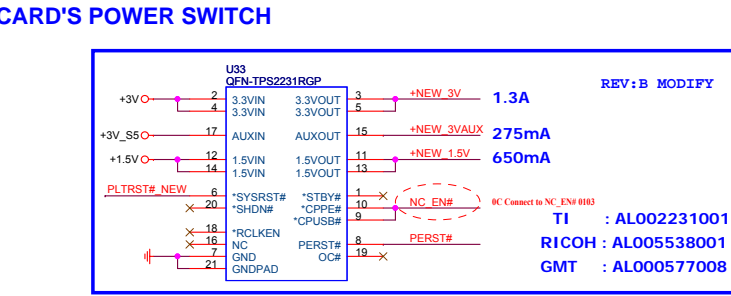
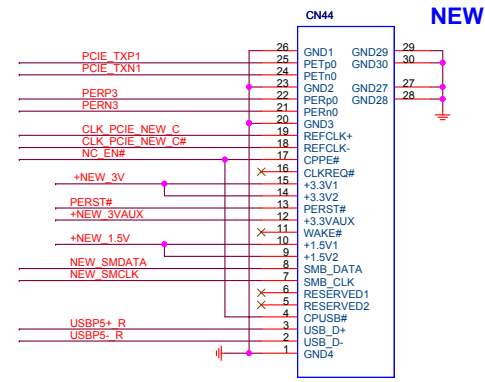
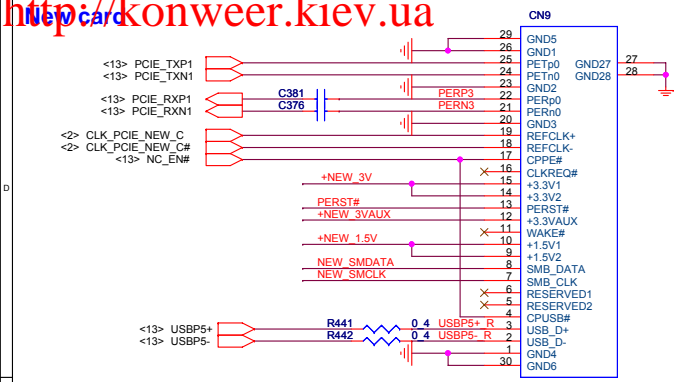
### CIR



### 2nd FAN







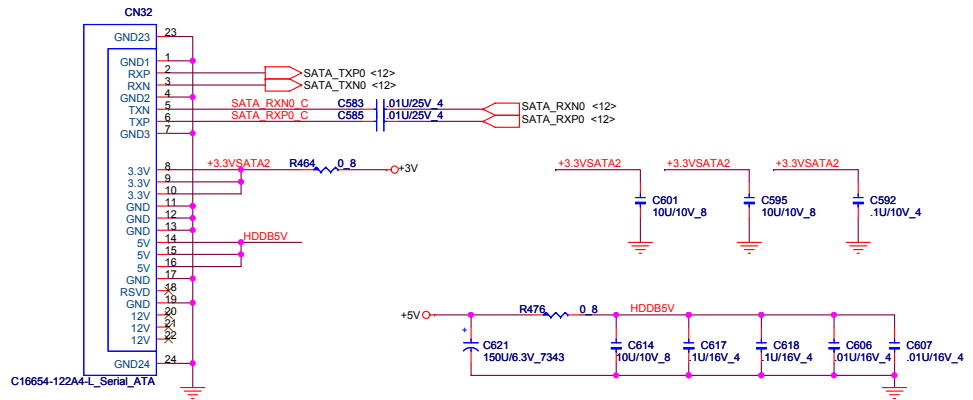
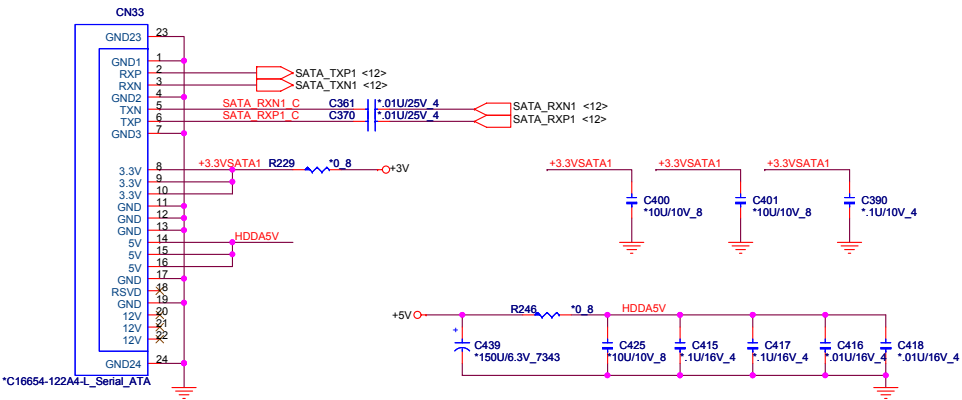
U27 *RClamp0514M_AG		U25 *RClamp0514M_AG	
HDMITX2P	1	10	HDMITX2P
HDMITX2N	2	9	HDMITX2N
	3	8	HDMITX1P
	4	7	HDMITX1N
	5	6	
			HDMICLK+
			HDMICLK-
			HDMI DDCCLK
			HDMI DDCCDATA

**PROJECT : ZD1**  
**Quanta Computer Inc.**

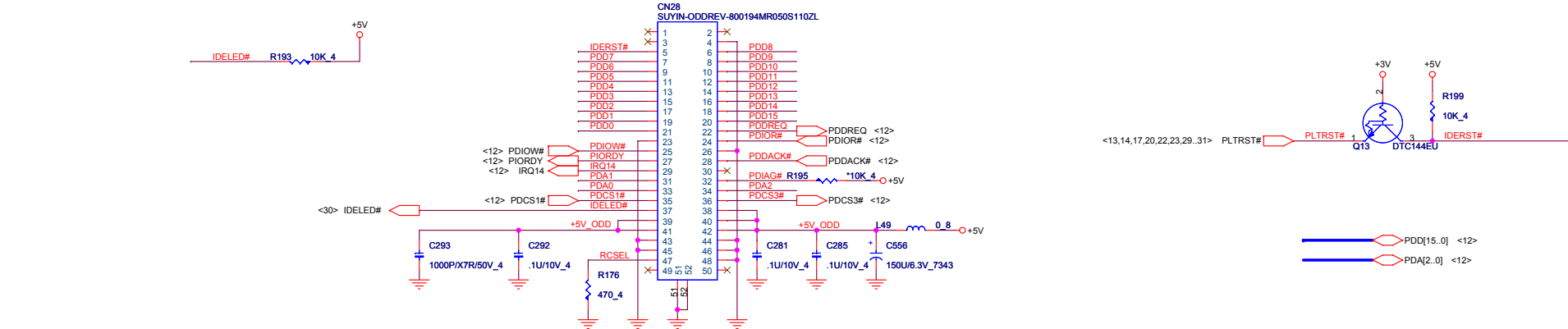
Size Document Number  
**NEW CARD/HDMI/LID**  
Date: Monday, May 07, 2007 Sheet 23 of 38

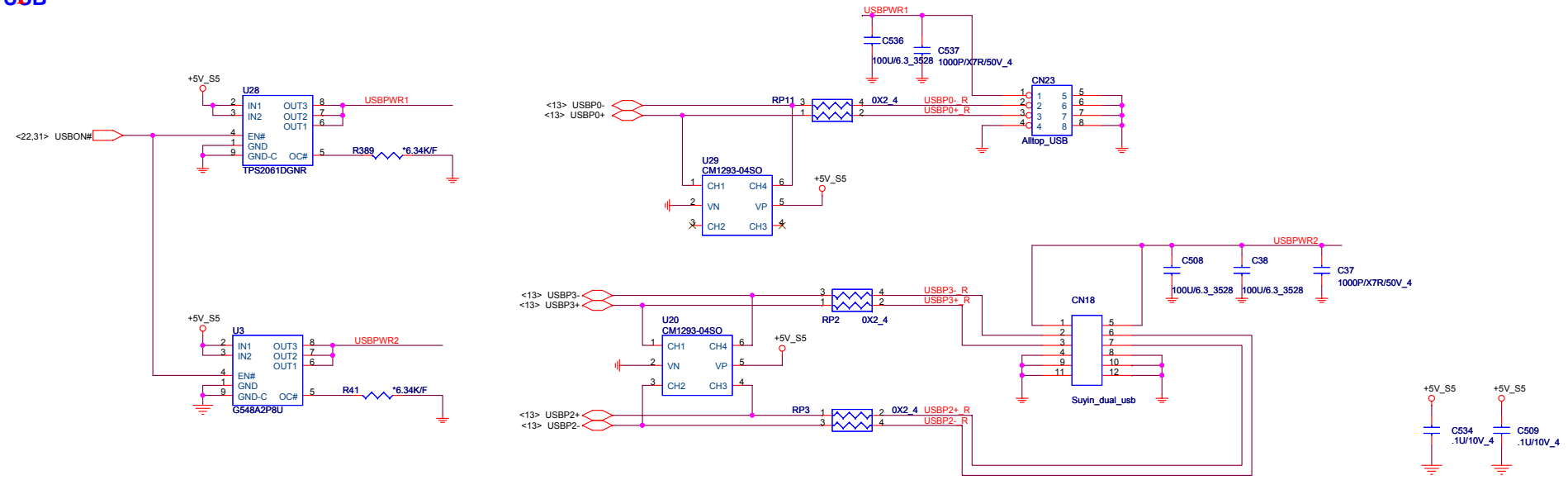
SATA HDD1

Main

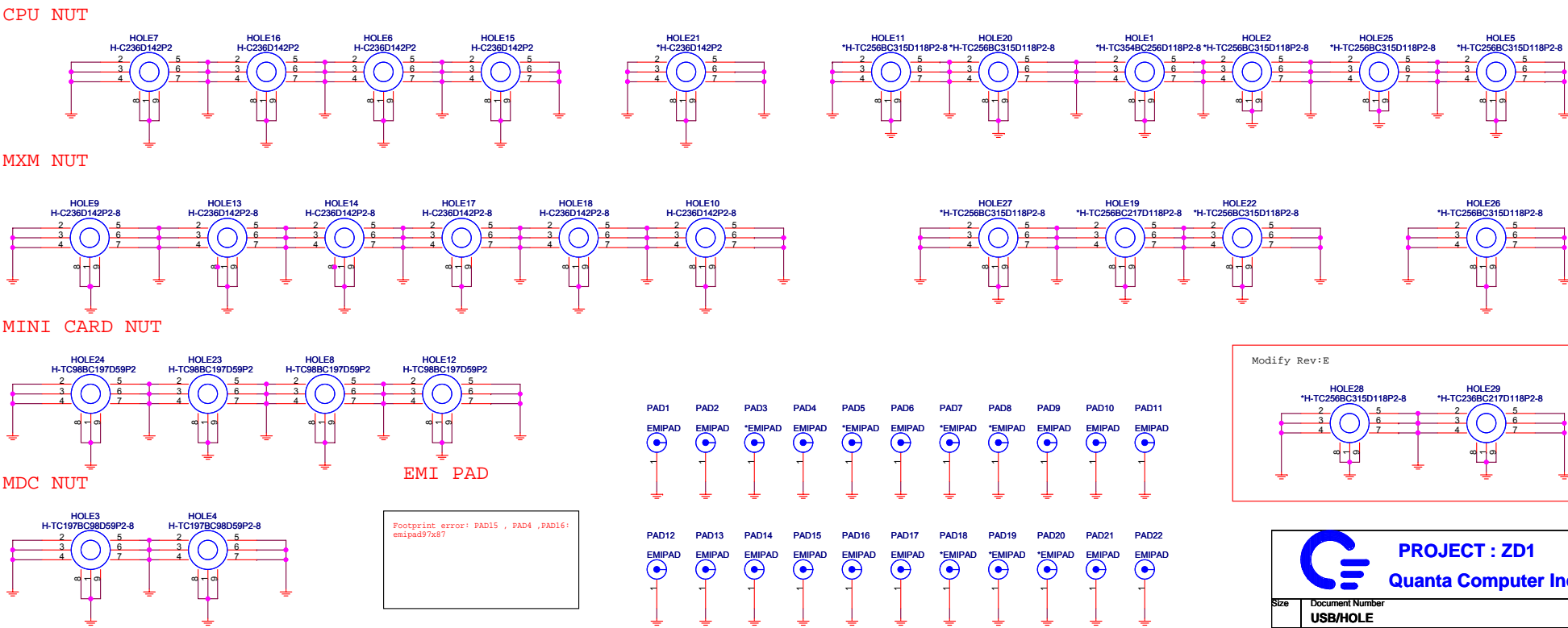


ODD (PATA)



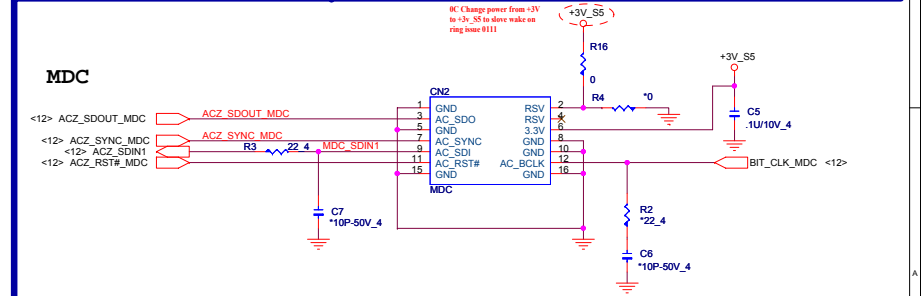
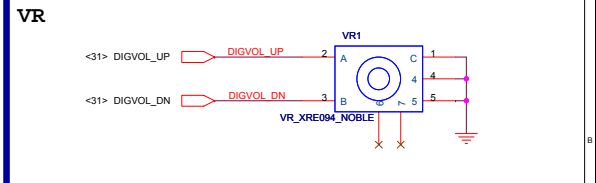
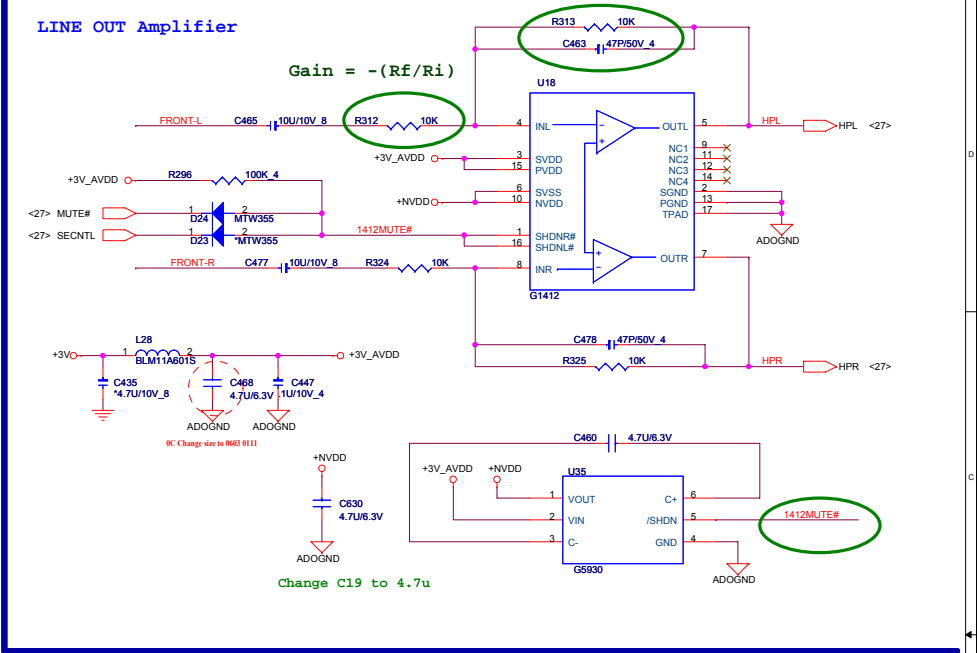
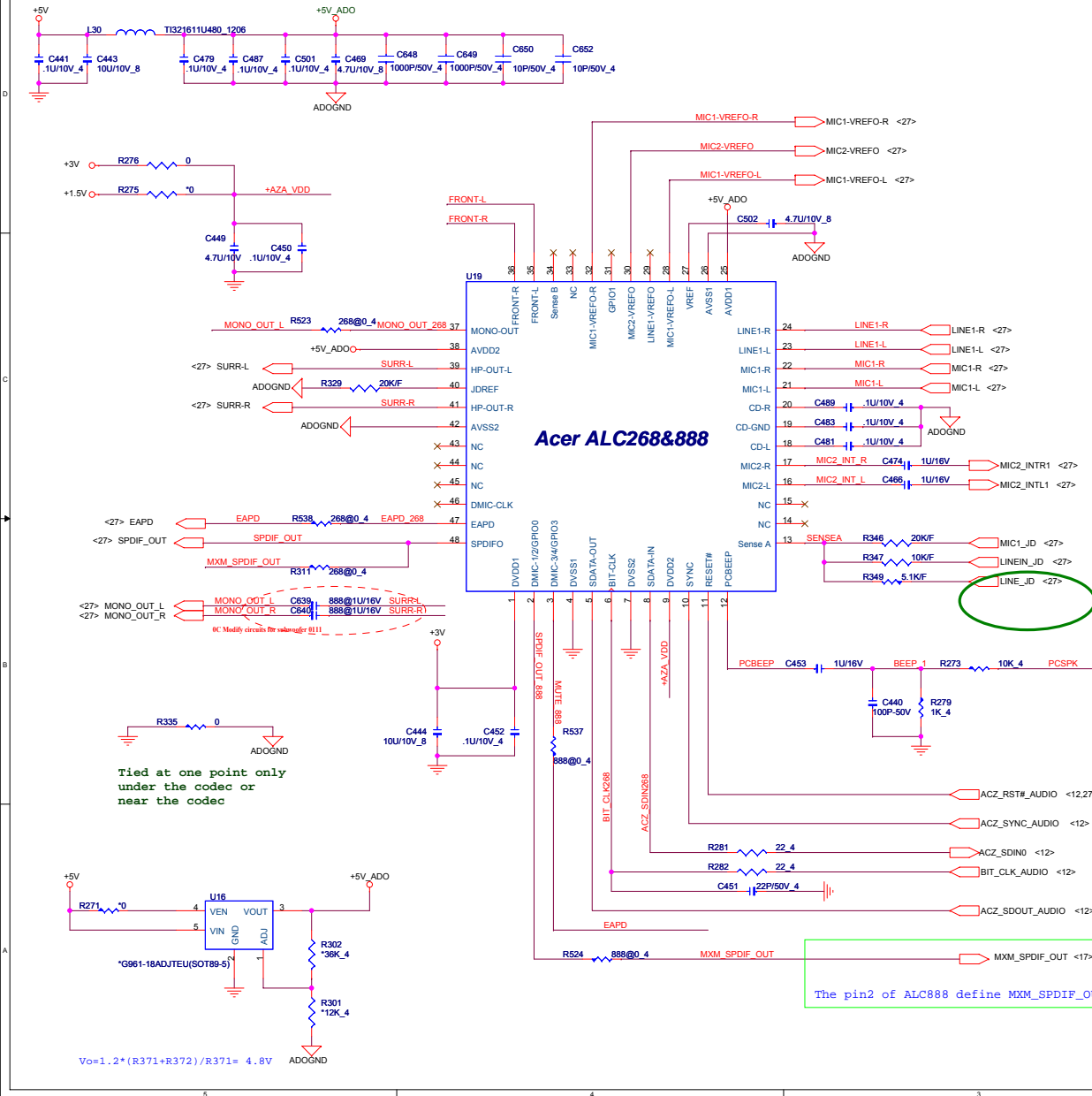


HOLES

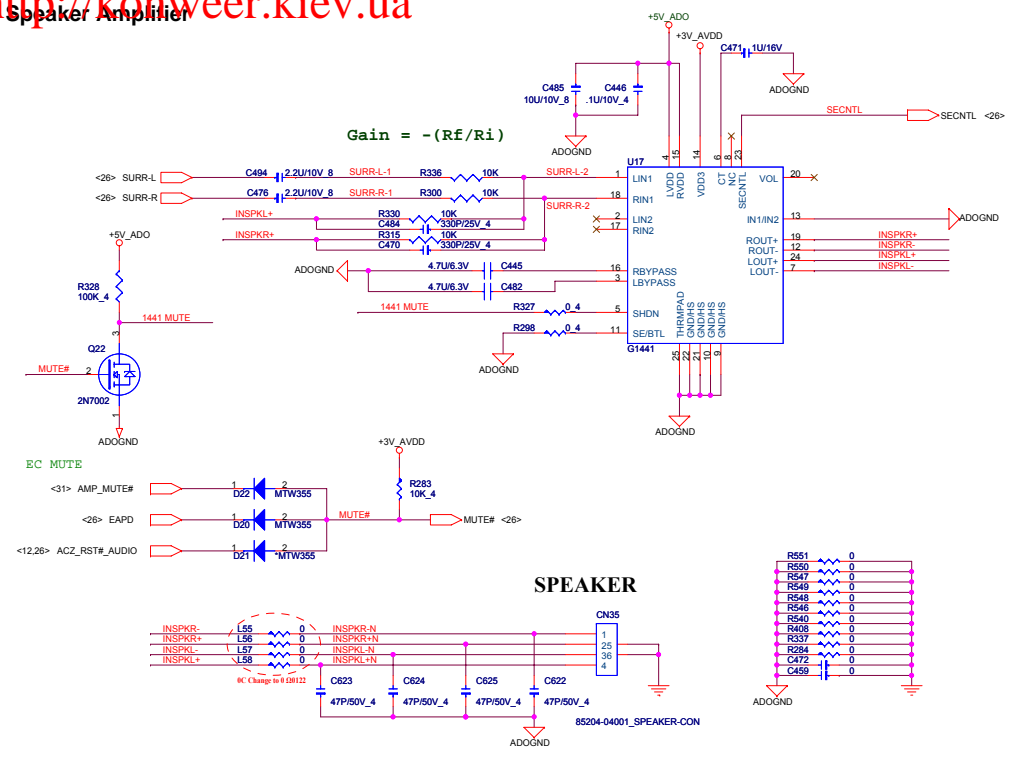


**PROJECT : ZD1**  
**Quanta Computer Inc.**

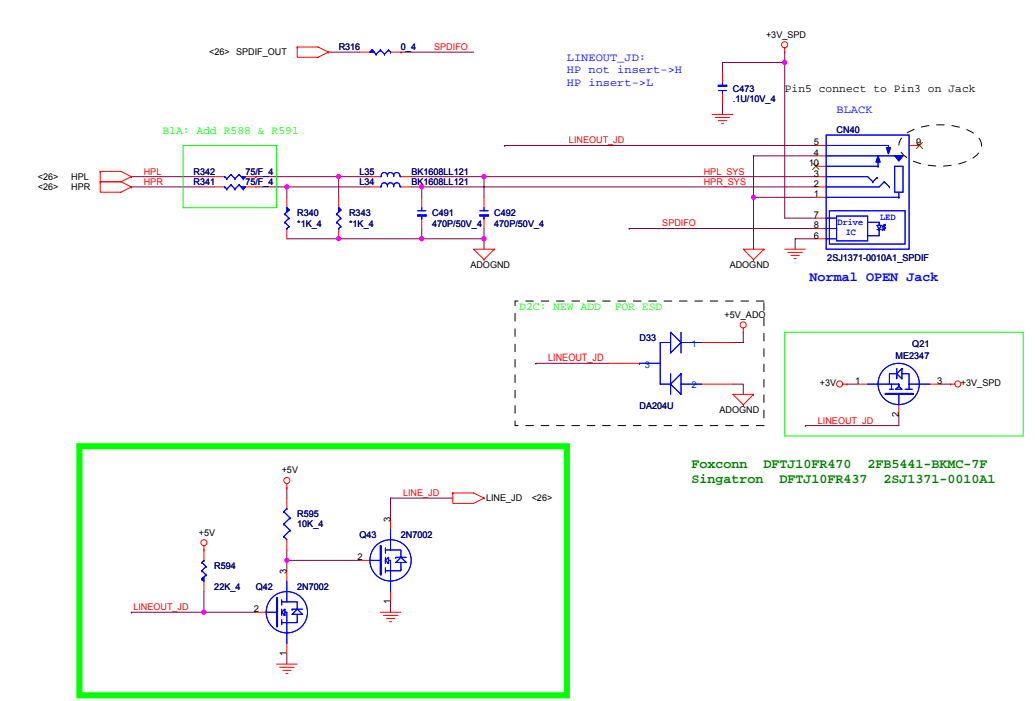
Size	Document Number	Rev
	<b>USB/HOLE</b>	E
Date:	Monday, May 07, 2007	Sheet 25 of 38



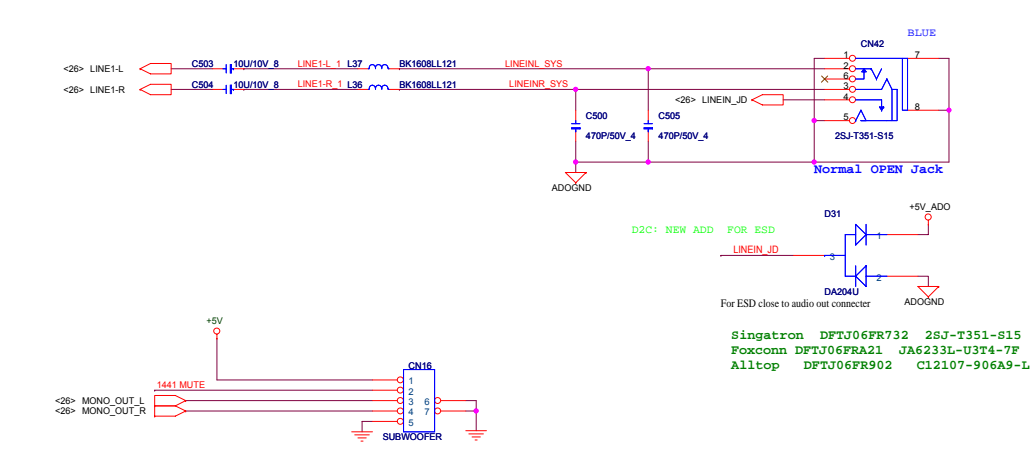
Speaker Amplifier



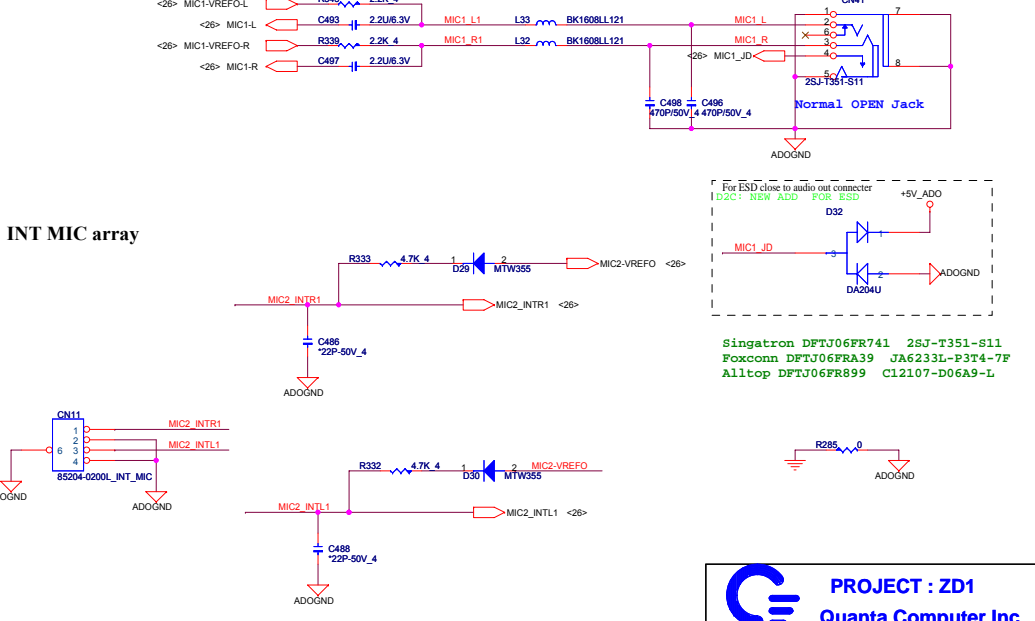
SYSTEM LINE OUT/SPDIF



SYSTEM LINE IN/SUBWOOFER

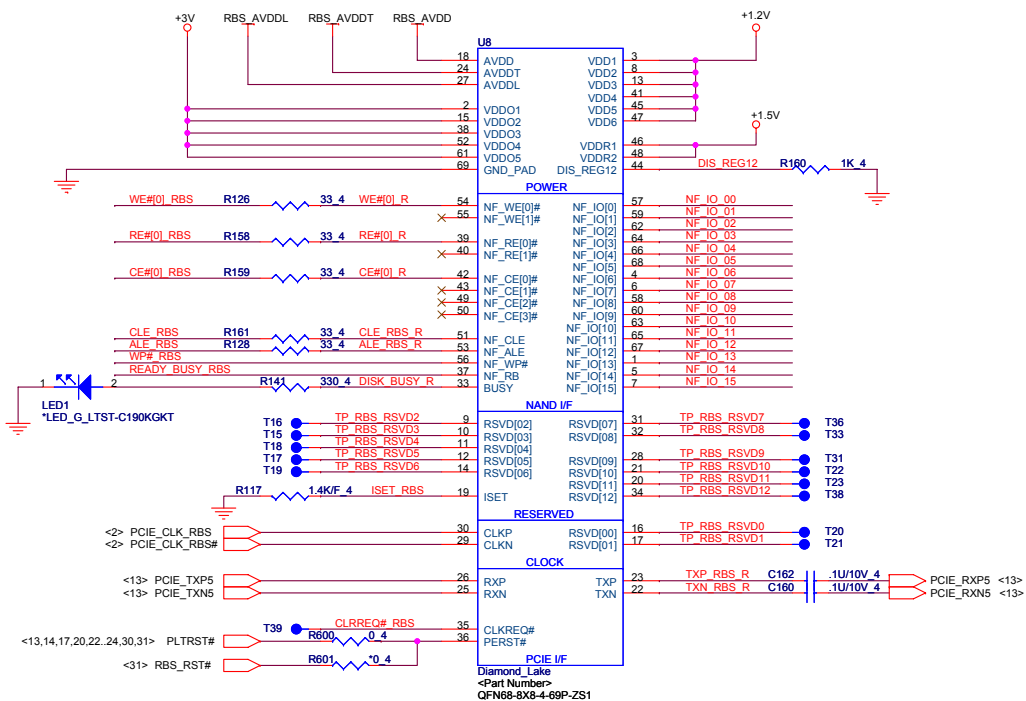


MIC





DIAMOND-LAKE ASIC

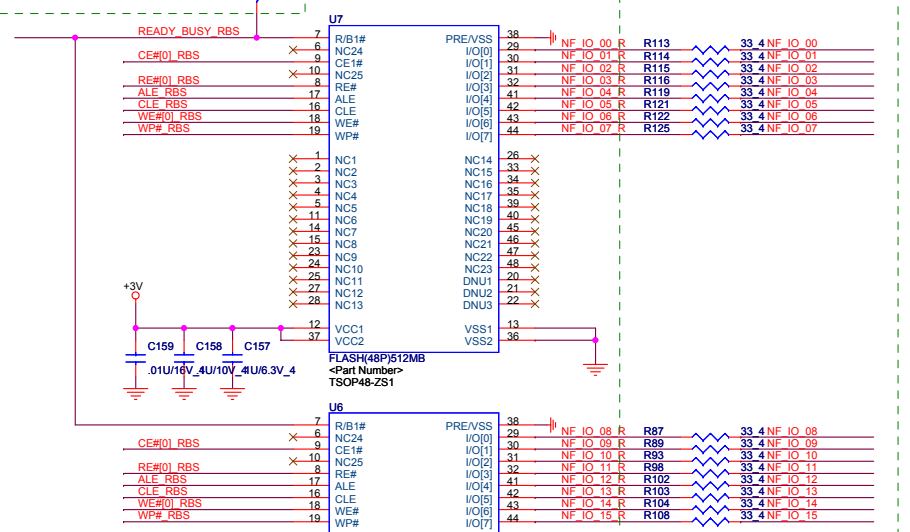


PLACE CLOSE TO NAND FLASH

**INTEL NAND FLASH**

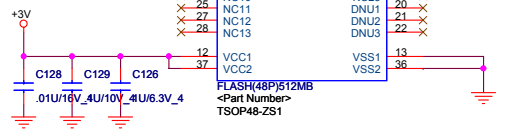
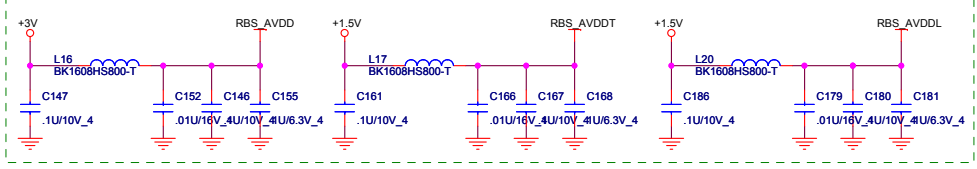
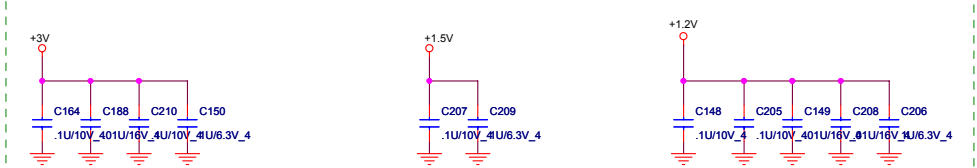
PLACE CLOSE TO NAND FLASH R120 1K\_4

PLACEMENT NOTE:  
PLACE TERMINATION RESISTORS AT 10% TO 25% DISTANCE FROM NAND FLASH.



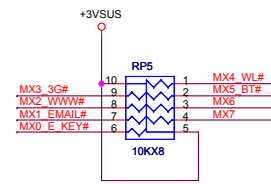
PLACE AS CLOSE AS POSSIBLE TO DIAMOND-LAKE ASIC.

STUFF: INDICATES A 2KB VIRTUAL PAGE => 256MB  
DESTUFF: INDICATES A 4KB VIRTUAL PAGE => 512MB & 1024MB



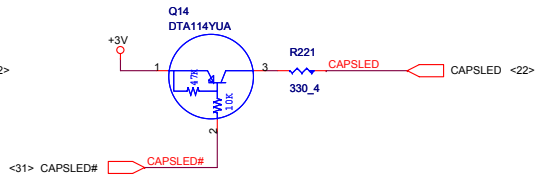
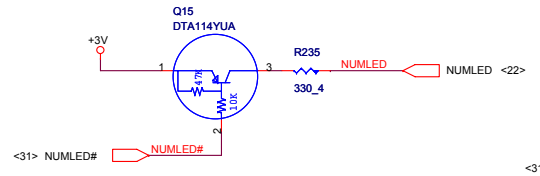
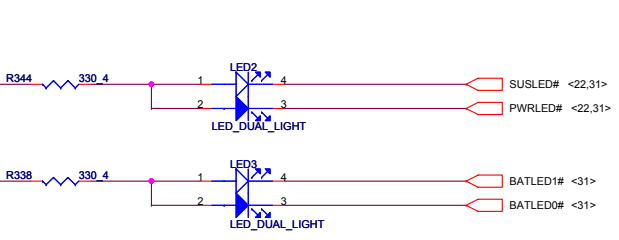
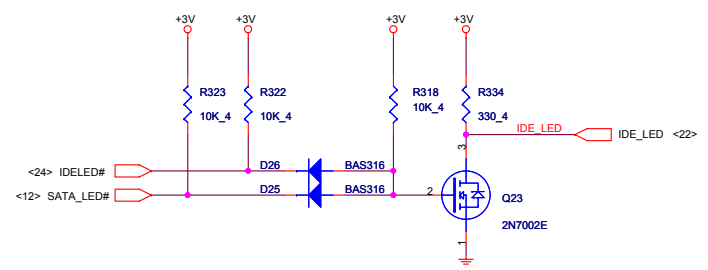
LAYOUT NOTE:  
ANY VIA ADDED BENEATH THE NAND FLASH NEEDS TO HAVE A SOLDERMASK ON IT.

<31> MY15	MY15	MY0	1
<31> MY14	MY14	MY1	2
<31> MY13	MY13	MY2	3
<31> MY12	MY12	MY3	4
<31> MY11	MY11	MY4	5
<31> MY10	MY10	MY5	6
<31> MY9	MY9	MY6	7
<31> MY8	MY8	MY7	8
<31> MY7	MY7	MY8	9
<31> MY6	MY6	MY9	10
<31> MY5	MY5	MY10	11
<31> MY4	MY4	MY11	12
<31> MY3	MY3	MY12	13
<31> MY2	MY2	MY13	14
<31> MY1	MY1	MY14	15
<22,31> MX5_BT#	MX5_BT#	MY15	16
<22,31> MX4_WL#	MX4_WL#	MY16	17
<22,31> MX3_3G#	MX3_3G#	MY17	18
<22,31> MX2_WWW#	MX2_WWW#	MX7	19
<31> MY1	MY1	MX6	20
<22,31> MX1_EMAIL#	MX1_EMAIL#	MX5_BT#	21
<22,31> MX0_E_KEY#	MX0_E_KEY#	MX4_WL#	22
<31> MY16	MY16	MX3_3G#	23
<31> MY17	MY17	MX2_WWW#	24
		MX1_EMAIL#	25
		MX0_E_KEY#	26

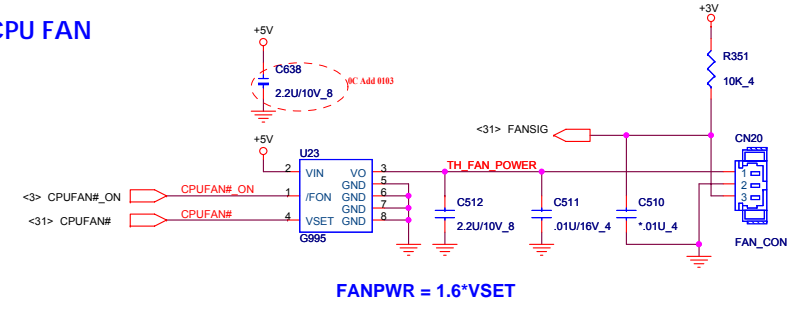


Acex 88502-2641

LED

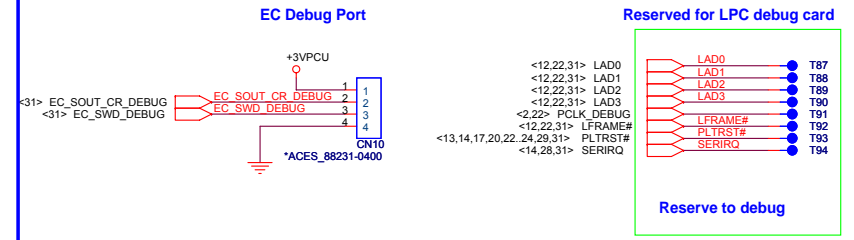


CPU FAN

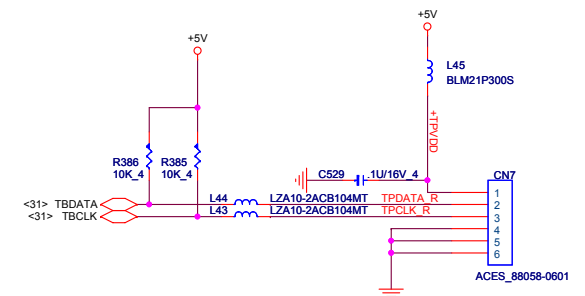


FANPWR = 1.6 \* VSET

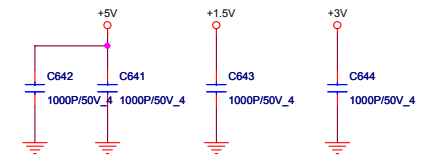
DEBUG PORT



T/P



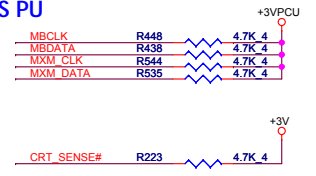
EMI solution



**PROJECT : ZD1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>FAN,LED,KB,DEBUG PORT,TP</b>	E
Date:	Monday, May 07, 2007	Sheet 30 of 38

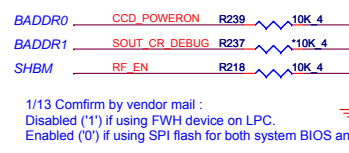
### SM BUS PU



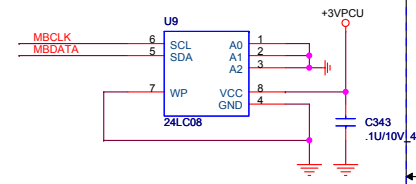
### I/O ADDRESS SETTING

I/O Address	
BADDR1-0	Index Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

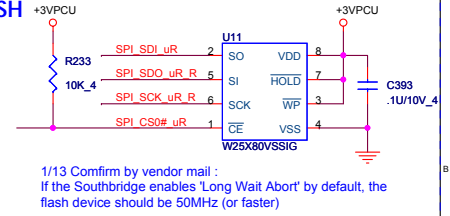
SHBM=0: Enable shared memory with host BIOS



### ACER ID



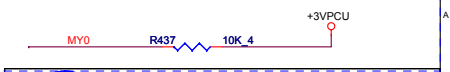
### SPI FLASH



### BUTTON ON KEYBOARD MATRIX



### INTERNAL KEYBOARD STRIP SET

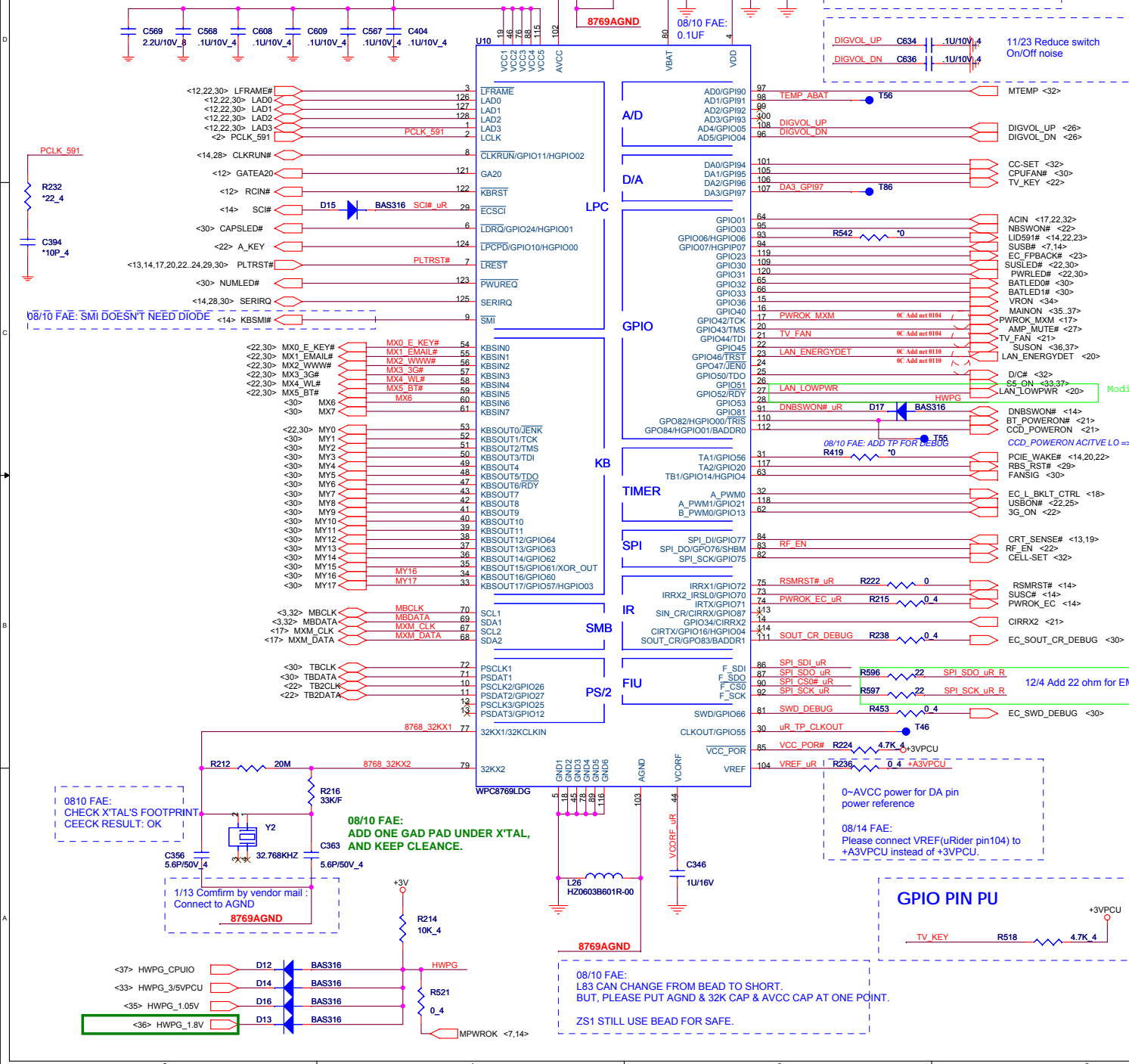


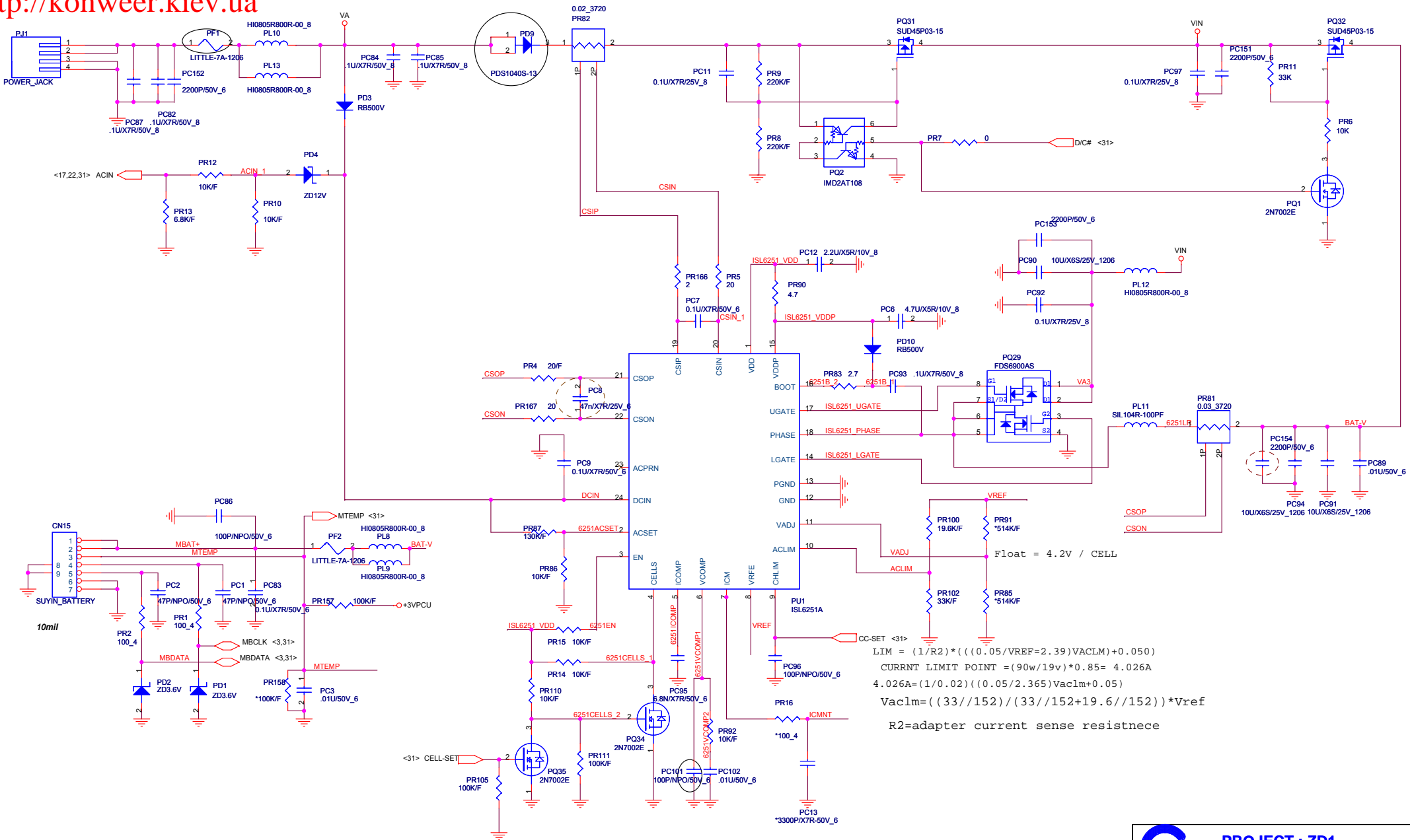
### GPIO PIN PU



**PROJECT : ZD1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>PC8769L &amp; FLASH</b>	E
Date:	Monday, May 07, 2007	Sheet 31 of 38





$$LIM = (1/R2) * (((0.05/VREF=2.39)VACLIM)+0.050)$$

$$CURRENT\ LIMIT\ POINT = (90w/19v) * 0.85 = 4.026A$$

$$4.026A = (1/0.02) * (((0.05/2.365)Vaclm)+0.05)$$

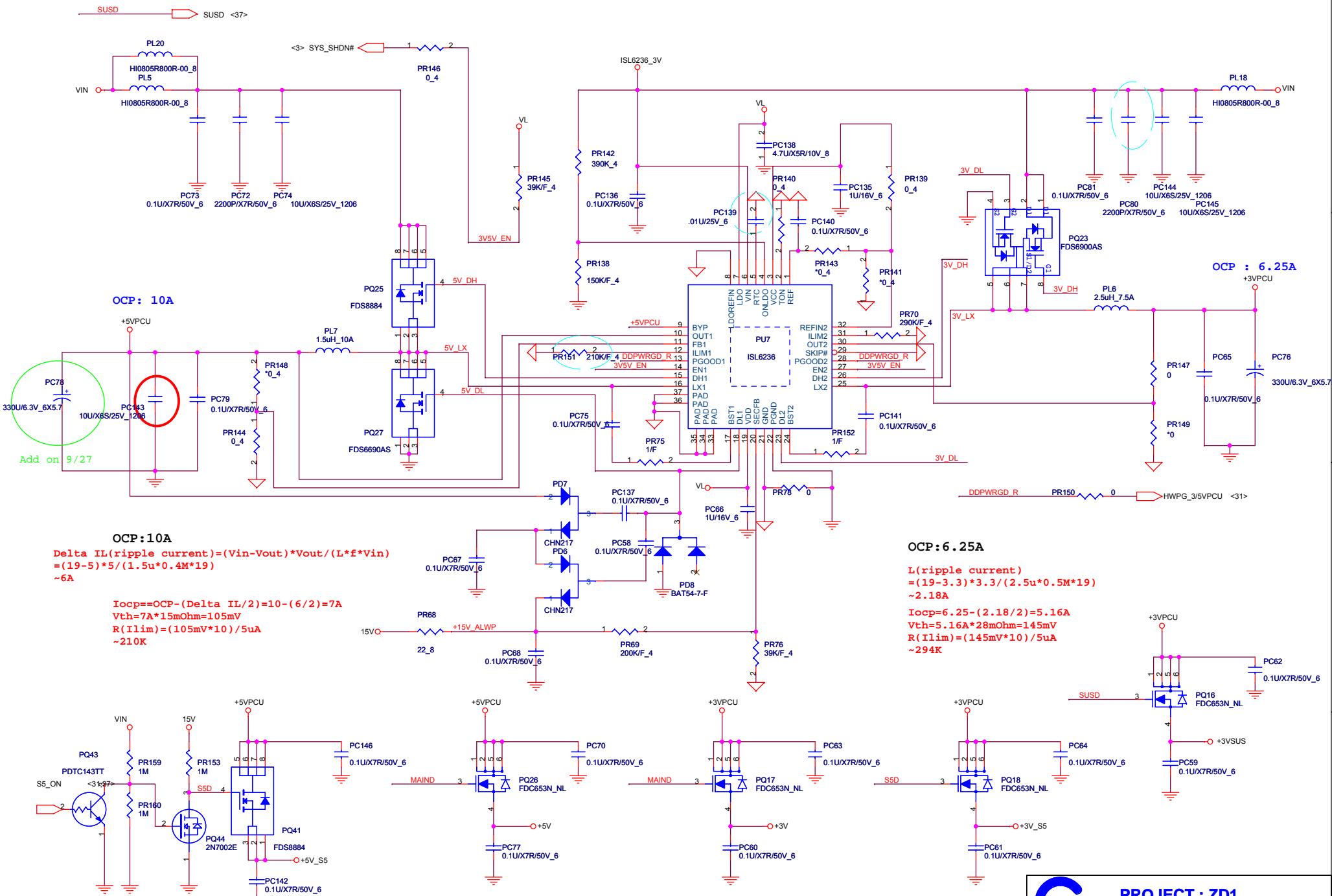
$$Vaclm = ((33//152) / ((33//152)+19.6//152)) * Vref$$

R2=adapter current sense resistnece

CELL-SET = Hi -----> Cells = VDD ----->4S  
 CELL-SET = Low -----> Cells = GND ----->3S

**PROJECT : ZD1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>ISL6251 CHARGER</b>	C
Date:	Monday, May 07, 2007	Sheet 32 of 38



OCP: 10A

$$\Delta I_L(\text{ripple current}) = (V_{in} - V_{out}) * I_{out} / (L * f * V_{in})$$

$$= (19 - 5) * 5 / (1.5 \mu * 0.4 \text{M} * 19) \sim 6\text{A}$$

$I_{ocp} = OCP - (\Delta I_L / 2) = 10 - (6 / 2) = 7\text{A}$

$V_{th} = 7\text{A} * 15\text{m}\Omega = 105\text{mV}$

$R(I_{lim}) = (105\text{mV} * 10) / 5\mu\text{A} \sim 210\text{K}$

OCP: 6.25A

$$L(\text{ripple current}) = (19 - 3.3) * 3.3 / (2.5 \mu * 0.5 \text{M} * 19) \sim 2.18\text{A}$$

$I_{ocp} = 6.25 - (2.18 / 2) = 5.16\text{A}$

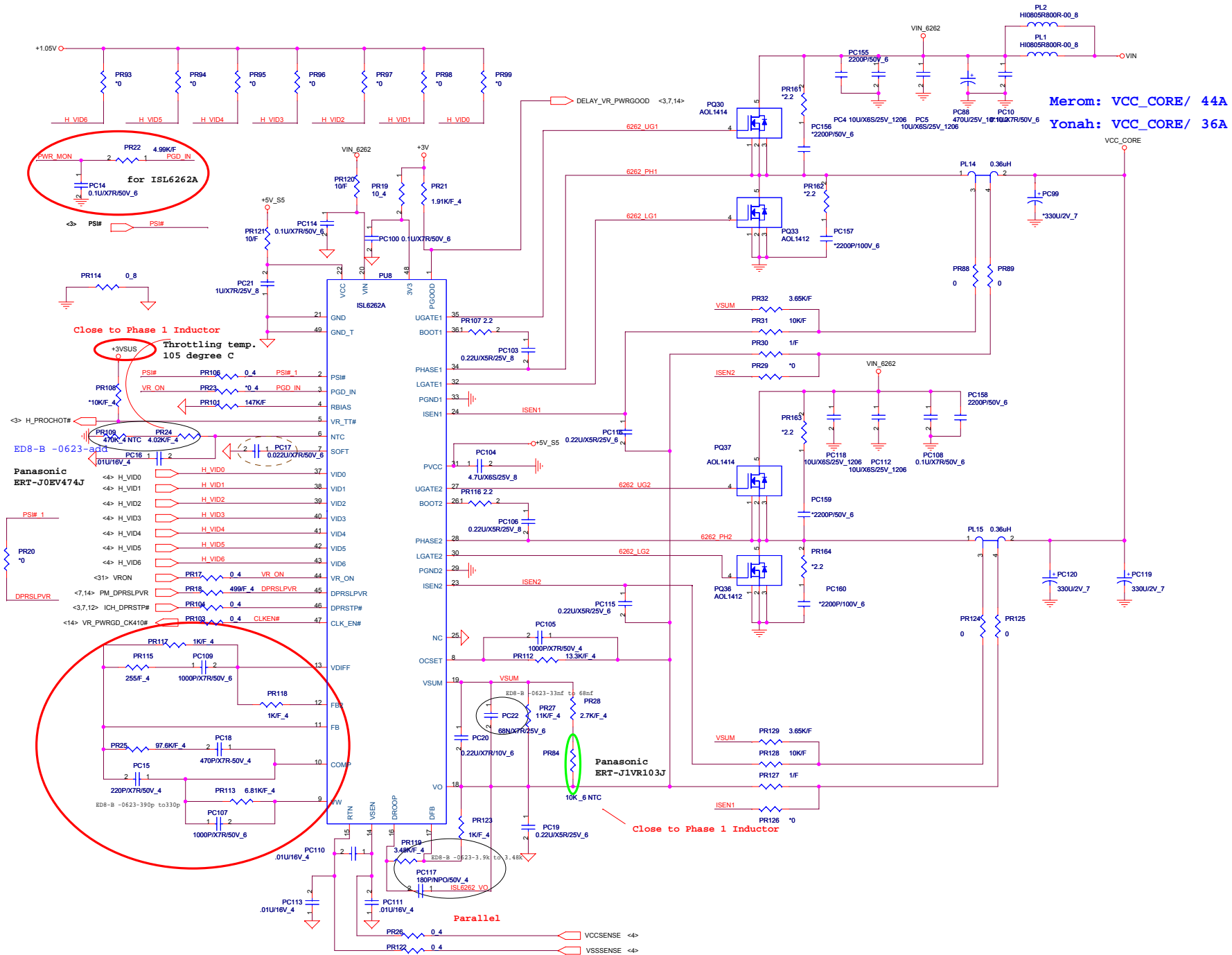
$V_{th} = 5.16\text{A} * 28\text{m}\Omega = 145\text{mV}$

$R(I_{lim}) = (145\text{mV} * 10) / 5\mu\text{A} \sim 294\text{K}$

modify 0103 2007

**PROJECT : ZD1**  
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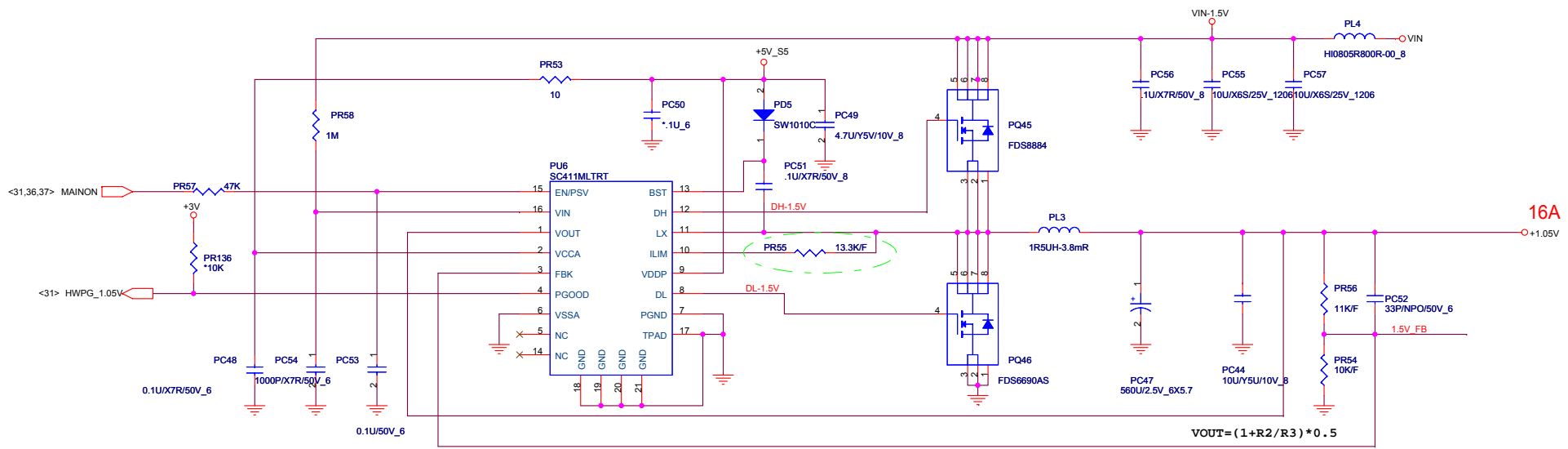
Size Custom	Document Number	Rev B
<b>ISL6251 CHARGER</b>		
Date: Monday, May 07, 2007	Sheet	33 of 38



Merom: VCC\_CORE/ 44A  
Yonah: VCC\_CORE/ 36A

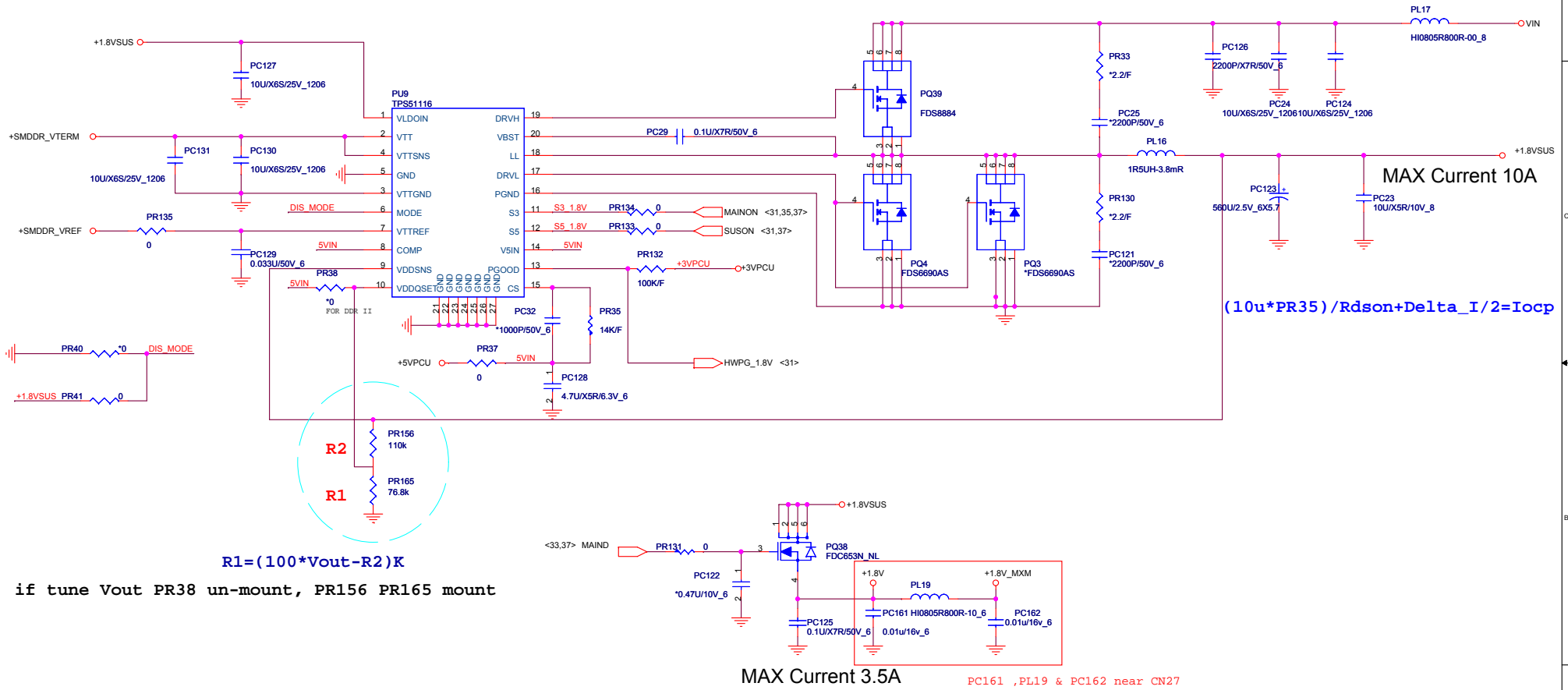
**PROJECT : ZD1**  
**Quanta Computer Inc.**

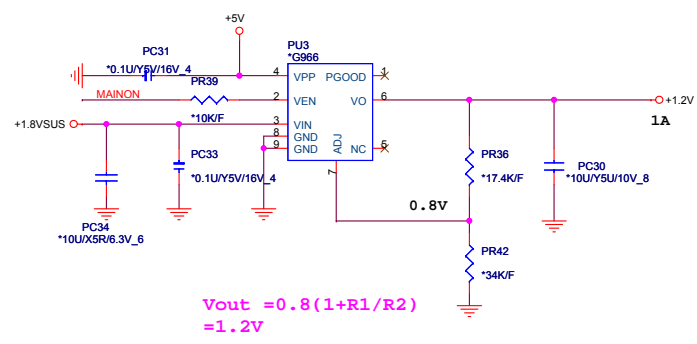
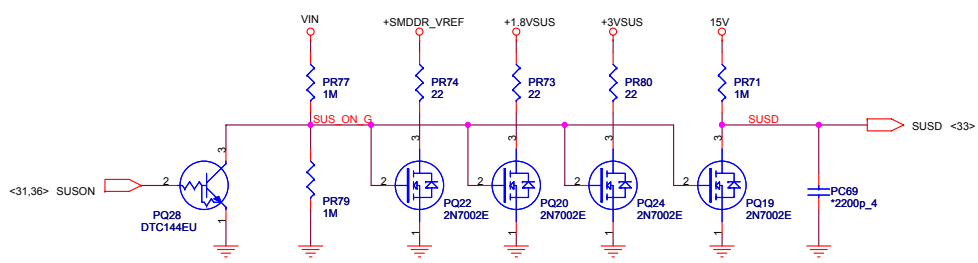
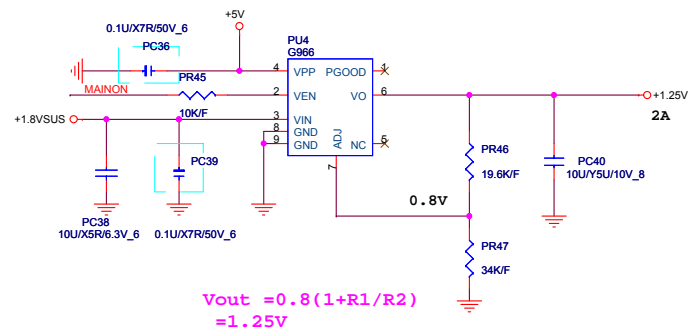
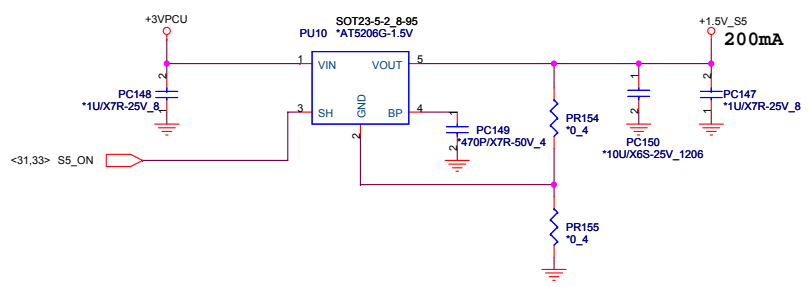
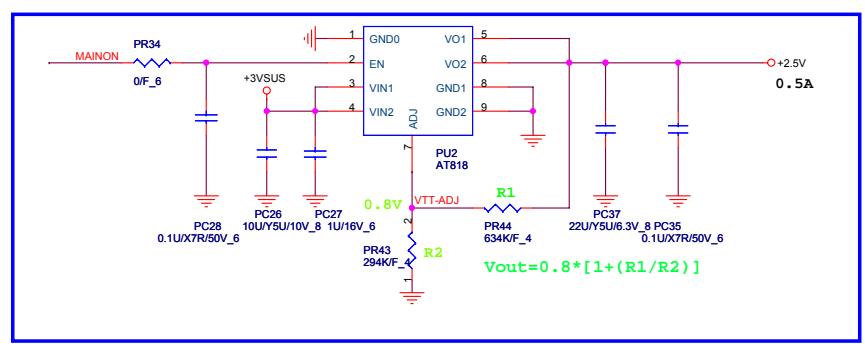
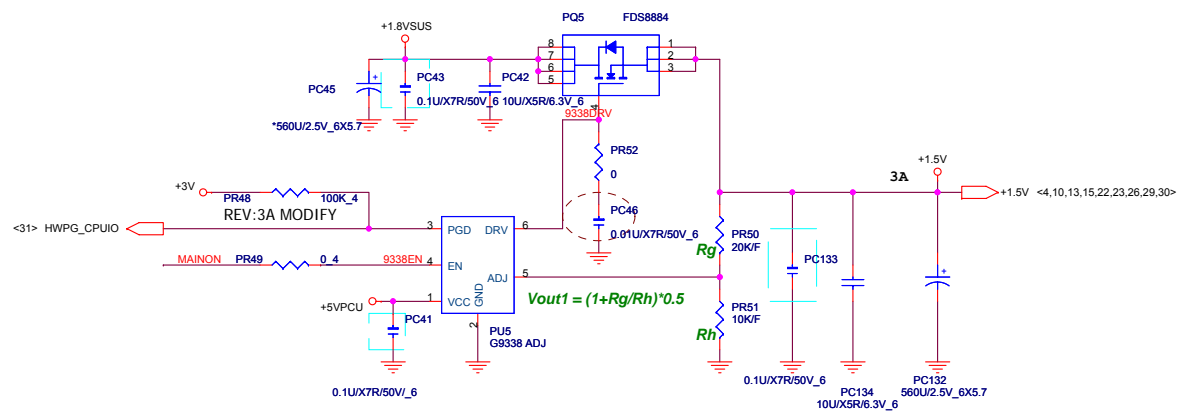
Size	Document Number	Rev
Custom	<b>CPU CORE(ISL6262)</b>	C
Date:	Monday, May 07, 2007	Sheet 34 of 38



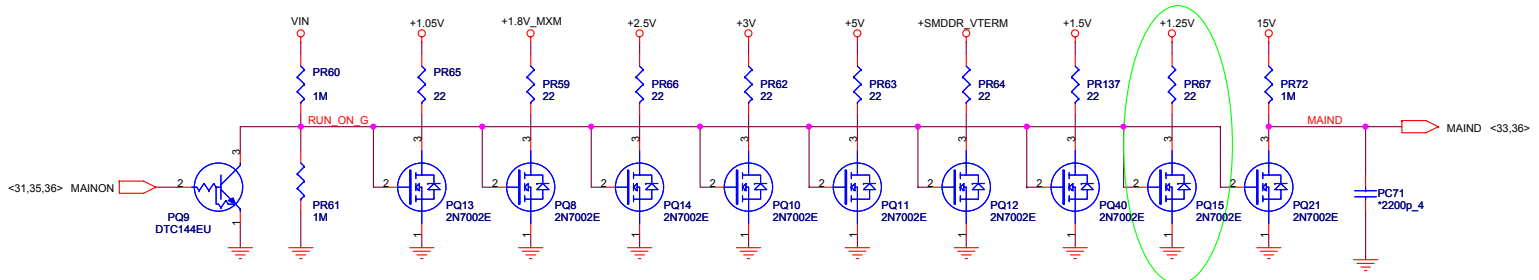
$R_{dson} * I_{ocp} = PR55 * 10u$        $R_{dson} = 15m \text{ ohm}$

$V_{OUT} = (1 + R2/R3) * 0.5$






Add by power on 10/19



Model	REV	CHANGE LIST	MODEL	ZY3		
				FROM	To	
ZD1 MB	1A	FIRST RELEASED: E200610-3793 (PCB: DA0ZD1MB6A0)	X	1A		
	2A	<p>Page10 : Depop R153 &amp; pop L23 for system can not boot</p> <p>Page14 : U36 package didn't math footprint, change P/N.</p> <p>Page26 : Remove R275, install R276; remove R4, install R16; Change R245, R247 power source from +1.5V_S5/+1.5V to +3V_S5/+3V , Follow customer request modem change support to +3VSUS.</p> <p>Page22 : MMB(CN8) PIN define error.</p> <p>Page22 : TV card change support to +1.5V.</p> <p>Page18 : Install R5, depop R7,: Follow customer request use EC to control backlight ON/OFF function.</p> <p>Page14 : GPIO10: Reserve PU, 10K +&gt; It is GPO and OD; GPIO14: Reserve PD, 10K =&gt; It is GPI as AC present and active high;</p> <p>Page6 : TV_DCONSEL[0:1], UMA =&gt;NC, External VGA tie to GND.</p> <p>Page31 : 2nd FAN change design</p> <p>Page23 : New card power SW (location: U33) change same as Z01</p> <p>Page31 : add 2 capacity 0.1uF(C634,C636) in DIGVOL_UP / DIGVOL_DN pins</p> <p>Page26 : Co-layout ALC268 and 888S</p> <p>Page28 : SD card can not be detected , U32(ES2) sample will fix this issue.</p> <p>Page28 : MMC card can not be detected , U32(ES2) sample will fix this issue.</p> <p>Page14 : The CLPWROK pin of ICH8 connect with HWFG signal</p> <p>Page22 : change CN7 pin definition for T/P no function.</p> <p>Page24 : change CN8 pin definition MMB no function.</p> <p>Page14 : The signal of KBSMI#_ICH add diode , and it PU to +3V_S5 The signal of LID591#_ICH add diode , and it PU to +3V_S5 for ICH8 electric leakage issue.</p> <p>Page26 : Change subwoofer from 4pin to 5pin connector.</p>	X	1A		
			1A	2A		
			1A	2A		
			1A	2A		
			1A	2A		
			1A	2A		
			1A	2A		
			1A	2A		
			1A	2A		
1A			2A			
2B	<p>Page 2 : Add C645 for EMI solution</p> <p>Page31 : Follow customer request 2nd FAN is controlled by EC</p> <p>Page19 : Floating CN13.16 &amp; CN13.17 ,CN14.15 &amp; CN14.16 for ESD test</p> <p>Page07 : DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK and DPLL_REF_SSCLK#. To GND</p> <p>Page36 : Add PI filter to reduce the power ripple of +1.8V.</p> <p>Page16 : Modify SMBus address A2 , The signal of B_SAL need to PU and B_SA0 need to PD</p> <p>Page26 : add 2 capacity 1uF(C639,C640) for subwoofer</p> <p>Page30 : add capacity 2.2uF(C638)</p>	1A	2A			
		1A	2A			
		1A	2A			
		1A	2A			
		1A	2A			
		1A	2A			
		2A	2B			
		2A	2B			
		2A	2B			
		2A	2B			
2C	<p>Page17 : Adding (Q52 &amp; R541 &amp; Q53) extra circuitry to prevent power leakage from system into MXM</p> <p>Page21 : Change power of CIR from +3VPCU and +5VPCU.</p> <p>Page31 : AEC pin24 is multi function pin, when EC power up, pin17 will change to JTAG/TCK function not GPIO. So,need to change from pin24 (GPIO47) to pin27 (GPIO52).</p> <p>Page22: Power/B connector add two LED control signal and change to 16 pin from 14-pin for meet ACER LED spec .</p> <p>Page22: Q35 change to AO3413 form DTAL14 for increase LED driving power.</p> <p>Page23: BL_ON pull up resistor from 10kohm to 100Kohm(R194 ).+3V pull up will cause power on leakage on BL_ON signal due to our VGA have 10kohm pull low.</p>	2A	2B			
		2A	2B			
		2A	2B			
		2B	3A			
		2B	3A			
		2B	3A			
		2B	3A			
		2B	3A			
		2B	3A			
		2B	3A			
2D	<p>Page19 : Connect CRT of CN13.16 &amp; 17 to GND for ESD</p> <p>Page17 : Add capacity 330uF(C647) &amp; Remove R541</p> <p>Page22 &amp; 25: Combine USB/B (CN17) and TV/B(CN30) connector, Connector change to 16 pin. and +5_S5 from 1pin to 2pin.</p> <p>Page25 : Connect HOLE 28 &amp; 29 to GND for ESD</p> <p>Page32-37 : Update power circuit</p> <p>Page37 : Remove 1.2V circuit</p> <p>Page26 : Add 1000pF and 10pF total 4 PCS Location: C648 , C649, C650, C652 (between +5V_ADOand AGND).</p> <p>Page22 : CN8.8 remove +5V &amp; R540 &amp; connect to +3V (K)</p> <p>Page27 : Modify and ADD. AGND bridge (R337,R284,C459 and C472 = 0 Ohm).</p> <p>Page34 : Remove PR16L, PR163, PC156, PC159</p> <p>Page22 : Add D45-D51 for ESD</p> <p>Page28 : Change CN36.37 &amp; 38 ,CN37.37 &amp; 38 ,CN38.42 &amp; 43 from ADOGND and GND.</p>					
3A	<p>Page32 : PD9 Change footprint</p> <p>Page25 : Add EMI Spring</p> <p>Page27 : Add GND &amp; AGND bridge (R546,R540,R408)</p> <p>Page22 : Modify pin define (TV/B(CN30) connector)</p>					
F	<p>Page23 &amp; 17 : HDMI circuits modify: Add level-shifter for MXM_HDMI_DDCCLK and MXM_HDMI_DDCDATA.( Location: Q54 ,Q55 , R75, R63, R297, R410 &amp; R602) .</p>					

 PROJECT : ZD1  
Quanta Computer Inc.

Size: Document Number: Rev: 1A  
Change list

Date: Monday, May 07, 2007 Sheet: 38 of 38

DOC NO.	PROJECT MODEL :	ZD1	APPROVED BY:	DATE:	2007/ 2/15
	PART NUMBER:		DRAWING BY:	REVISION:	3A