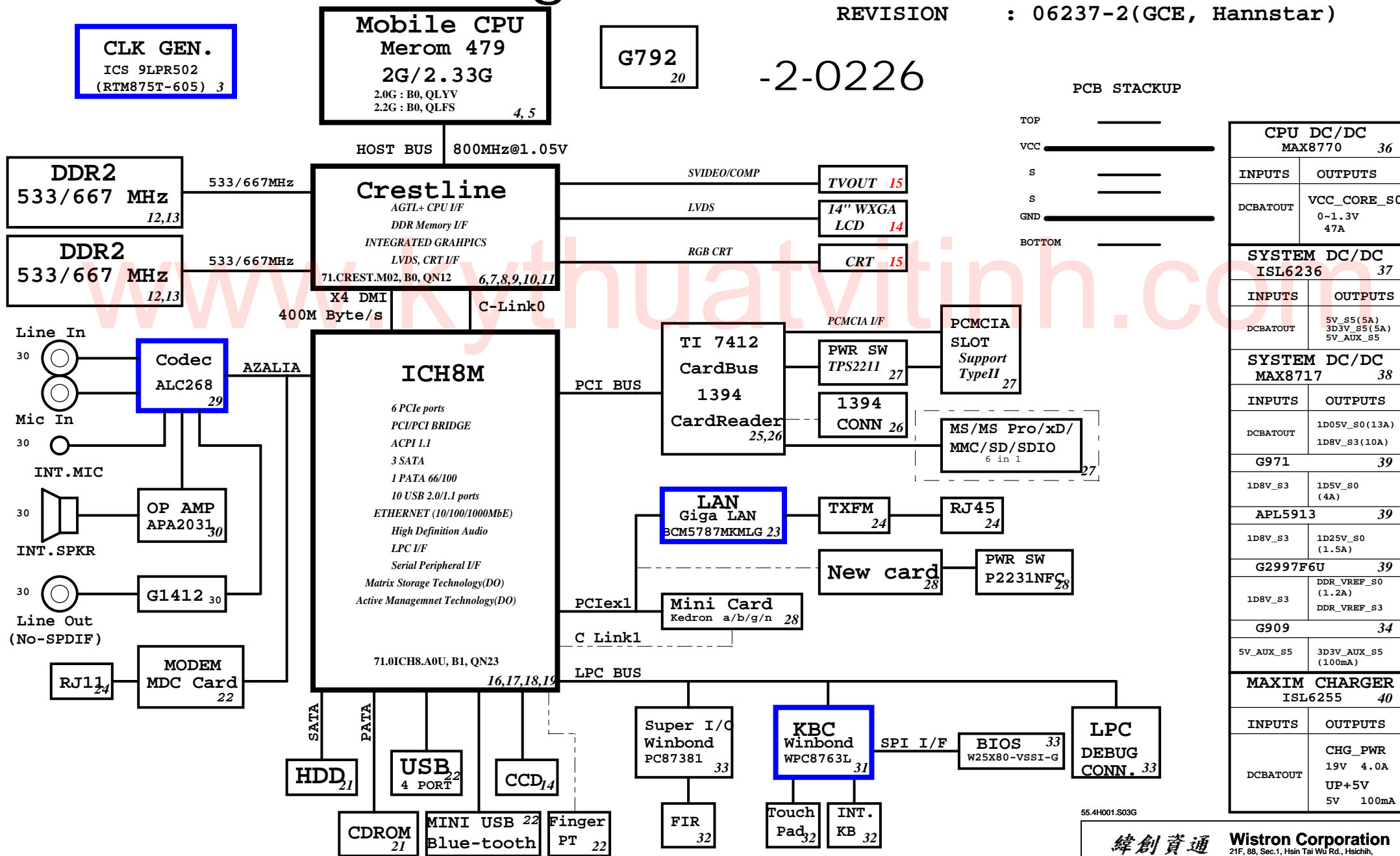


Biwa Block Diagram

Project code: 91.4H001.001
 PCB P/N : 55.4H001.XXX
 REVISION : 06237-2(GCE, Hannstar)



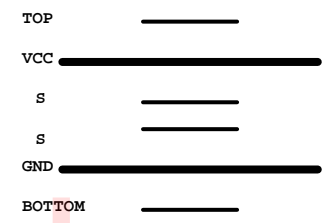
CLK GEN.
 ICS 9LPR502
 (RTM875T-605) 3

Mobile CPU
 Merom 479
 2G/2.33G
 2.0G : B0, QLYV
 2.2G : B0, QLFS
 4, 5

G792
 20

-2-0226

PCB STACKUP



CPU DC/DC MAX8770 36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0-1.3V 47A
SYSTEM DC/DC ISL6236 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A) 5V_AUX_S5
SYSTEM DC/DC MAX8717 38	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(13A) 1D8V_S3(10A)
G971 39	
1D8V_S3	1D5V_S0 (4A)
APL5913 39	
1D8V_S3	1D25V_S0 (1.5A)
G2997F6U 39	
1D8V_S3	DDR_VREF_S0 (1.2A) DDR_VREF_S3
G909 34	
5V_AUX_S5	3D3V_AUX_S5 (100mA)
MAXIM CHARGER ISL6255 40	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 19V 4.0A UP+5V 5V 100mA

55.4H001.S03G

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

Size A3 Document Number **Biwa** Rev **-2**

Date: Thursday, March 01, 2007 Sheet 1 of 42

Table with 3 columns: Signal, Usage/When Sampled, Comment. Lists various signals like HDA_SDOUT, HDA_SYNC, GNT2#, etc.

Table with 2 columns: SIGNAL, Resistor Type/Value. Lists signals like HDA_BIT_CLK, HDA_RST#, HDA_SDIN[3:0], etc.

Table with 3 columns: Pin Name, Strap Description, Configuration. Lists configurations for signals like CFG[2:0], CFG[4:3], etc.

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWOK in signal.

History

- 2007/02/16
1. Page 33: Add SIO 87381 for FIR Issue.
2. Page 31, change KBC from 8768L to 8763L.
3. Page 33, del U33(LPC golden Finger).
4. Page 24/32, change ERC1/ERC2 due to 77.61021.02L is Obsoleted Part !
5. Page 37, del TC22/TC19.
6. Page 38, del TC1/TC4.

ICH8M IDE Integrated Series Termination Resistors

Table with 2 columns: Signal, Value. Lists signals like DD[15:0], DDACK#, etc.

PCI Routing

Table with 5 columns: IDSEL, INT, REQ, GNT. Lists PCI routing details for TI7412.

USB Table

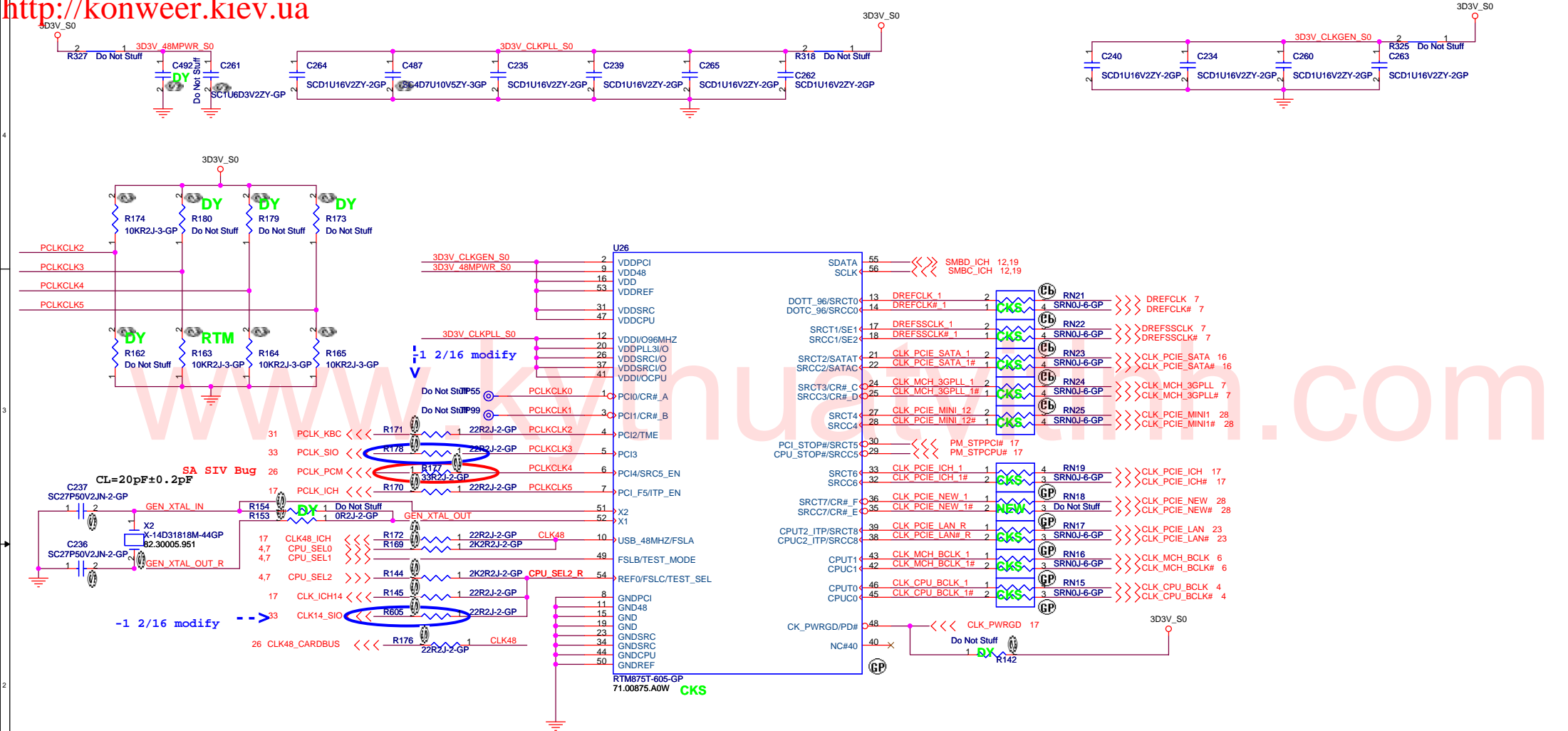
Table with 2 columns: Pair, Device. Lists USB pairs from 0 to 9.

PCIE Routing

Table with 2 columns: Lane, Device. Lists PCIE routing for LANE1, LANE2, LANE3.

55.4H001.S03G

Wistron Corporation logo and reference information including title, document number, date, and sheet number.



ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 = SRCB/SRCB# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRCB/SRCB# 1 = ITP/ITP#

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

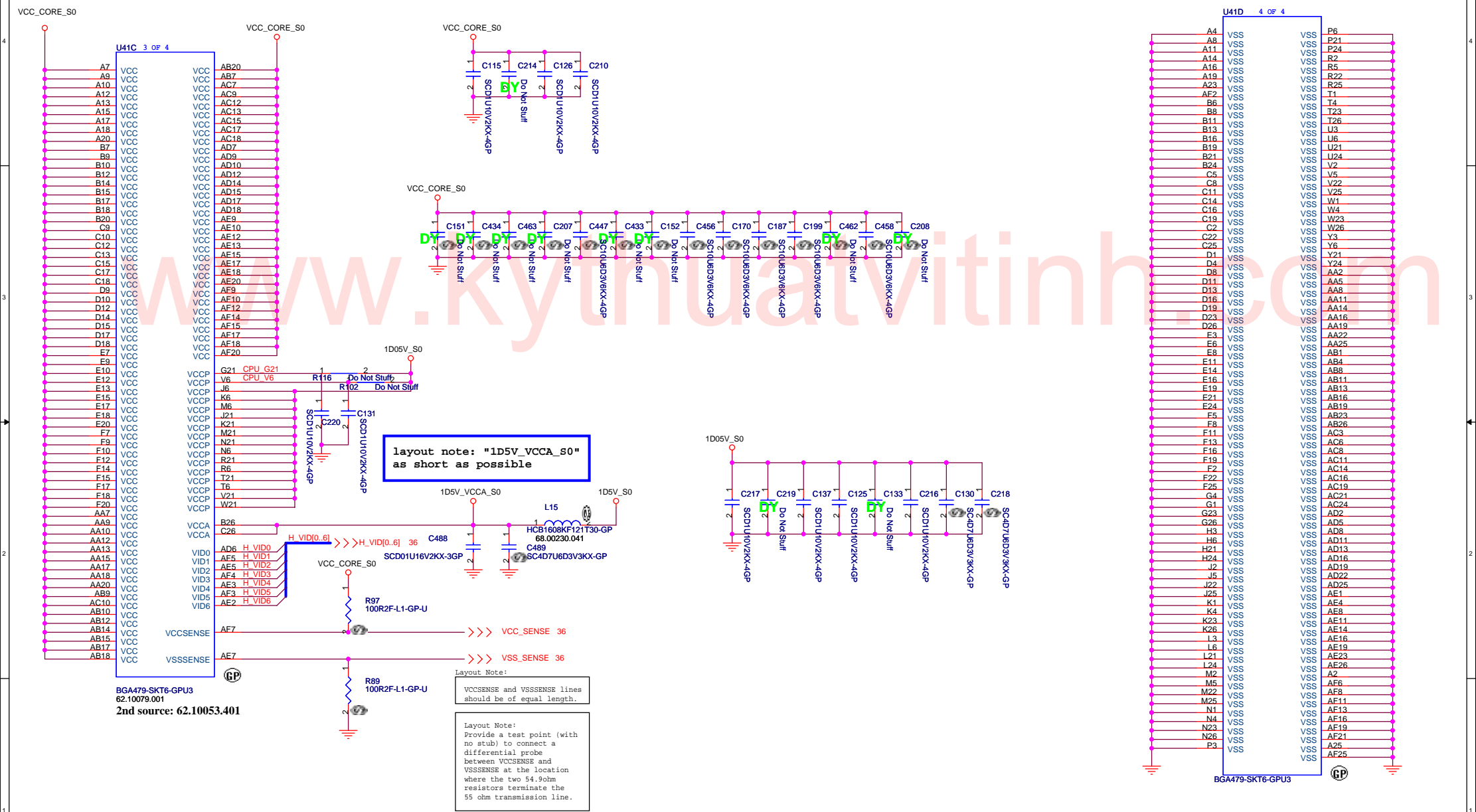
55.4H001.S03G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator**

Size: Document Number **Biwa** Rev: **-2**

Date: Thursday, March 01, 2007 Sheet 3 of 42



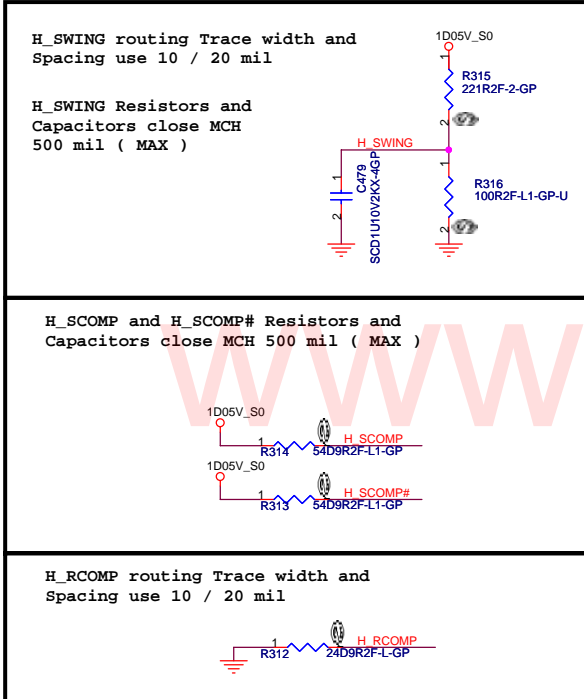
BGA479-SKT6-GPU3
 62.10079.001
 2nd source: 62.10053.401

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

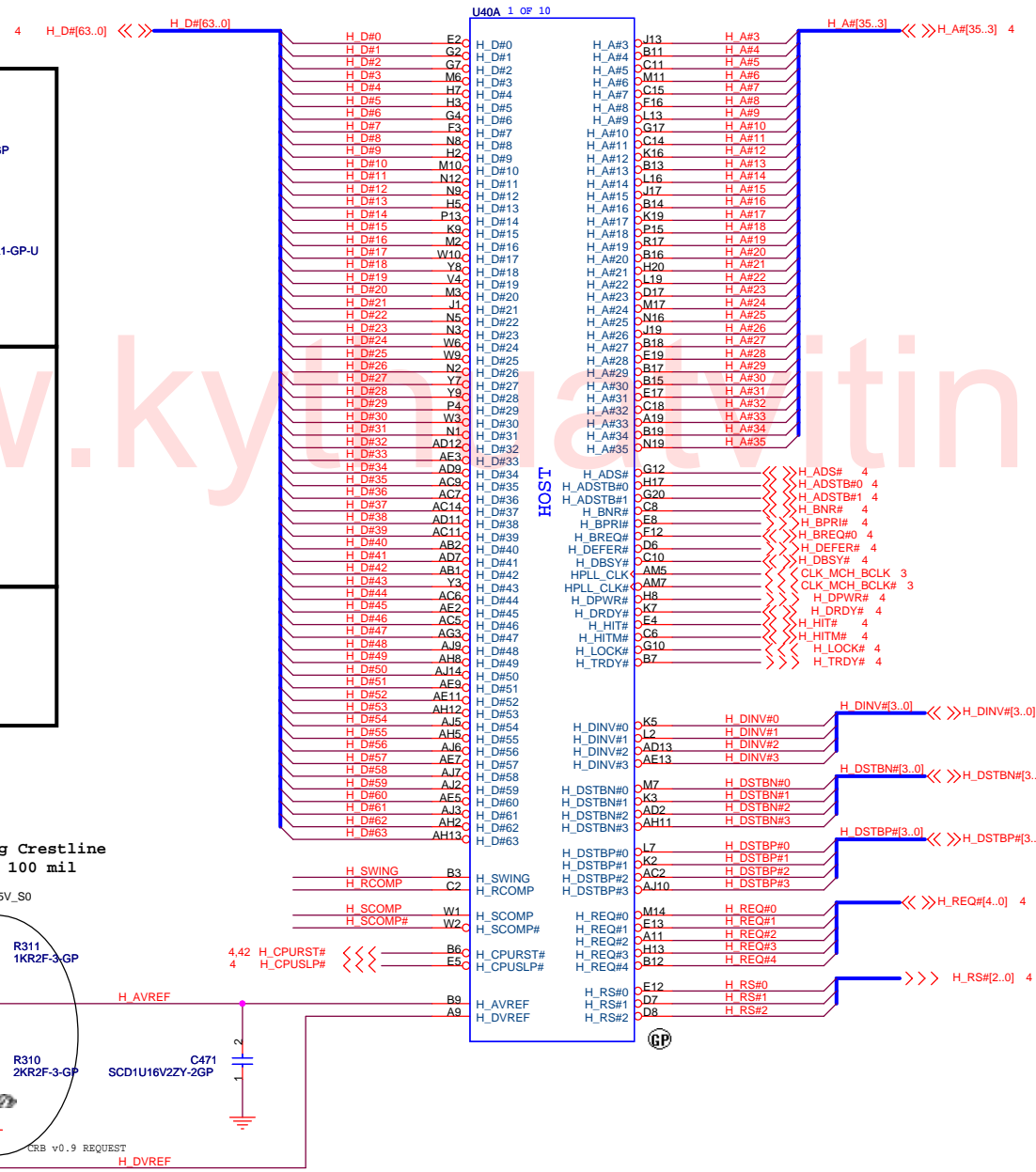
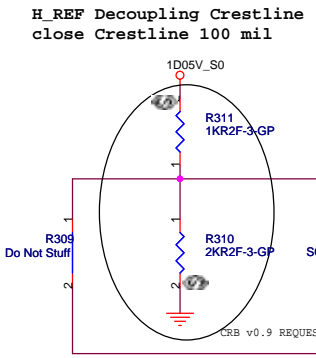
Title: **CPU (2 of 2)**

Size: Document Number: **Biwa** Rev: SA

Date: Thursday, March 01, 2007 Sheet 5 of 42



Place them near to the chip (< 0.5")



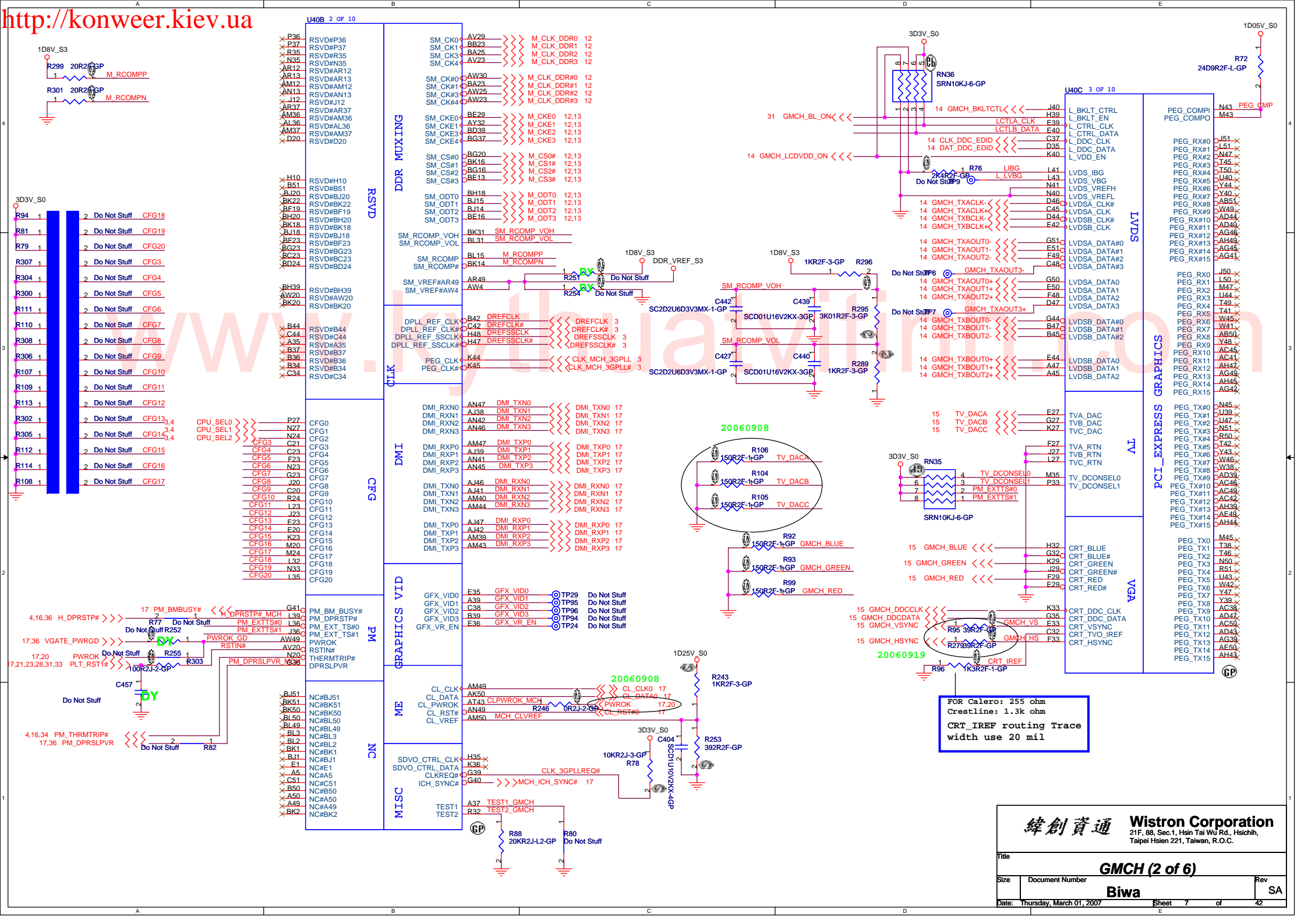
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (1 of 6)**

Size: Document Number: **Biwa** Rev: SA

Date: Thursday, March 01, 2007 Sheet 6 of 42



FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT IREF routing Trace
width use 20 mil

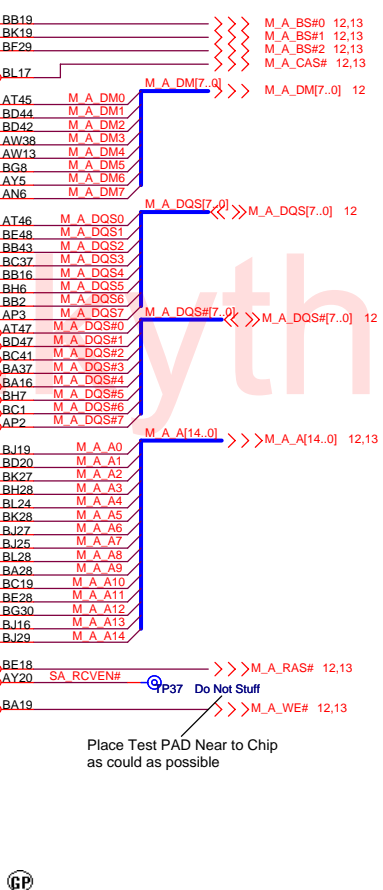
12 M_A_DQ[63..0] <<>> M_A_DQ[63..0]

U40D 4 OF 10

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M_A_DQ1	AW44	SA_DQ1
M_A_DQ2	BA45	SA_DQ2
M_A_DQ3	AY46	SA_DQ3
M_A_DQ4	AR41	SA_DQ4
M_A_DQ5	AR45	SA_DQ5
M_A_DQ6	AT42	SA_DQ6
M_A_DQ7	AW47	SA_DQ7
M_A_DQ8	BB45	SA_DQ8
M_A_DQ9	BF48	SA_DQ9
M_A_DQ10	BG47	SA_DQ10
M_A_DQ11	BH45	SA_DQ11
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M_A_DQ26	AW36	SA_DQ26
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M_A_DQ42	BD8	SA_DQ42
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M_A_DQ58	AM8	SA_DQ58
M_A_DQ59	AN10	SA_DQ59
M_A_DQ60	AT9	SA_DQ60
M_A_DQ61	AN9	SA_DQ61
M_A_DQ62	AM9	SA_DQ62
M_A_DQ63	AN11	SA_DQ63

SA_BSO	BB19	SA_BSO
SA_BS1	BK19	SA_BS1
SA_BS2	BF29	SA_BS2
SA_CAS#	BL17	SA_CAS#
SA_DM0	AT45	SA_DM0
SA_DM1	BD44	SA_DM1
SA_DM2	BD42	SA_DM2
SA_DM3	AW38	SA_DM3
SA_DM4	AW13	SA_DM4
SA_DM5	BG8	SA_DM5
SA_DM6	AY5	SA_DM6
SA_DM7	AN6	SA_DM7
SA_DQS0	AT46	SA_DQS0
SA_DQS1	BE48	SA_DQS1
SA_DQS2	BC37	SA_DQS2
SA_DQS3	BB16	SA_DQS3
SA_DQS4	BH6	SA_DQS4
SA_DQS5	BB2	SA_DQS5
SA_DQS6	AP3	SA_DQS6
SA_DQS7	AT47	SA_DQS7
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SA_DQS#7	AP2	SA_DQS#7
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SA_MA1	BD20	SA_MA1
SA_MA2	BK27	SA_MA2
SA_MA3	BH28	SA_MA3
SA_MA4	BL24	SA_MA4
SA_MA5	BK28	SA_MA5
SA_MA6	BJ27	SA_MA6
SA_MA7	BJ25	SA_MA7
SA_MA8	BL28	SA_MA8
SA_MA9	BA28	SA_MA9
SA_MA10	BC19	SA_MA10
SA_MA11	BE28	SA_MA11
SA_MA12	BC30	SA_MA12
SA_MA13	BL16	SA_MA13
SA_MA14	BJ29	SA_MA14
SA_RAS#	BE18	SA_RAS#
SA_RCVEN#	AY20	SA_RCVEN#
SA_WE#	BA19	SA_WE#

DDR SYSTEM MEMORY A



Place Test PAD Near to Chip as could as possible

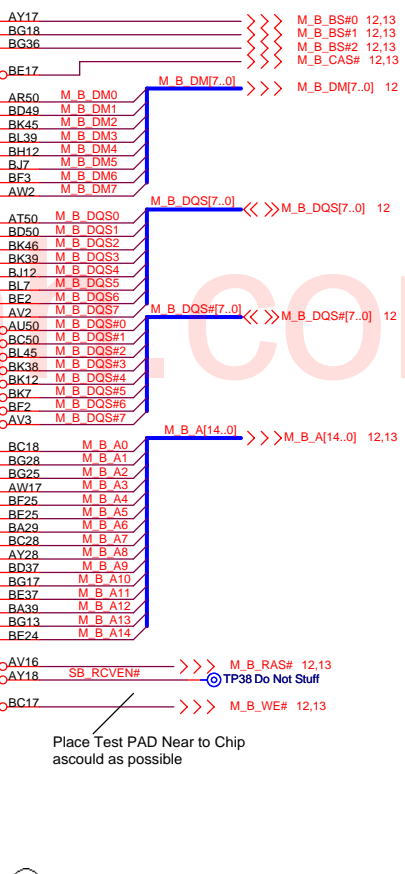
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U40E 5 OF 10

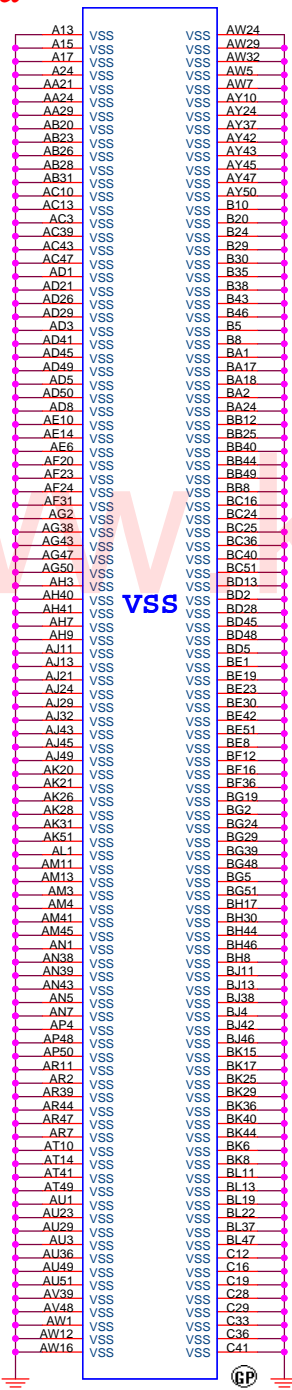
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M_B_DQ5	AN50	SB_DQ5
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M_B_DQ7	AV49	SB_DQ7
M_B_DQ8	BA50	SB_DQ8
M_B_DQ9	BB50	SB_DQ9
M_B_DQ10	BE50	SB_DQ10
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M_B_DQ12	BA51	SB_DQ12
M_B_DQ13	AY49	SB_DQ13
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M_B_DQ16	BJ50	SB_DQ16
M_B_DQ17	BJ44	SB_DQ17
M_B_DQ18	BJ43	SB_DQ18
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M_B_DQ20	BK47	SB_DQ20
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M_B_DQ23	BK43	SB_DQ23
M_B_DQ24	BJ41	SB_DQ24
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M_B_DQ38	BC12	SB_DQ38
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M_B_DQ40	BJ10	SB_DQ40
M_B_DQ41	BL9	SB_DQ41
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M_B_DQ46	BJ8	SB_DQ46
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M_B_DQ63	AT2	SB_DQ63

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SB_BS2	BG38	SB_BS2
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SB_DM7	AW2	SB_DM7
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SB_DQS2	BK46	SB_DQS2
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SB_MA8	AY28	SB_MA8
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SB_MA10	BG17	SB_MA10
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SB_MA12	BA39	SB_MA12
SB_MA13	BG13	SB_MA13
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SB_WE#	BC17	SB_WE#

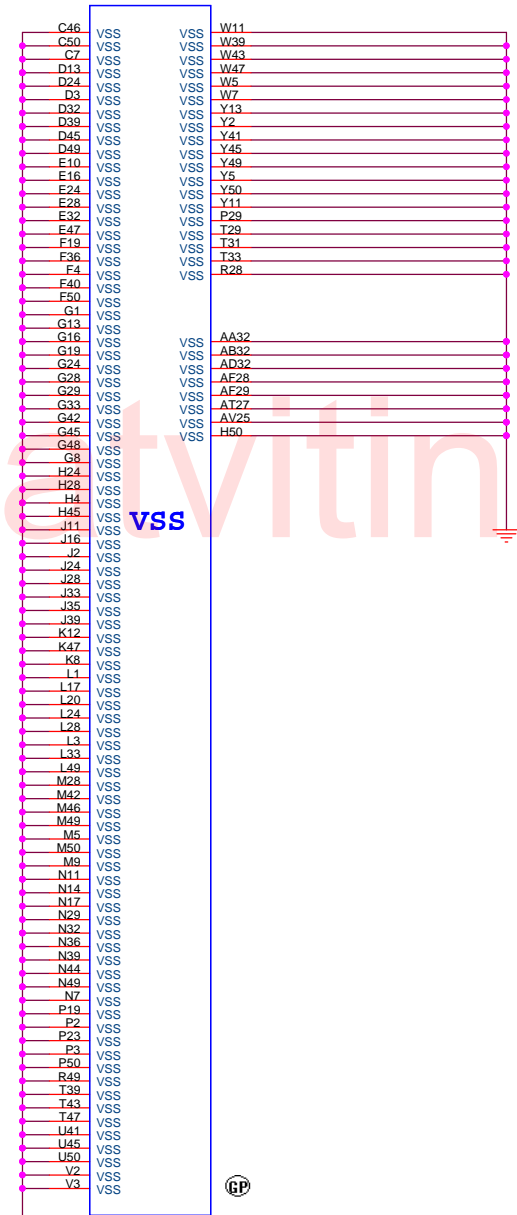
DDR SYSTEM MEMORY B



Place Test PAD Near to Chip as could as possible



VSS



VSS

www.kythuactvvinh.com

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Title: **GMCH (6 of 6)**

Size: Document Number: **Biwa** Rev: SA

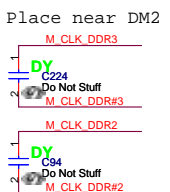
Date: Thursday, March 01, 2007 Sheet 11 of 42

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M B A1	101	A1
M B A2	100	A2
M B A3	99	A3
M B A4	98	A4
M B A5	97	A5
M B A6	94	A6
M B A7	92	A7
M B A8	93	A8
M B A9	91	A9
M B A10	105	A10/AP
M B A11	89	A11
M B A12	90	A12
M B A13	116	A13
M B A14	86	A14
M B A15	84	A15
M B A16/BA2	85	A16/BA2
M B BS0	107	BA0
M B BS1	106	BA1
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M B DQ2	17	DO2
M B DQ3	19	DO3
M B DQ4	4	DO4
M B DQ5	6	DO5
M B DQ6	14	DO6
M B DQ7	23	DO7
M B DQ8	16	DO8
M B DQ9	25	DO9
M B DQ10	35	DO10
M B DQ11	37	DO11
M B DQ12	20	DO12
M B DQ13	22	DO13
M B DQ14	36	DO14
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M B DQ18	56	DO18
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M B DQ22	56	DO22
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M B DQ45	142	DO45
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M B DQ62	192	DO62
M B DQ63	194	DO63
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M B DQS#2	49C	DO52#
M B DQS#3	68C	DO53#
M B DQS#4	129C	DO54#
M B DQS#5	148C	DO55#
M B DQS#6	167C	DO56#
M B DQS#7	186C	DO57#
M B DQSO	13	DO50
M B DQS1	31	DO51
M B DQS2	51	DO52
M B DQS3	70	DO53
M B DQS4	131	DO54
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M B DQS6	169	DO56
M B DQS7	188	DO57
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		GND
		MH1
		MH2

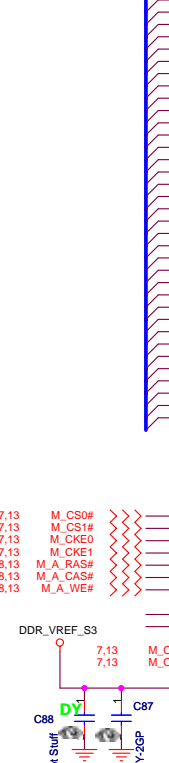
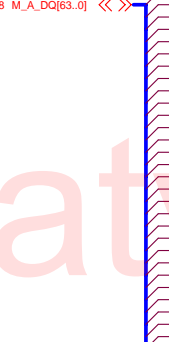
NORMAL TYPE

62.10017.A61 2nd source: 62.10017.A51 High 9.2mm

RAS#	108	M_B_RAS# 8,13
WE#	109	M_B_WE# 8,13
CAS#	113	M_B_CAS# 8,13
CS0#	110	M_CS# 7,13
CS1#	115	M_CS# 7,13
CKE0	79	M_CKE2 7,13
CKE1	80	M_CKE3 7,13
CK0	30	M_CLK_DDR2 7
CK0#	32	M_CLK_DDR#2 7
CK1	164	M_CLK_DDR3 7
CK1#	166	M_CLK_DDR#3 7
DM0	10	M_B_DM0
DM1	26	M_B_DM1
DM2	52	M_B_DM2
DM3	67	M_B_DM3
DM4	130	M_B_DM4
DM5	147	M_B_DM5
DM6	170	M_B_DM6
DM7	185	M_B_DM7
SDA	195	SMBD_I2C 3,19
SCL	197	SMBD_I2C 3,19
VDDSPD	199	
SA0	198	DDR# SA0
SA1	200	DDR# SA0
NC#50	69	X
NC#69	83	X
NC#63	120	X
NC#120	163	X
NC#163/TEST		
VDD	81	
VDD	82	
VDD	87	
VDD	88	
VDD	95	
VDD	96	
VDD	103	
VDD	104	
VDD	111	
VDD	112	
VDD	117	
VDD	118	
VSS	3	
VSS	8	
VSS	12	
VSS	15	
VSS	18	
VSS	21	
VSS	24	
VSS	27	
VSS	28	
VSS	33	
VSS	34	
VSS	39	
VSS	40	
VSS	41	
VSS	42	
VSS	47	
VSS	48	
VSS	53	
VSS	54	
VSS	59	
VSS	60	
VSS	65	
VSS	66	
VSS	71	
VSS	72	
VSS	77	
VSS	78	
VSS	121	
VSS	122	
VSS	127	
VSS	128	
VSS	132	
VSS	133	
VSS	138	
VSS	139	
VSS	144	
VSS	145	
VSS	149	
VSS	150	
VSS	155	
VSS	156	
VSS	161	
VSS	162	
VSS	165	
VSS	168	
VSS	171	
VSS	172	
VSS	177	
VSS	178	
VSS	183	
VSS	184	
VSS	187	
VSS	190	
VSS	193	
VSS	196	
GND	201	
GND		
MH1		
MH2		



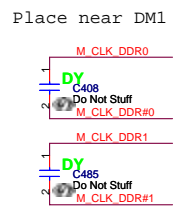
M A A0	102	A0
M A A1	101	A1
M A A2	100	A2
M A A3	99	A3
M A A4	98	A4
M A A5	97	A5
M A A6	94	A6
M A A7	92	A7
M A A8	93	A8
M A A9	91	A9
M A A10	105	A10/AP
M A A11	89	A11
M A A12	90	A12
M A A13	116	A13
M A A14	86	A14
M A A15	84	A15
M A A16/BA2	85	A16/BA2
M A BS#0	107	BA0
M A BS#1	106	BA1
M A DQ0	5	DO0
M A DQ1	7	DO1
M A DQ2	17	DO2
M A DQ3	19	DO3
M A DQ4	4	DO4
M A DQ5	6	DO5
M A DQ6	14	DO6
M A DQ7	23	DO7
M A DQ8	16	DO8
M A DQ9	25	DO9
M A DQ10	35	DO10
M A DQ11	37	DO11
M A DQ12	20	DO12
M A DQ13	22	DO13
M A DQ14	36	DO14
M A DQ15	38	DO15
M A DQ16	43	DO16
M A DQ17	45	DO17
M A DQ18	56	DO18
M A DQ19	57	DO19
M A DQ20	44	DO20
M A DQ21	46	DO21
M A DQ22	56	DO22
M A DQ23	58	DO23
M A DQ24	63	DO24
M A DQ25	61	DO25
M A DQ26	73	DO26
M A DQ27	75	DO27
M A DQ28	62	DO28
M A DQ29	64	DO29
M A DQ30	74	DO30
M A DQ31	76	DO31
M A DQ32	123	DO32
M A DQ33	125	DO33
M A DQ34	135	DO34
M A DQ35	137	DO35
M A DQ36	124	DO36
M A DQ37	126	DO37
M A DQ38	134	DO38
M A DQ39	136	DO39
M A DQ40	141	DO40
M A DQ41	143	DO41
M A DQ42	151	DO42
M A DQ43	153	DO43
M A DQ44	140	DO44
M A DQ45	142	DO45
M A DQ46	152	DO46
M A DQ47	154	DO47
M A DQ48	157	DO48
M A DQ49	159	DO49
M A DQ50	173	DO50
M A DQ51	175	DO51
M A DQ52	158	DO52
M A DQ53	160	DO53
M A DQ54	174	DO54
M A DQ55	176	DO55
M A DQ56	179	DO56
M A DQ57	181	DO57
M A DQ58	189	DO58
M A DQ59	191	DO59
M A DQ60	180	DO60
M A DQ61	182	DO61
M A DQ62	192	DO62
M A DQ63	194	DO63
M A DQS#0	111	DO50#
M A DQS#1	29C	DO51#
M A DQS#2	49C	DO52#
M A DQS#3	68C	DO53#
M A DQS#4	129C	DO54#
M A DQS#5	148C	DO55#
M A DQS#6	167C	DO56#
M A DQS#7	186C	DO57#
M A DQSO	13	DO50
M A DQS1	31	DO51
M A DQS2	51	DO52
M A DQS3	70	DO53
M A DQS4	131	DO54
M A DQS5	148	DO55
M A DQS6	169	DO56
M A DQS7	188	DO57
DDR_VREF_S3	7,13	OTD0
	7,13	OTD1
		VREF
		VSS
		GND
		MH1
		MH2



NORMAL TYPE

62.10017.661 High 5.2mm 2nd source: 62.10017.A41

MH1	MH2	MH2
DQS0	13	M A DQS0
DQS1	31	M A DQS1
DQS2	51	M A DQS2
DQS3	70	M A DQS3
DQS4	131	M A DQS4
DQS5	148	M A DQS5
DQS6	169	M A DQS6
DQS7	188	M A DQS7
DQS#0	111	M A DQS#0
DQS#1	29	M A DQS#1
DQS#2	49	M A DQS#2
DQS#3	68	M A DQS#3
DQS#4	129	M A DQS#4
DQS#5	148	M A DQS#5
DQS#6	167	M A DQS#6
DQS#7	186	M A DQS#7
DM0	10	M A DM0
DM1	26	M A DM1
DM2	52	M A DM2
DM3	67	M A DM3
DM4	130	M A DM4
DM5	147	M A DM5
DM6	170	M A DM6
DM7	185	M A DM7
CK0	30	M_CLK_DDR0 7
CK0#	32	M_CLK_DDR#0 7
CK1	164	M_CLK_DDR1 7
CK1#	166	M_CLK_DDR#1 7
SA0	198	
SA1	200	
VDD	81	
VDD	82	
VDD	87	
VDD	88	
VDD	95	
VDD	96	
VDD	103	
VDD	104	
VDD	111	
VDD	112	
VDD	117	
VDD	118	
VSS	2	
VSS	3	
VSS	8	
VSS	9	
VSS	12	
VSS	15	
VSS	18	
VSS	21	
VSS	24	
VSS	27	
VSS	28	
VSS	33	
VSS	34	
VSS	39	
VSS	40	
VSS	41	
VSS	42	
VSS	47	
VSS	48	
VSS	53	
VSS	54	
VSS	59	
VSS	60	
VSS	65	
VSS	66	
VSS	71	
VSS	72	
VSS	77	
VSS	78	
VSS	121	
VSS	122	
VSS	127	
VSS	128	
VSS	132	
VSS	133	
VSS	138	
VSS	139	
VSS	144	
VSS	145	
VSS	149	
VSS	150	
VSS	155	
VSS	156	
VSS	161	
VSS	162	
VSS	165	
VSS	168	
VSS	171	
VSS	172	
VSS	177	
VSS	178	
VSS	183	
VSS	184	
VSS	187	
VSS	190	
VSS	193	
VSS	196	
GND	201	
GND		
MH1		
MH2		



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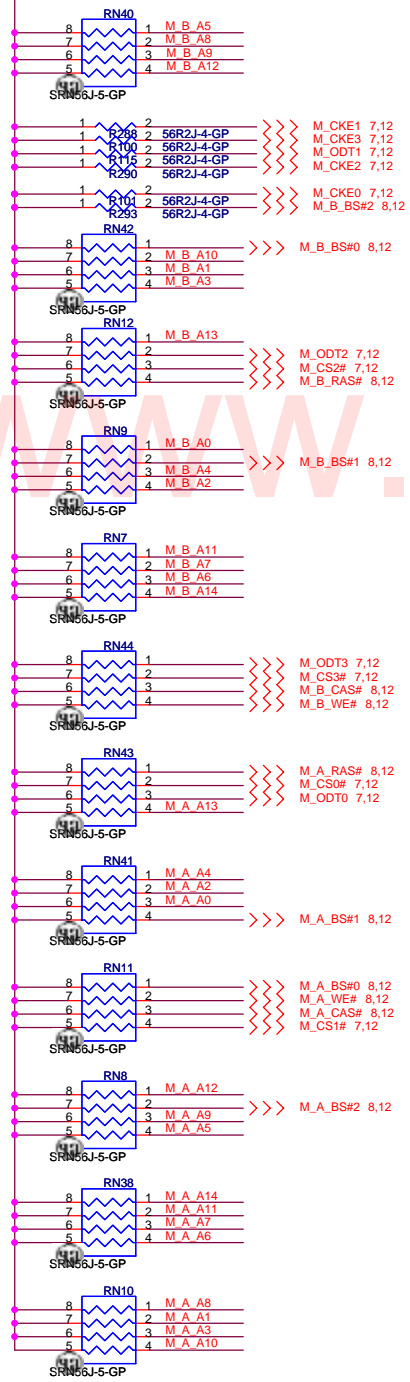
DDR2 Socket

Biwa

Thursday, March 01, 2007

PARALLEL TERMINATION

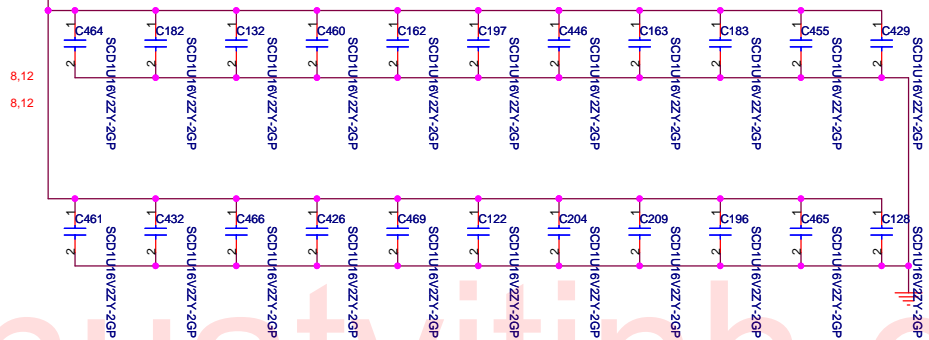
DDR_VREF_S0 Put decap near power(0.9V) and pull-up resistor



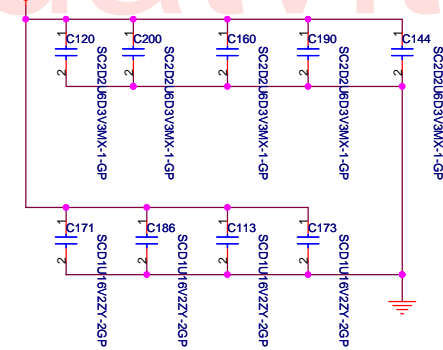
M_A A[14..0] <<> M_A_A[14..0] 8,12
 M_B A[14..0] <<> M_B_B_A[14..0] 8,12

Decoupling Capacitor

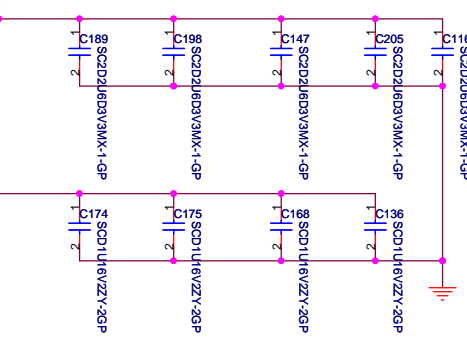
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



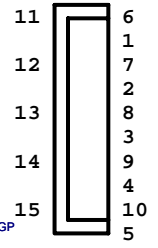
緯創資通 Wistron Corporation
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Title: **DDR2 Termination Resistor**

Size: Document Number **Biwa** Rev **SB**

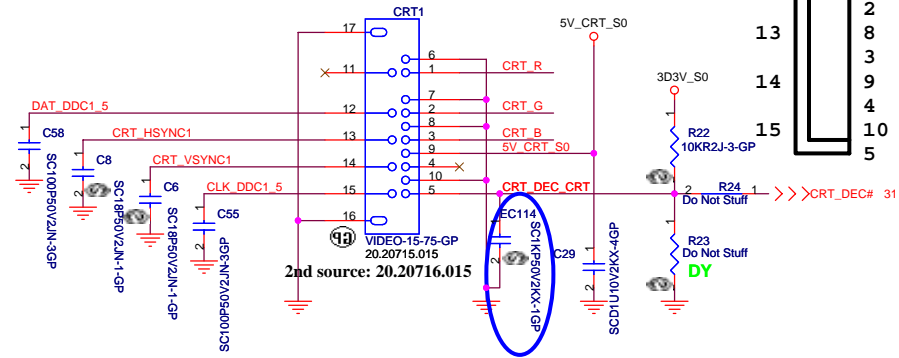
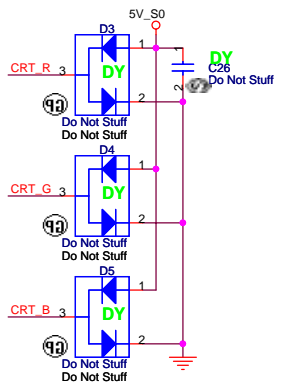
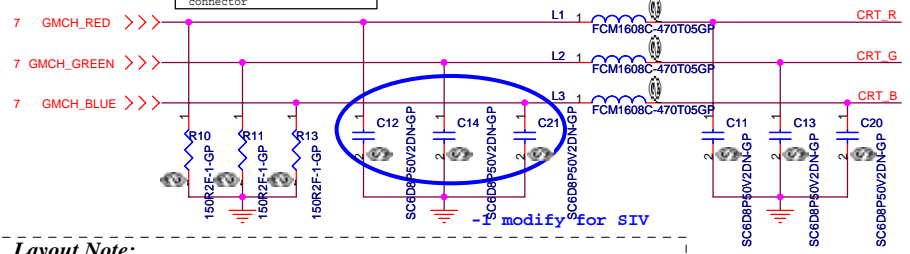
Date: Thursday, March 01, 2007 Sheet 13 of 42

CRT I/F & CONNECTOR



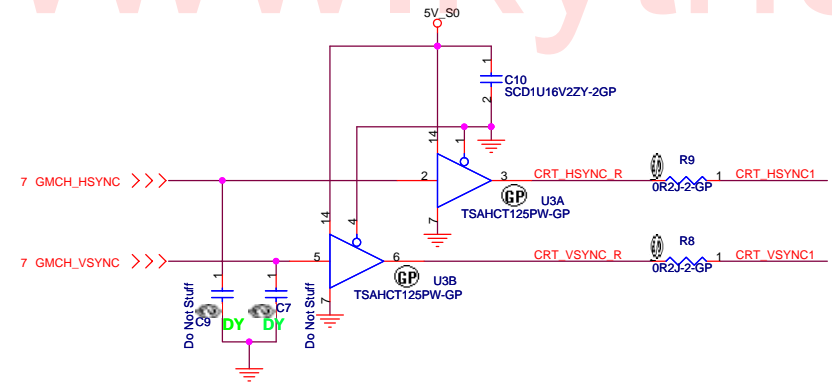
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 47 ohm@100MHz;

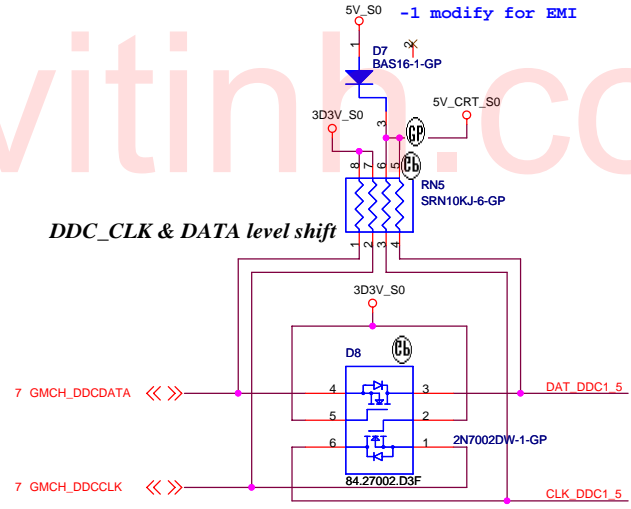


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

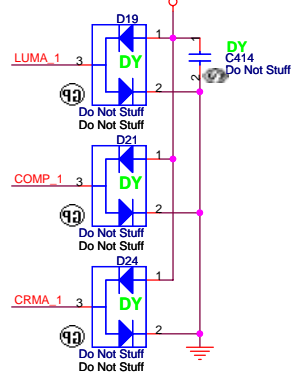
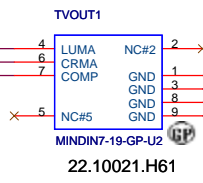
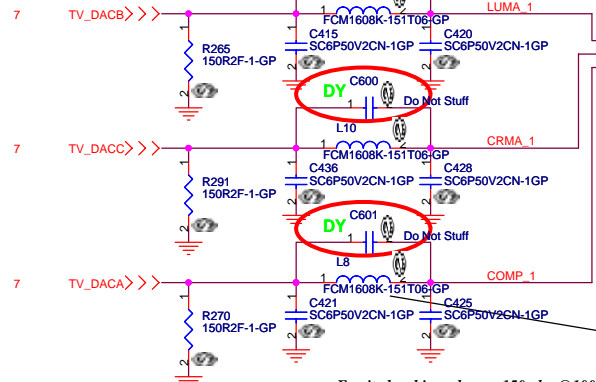


DDC_CLK & DATA level shift



TV CONN

SB modify for SIV



Ferrite bead impedance: 150 ohm@100MHz; 100mA(min) design recommend

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Title: CRT/TV Connector

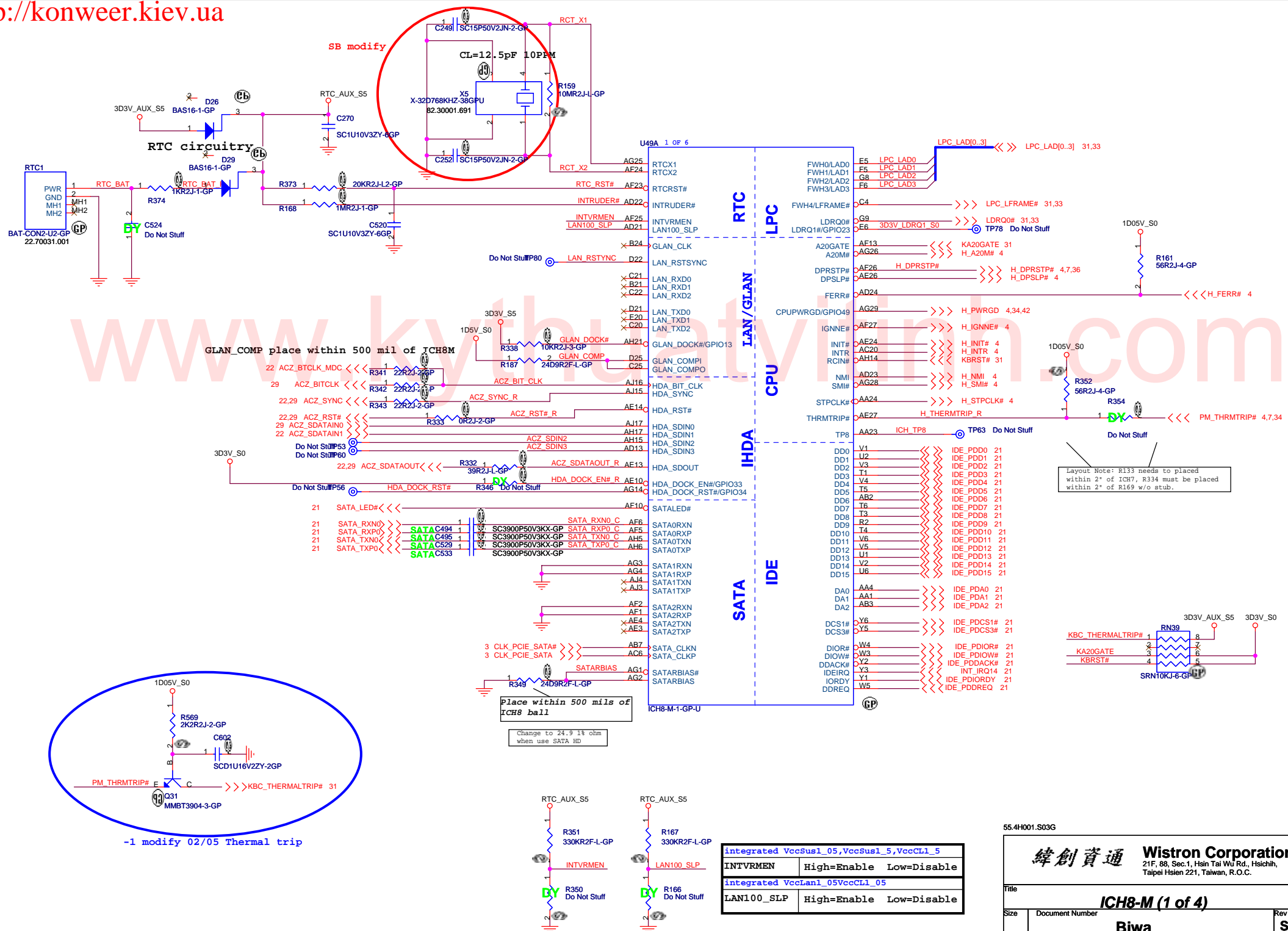
Size: Document Number

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Rev -1

Biwa



55.4H001.S03G

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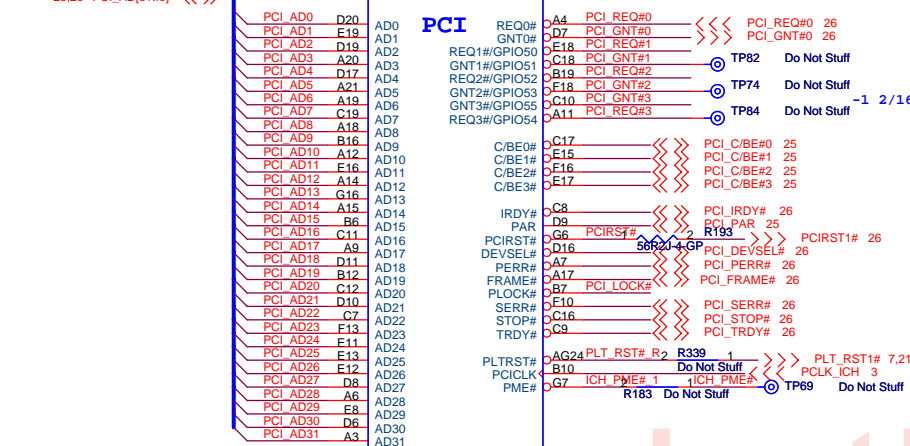
Title: **ICH8-M (1 of 4)**

Size: Document Number Rev: **SB**

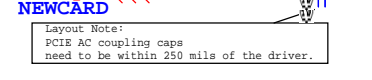
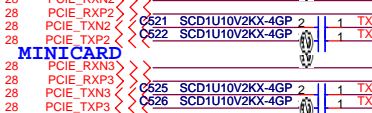
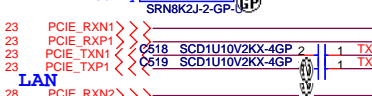
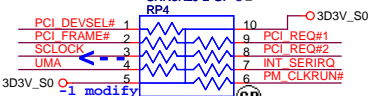
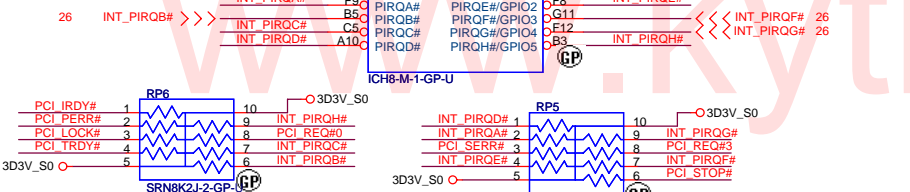
Date: Thursday, March 01, 2007 Sheet 16 of 42

25,26 PCI_AD[31..0] <<>

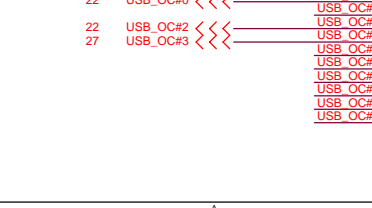
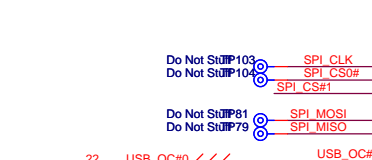
U49C 0F 6



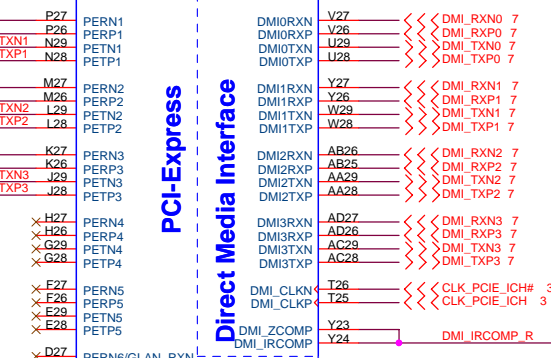
Interrupt I/F



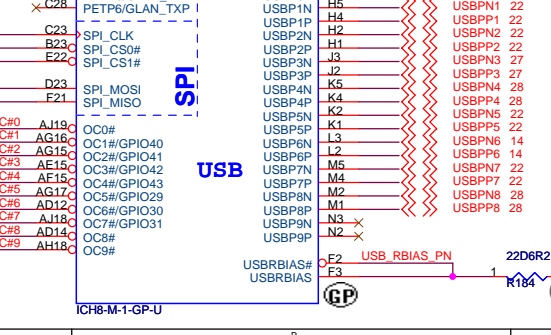
Layout Note: PCIE AC coupling caps need to be within 250 mils of the driver.



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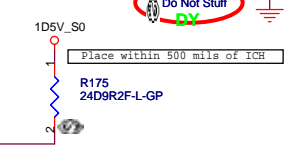
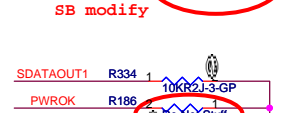
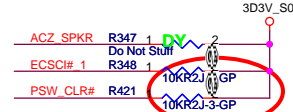


Direct Media Interface



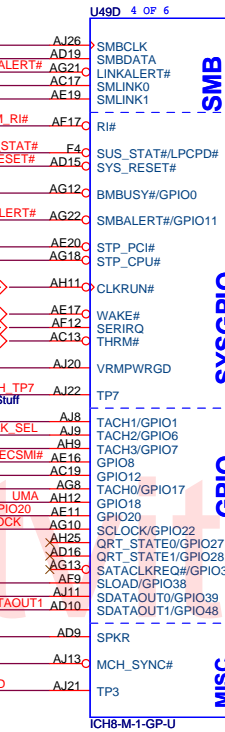
No Reboot Strap

SPKR LOW = Default
 HIGH = No Reboot

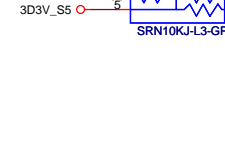
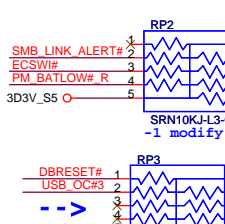


USB

Pair	Device
0	USB1
1	USB2
2	USB3
3	USB4 (Bd)
5	BT
6	CCD
7	Finger
8	New
9	NC

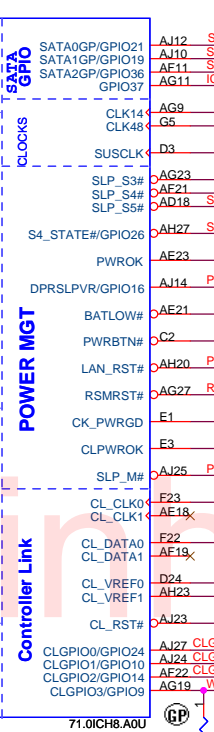
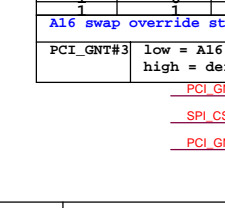


Controller Link

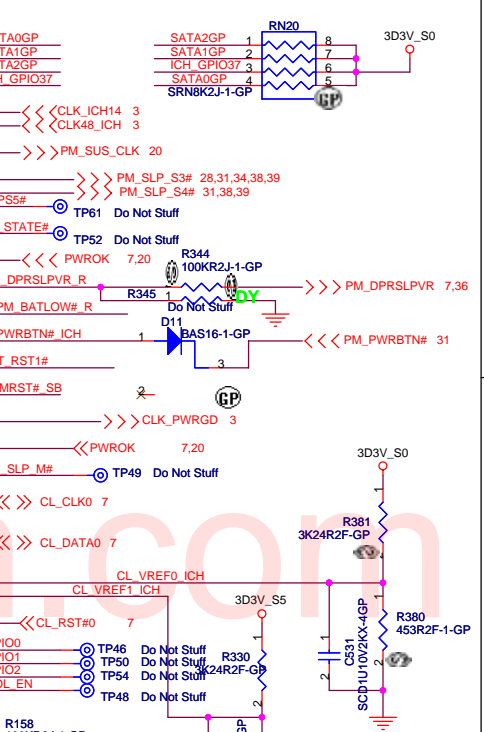
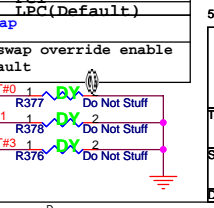
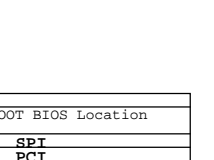
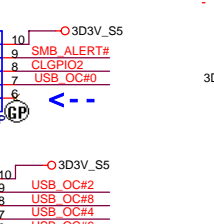


BOOT BIOS Strap

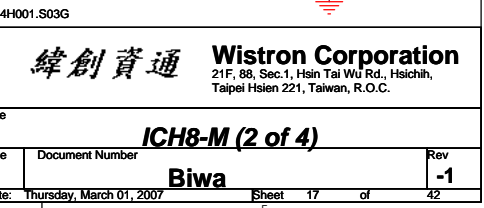
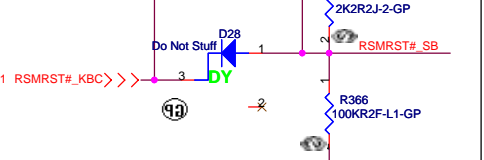
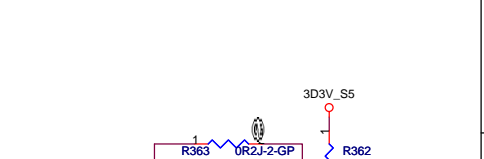
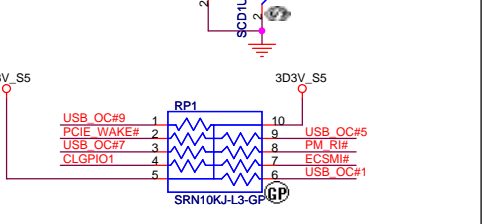
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCI
1	1	LPC (Default)



POWER MGT



POWER MGT

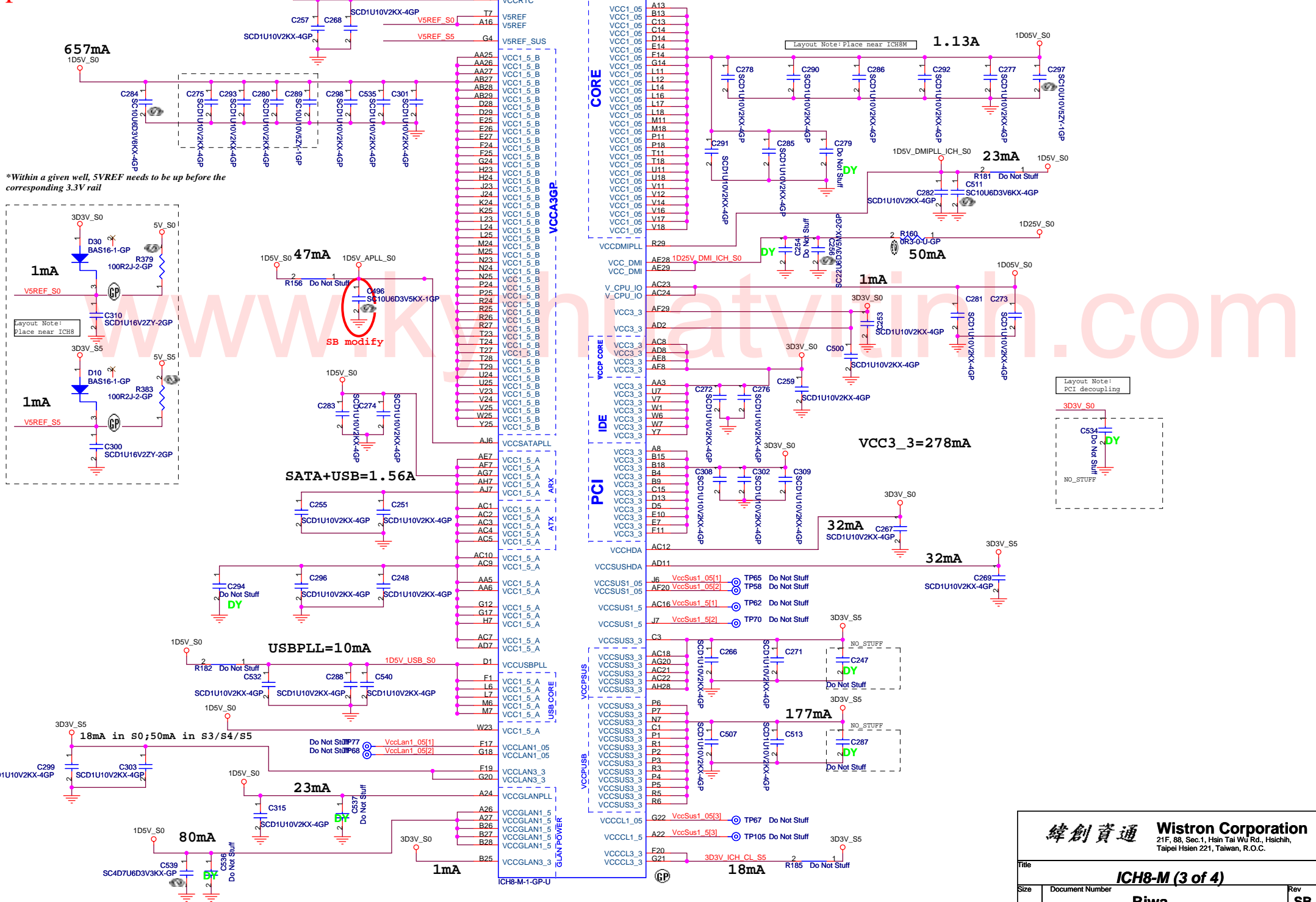


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File: **ICH8-M (3 of 4)**

Size: Document Number: **Biwa** Rev: **SB**

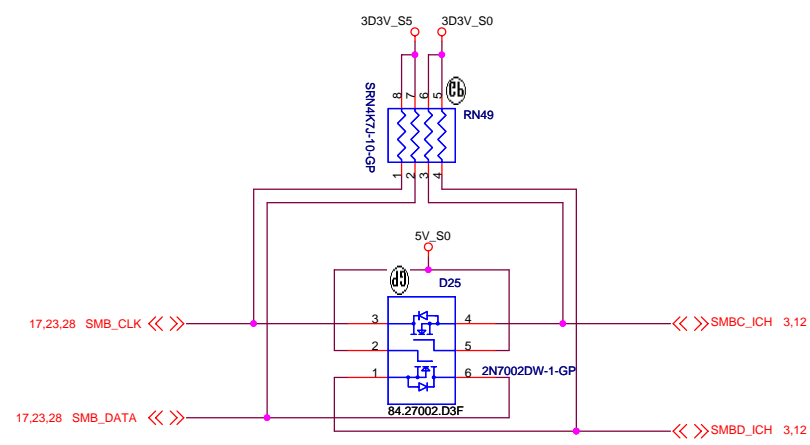
Date: Thursday, March 01, 2007 Sheet 18 of 42

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A23	VSS	K7
A5	VSS	L1
AA2	VSS	L13
AA7	VSS	L15
A25	VSS	L26
AB1	VSS	L27
AB24	VSS	L4
AC11	VSS	L5
AC14	VSS	M12
AC25	VSS	M13
AC26	VSS	M14
AC27	VSS	M15
AD17	VSS	M16
AD20	VSS	M17
AD28	VSS	M23
AD29	VSS	M28
AD3	VSS	M29
AD4	VSS	M3
AD6	VSS	N1
AE1	VSS	N11
AE12	VSS	N12
AE2	VSS	N13
AE22	VSS	N14
AD1	VSS	N15
AE25	VSS	N16
AE5	VSS	N17
AE6	VSS	N18
AE9	VSS	N26
AF14	VSS	N27
AF16	VSS	N4
AF18	VSS	N5
AF3	VSS	N6
AF4	VSS	P12
AG5	VSS	P13
AG6	VSS	P14
AH10	VSS	P15
AH13	VSS	P16
AH16	VSS	P17
AH19	VSS	P23
AH2	VSS	P28
AE28	VSS	P29
AH22	VSS	R11
AH24	VSS	R12
AH26	VSS	R13
AH3	VSS	R14
AH4	VSS	R15
AH8	VSS	R16
AJ5	VSS	R17
B11	VSS	R18
B14	VSS	R28
B17	VSS	R4
B2	VSS	T12
B20	VSS	T13
B22	VSS	T14
B3	VSS	T15
C24	VSS	T16
C26	VSS	T17
C27	VSS	T2
C6	VSS	U12
D12	VSS	U13
D15	VSS	U14
D18	VSS	U15
D2	VSS	U16
D4	VSS	U17
E21	VSS	U23
E24	VSS	U26
E4	VSS	U27
E9	VSS	U3
F15	VSS	U5
E23	VSS	V13
F28	VSS	V15
F29	VSS	V28
F7	VSS	V29
G1	VSS	W2
F2	VSS	W26
G10	VSS	W27
G13	VSS	Y28
G19	VSS	Y29
G23	VSS	Y4
G25	VSS	AB4
G26	VSS	AB23
G27	VSS	AB5
H25	VSS	AB6
H28	VSS	AD5
H29	VSS	U4
H3	VSS	W24
H6	VSS	A1
J1	VSS	A2
J25	VSS_NCTF	A28
J26	VSS_NCTF	A29
J27	VSS_NCTF	AJ28
J4	VSS_NCTF	AH1
J5	VSS_NCTF	AH29
K23	VSS_NCTF	AJ1
K28	VSS_NCTF	AJ2
K29	VSS_NCTF	AJ29
K3	VSS_NCTF	B1
K6	VSS_NCTF	B29
	VSS_NCTF	A1
	VSS_NCTF	A2
	VSS_NCTF	A28
	VSS_NCTF	A29
	VSS_NCTF	AJ28
	VSS_NCTF	AH1
	VSS_NCTF	AH29
	VSS_NCTF	AJ1
	VSS_NCTF	AJ2
	VSS_NCTF	AJ29
	VSS_NCTF	B1
	VSS_NCTF	B29

ICH8-M-1-GP-U

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D55 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

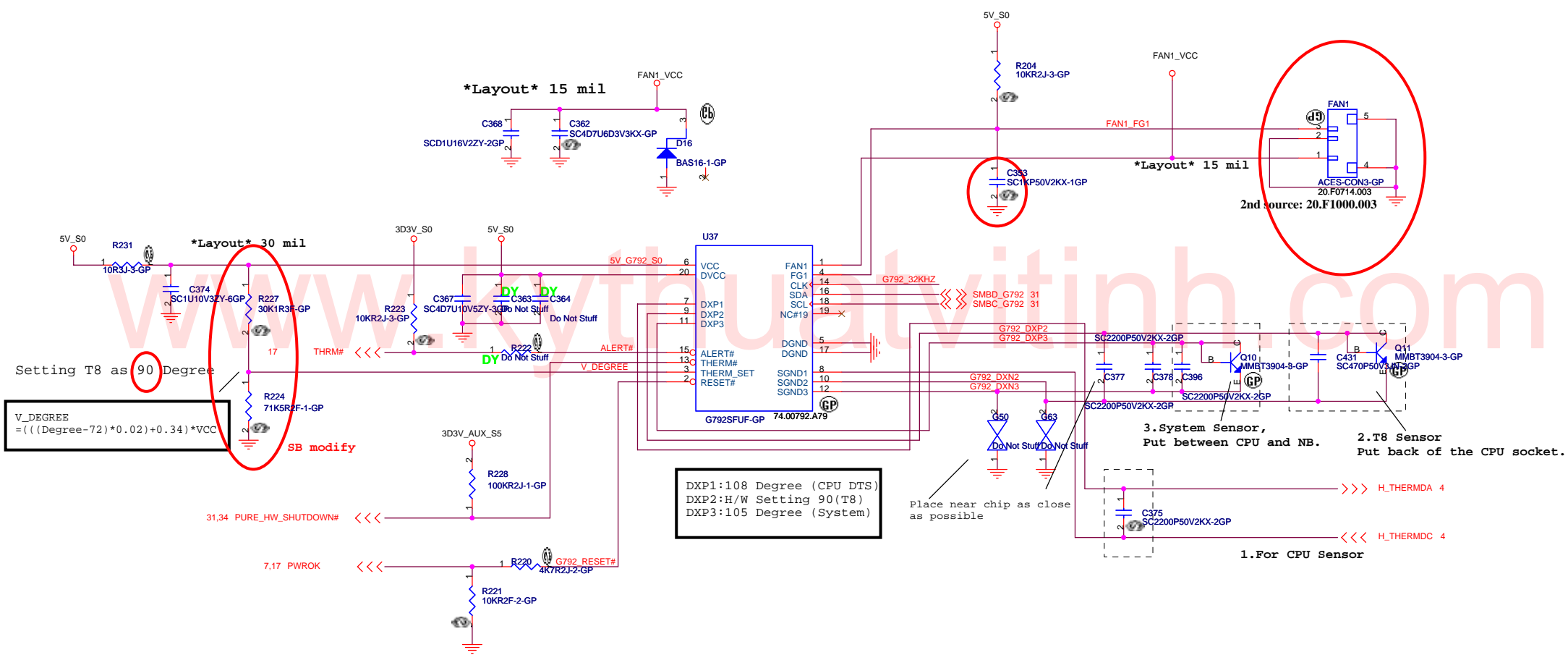
SMBUS

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Title: **ICH8-M (4 of 4)**

Size: Document Number: **Biwa** Rev: SA

Date: Thursday, March 01, 2007 Sheet 19 of 42



V_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC

DXP1:108 Degree (CPU DTS)
DXP2:H/W Setting 90(T8)
DXP3:105 Degree (System)

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

Biwa Thermal Table 1106

		T6	T7
Sensor 0	CPU DTS	100	102
Sensor 1	CPU G792 Analog	110	113
Sensor 2	System G792	85	87
Sensor 3	T8		
Sensor 4	ADIA status		

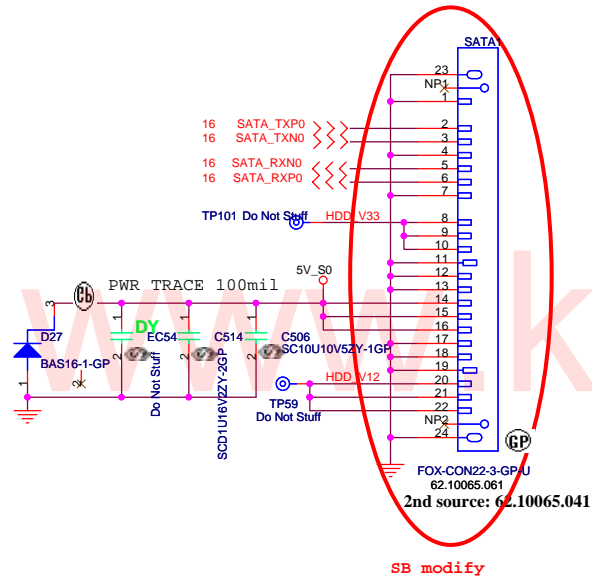
緯創資通 Wistron Corporation
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Title: **Thermal/Fan Controller**

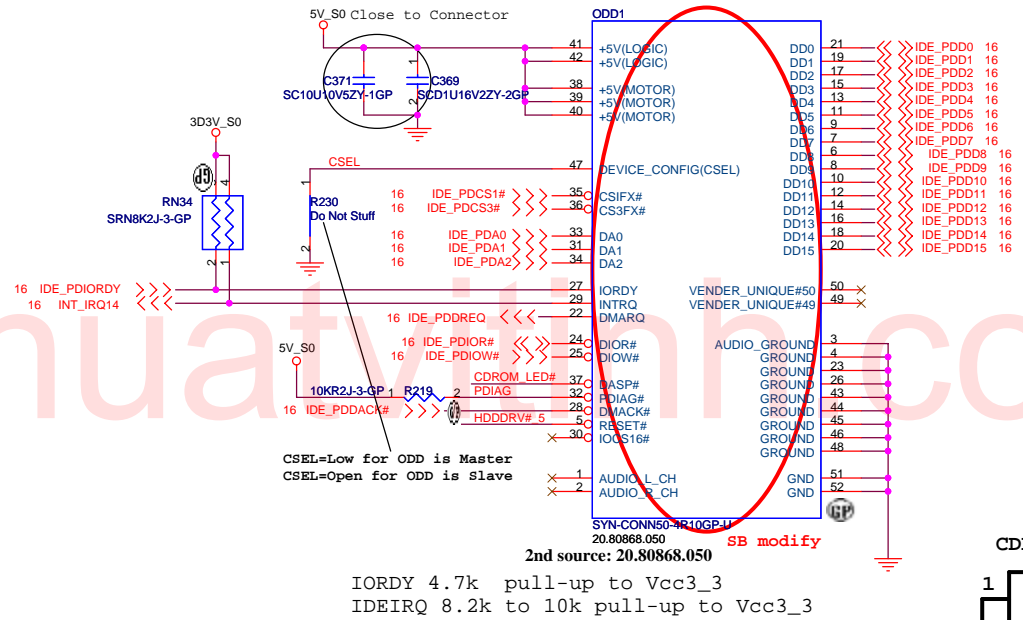
Size: Document Number: **Biwa** Rev: **SB**

Date: Thursday, March 01, 2007 Sheet 20 of 42

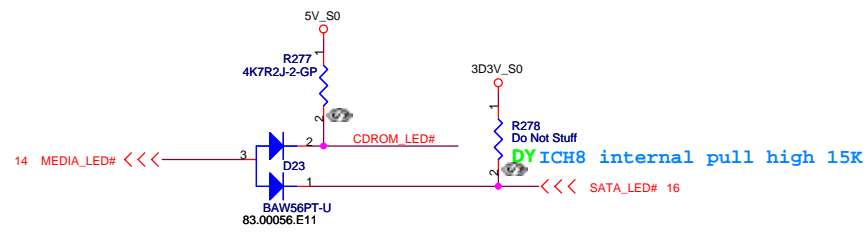
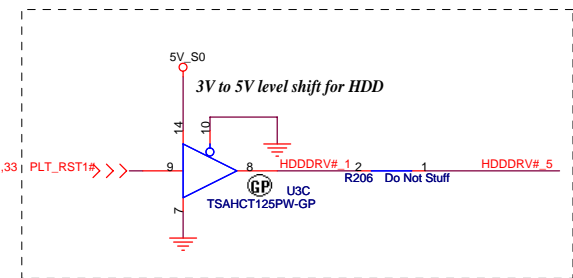
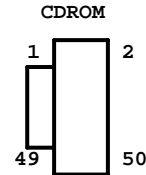
SATA Connector



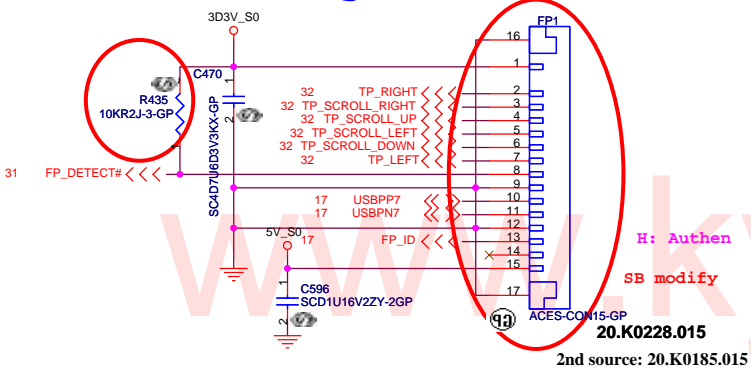
ODD Connector



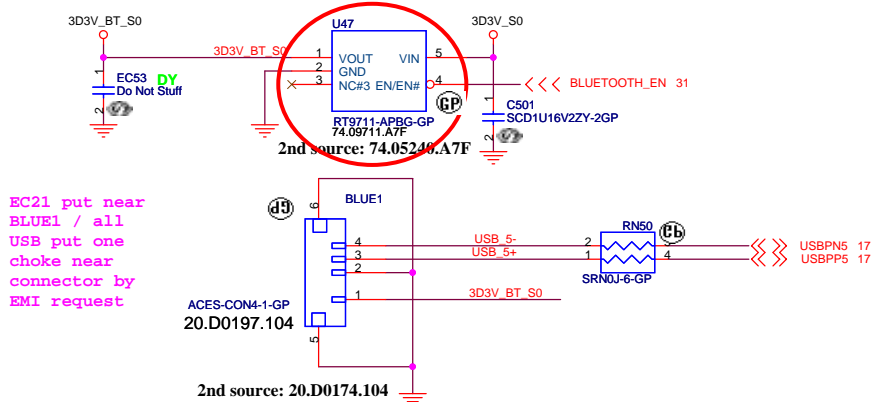
IORDY 4.7k pull-up to Vcc3_3
 IDEIRQ 8.2k to 10k pull-up to Vcc3_3



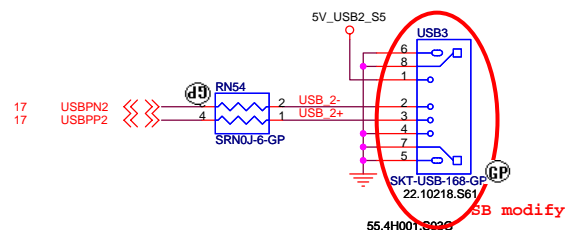
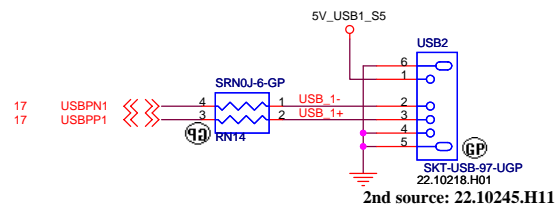
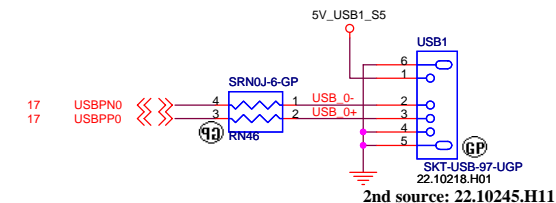
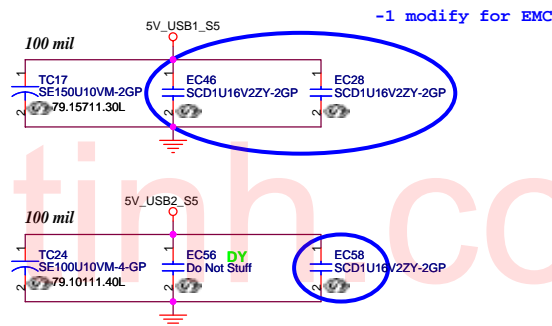
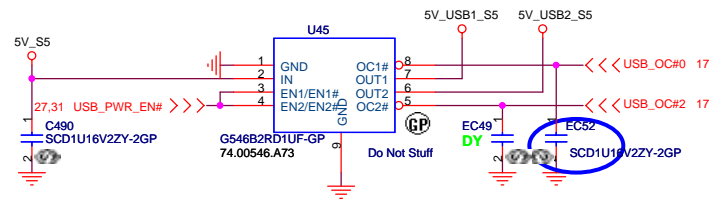
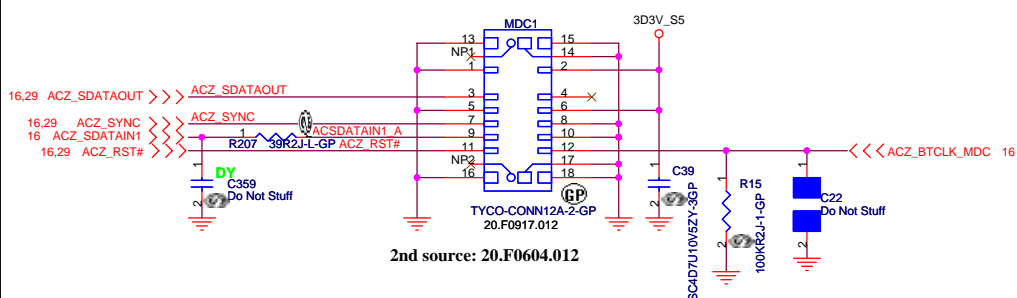
Finger Print



BLUETOOTH MODULE



MDC 1.5 CONN



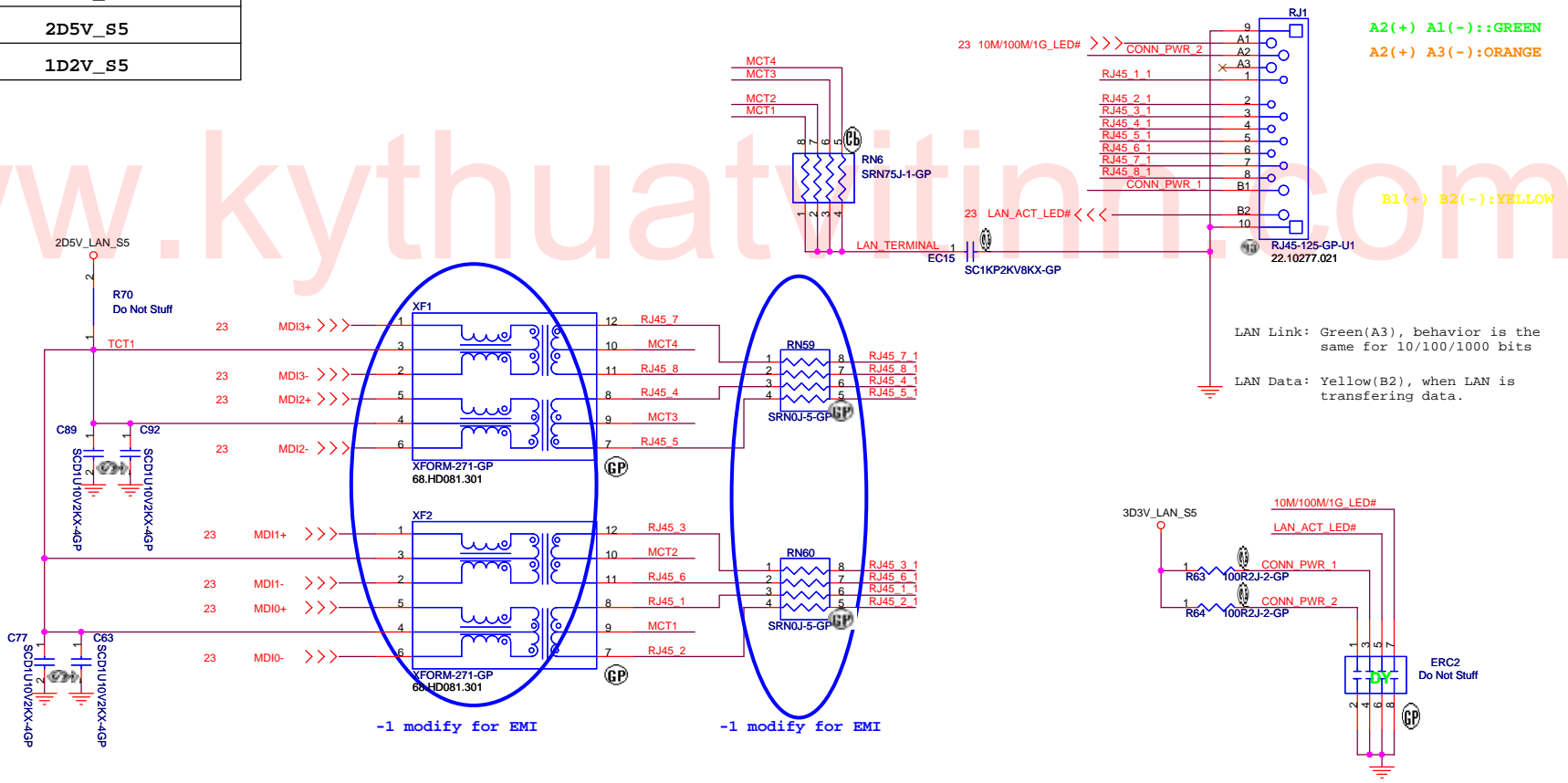
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector

LED COLOR

A2(+) A1(-)::GREEN
A2(+) A3(-):ORANGE

B1(+) B2(-):YELLOW



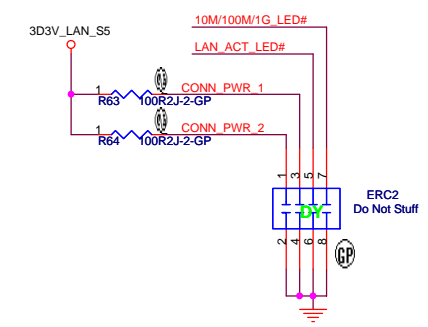
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

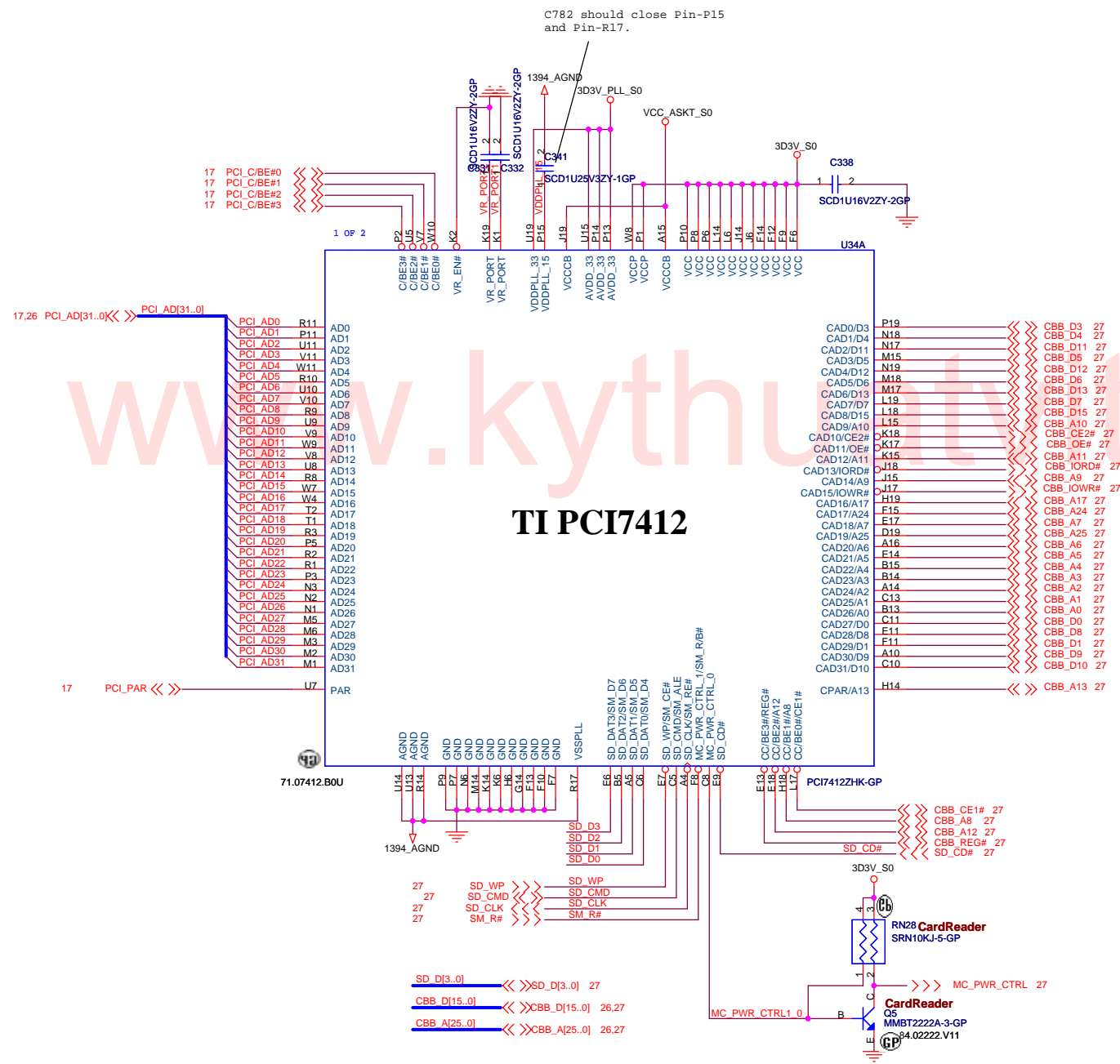


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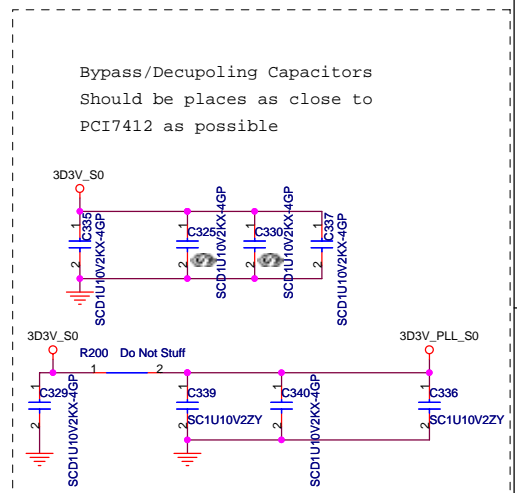
Title LAN Connector		
Size A3	Document Number Biwa	Rev -1
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C782 should close Pin-P15 and Pin-R17.

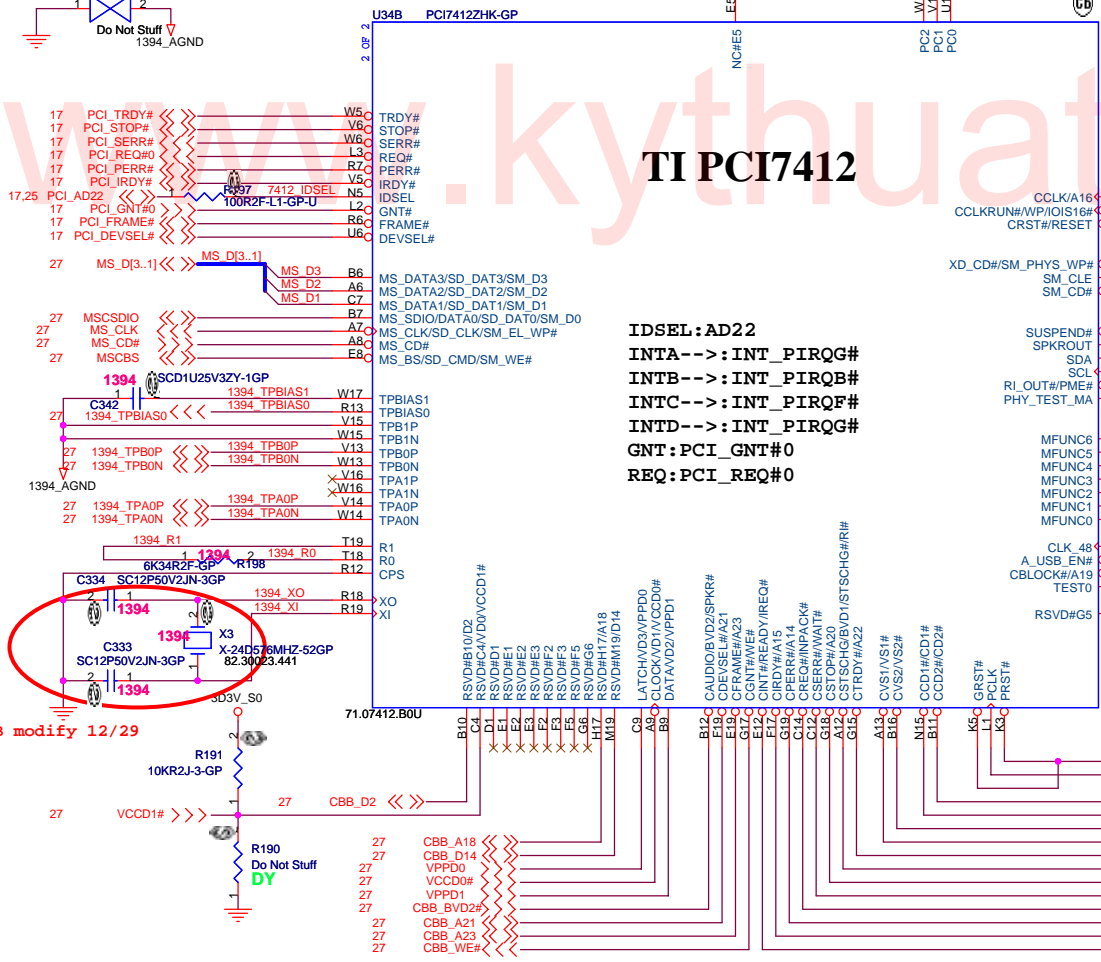
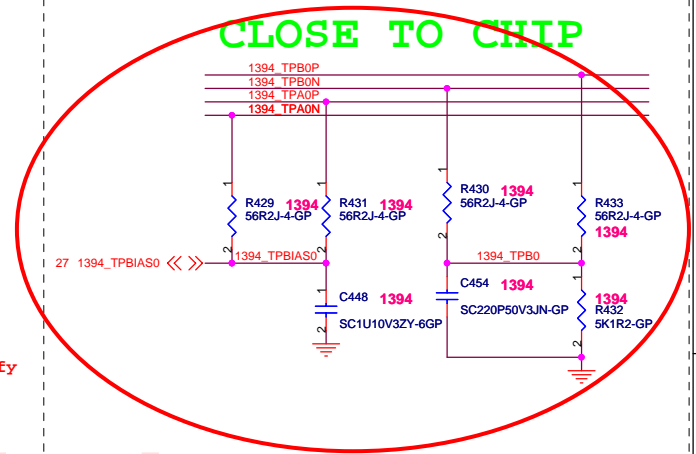
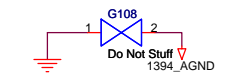


TI PCI7412

• All 1394 signals must be routed on top side only
 • Differential pairs of each ports should have equal trace length
 • Stubs must be keep as short as possible



CLOSE TO CHIP



TI PCI7412

IDSEL: AD22
INTA---: INT_PIRQG#
INTB---: INT_PIRQB#
INTC---: INT_PIRQF#
INTD---: INT_PIRQG#
GNT: PCI_GNT#0
REQ: PCI_REQ#0

INTA# CARBUS 1 (INT_PIRQG#)
 INTB# 1394 (INT_PIRQB#)
 INTC# Flash Media (INT_PIRQF#)
 INTD# SD Host (INT_PIRQG#) share
 MFUNC4: use bit 19-16 Register define.

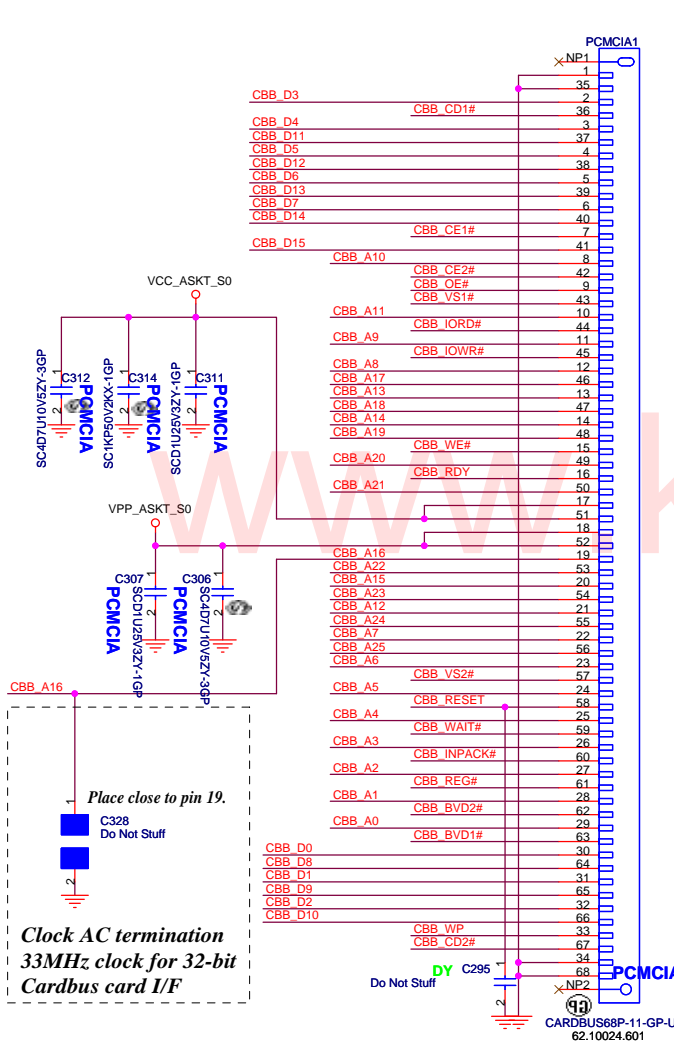
SB modify 12/29

SB modify

55.4H001.S03G

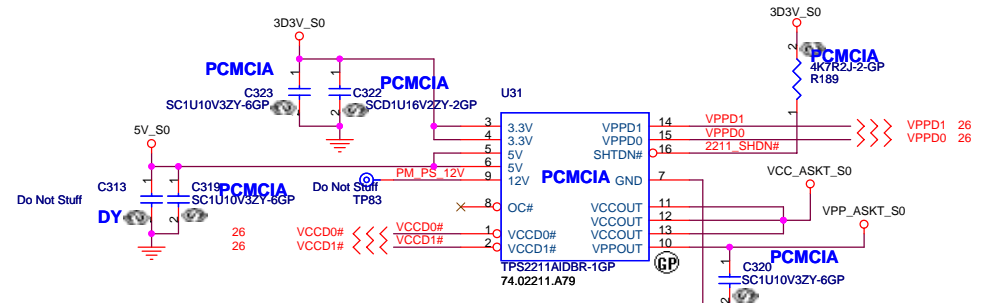
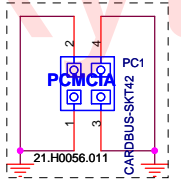
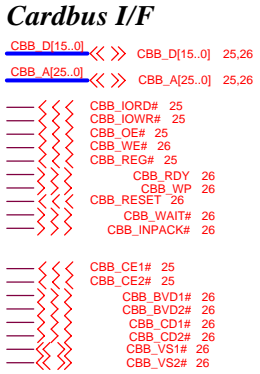
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Title: **TI PCI7412 (2 of 2)**
 Size: Document Number
 Date: Thursday, March 01, 2007
 Sheet: 26 of 42
 Rev: **SB**

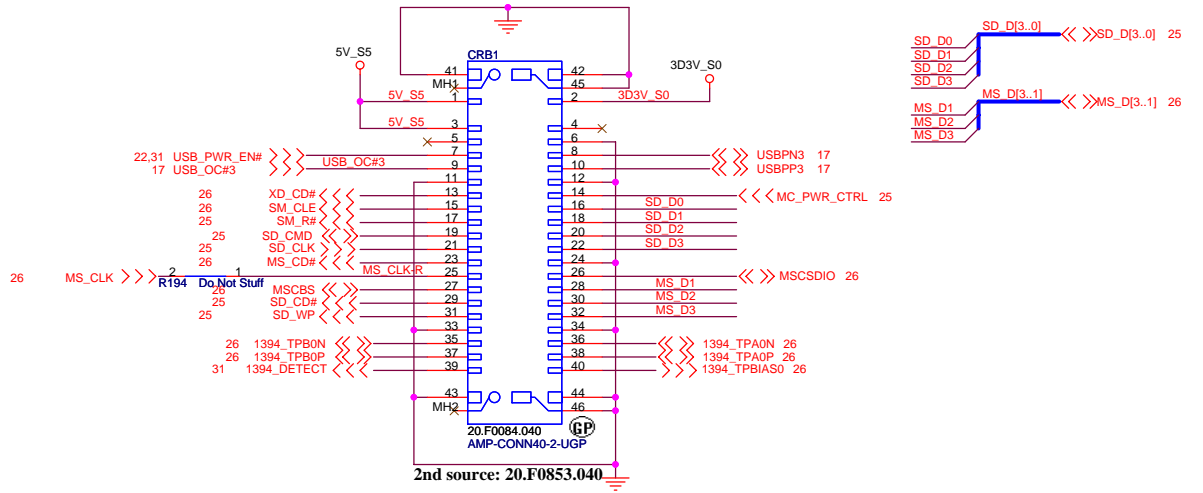


Place close to pin 19.
C328
Do Not Stuff

Clock AC termination
33MHz clock for 32-bit
Cardbus card I/F



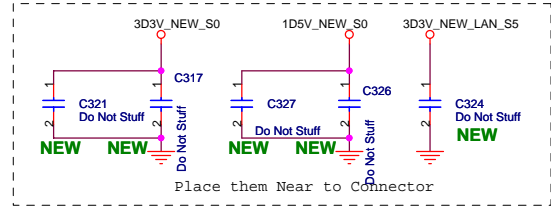
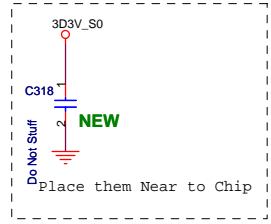
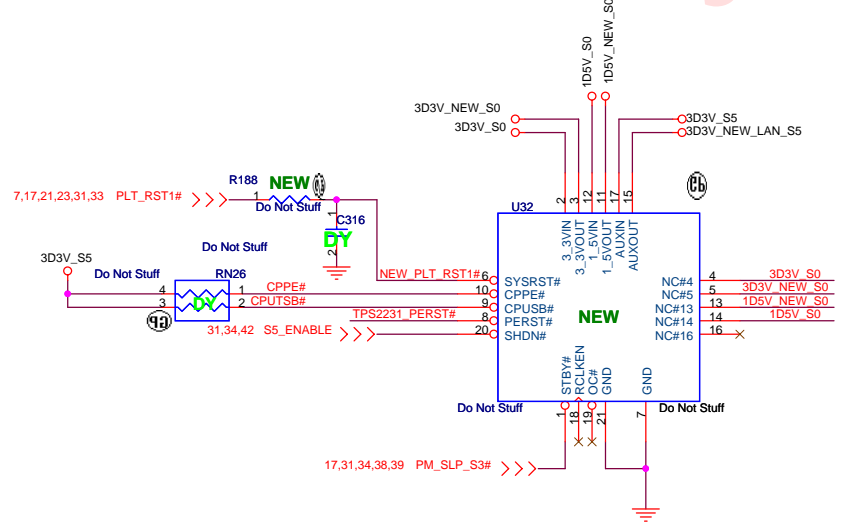
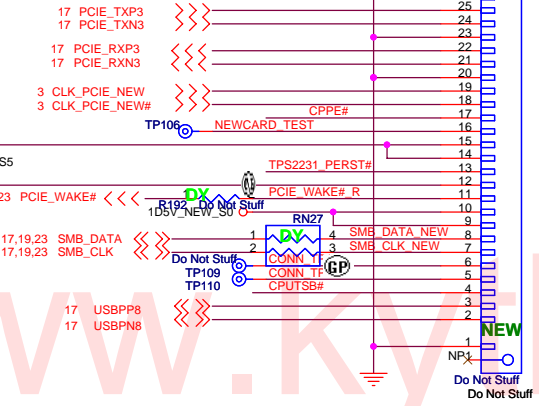
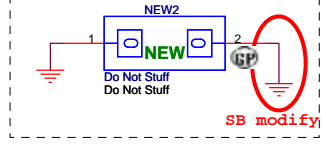
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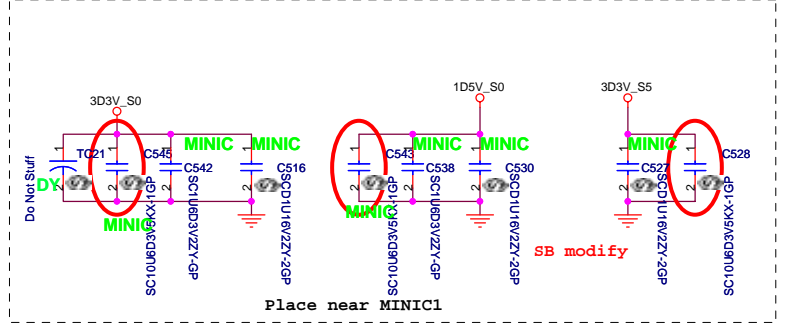
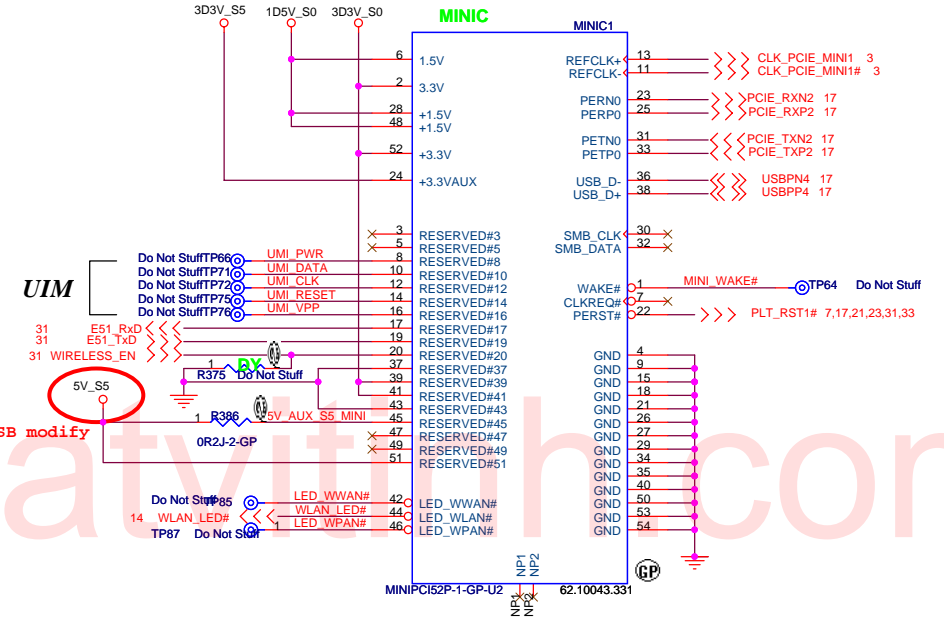
XD
MS / MS PRO
SD / SD IO / MMC

NEWCARD Connector

Reserve the symbol for bottom side connector

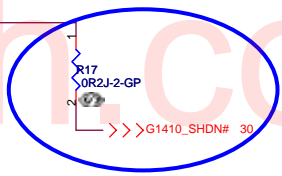
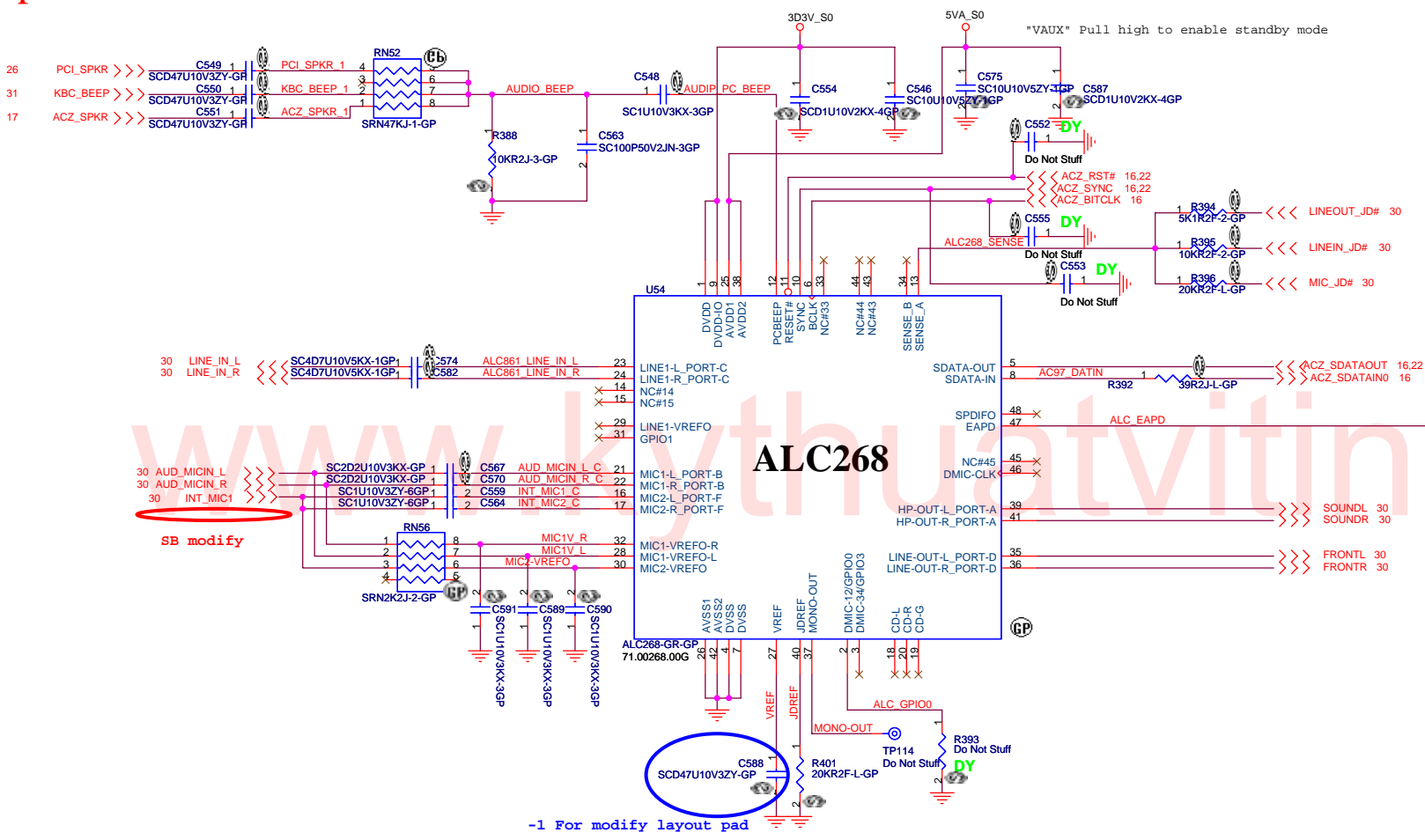


Mini Card Connector

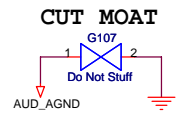
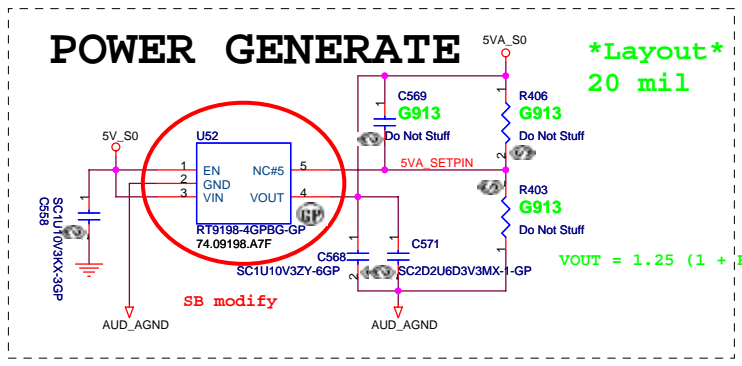


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MINI CARD / NEW CARD	
Biwa	
Title	Rev
Size	Document Number
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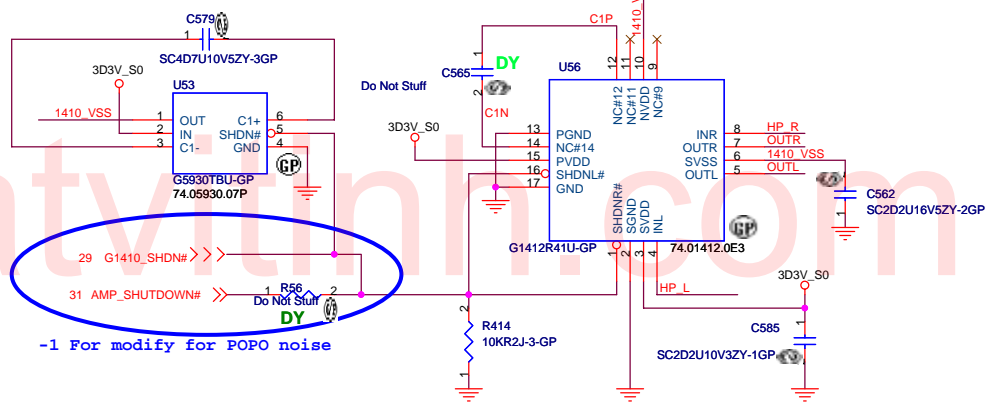
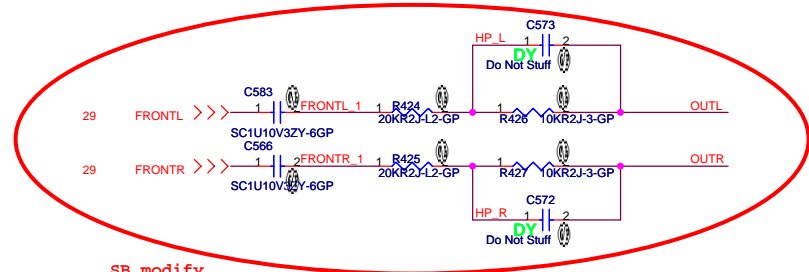
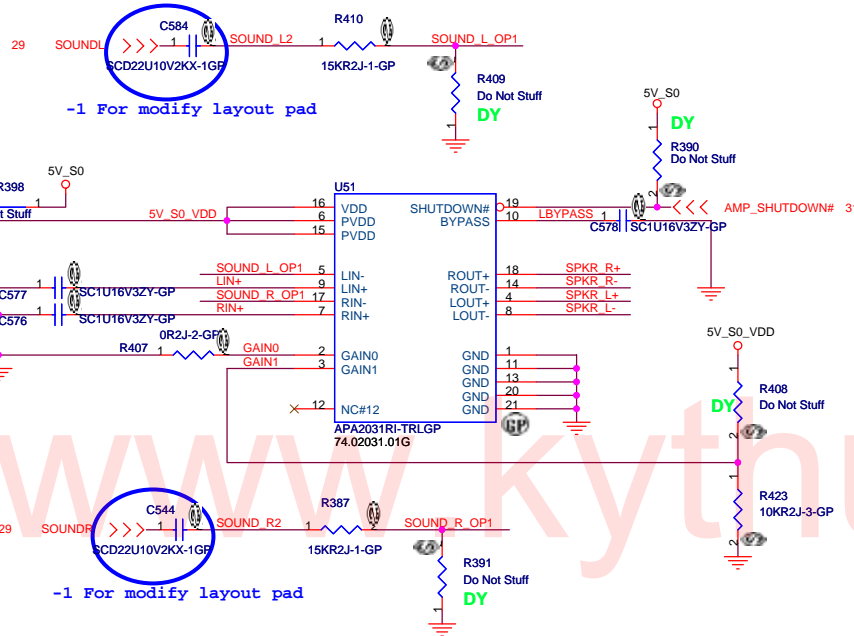
-1 For modify for POPO noise



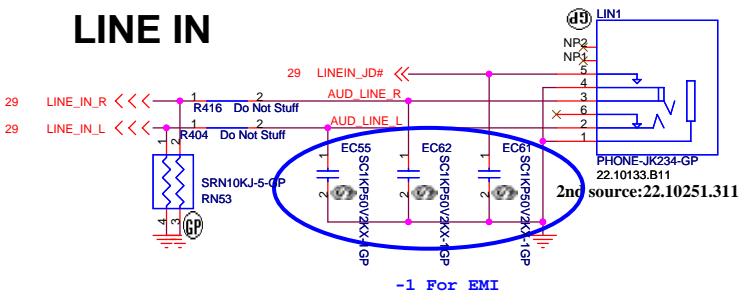
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AZALIA CODEC - ALC268	
Title	
Size	Document Number Biwa
Date: Thursday, March 01, 2007	Rev -1
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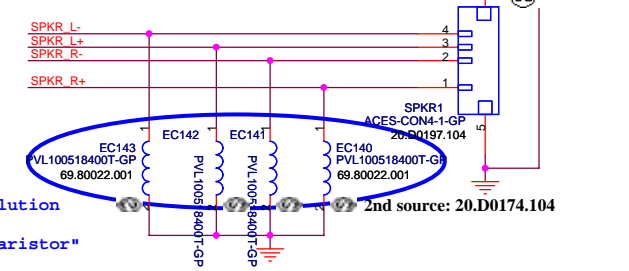
I/P signal level need +5V level



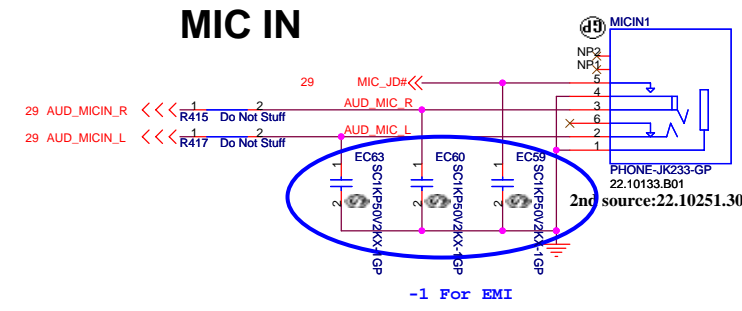
LINE IN



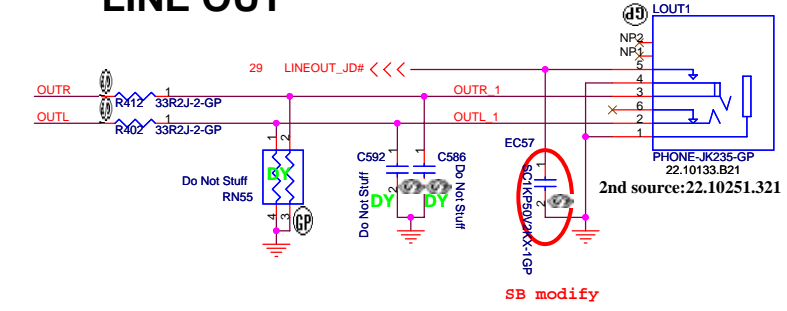
Internal Speaker



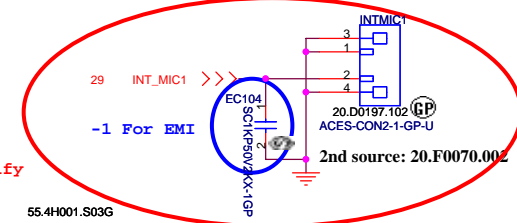
MIC IN



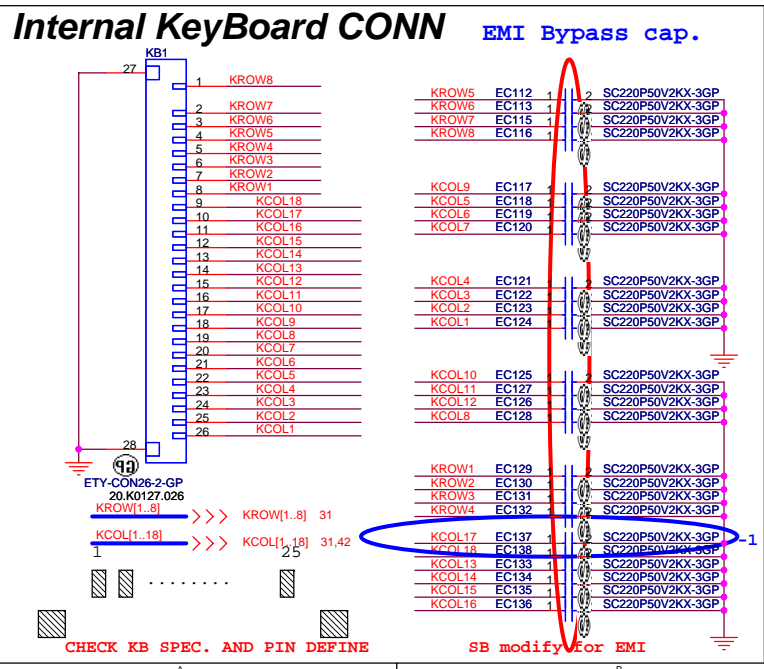
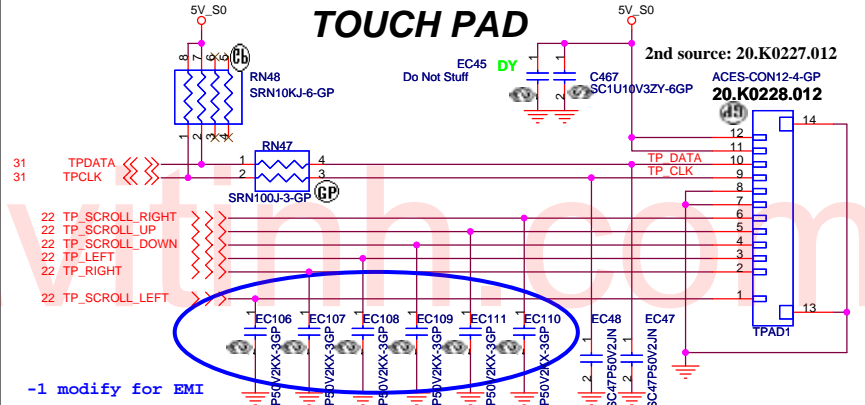
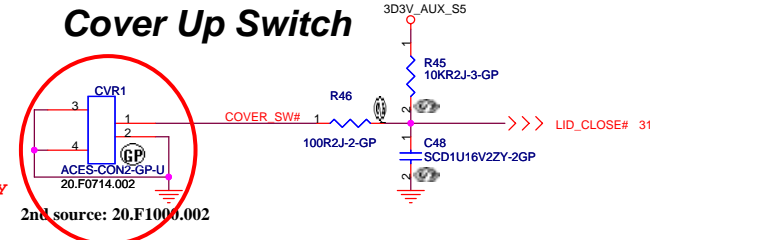
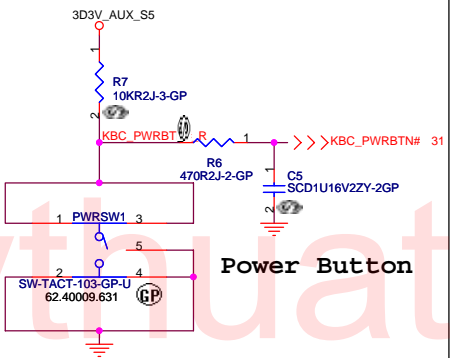
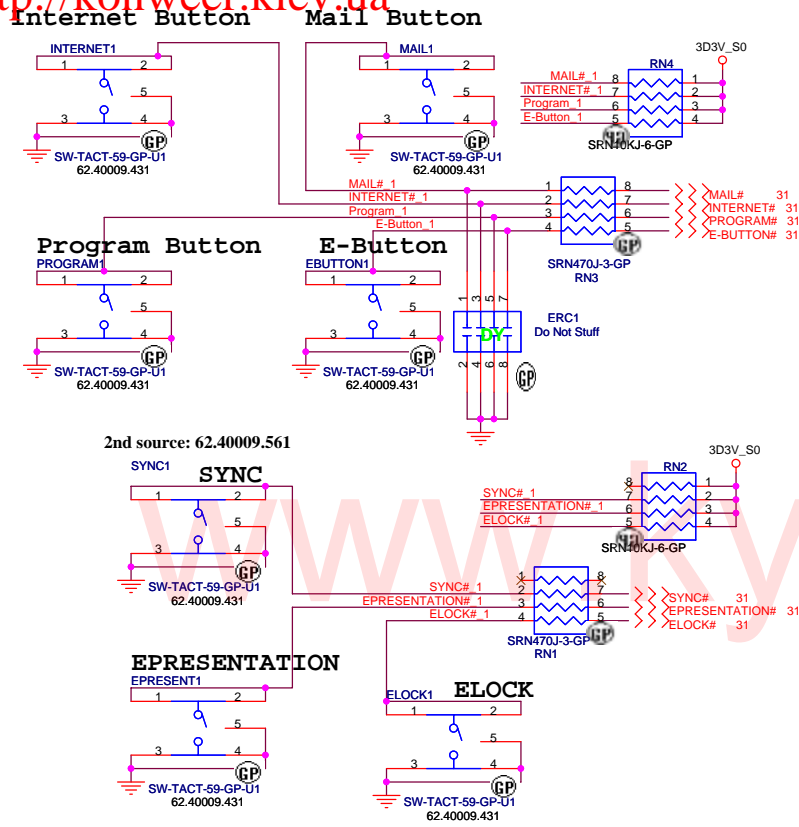
LINE OUT



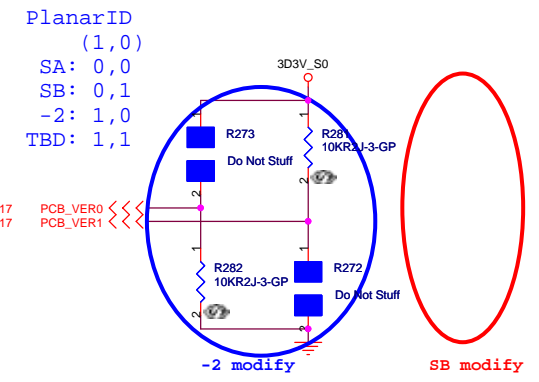
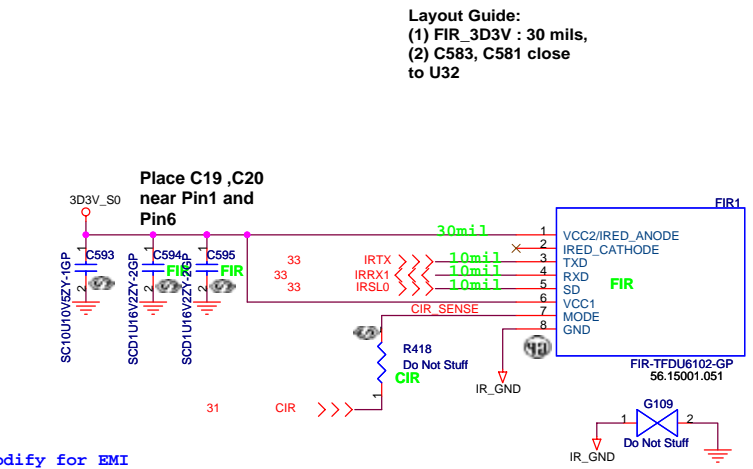
Internal Microphone

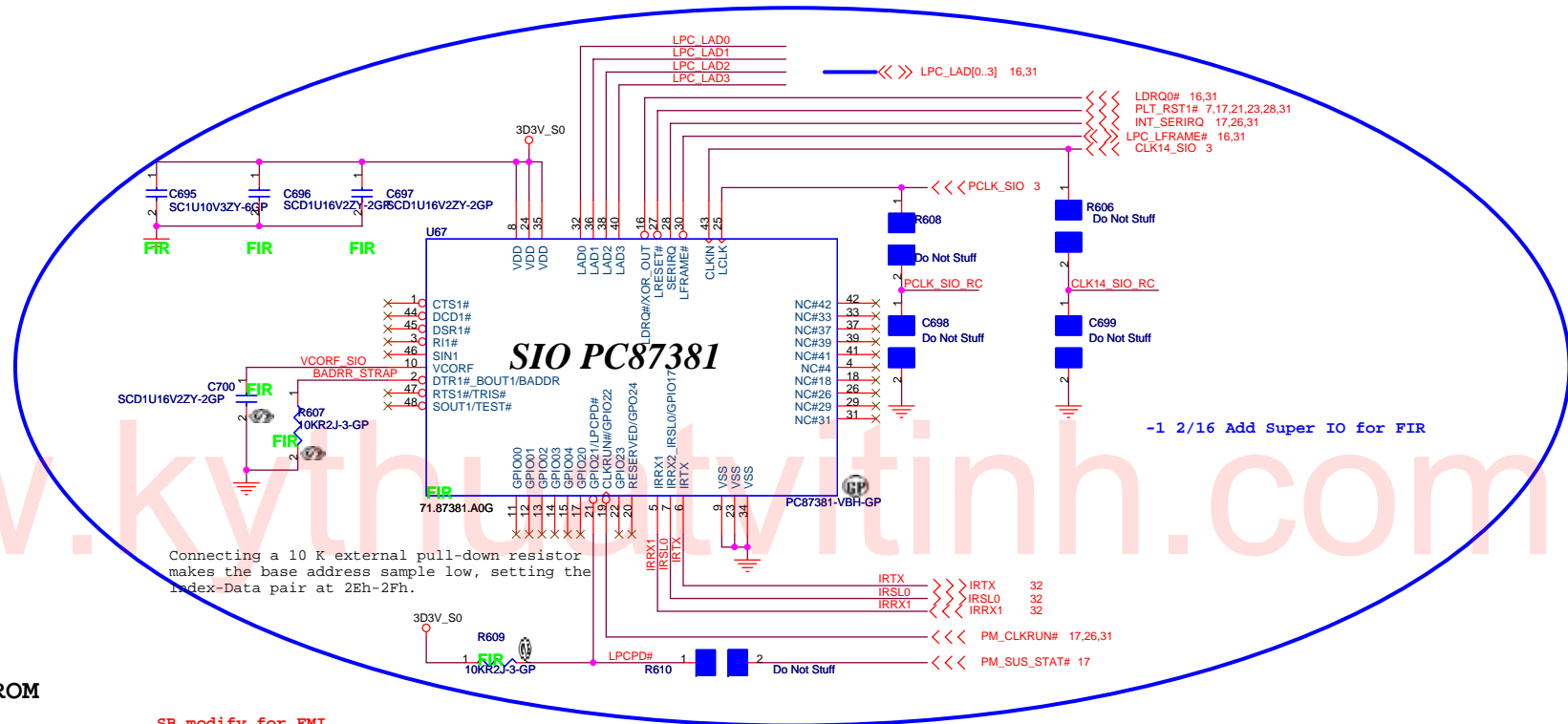


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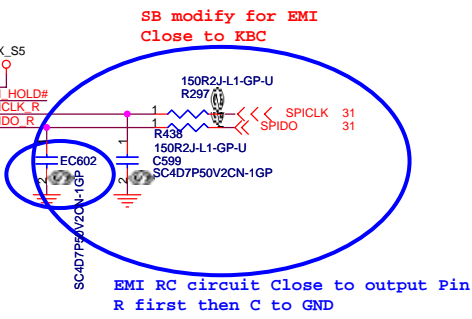
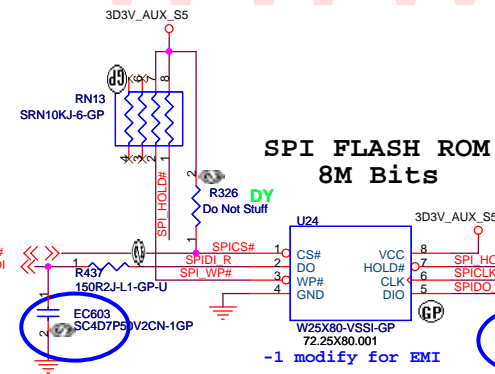
VISHAY FIR Module





Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.

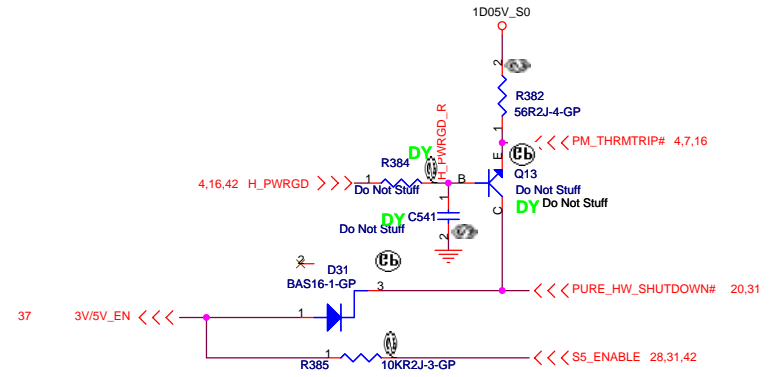
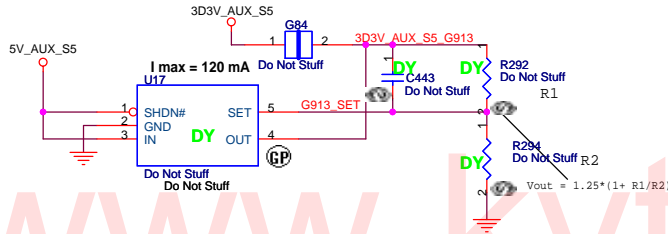
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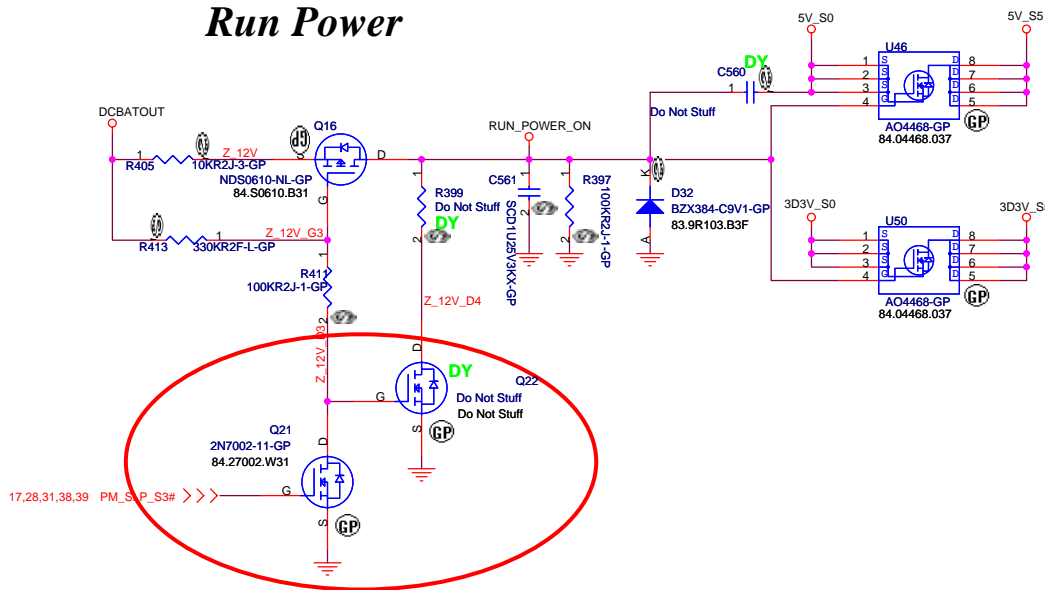
緯創資通		Wistron Corporation	
		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
BIOS & Super IO			
Title			
Size A3	Document Number	Rev	
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Aux Power 3D3V_AUX_S5

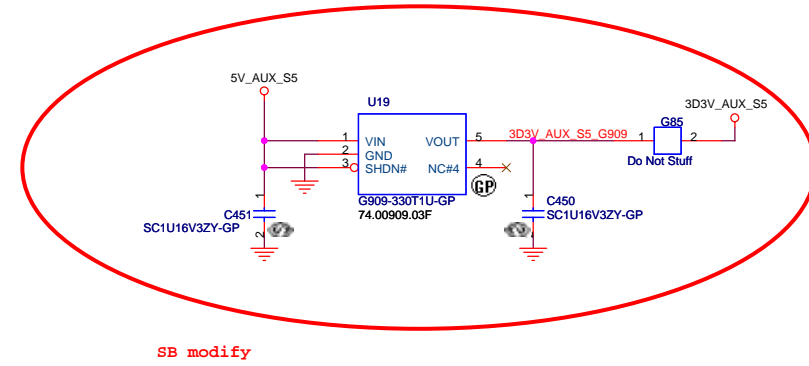


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Run Power



Aux Power 3D3V_AUX_S5

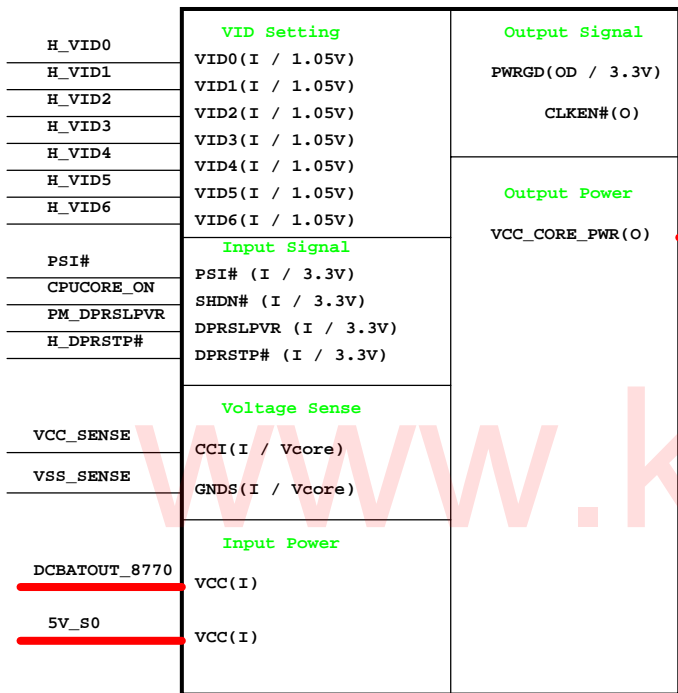


SB modify

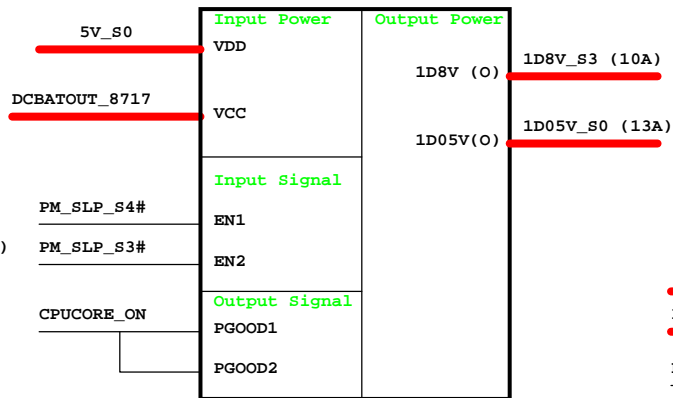
55.4H001.S03G

緯創資通 Wistron Corporation	
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File RUN POWER and 3D3V_AUX_S5	
Size	Document Number
Biwa	
Date: Thursday, March 01, 2007	Sheet 34 of 42

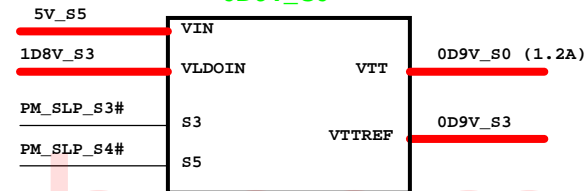
CPU_CORE
MAXIM MAX8770



MAX8717
1D8V/1D05V

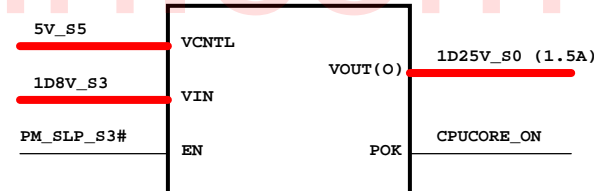


0D9V_S0



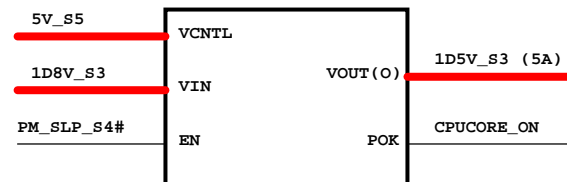
TPS51100

1D25V_S0



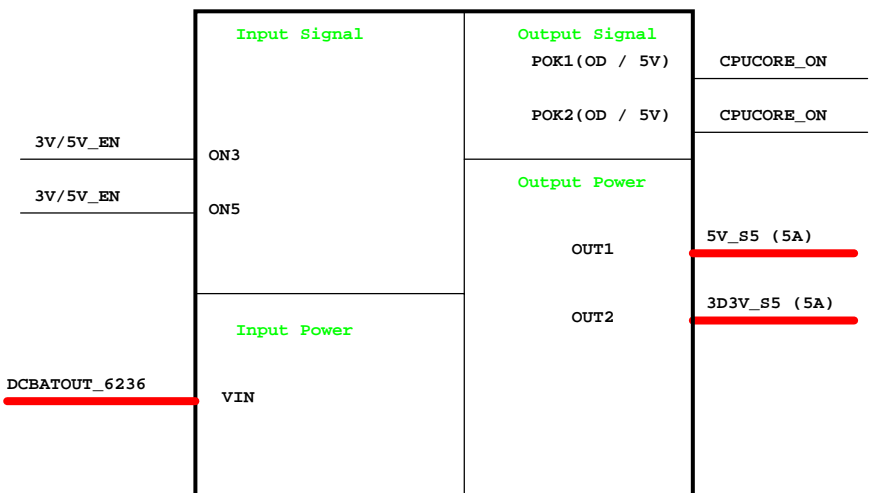
APL5915

1D5V_S3

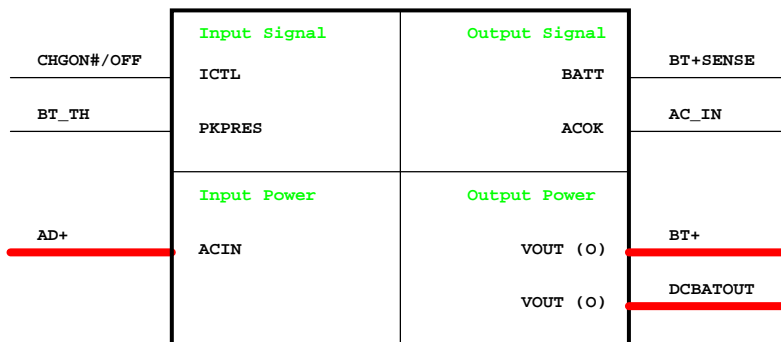


APL5912

ISL6236
5V/3D3V

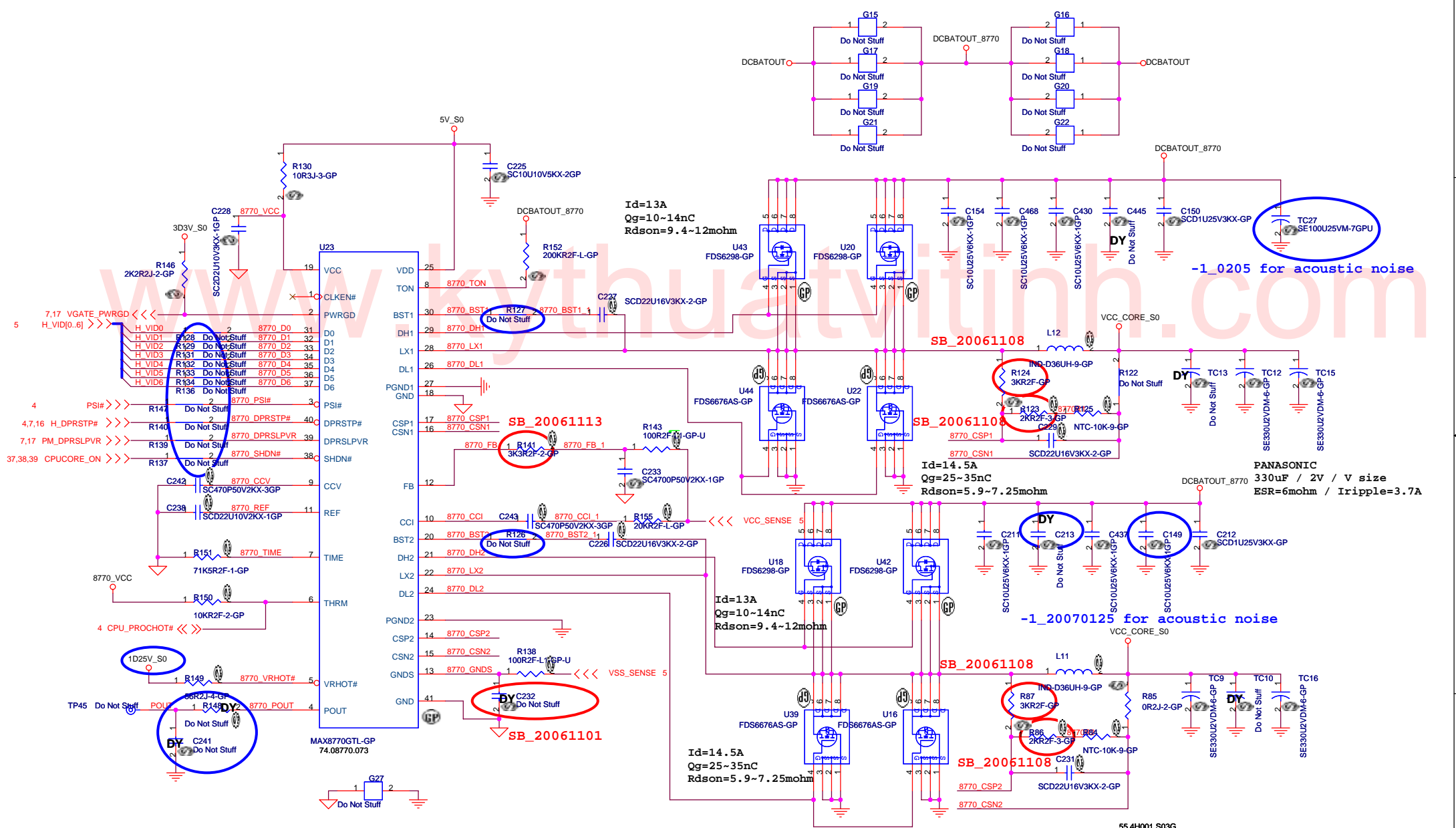


Charger ISL6255



55.4H001.S03G

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Power Block Diagram			
Title	Document Number		Rev
Size A3	Biwa		SA
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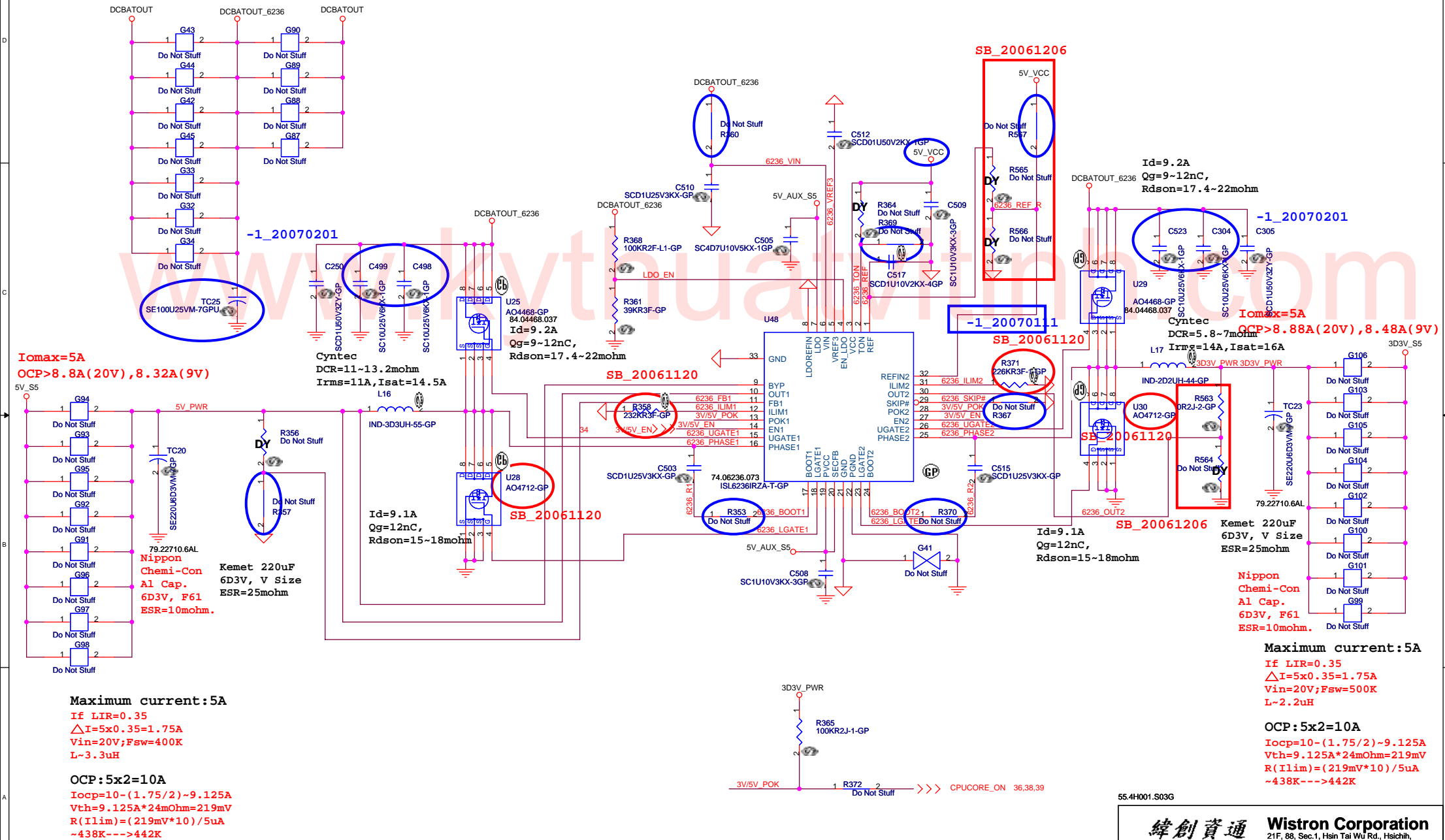
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Title: **VCC CORE**

Size: A3 Document Number: **Biwa** Rev: **-1**

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I_{omax}=5A
OCP>8.8A (20V), 8.32A (9V)

5V_S5
 G94, G93, G95, G92, G91, G96, G97, G98
 Do Not Stuff
 TC20
 SEZ20U6D3VMM-7GP
 R356, R357
 Do Not Stuff
 Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
 Kemet 220uF 6D3V, V Size ESR=25mohm

Maximum current:5A
 If LIR=0.35
 $\Delta I = 5 \times 0.35 = 1.75A$
 $V_{in} = 20V; F_{sw} = 400K$
 $L > 3.3\mu H$
OCP: 5x2=10A
 $I_{ocp} = 10 - (1.75/2) \sim 9.125A$
 $V_{th} = 9.125A * 24m\Omega = 219mV$
 $R(I_{lim}) = (219mV * 10) / 5uA$
 $\sim 438K \rightarrow 442K$

-1_20070201
 TC25
 SE100U25VM-7GPU
 C250, C499, C498
 SCD1U60V32Y-GP
 SC10U25V6KX-1GP
 SC10U25V6KX-1GP
 U25
 AO4468-GP
 84.04468.037
I_d=9.2A
Q_g=9~12nC,
R_{dson}=17.4~22mohm
 Cyntec
 DCR=11~13.2mohm
 I_{rms}=11A, I_{sat}=14.5A

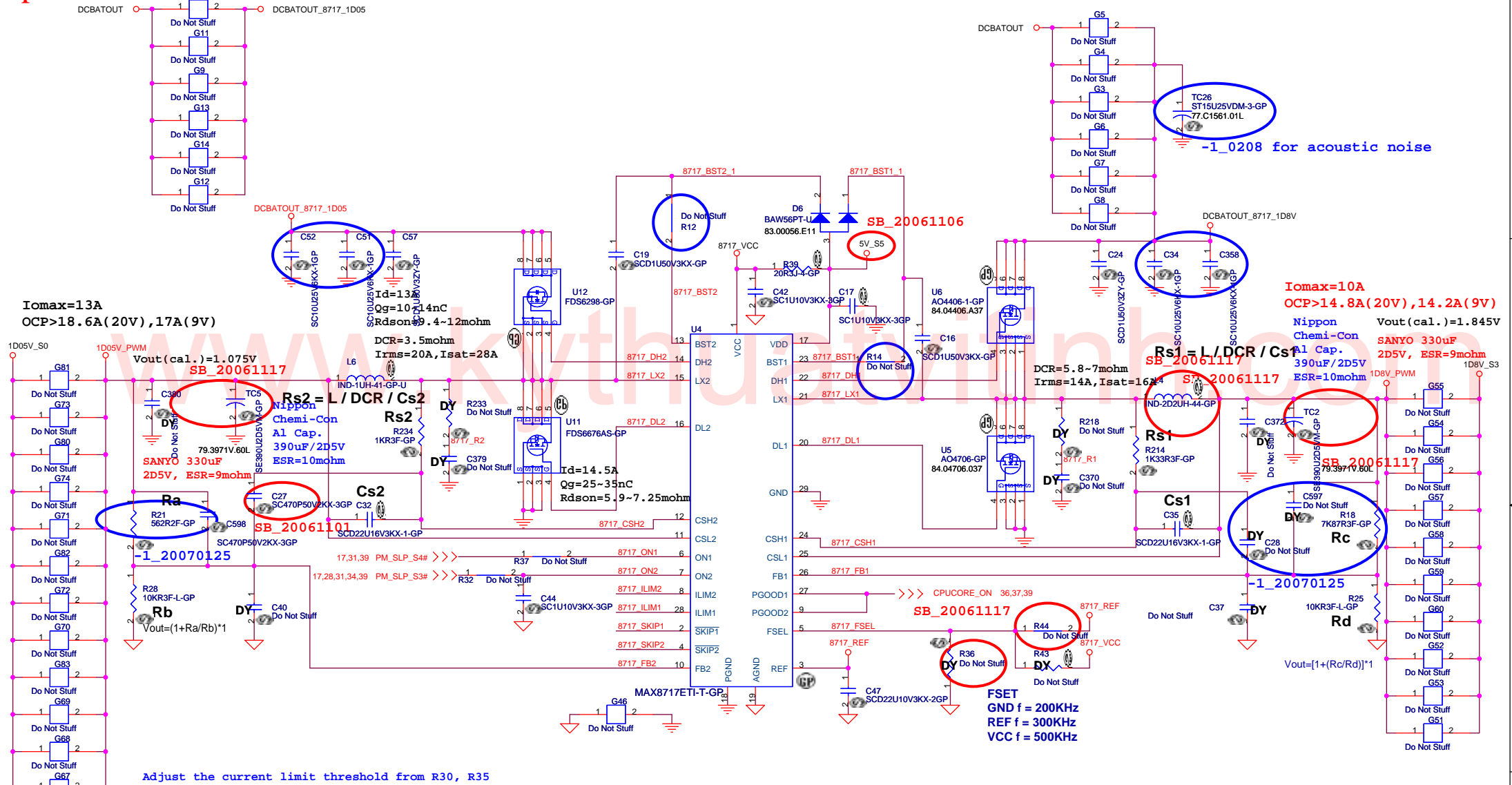
SB_20061120
 R358, R359, R360
 232KR3F-GP
 3V/5V_POK
 3V/5V_EN
 6236_UGATE1
 6236_PHASE1
 U28
 AO4712-GP
I_d=9.1A
Q_g=12nC,
R_{dson}=15~18mohm

SB_20061120
 R353, R354, R355, R356
 Do Not Stuff
 6236_BOOT1
 6236_LGATE1
 U48
 ISL6236RZA-T-GP
I_d=9.1A
Q_g=12nC,
R_{dson}=15~18mohm

SB_20061206
 R565, R566
 Do Not Stuff
 6236_REF_R
I_d=9.2A
Q_g=9~12nC,
R_{dson}=17.4~22mohm

-1_20070201
 C523, C304, C305
 SC10U25V6KX-1GP
 SC10U25V6KX-1GP
 U29
 AO4468-GP
 84.04468.037
I_{omax}=5A
 Cyntec
 DCR=5.8~7mohm
OCP>8.8A (20V), 8.48A (9V)
 L17
 I_{rms}=14A, I_{sat}=16A
SB_20061120
 R371, R367
 226KR3F-GP
 Do Not Stuff
SB_20061206
 U30
 AO4712-GP
 R563, R564
 0R2J-2-GP
 Do Not Stuff
 TC23
 SEZ20U6D3VMM-7GP
 Kemet 220uF 6D3V, V Size ESR=25mohm
 Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.

Maximum current:5A
 If LIR=0.35
 $\Delta I = 5 \times 0.35 = 1.75A$
 $V_{in} = 20V; F_{sw} = 500K$
 $L > 2.2\mu H$
OCP: 5x2=10A
 $I_{ocp} = 10 - (1.75/2) \sim 9.125A$
 $V_{th} = 9.125A * 24m\Omega = 219mV$
 $R(I_{lim}) = (219mV * 10) / 5uA$
 $\sim 438K \rightarrow 442K$



I_{omax}=13A
OCP>18.6A (20V), 17A (9V)

I_{omax}=10A
OCP>14.8A (20V), 14.2A (9V)
Nippon Chemi-Con SANYO 330uF
Al Cap. 2D5V, ESR=9mohm
ESR=1.0mohm
V_{out} (cal.) = 1.845V

TC26
 ST15U25VDM-3-GP
 77.C1561.01L

-1_0208 for acoustic noise

SB_20061117

SB_20061117

SB_20061117

SB_20061117

SB_20061117

SB_20061117

SB_20061117

SB_20061117

SB_20061117

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SB_20061117

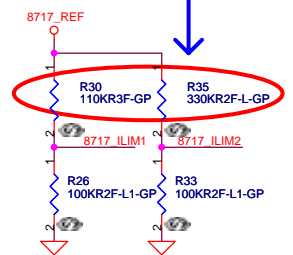
SB_20061117

SB_20061117

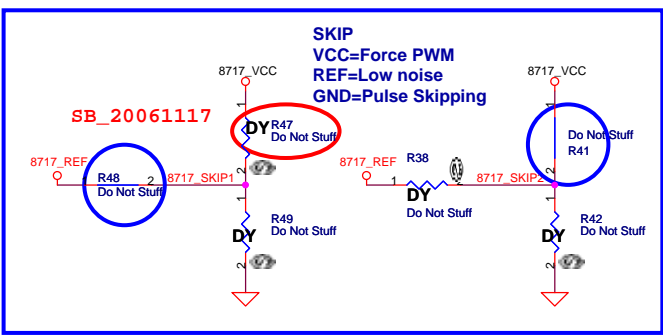
SB_20061117

Adjust the current limit threshold from R30, R35

SB_20061120



VILIM = 0.5V-2.0V
Output Current =
 $ILIM / 10 / LDCR - dI/2$



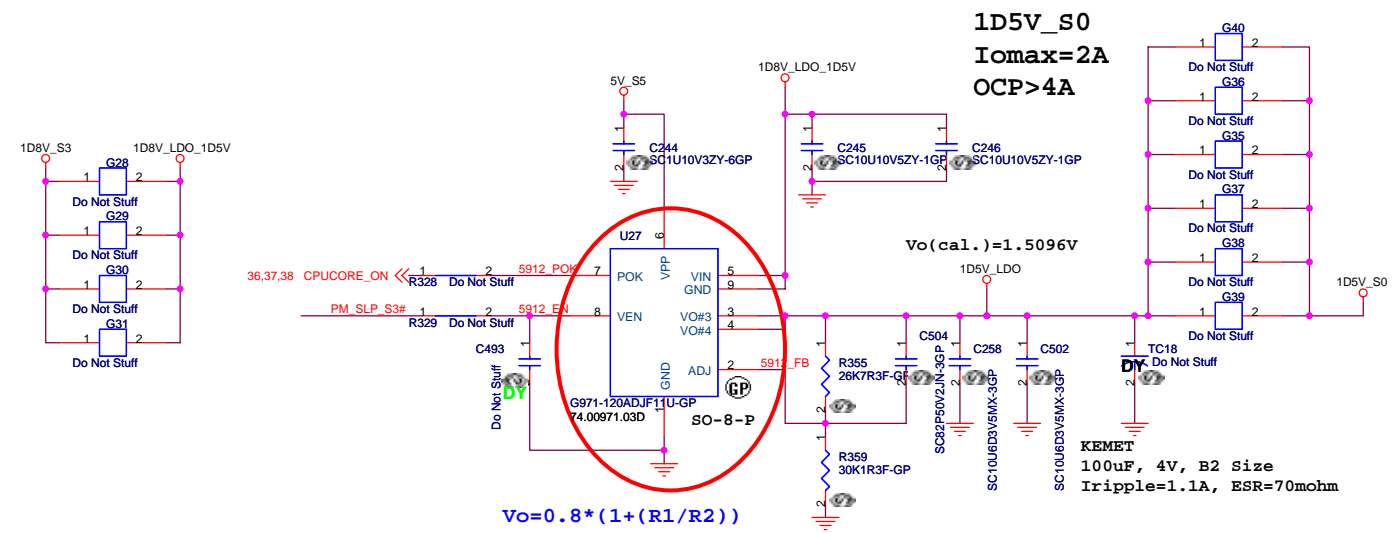
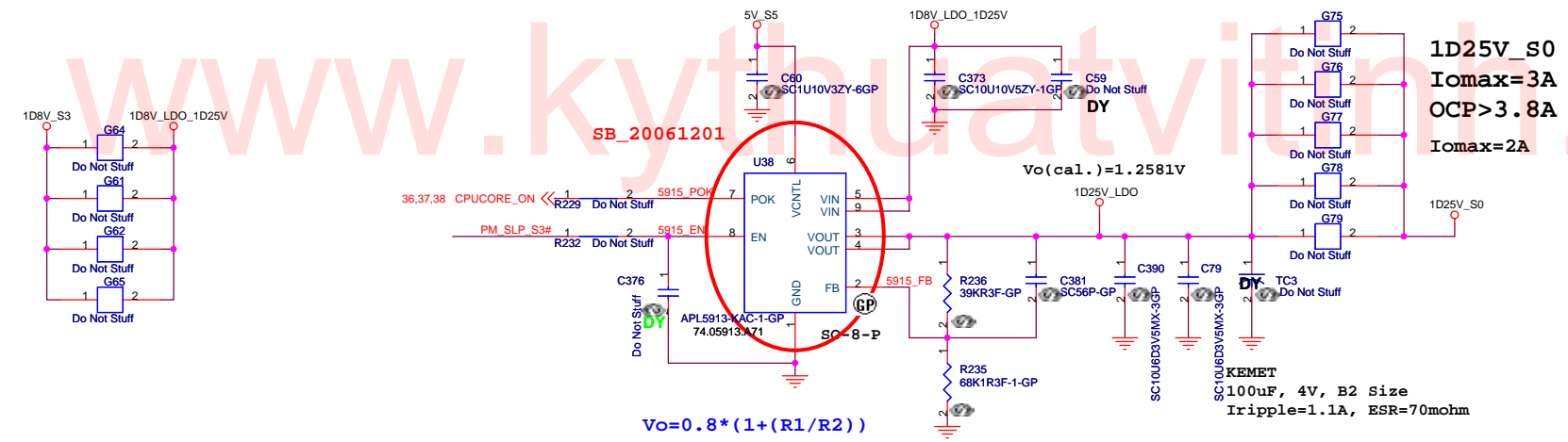
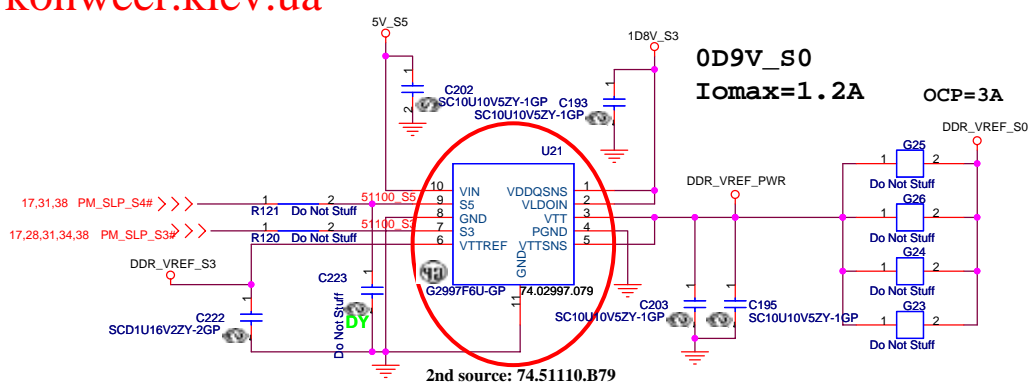
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping

FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz

55.4H001.S03G

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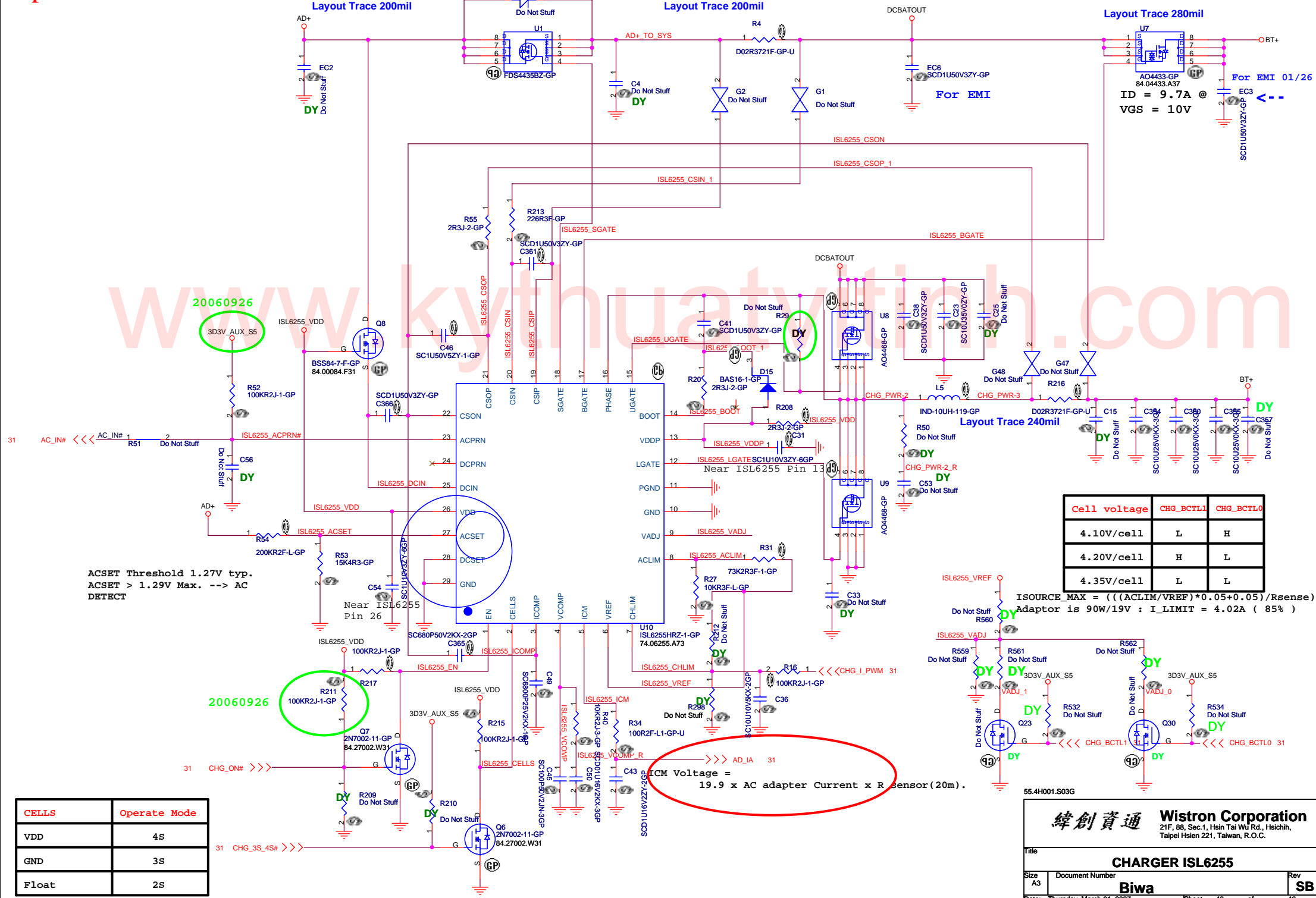
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Size	Document Number				Rev
A3			Biwa		-2
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55.4H001.S03G

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Title		1D25V/1D5V/0D9V	
Size	Document Number	Rev	
A3	Biwa	SB	
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20060926

20060926

ACSET Threshold 1.27V typ.
ACSET > 1.29V Max. --> AC DETECT

ICM Voltage = $19.9 \times \text{AC adapter Current} \times \text{R sensor (20m)}$

Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

ISOURCE_MAX = $((\text{ACLIM}/\text{VREF}) * 0.05 + 0.05) / \text{Rsense}$
Adaptor is 90W/19V : I_LIMIT = 4.02A (85%)

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

55.4H001.S03G

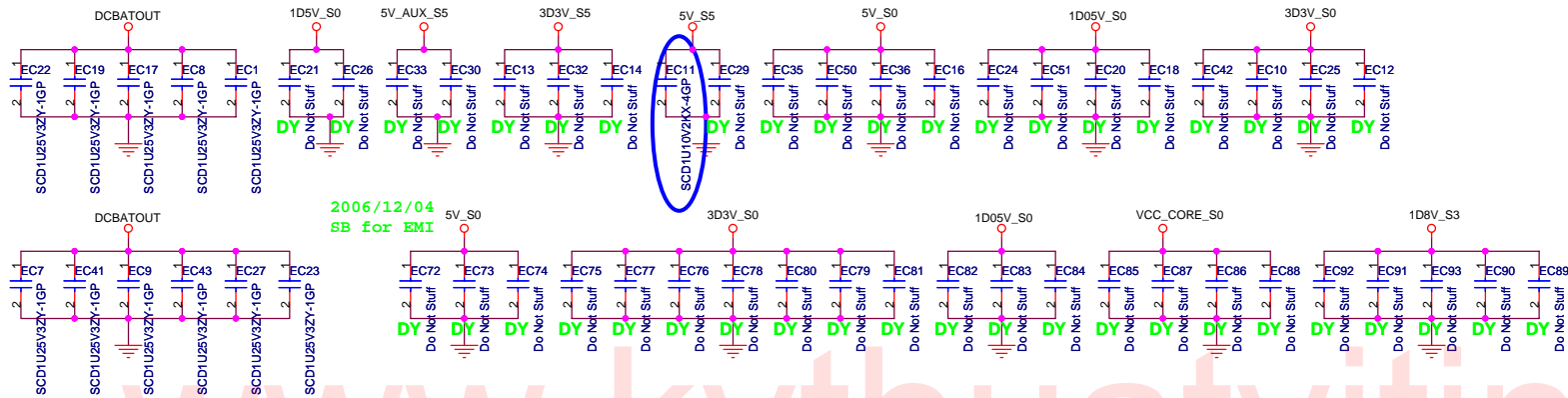
緯創資通 Wistron Corporation
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Title: **CHARGER ISL6255**

Size A3	Document Number	Rev
	Biwa	SB

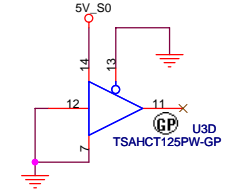
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EMI Capacitor

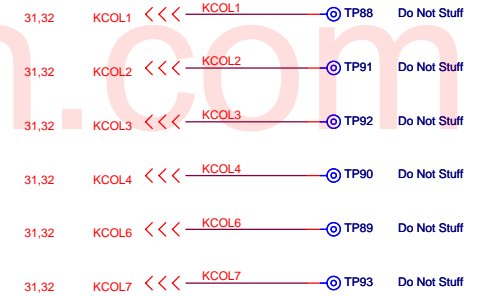


2006/12/04
SB for EMI

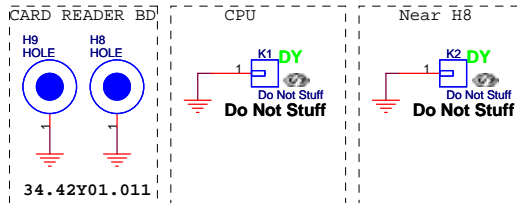
Unused gate



KBC JTAG Test Pad

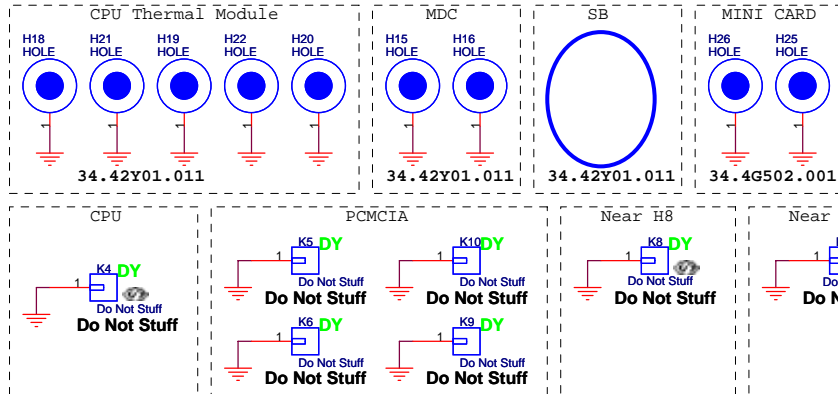


TOP



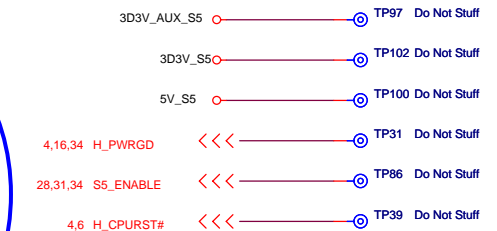
-1_0131 for thermal

BOTTOM



-1_20070206

DFX Test Point



Test Point放在Dimm Door打開可量測處

55.4H001.S03G

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Title: **EMI/Spring/Boss**

Size: Document Number: **Biwa** Rev: **-1**

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