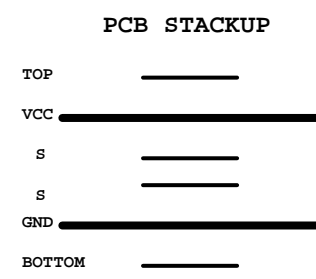
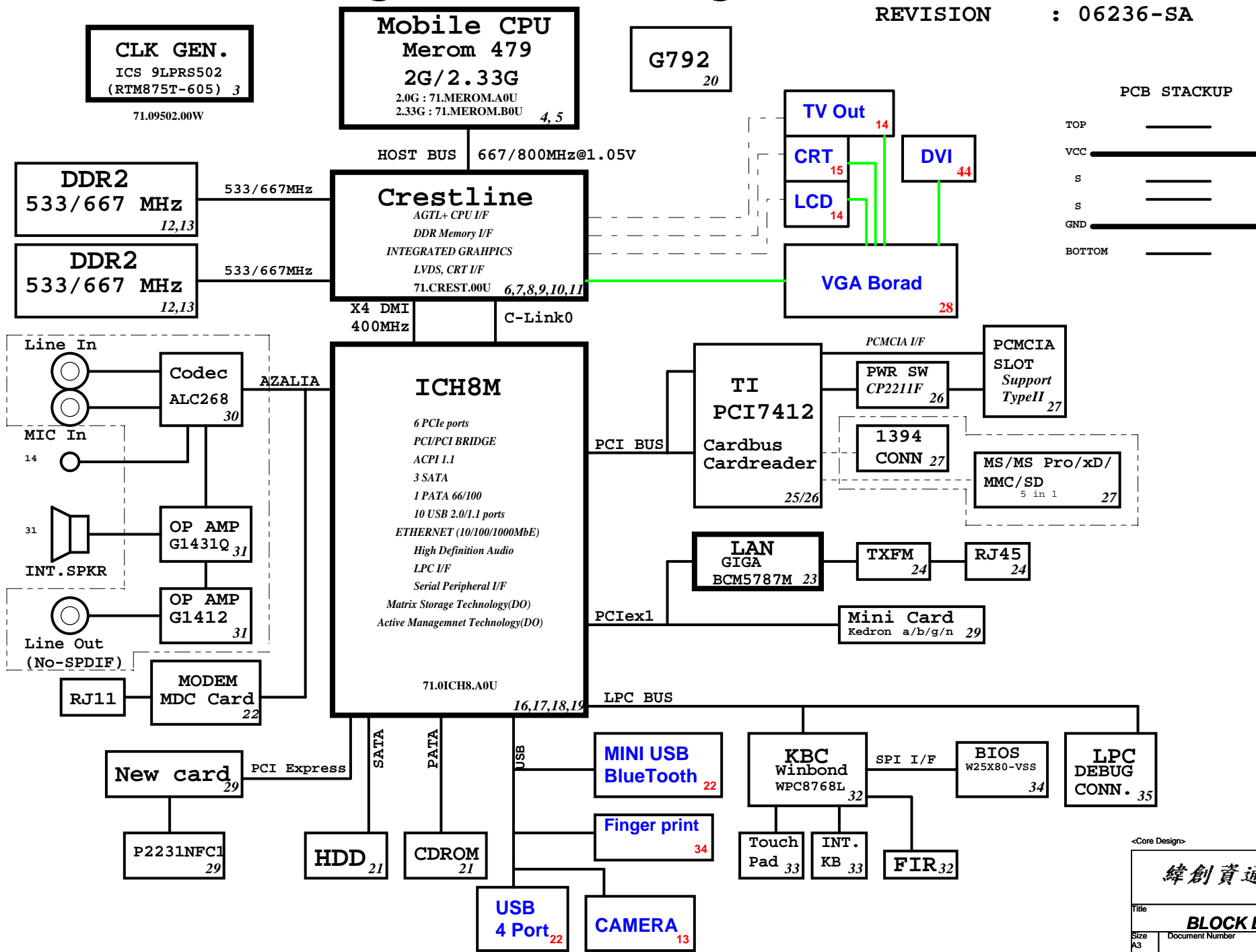


# Columbia/Tangiz Block Diagram

Project code: 91.4T301.001  
 PCB P/N : 48.4T301.0SA  
 REVISION : 06236-SA



<b>SYSTEM DC/DC</b> MAX8744 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)
<b>SYSTEM DC/DC</b> Max8717 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)
TPS51100 41	
1D8V_S3	DDR_VREF_S0(1.5A) DDR_VREF_S3
APL5915 41	
1D8V_S3	1D25V_S0(2A)
APL531230	
3D3V_S0	2D5V_S0(300mA)
APW5912 40	
3D3V_S5	1D5V_S3(7.5A)
<b>ISL CHARGER</b> ISL6255 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA
<b>CPU DC/DC</b> MAX8770 35,36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 and VccSus1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE X1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWROK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

USB Table

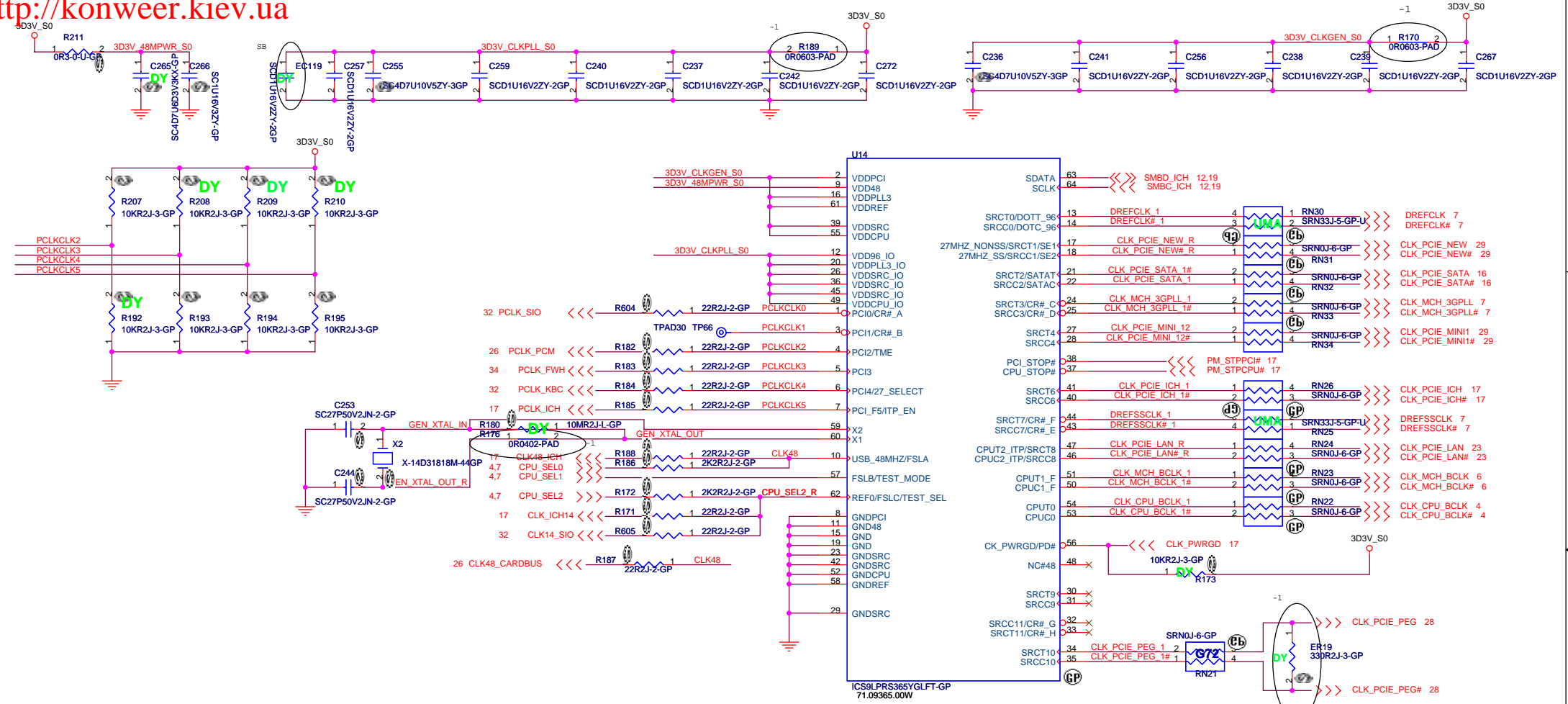
USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

UMA

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Reference</b>			
Title	Document Number		Rev
Size A3	Columbia/Tangiz		-1
Date: Monday, February 26, 2007	Sheet 2	of	45



UMA:71.09502.A0W=>56pin  
 G72:71.09365.00W=>64pin  
 U14上56pin時  
 RN22,23,24,26,31,32,33,34改成66.33036.04L

ICS9LPRS502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#A enabled. Byte 5, bit 6 controls whether CR#A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#A controls SRC0 pair (default), 1 = CR#A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#B enabled. Byte 5, bit 6 controls whether CR#B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#B controls SRC1 pair (default) 1 = CR#B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#A enabled. Byte 5, bit 6 controls whether CR#A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#A controls SRC0 pair (default), 1 = CR#A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#B enabled. Byte 5, bit 6 controls whether CR#B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#B controls SRC1 pair (default) 1 = CR#B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

UMA

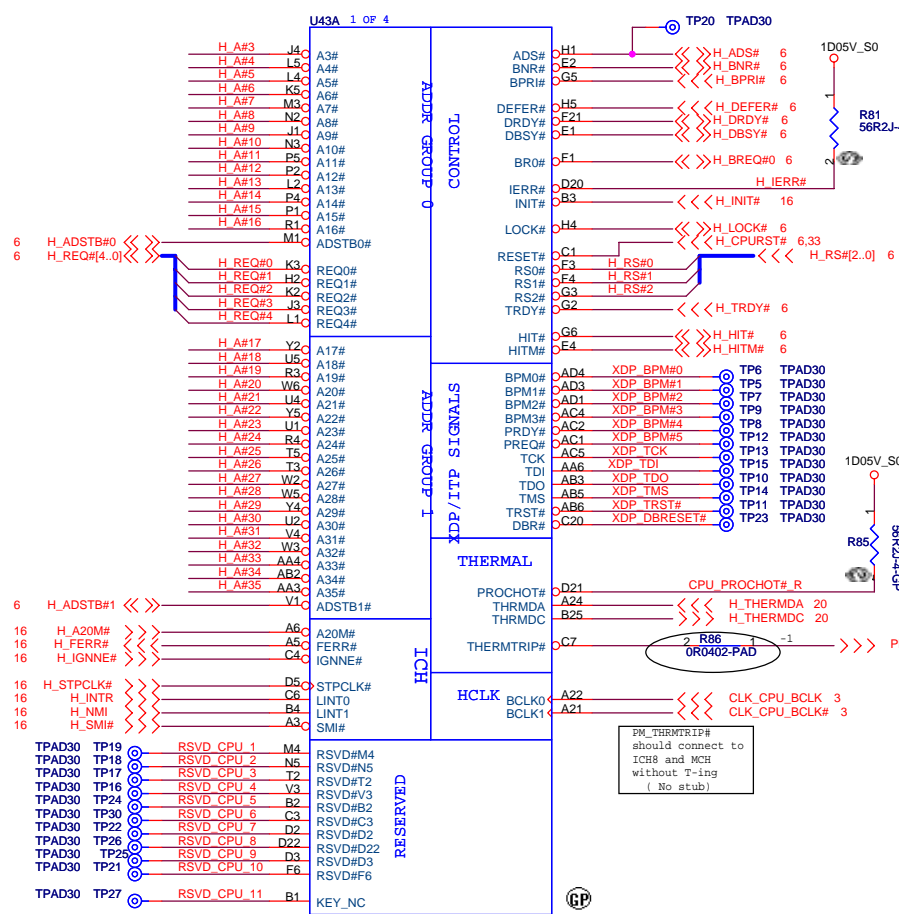
緯創資通 Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

Size: Document Number Columbia/Tangiz Rev SA

Date: Monday, February 26, 2007 Sheet 3 of 45

6 H\_A#(35..3) <<>> H\_A#(35..3)



Place testpoint on H\_IERR# with a GND 0.1" away

Layout Note: "CPU\_GTLREF0" 0.5" max length.

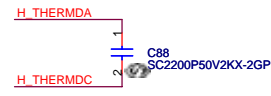
PM\_THRMTRIP# should connect to ICH8 and MCH without T-ling (No stub)

H\_DINV#(3..0) <<>> H\_DINV#(3..0) 6

H\_DSTBN#(3..0) <<>> H\_DSTBN#(3..0) 6

H\_DSTBP#(3..0) <<>> H\_DSTBP#(3..0) 6

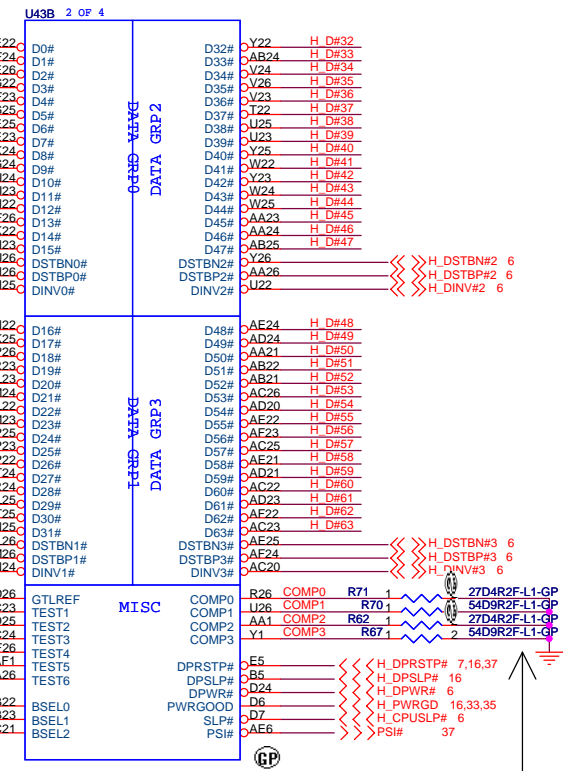
H\_D#(63..0) <<>> H\_D#(63..0) 6



6 H\_DSTBN#0

6 H\_DSTBP#0

6 H\_DINV#0



6 H\_DSTBN#1

6 H\_DSTBP#1

6 H\_DINV#1

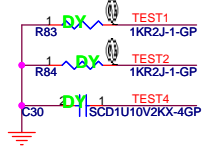
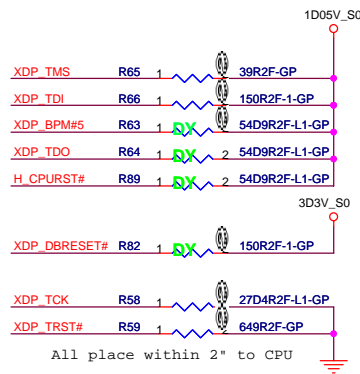
3.7 CPU\_SEL0

3.7 CPU\_SEL1

3.7 CPU\_SEL2

Layout Note:  
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5"  
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"

Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals



UMA

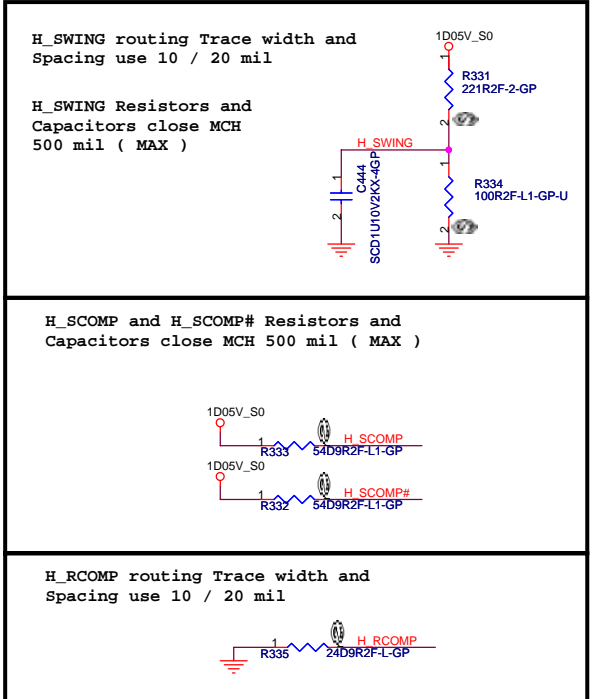
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (1 of 2)**

Size: Document Number Rev -1

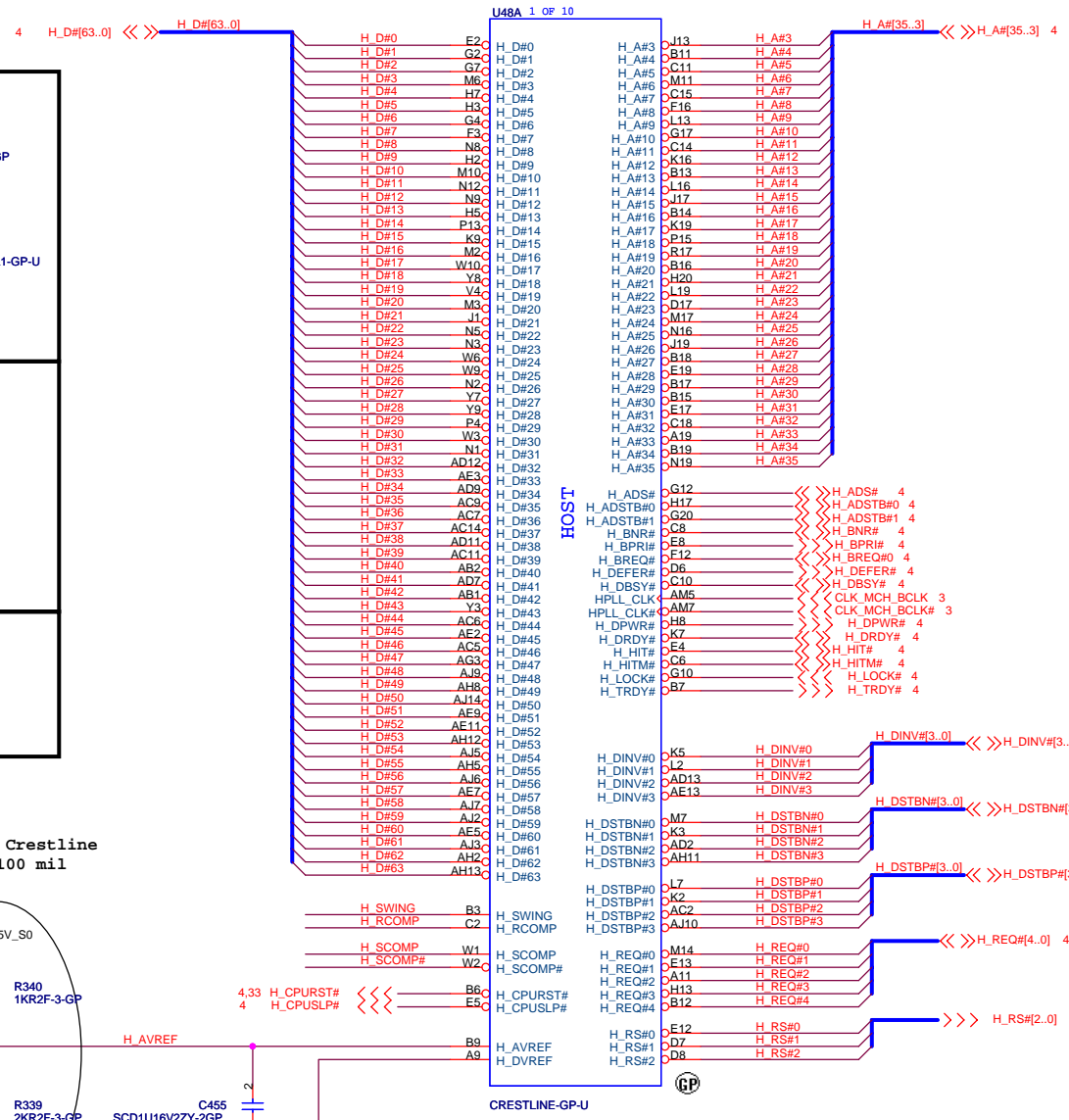
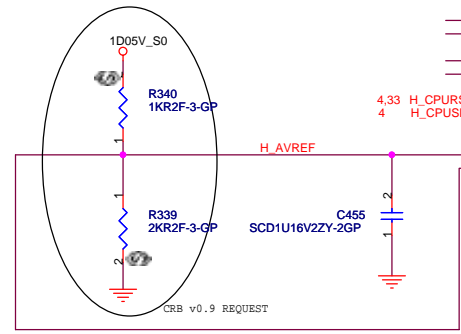
Date: Monday, February 26, 2007 Sheet 4 of 45





Place them near to the chip ( < 0.5" )

**H\_REF Decoupling Crestline close Crestline 100 mil**



UMA

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Title: **GMCH (1 of 6)**

Size: Document Number: **Columbia/Tangiz** Rev: **-1**

Date: Monday, February 26, 2007 Sheet 6 of 45

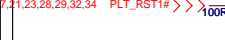
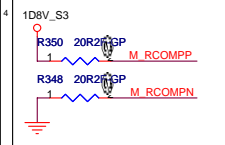
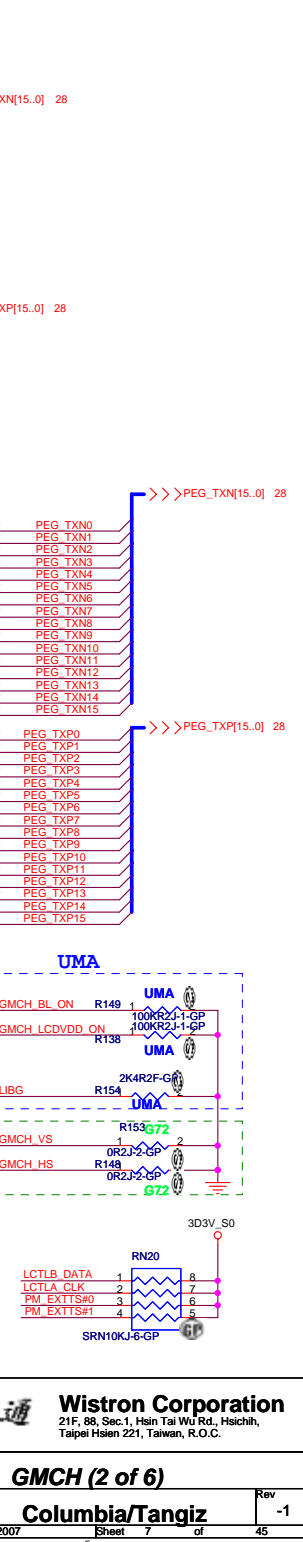
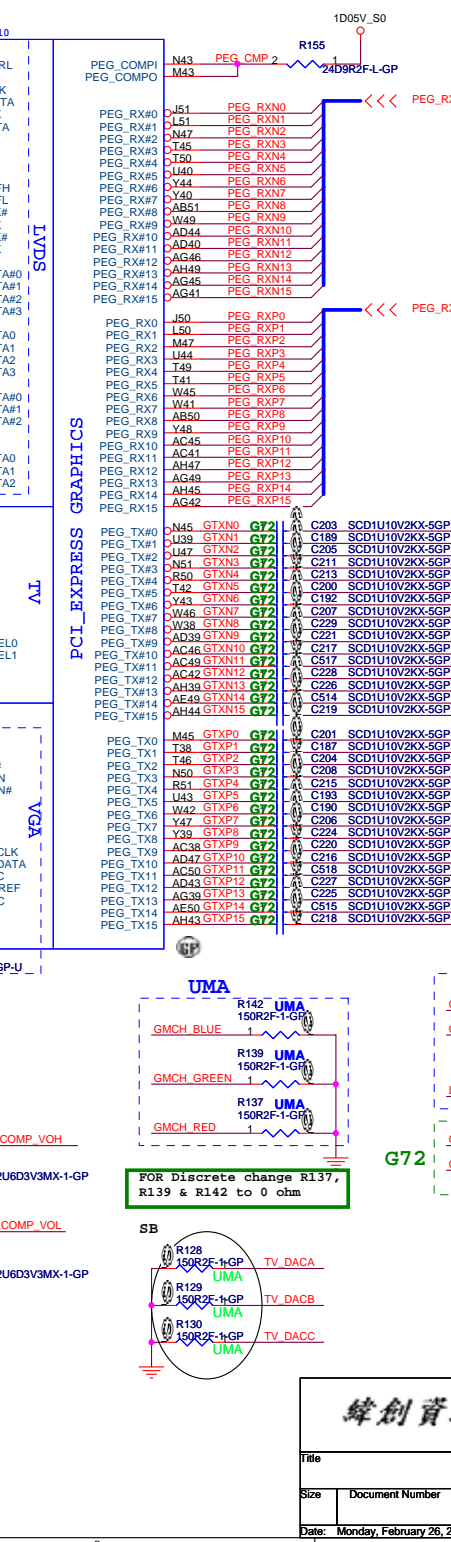
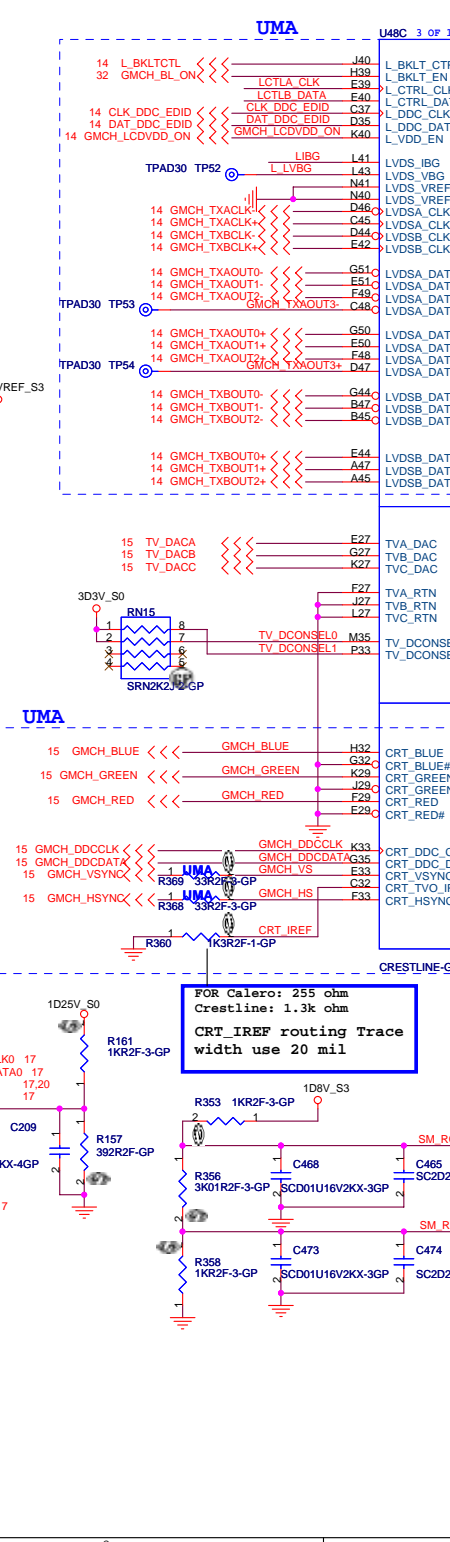


Table of pin connections for U48B 2 OF 10, including SM, RSVD, DMI, CFG, GRAPHICS VID, ME, and MISC sections.

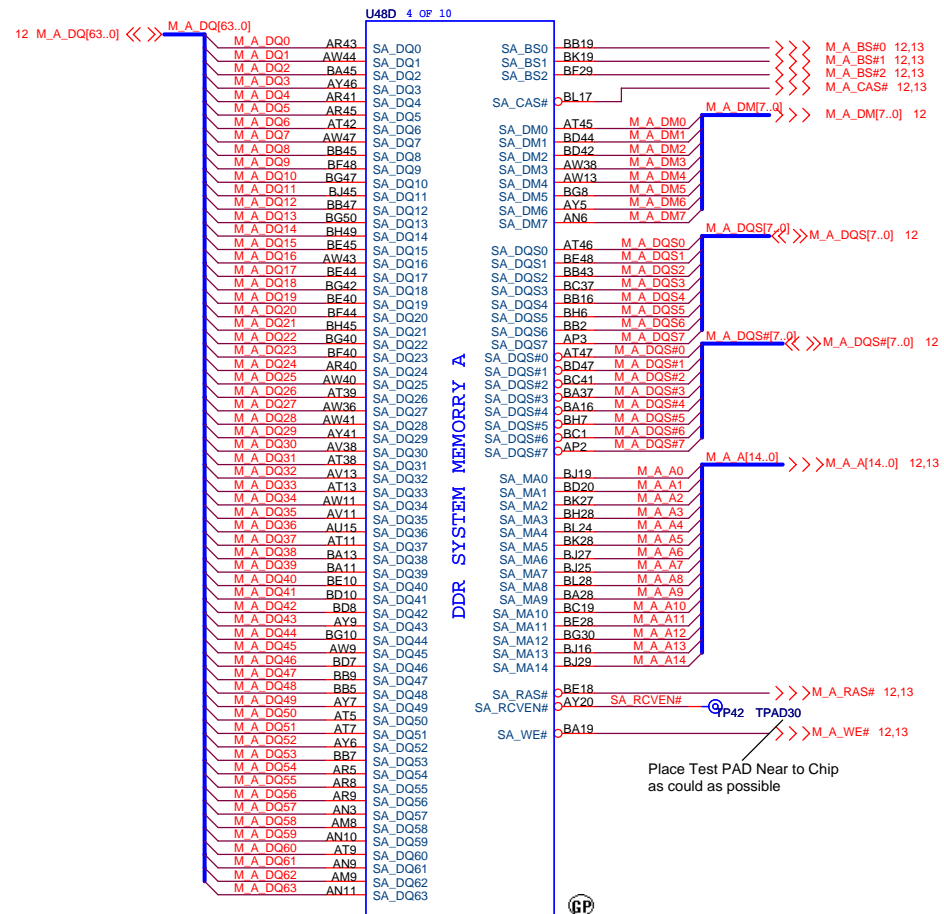
Table of pin connections for U48C 3 OF 10, including CLK, DMI, CFG, GRAPHICS VID, ME, and MISC sections.



FOR Calero: 255 ohm  
Crestline: 1.3k ohm  
CRT IREF routing Trace  
width use 20 mil

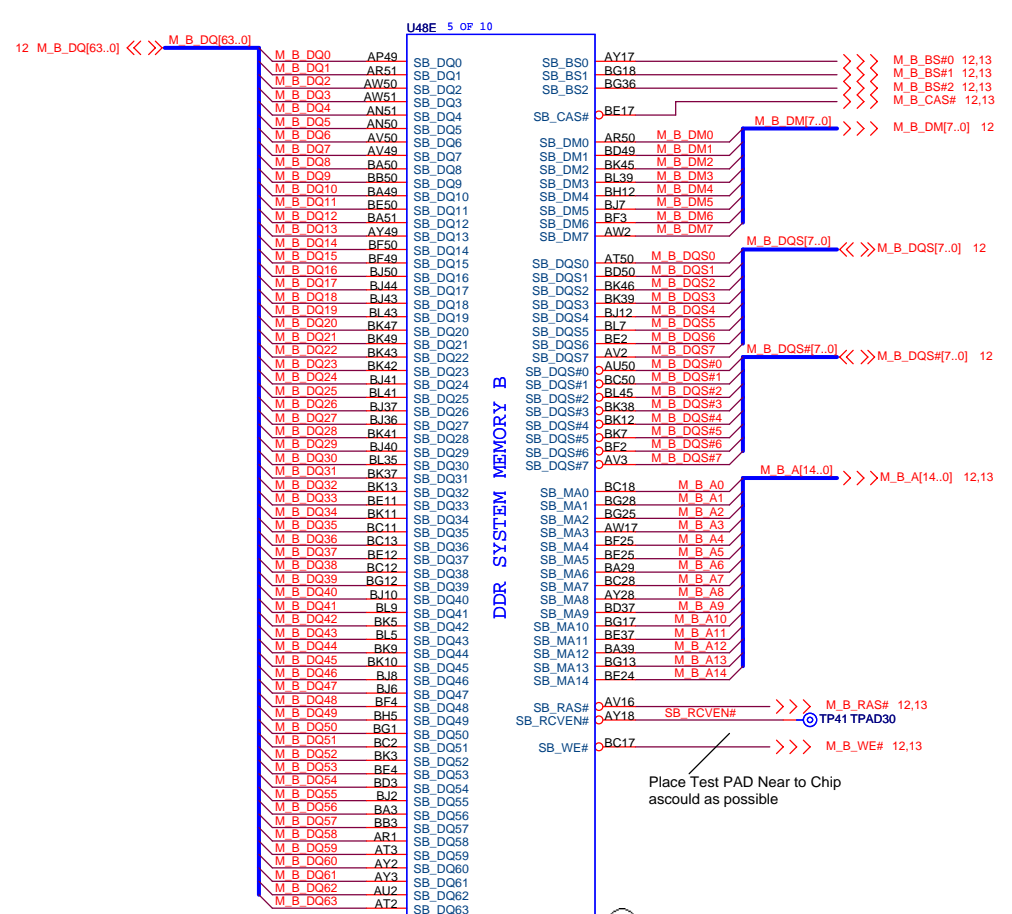
FOR Discrete change R137,  
R139 & R142 to 0 ohm

Wistron Corporation logo and contact information, including address and date: Monday, February 26, 2007.



DDR SYSTEM MEMORY A

CRESTLINE-GP-U

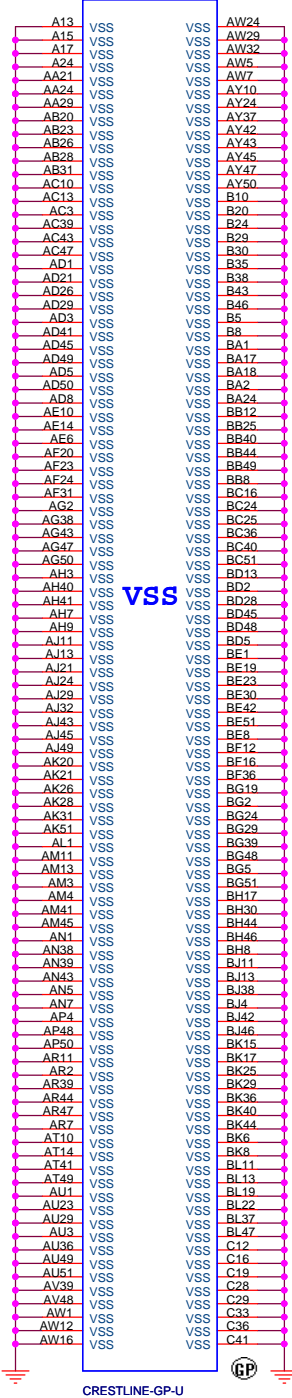


DDR SYSTEM MEMORY B

CRESTLINE-GP-U

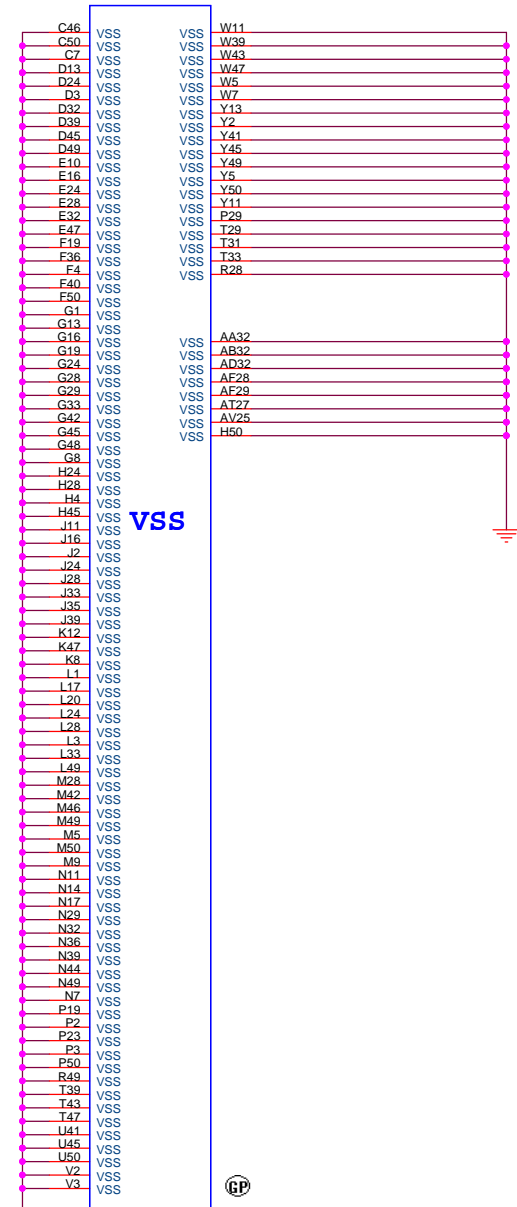






VSS

CRESTLINE-GP-U



VSS

CRESTLINE-GP-U

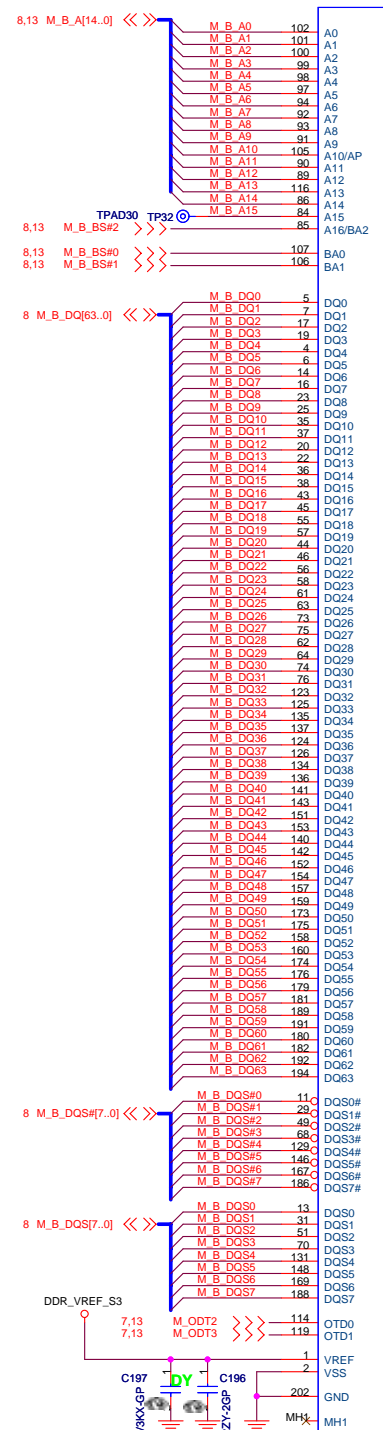


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 Taipei Hsien 221, Taiwan, R.O.C.

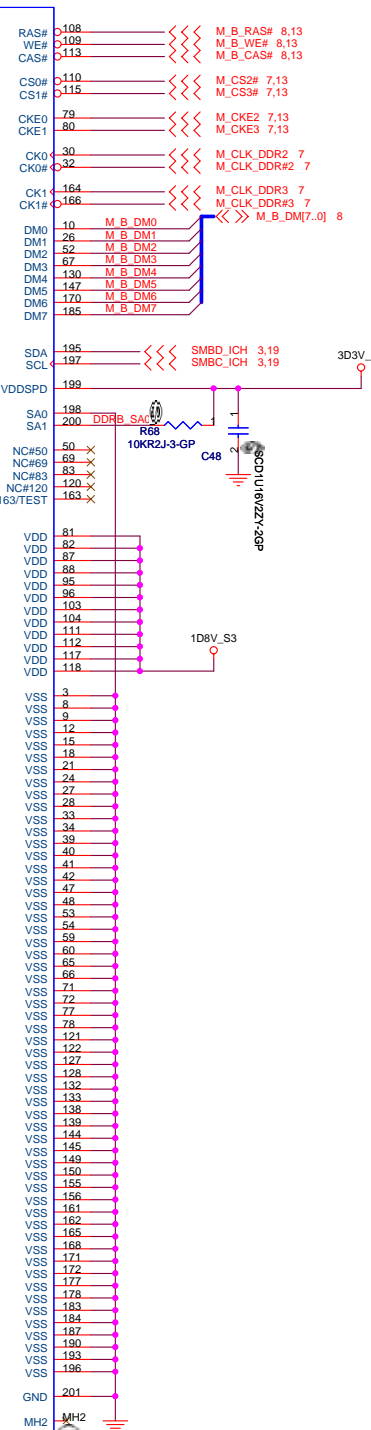
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Size: Document Number Rev: -1

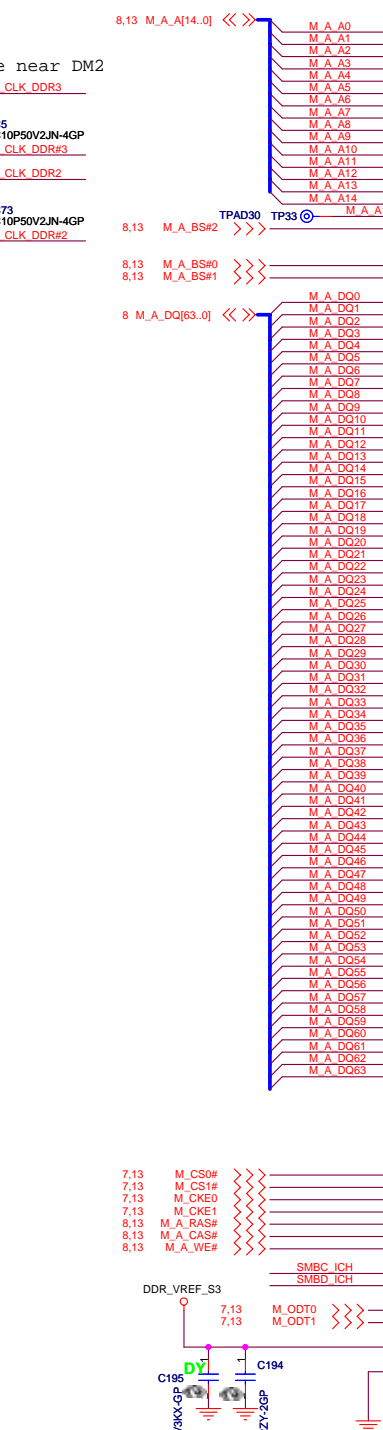
Date: Monday, February 26, 2007 Sheet 11 of 45



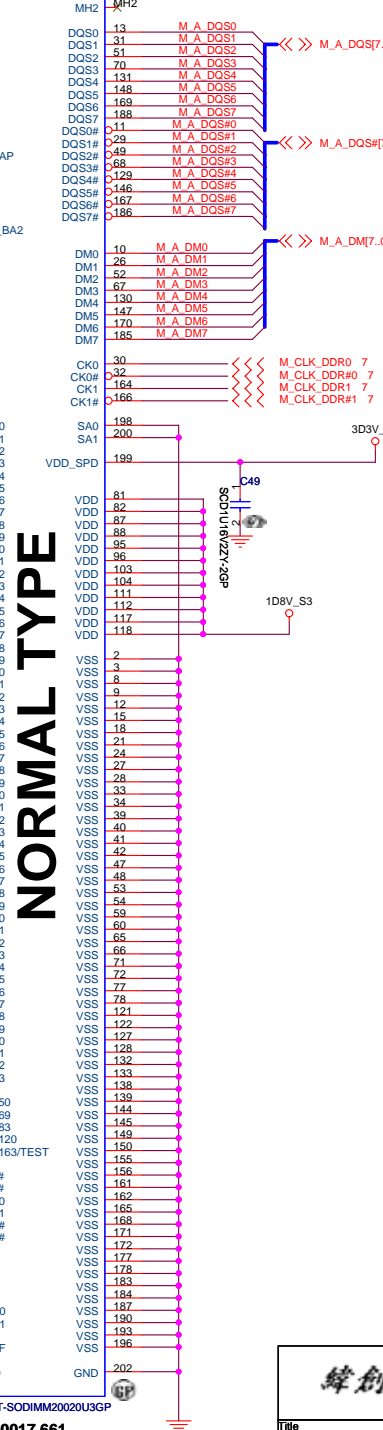
NORMAL TYPE



NORMAL TYPE



NORMAL TYPE



NORMAL TYPE



DDR2-200P-22-GP-U1  
62.10017.A61  
High 9.2mm

SKT-SODIMM200U3GP  
62.10017.661  
High 5.2mm

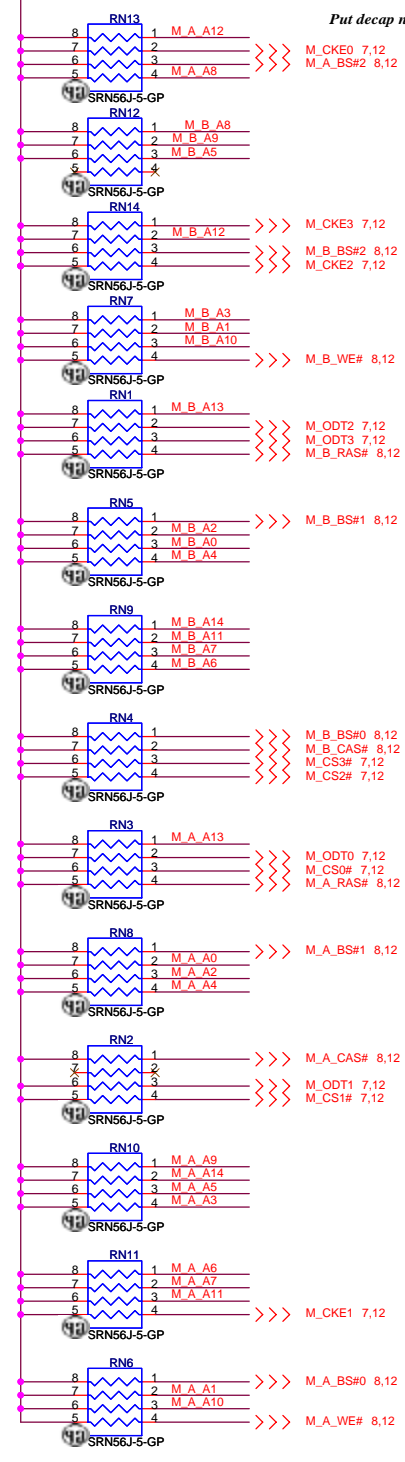
緯創資通 Wistron Corporation  
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Title: **DDR2 Socket**

Size: Document Number: Columbia/Tangiz

Date: Monday, February 26, 2007 Sheet 12 of 45

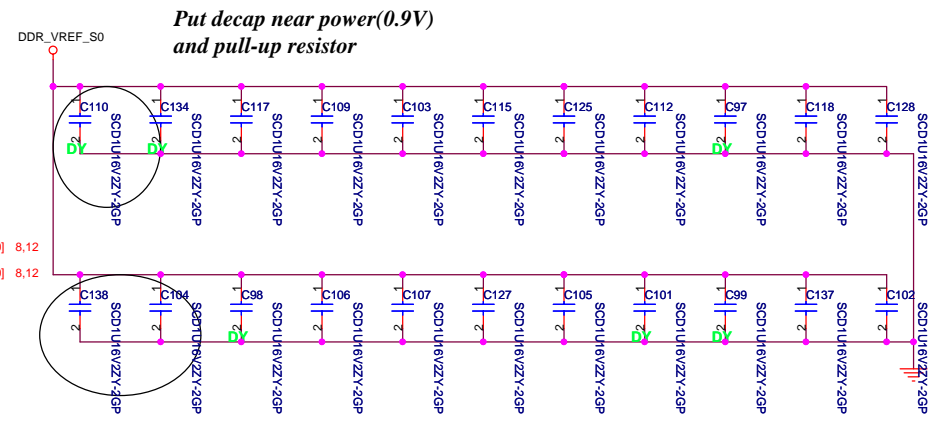
# PARALLEL TERMINATION



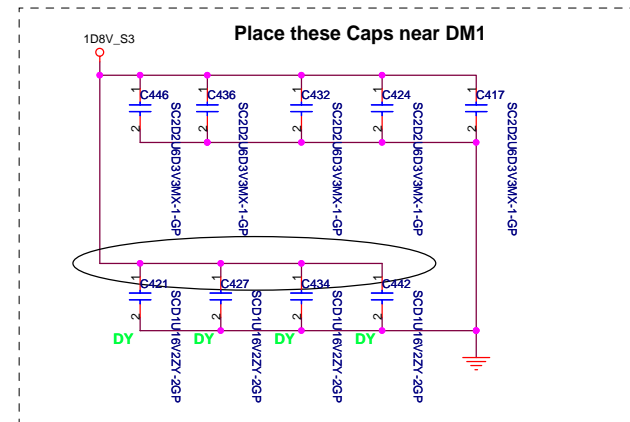
Put decap near power(0.9V) and pull-up resistor

M\_A\_A[14..0] <<< M\_A\_A[14..0] 8,12  
M\_B\_A[14..0] <<< M\_B\_A[14..0] 8,12

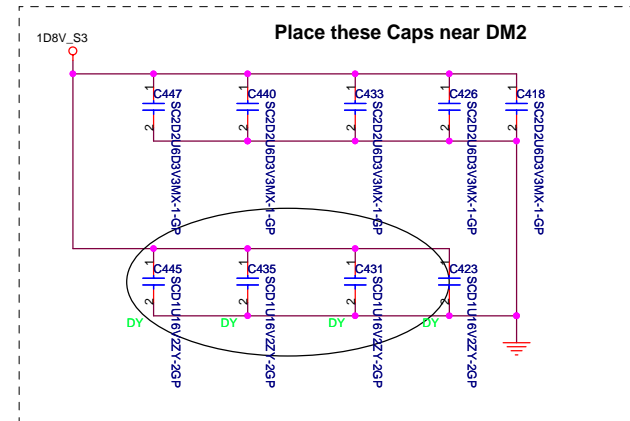
# Decoupling Capacitor



Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2

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Title: **DDR2 Termination Resistor**

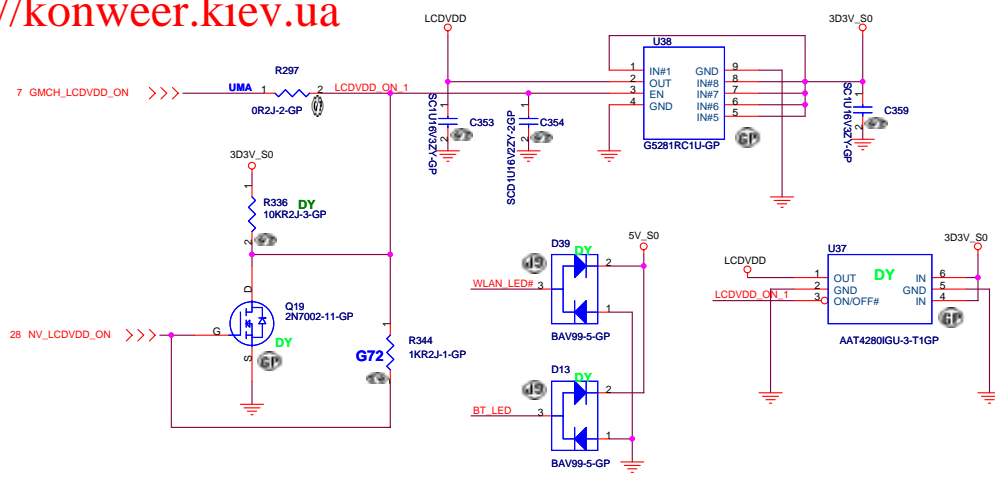
Size: Document Number

Date: Monday, February 26, 2007

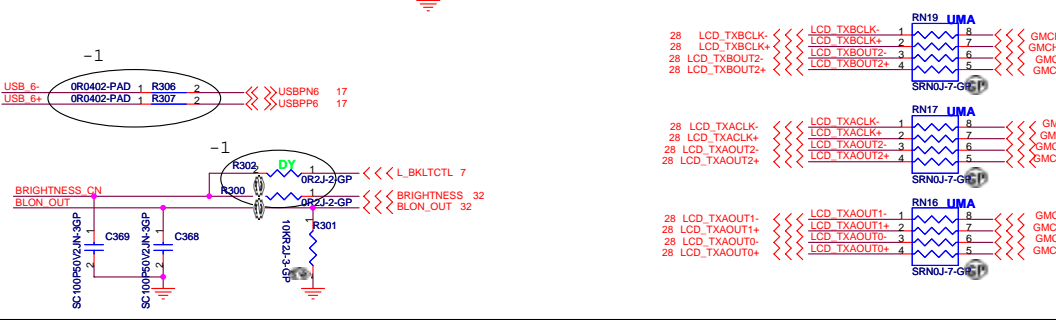
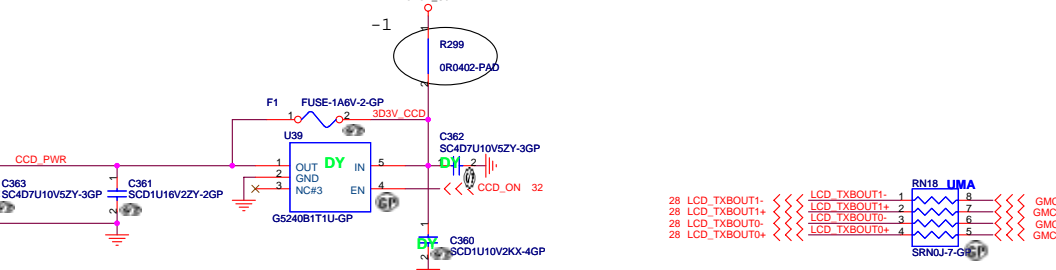
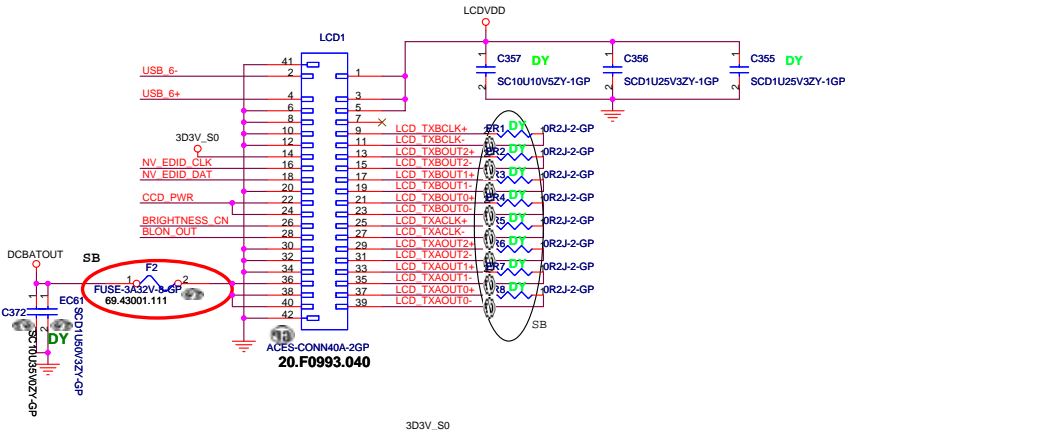
Sheet 13 of 45

Rev -1

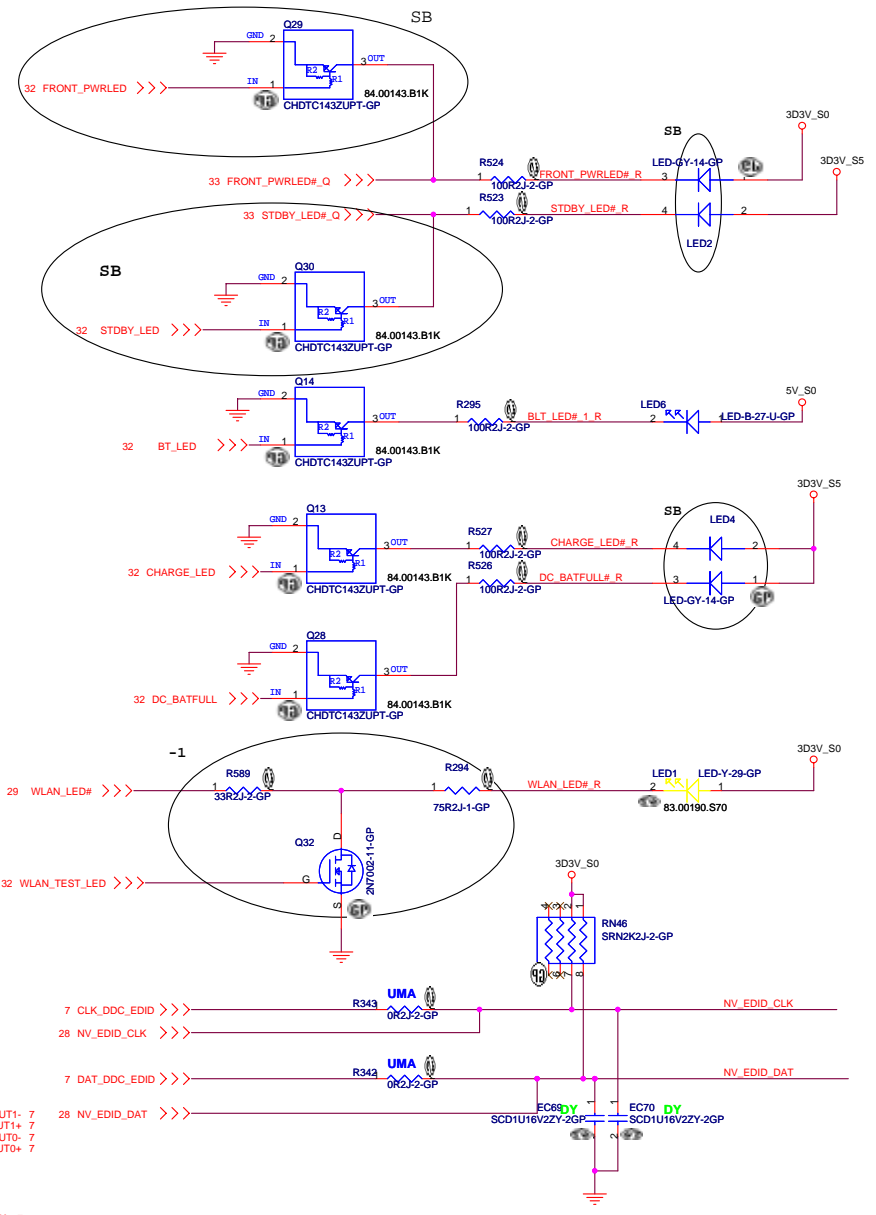
Columbia/Tangiz



### LCD/INVERTER CONN



- 28 LCD\_TXBOUT1- <<< LCD\_TXBOUT1- 8 <<< GMCH\_TXBOUT1- 7
- 28 LCD\_TXBOUT1+ <<< LCD\_TXBOUT1+ 7 <<< GMCH\_TXBOUT1+ 7
- 28 LCD\_TXBOUT0- <<< LCD\_TXBOUT0- 6 <<< GMCH\_TXBOUT0- 7
- 28 LCD\_TXBOUT0+ <<< LCD\_TXBOUT0+ 5 <<< GMCH\_TXBOUT0+ 7
- 28 LCD\_TXBCLK- <<< LCD\_TXBCLK- 1 8 <<< GMCH\_TXBCLK- 7
- 28 LCD\_TXBCLK+ <<< LCD\_TXBCLK+ 2 7 <<< GMCH\_TXBCLK+ 7
- 28 LCD\_TXBOUT2- <<< LCD\_TXBOUT2- 3 6 <<< GMCH\_TXBOUT2- 7
- 28 LCD\_TXBOUT2+ <<< LCD\_TXBOUT2+ 4 5 <<< GMCH\_TXBOUT2+ 7
- 28 LCD\_TXACLK- <<< LCD\_TXACLK- 1 8 <<< GMCH\_TXACLK- 7
- 28 LCD\_TXACLK+ <<< LCD\_TXACLK+ 2 7 <<< GMCH\_TXACLK+ 7
- 28 LCD\_TXAOUT2- <<< LCD\_TXAOUT2- 3 6 <<< GMCH\_TXAOUT2- 7
- 28 LCD\_TXAOUT2+ <<< LCD\_TXAOUT2+ 4 5 <<< GMCH\_TXAOUT2+ 7
- 28 LCD\_TXAOUT1- <<< LCD\_TXAOUT1- 1 8 <<< GMCH\_TXAOUT1- 7
- 28 LCD\_TXAOUT1+ <<< LCD\_TXAOUT1+ 2 7 <<< GMCH\_TXAOUT1+ 7
- 28 LCD\_TXAOUT0- <<< LCD\_TXAOUT0- 3 6 <<< GMCH\_TXAOUT0- 7
- 28 LCD\_TXAOUT0+ <<< LCD\_TXAOUT0+ 4 5 <<< GMCH\_TXAOUT0+ 7



<Variant Name>

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File: **LCD CONN & LED**

Size: Document Number

Date: Monday, February 26, 2007

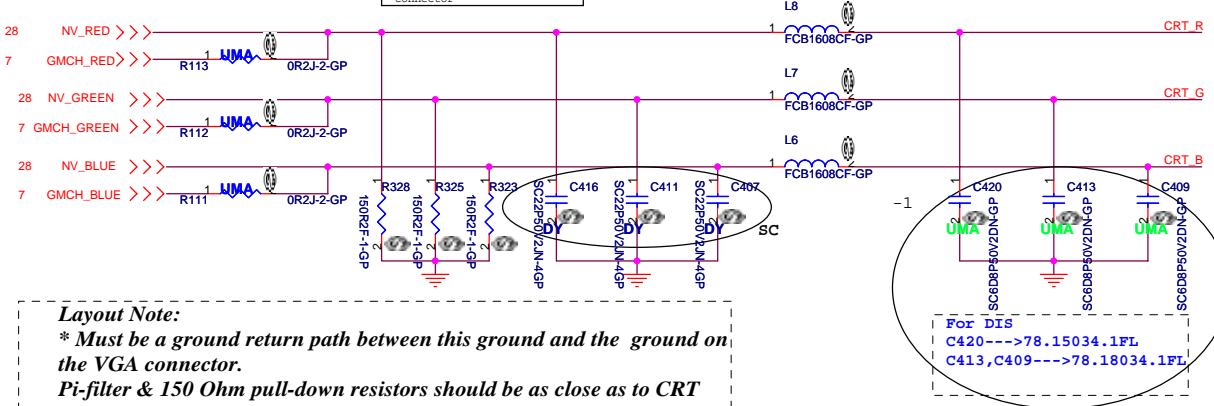
Sheet 14 of 45

Rev -1

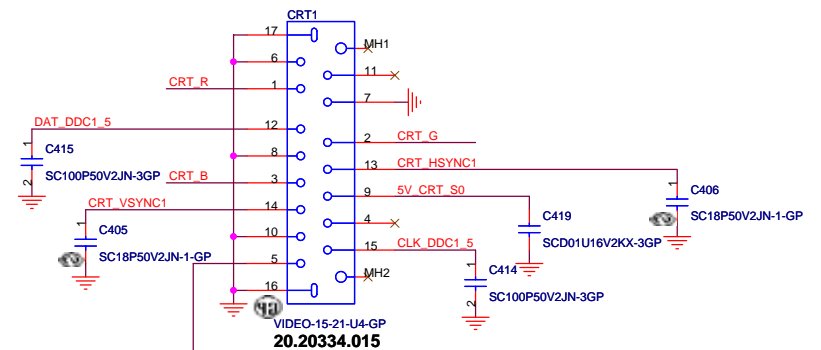
Columbia/Tangiz

Layout Note:  
Place these resistors  
close to the CRT-out  
connector

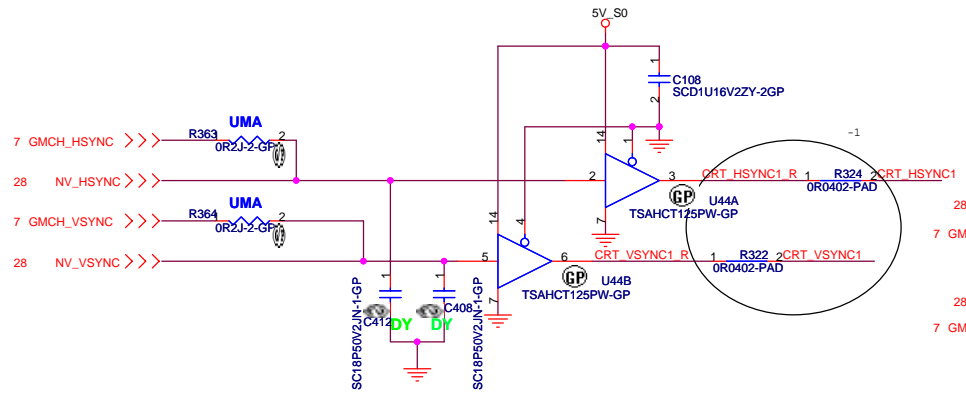
Ferrite bead impedance: 10 ohm@100MHz



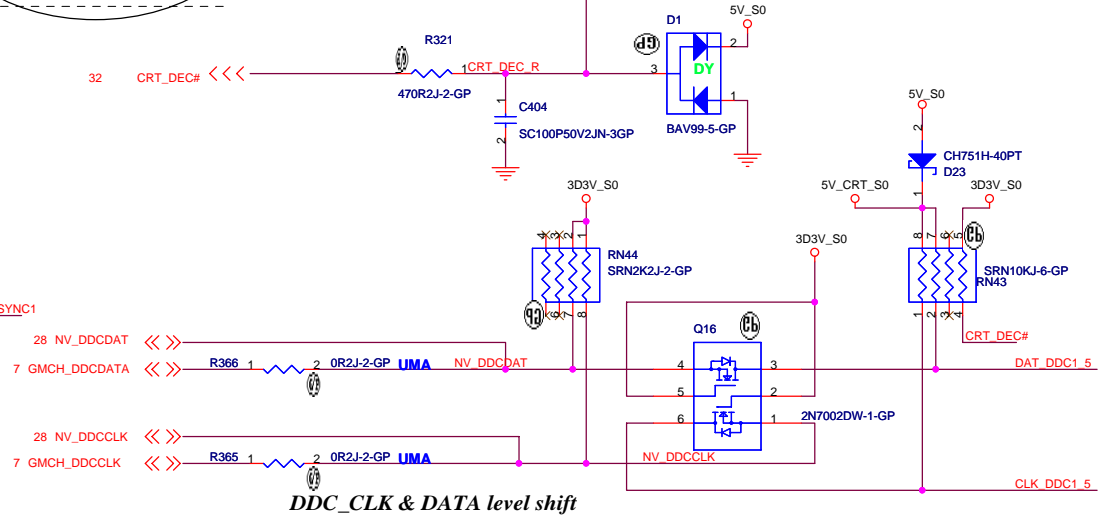
**Layout Note:**  
 \* Must be a ground return path between this ground and the ground on the VGA connector.  
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



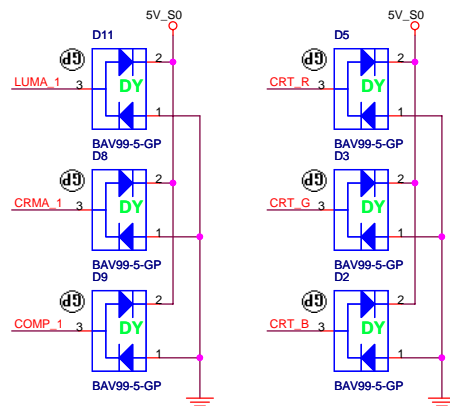
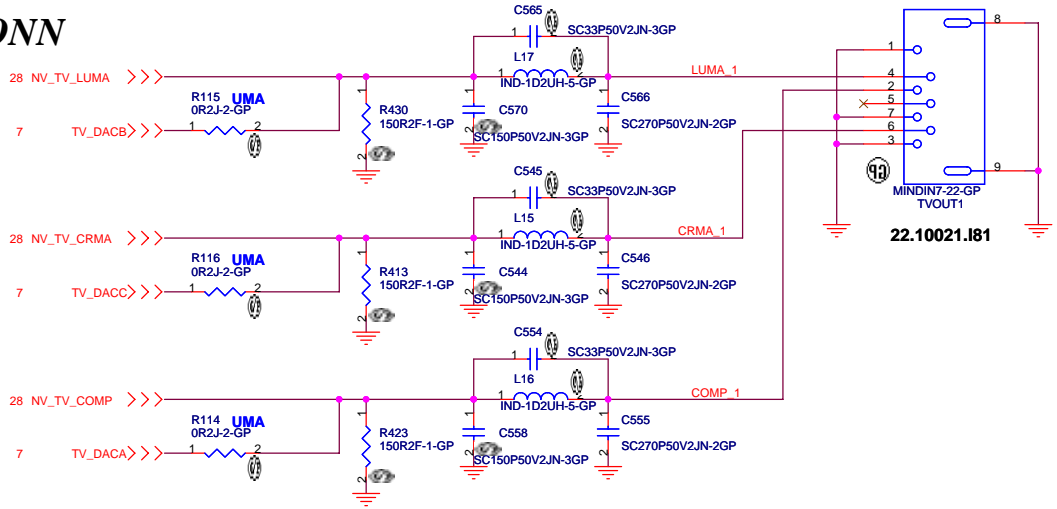
### Hsync & Vsync level shift



### DDC\_CLK & DATA level shift



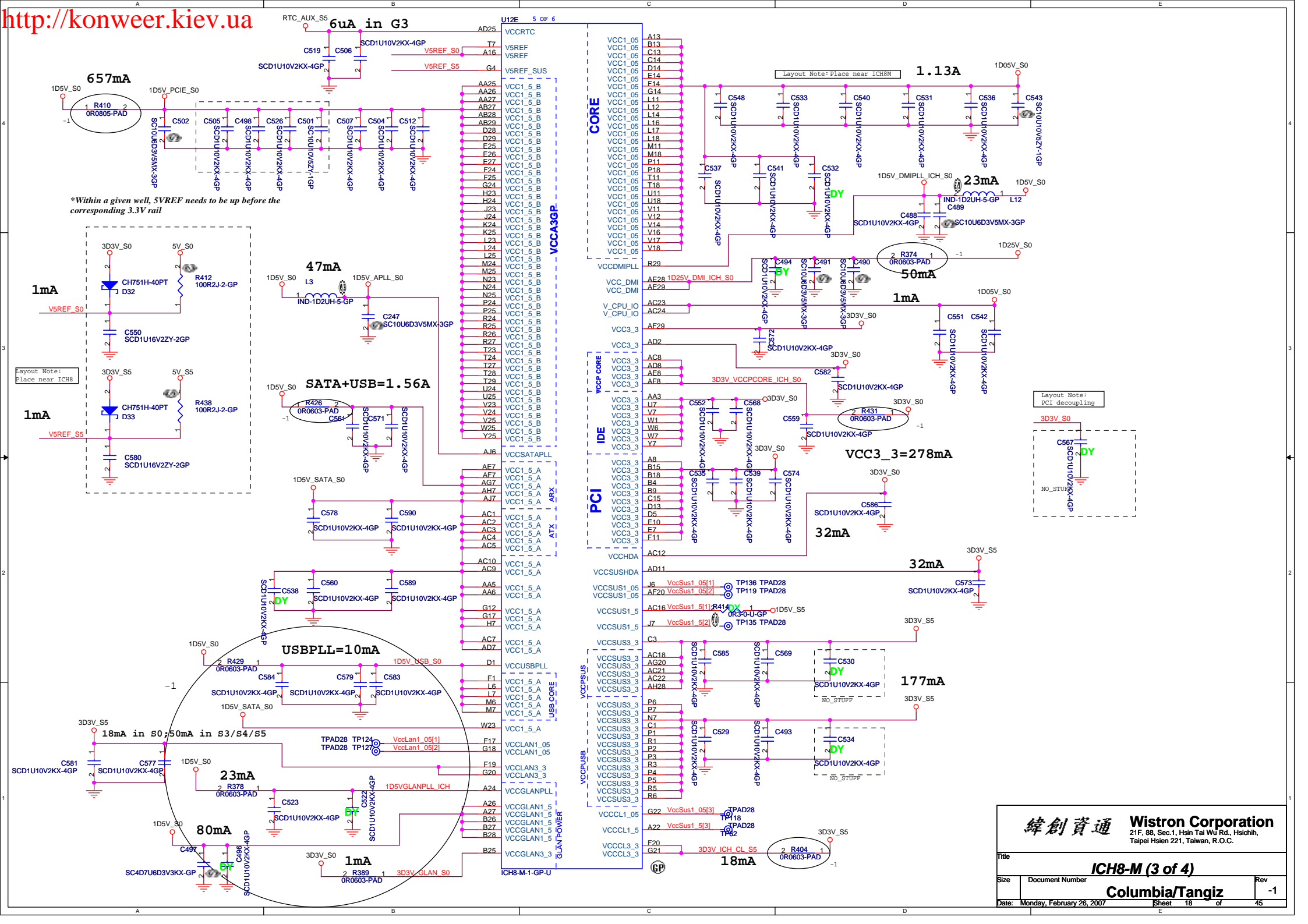
## TV CONN



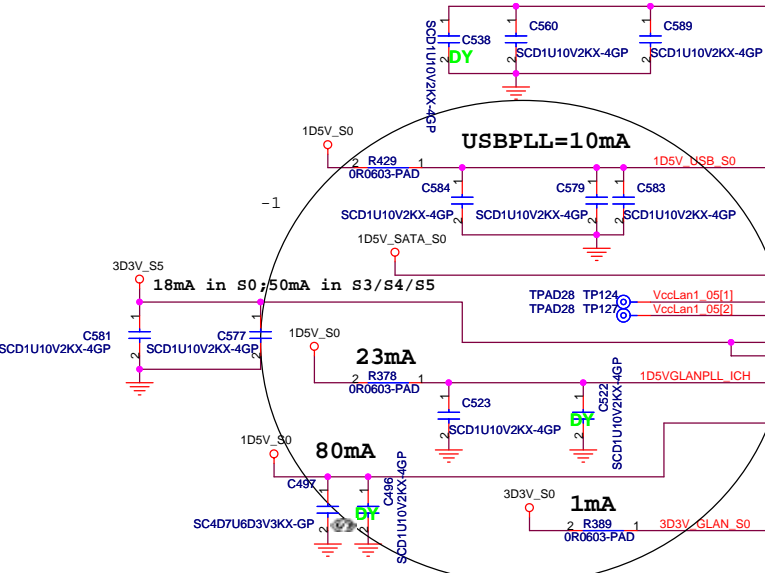
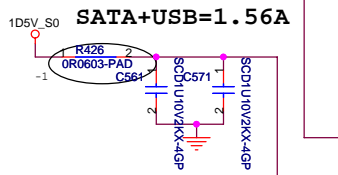
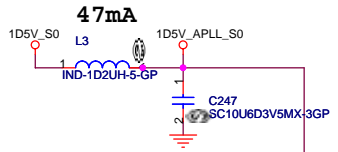
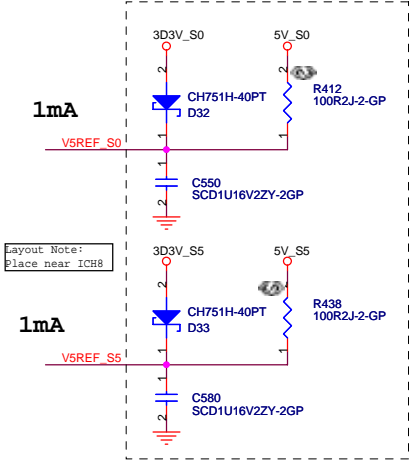
<b>緯創資通 Wistron Corporation</b>	
<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title <b>CRT/TV Connector</b>	
Size	Document Number
Columbia/Tangiz	
Date: Monday, February 26, 2007	Rev -1







\*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail



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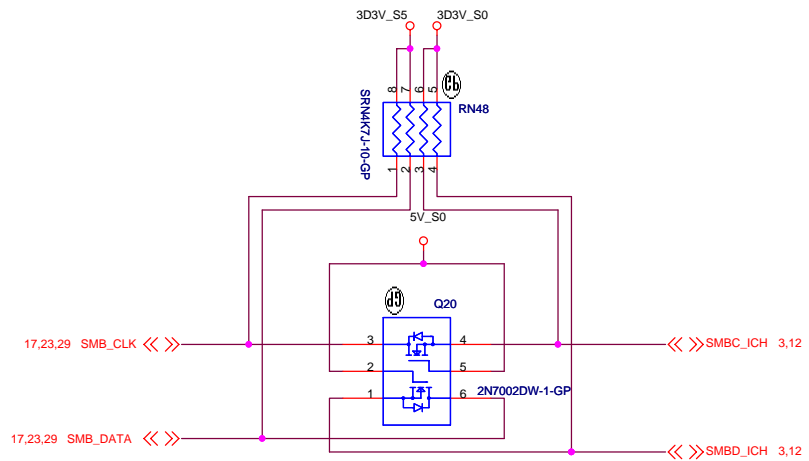
File	IC8-M (3 of 4)	
Size	Document Number	Rev
Date	Monday, February 26, 2007	Sheet 18 of 45

Columbia/Tangiz -1

U12F 6 OF 6

A23	VSS	K7
A5	VSS	L1
A2	VSS	L13
AA7	VSS	L15
A25	VSS	L26
AB1	VSS	L27
AB24	VSS	L4
AC11	VSS	L5
AC14	VSS	M12
AC25	VSS	M13
AC26	VSS	M14
AC27	VSS	M15
AD17	VSS	M16
AD20	VSS	M17
AD28	VSS	M23
AD29	VSS	M28
AD3	VSS	M29
AD4	VSS	M3
AD6	VSS	N1
AE1	VSS	N11
AE12	VSS	N12
AE2	VSS	N13
AE22	VSS	N14
AD1	VSS	N15
AE25	VSS	N16
AE5	VSS	N17
AE6	VSS	N18
AE9	VSS	N26
AF14	VSS	N27
AF16	VSS	N4
AF18	VSS	N5
AF3	VSS	N6
AF4	VSS	P12
AG5	VSS	P13
AG6	VSS	P14
AH10	VSS	P15
AH13	VSS	P16
AH16	VSS	P17
AH19	VSS	P23
AH2	VSS	P28
AE28	VSS	P29
AH22	VSS	R11
AH24	VSS	R12
AH26	VSS	R13
AH3	VSS	R14
AH4	VSS	R15
AH8	VSS	R16
AJ5	VSS	R17
B11	VSS	R18
B14	VSS	R28
B17	VSS	R4
B2	VSS	T12
B20	VSS	T13
B22	VSS	T14
B3	VSS	T15
C24	VSS	T16
C26	VSS	T17
C27	VSS	T2
C6	VSS	U12
D12	VSS	U13
D15	VSS	U14
D18	VSS	U15
D2	VSS	U16
D4	VSS	U17
E21	VSS	U23
E24	VSS	U26
E4	VSS	U27
E9	VSS	U3
F15	VSS	U5
E23	VSS	V13
F28	VSS	V15
F29	VSS	V28
F7	VSS	V29
G1	VSS	W2
F2	VSS	W26
G10	VSS	W27
G13	VSS	Y28
G19	VSS	Y29
G23	VSS	Y4
G25	VSS	AB4
G26	VSS	AB23
G27	VSS	AB5
H25	VSS	AB6
H28	VSS	AD5
H29	VSS	U4
H3	VSS	W24
H6	VSS	A1
J1	VSS	A2
J25	VSS	A28
J26	VSS	A29
J27	VSS	AJ28
J4	VSS	AH1
J5	VSS	AH29
K23	VSS	AJ1
K28	VSS	AJ2
K29	VSS	AJ29
K3	VSS	B1
K6	VSS	B29
	VSS	A1
	VSS	A2
	VSS	A28
	VSS	A29
	VSS	AJ28
	VSS	AH1
	VSS	AH29
	VSS	AJ1
	VSS	AJ2
	VSS	AJ29
	VSS	B1
	VSS	B29

ICH8-M-1-GP-U

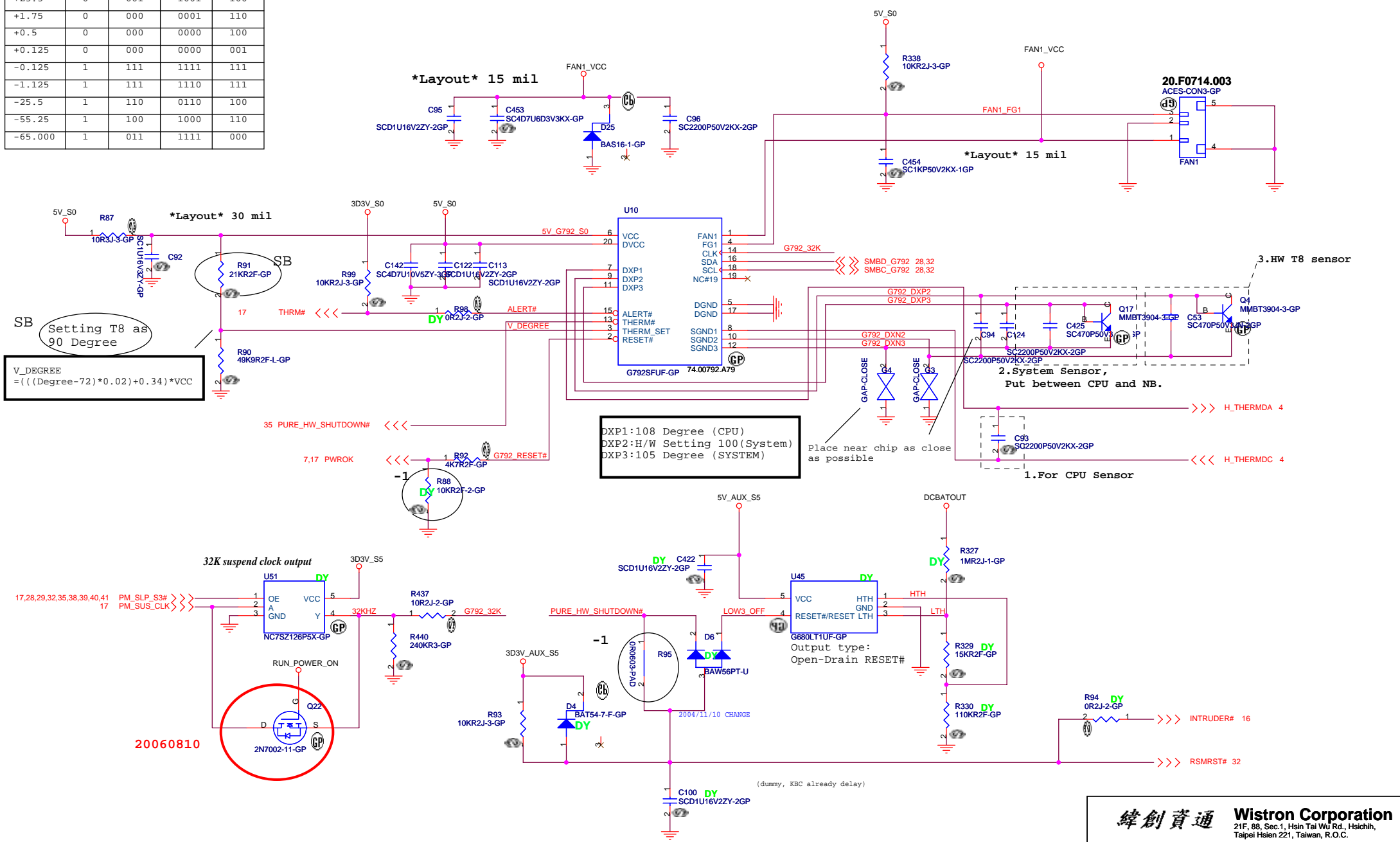


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBUS 2.0 compliance

SMBUS

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<p>Title</p> <p><b>ICH8-M (4 of 4)</b></p>	
Size	Document Number
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Sheet 19	of 45

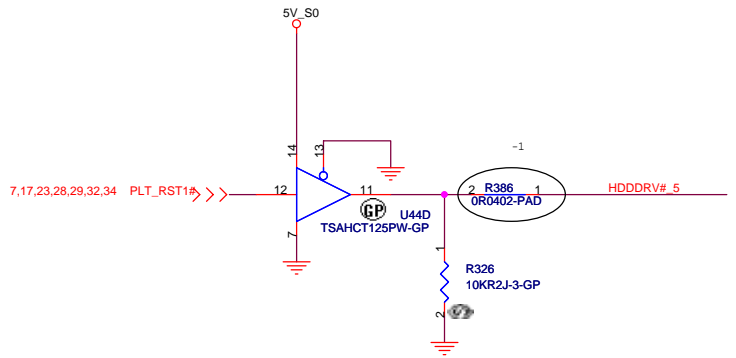
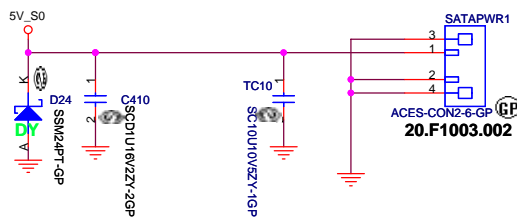
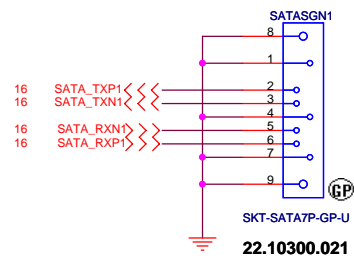
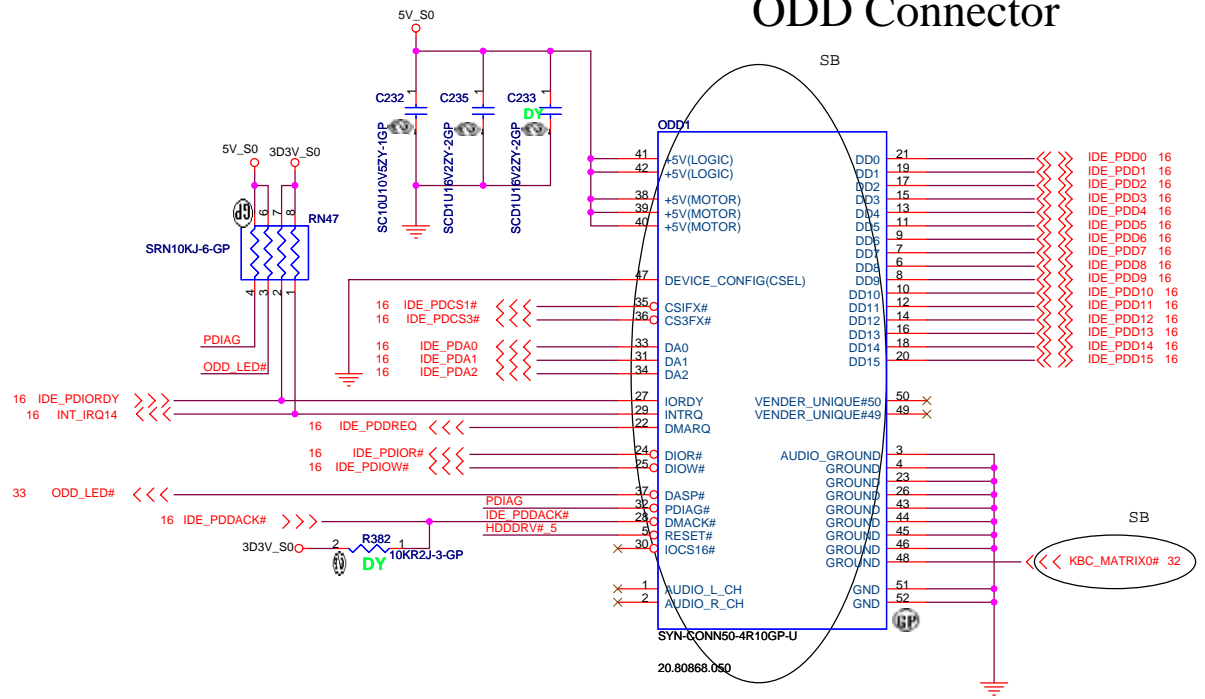
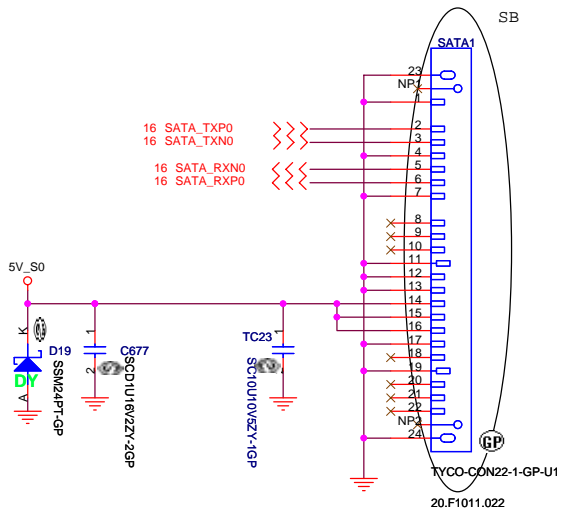
TEMP.	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



SB  
Setting T8 as 90 Degree

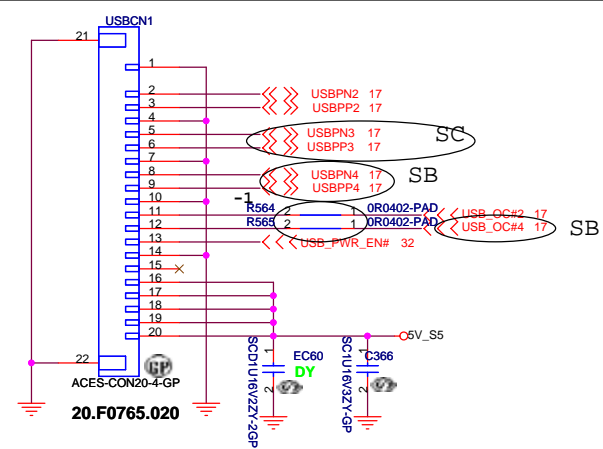
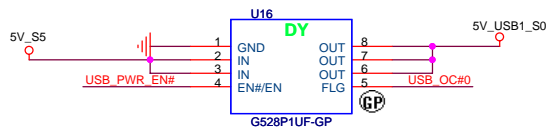
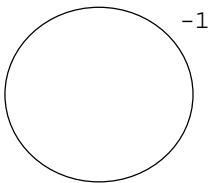
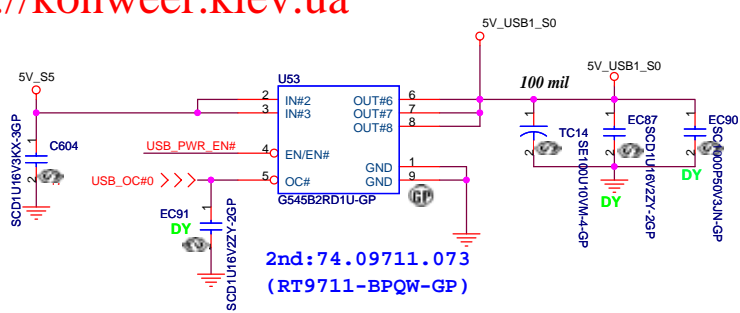
$$V\_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

DXP1:108 Degree (CPU)  
DXP2:H/W Setting 100(System)  
DXP3:105 Degree (SYSTEM)

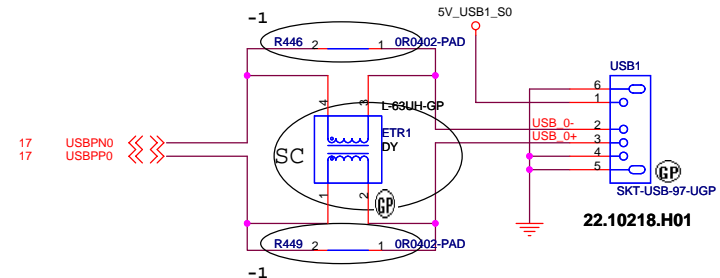
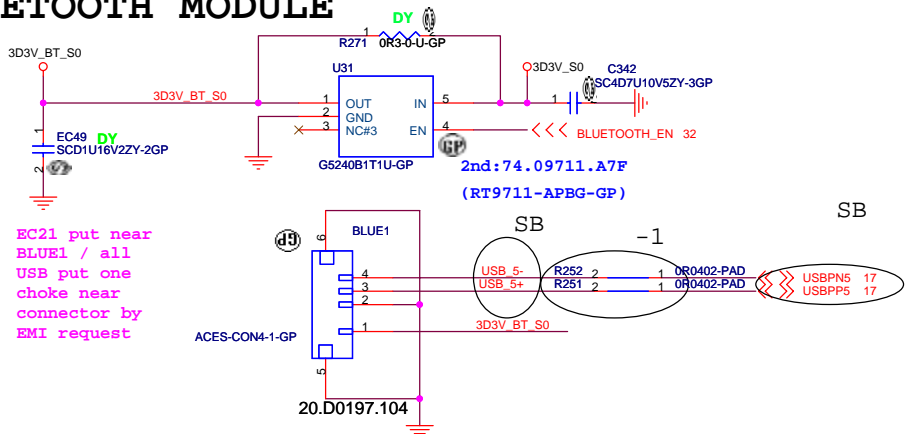


bom1

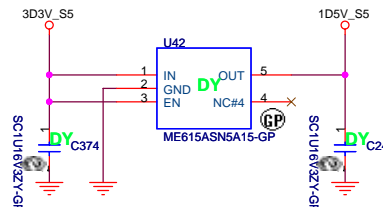
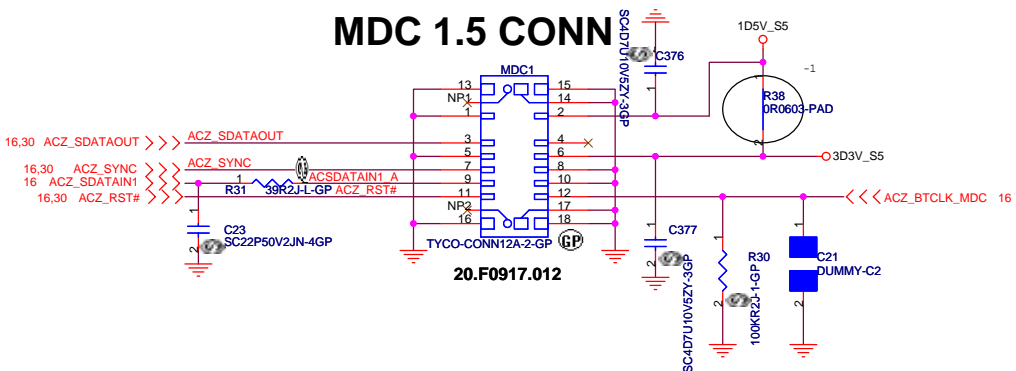
<b>緯創資通 Wistron Corporation</b>	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>HDD and CDROM</b>	
Title	Document Number
<b>Columbia/Tangiz</b>	
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**BLUETOOTH MODULE**



**MDC 1.5 CONN**



bom1

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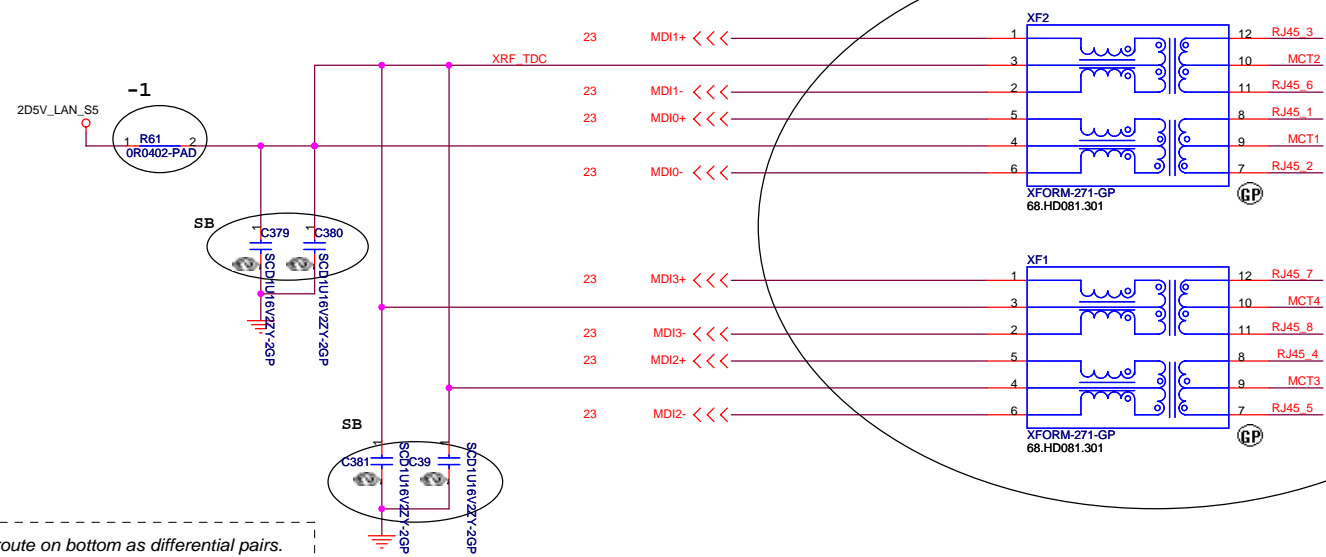
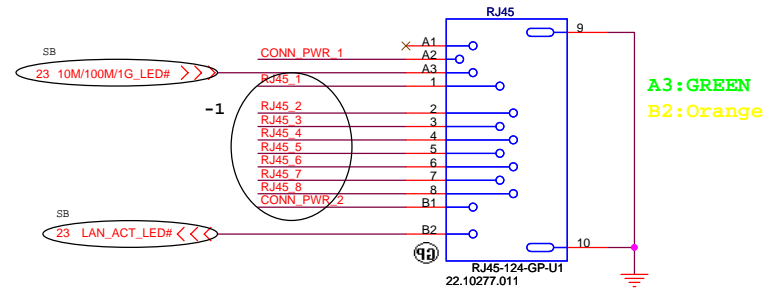
File		
<b>USB / MDC / BLUETOOTH</b>		
Size	Document Number	Rev
		<b>-1</b>
Date: Monday, February 26, 2007	Sheet 22	of 45



# LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

## GIGA Lan Transformer



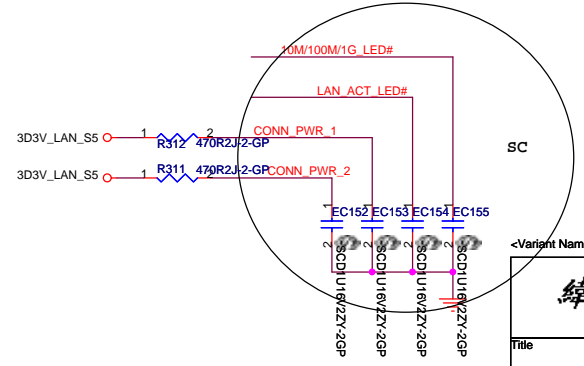
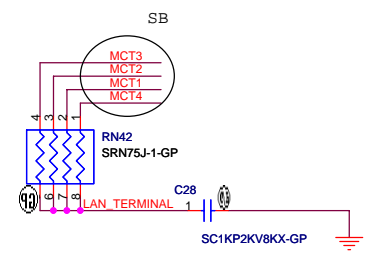
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits  
LAN Data: Yellow(B2), when LAN is transferring data.

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

**RJ11 signal must leave the other signal or power plane 100mil.**

DOC\_TIP,DOC\_RING,TIP,RING:  
W/S : 10/100 @ Surface layers  
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



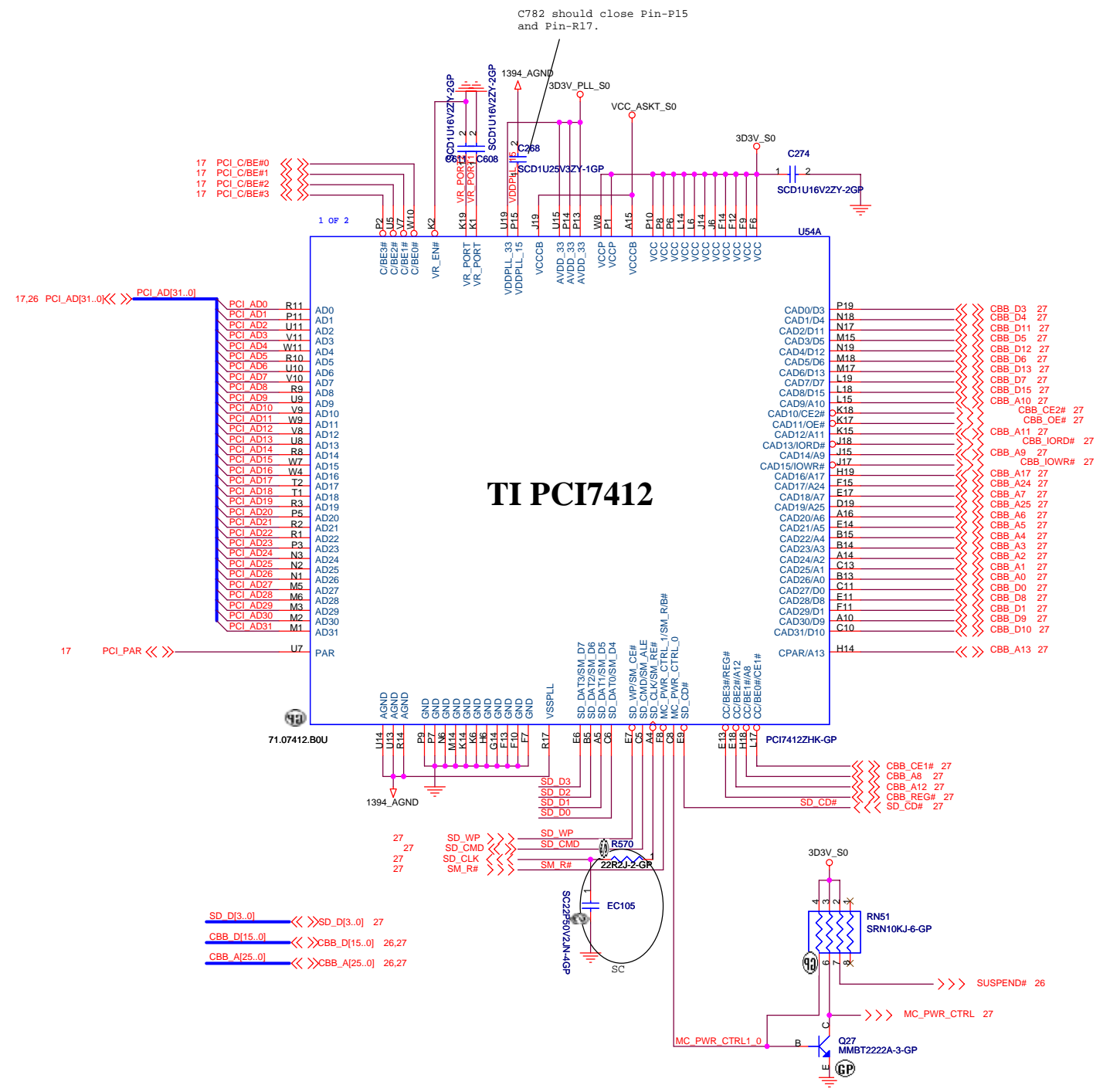
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector

Size A3 Document Number Columbia/Tangiz Rev -1

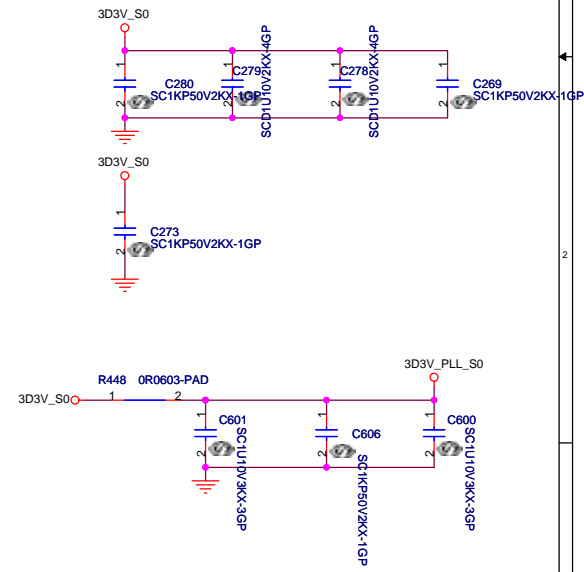
Date: Monday, February 26, 2007 Sheet 24 of 45

C782 should close Pin-P15 and Pin-R17.



\* All 1394 signals must be routed on top side only  
 \* Differential pairs of each ports should have equal trace length  
 \* Stubs must be keep as short as possible

Bypass/Decoupling Capacitors  
 Should be places as close to  
 PCI7412 as possible



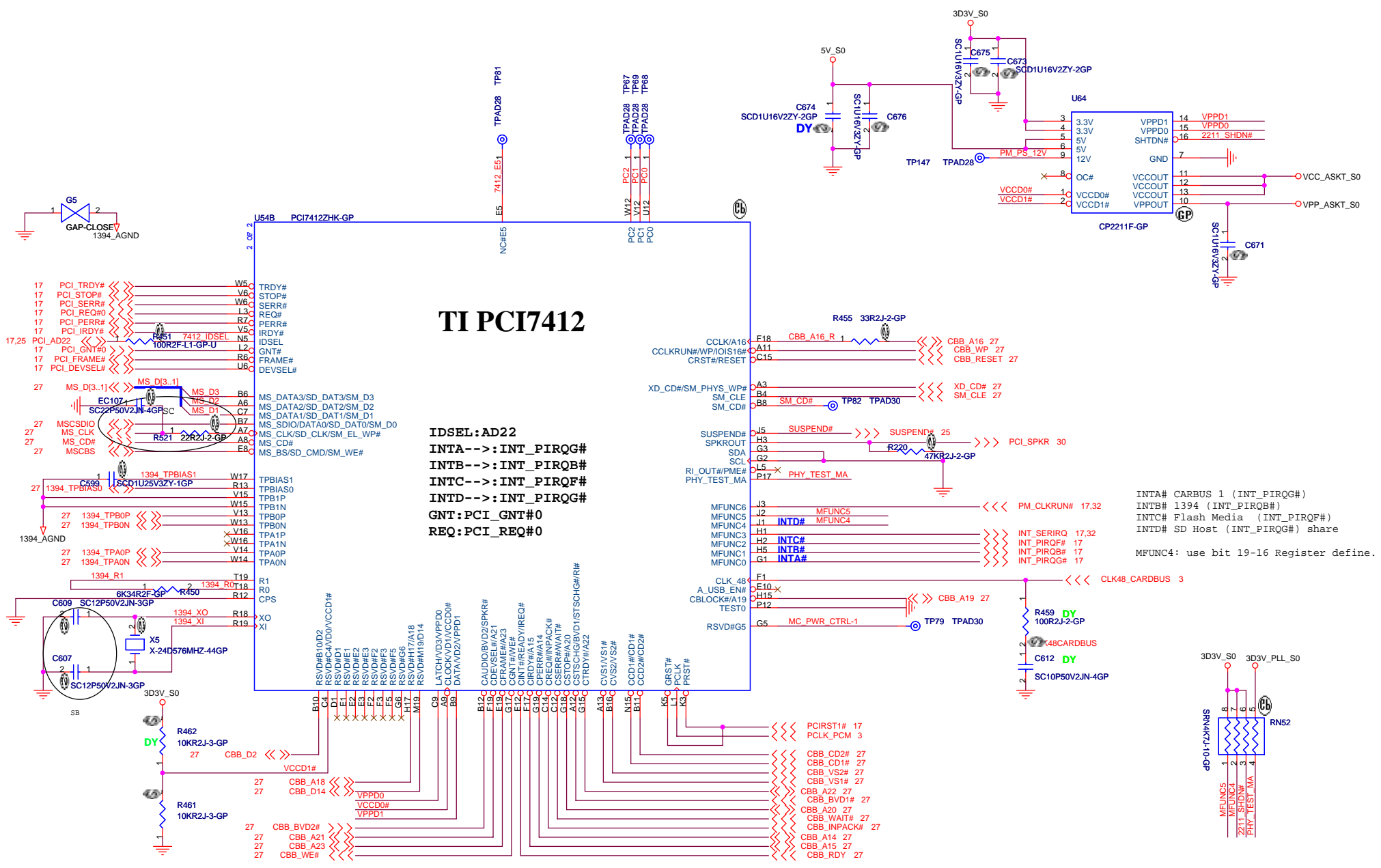
<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **TI PCI7412 (1 of 2)**

Size: Document Number: Columbia/Tangiz Rev: -1

Date: Monday, February 26, 2007 Sheet 25 of 45



# TI PCI7412

**IDSEL: AD22**  
**INTA-->: INT\_PIRQ#**  
**INTB-->: INT\_PIRQ#**  
**INTC-->: INT\_PIRQ#**  
**INTD-->: INT\_PIRQ#**  
**GNT: PCI\_GNT#0**  
**REQ: PCI\_REQ#0**

<Variant Name>

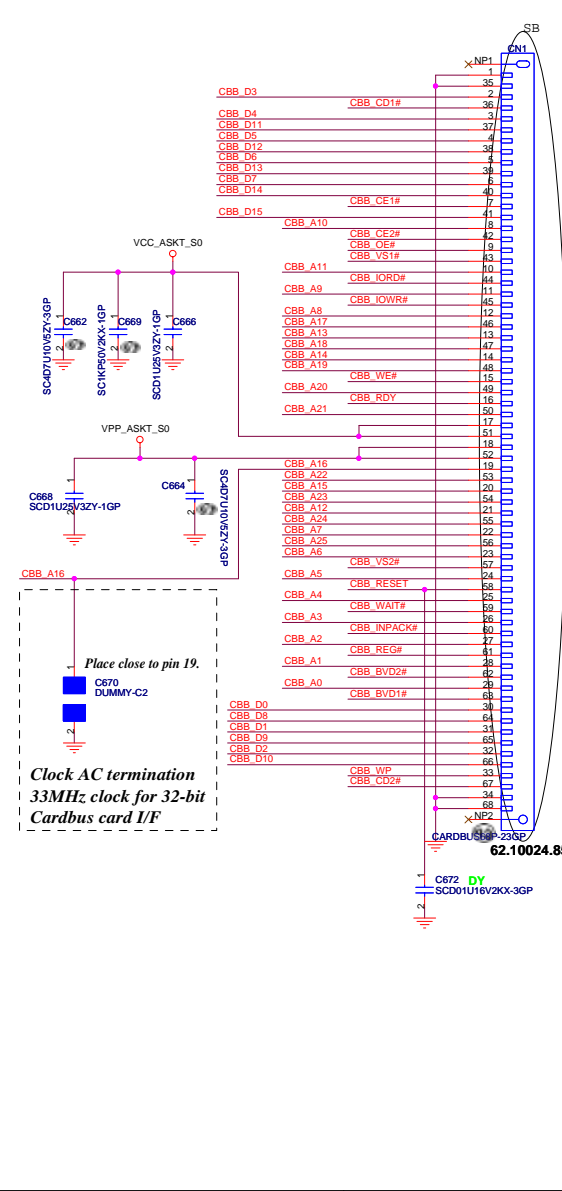
**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **TI PCI7412 (2 of 2)**

Size: Document Number Rev: -1

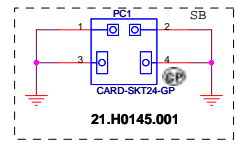
Date: Monday, February 26, 2007 Sheet 26 of 45

# PCMCIA Socket



## Cardbus I/F

- CBB\_D[15..0] <<>> CBB\_D[15..0] 25,26
- CBB\_A[25..0] <<>> CBB\_A[25..0] 25,26
- CBB\_IORD# 25
- CBB\_IOWR# 25
- CBB\_OE# 25
- CBB\_WE# 26
- CBB\_REG# 25
- CBB\_RDY 26
- CBB\_WP 26
- CBB\_RESET 26
- CBB\_WAIT# 26
- CBB\_INPACK# 26
- CBB\_CE1# 25
- CBB\_CE2# 25
- CBB\_BVD1# 26
- CBB\_BVD2# 26
- CBB\_CD1# 26
- CBB\_CD2# 26
- CBB\_VS1# 26
- CBB\_VS2# 26

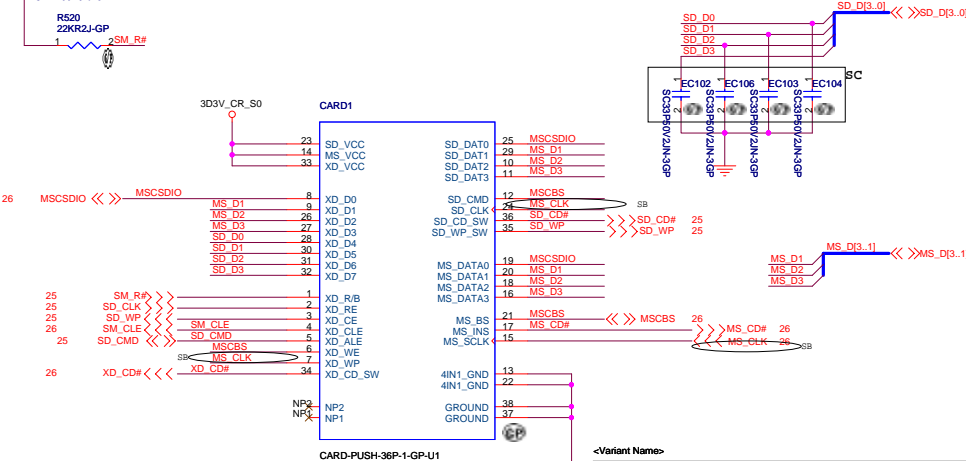
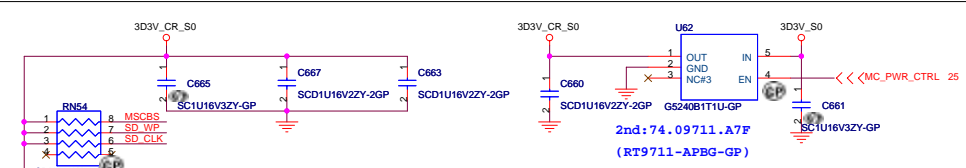
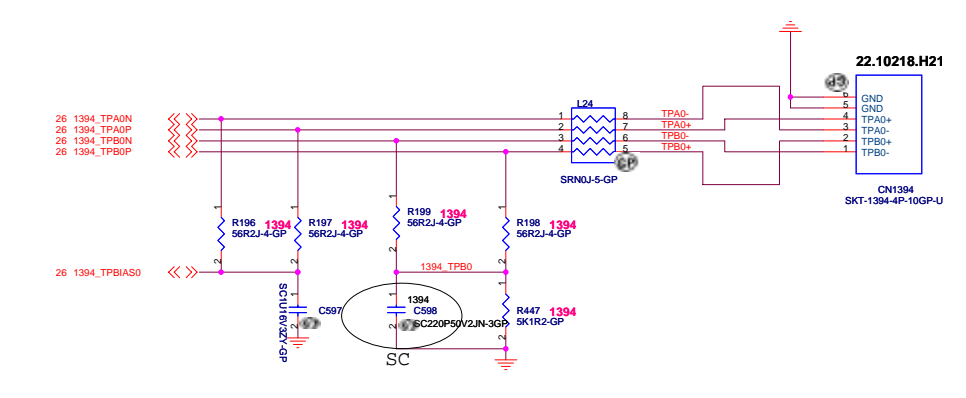


21.H0145.001

Place close to pin 19.

Clock AC termination  
33MHz clock for 32-bit  
Cardbus card I/F

# 1394 Connector



XD  
MS / MS PRO  
SD / SD IO / MMC

<Variant Name>

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien Z21, Taiwan, R.O.C.

Title: **PCMCIA / 1394 / CARD READER**

Size: Document Number  
Columbia/Tanqiz

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NV SMBus  
A(pin143&145) : VGA(CRT) / DOCK  
B(pin218&220) : DVI  
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

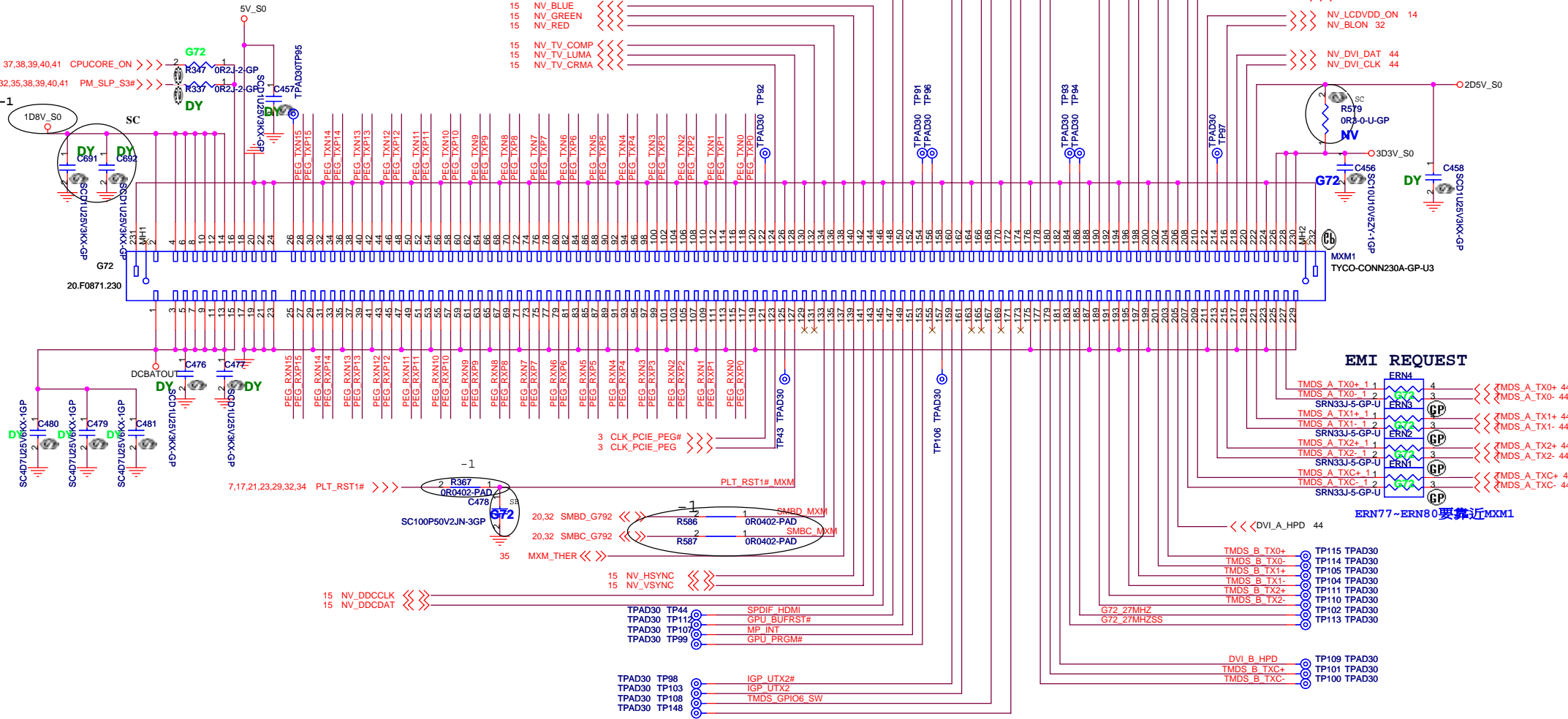
- 7 PEG\_TXP[15.0] <<<
- 7 PEG\_TXN[15.0] <<<
- 7 PEG\_RXP[15.0] <<<
- 7 PEG\_RXN[15.0] <<<

- 14 LCD\_TXBOUT0+
- 14 LCD\_TXBOUT1+
- 14 LCD\_TXBOUT1-
- 14 LCD\_TXBOUT2+
- 14 LCD\_TXBOUT2-

- 14 LCD\_TXBCLK+
- 14 LCD\_TXBCLK-
- 15 NV\_BLUE
- 15 NV\_GREEN
- 15 NV\_RED
- 15 NV\_TV\_COMP
- 15 NV\_TV\_LUMA
- 15 NV\_TV\_CRMA

- LCD\_TXACLK- 14
- LCD\_TXACLK+ 14
- LCD\_TXAOUT2- 14
- LCD\_TXAOUT2+ 14
- LCD\_TXAOUT1- 14
- LCD\_TXAOUT1+ 14
- LCD\_TXAOUT0- 14
- LCD\_TXAOUT0+ 14

- >>> NV\_EDID\_DAT 14
- >>> NV\_EDID\_CLK 14
- >>> NV\_LCDVDD\_ON 14
- >>> NV\_BLON 32
- >>> NV\_DVI\_DAT 44
- >>> NV\_DVI\_CLK 44



EMI REQUEST

- TMDS A\_TX0+ 1 4
- TMDS A\_TX0- 1 2
- SRN33J-5-GP-U 1 3
- TMDS A\_TX1+ 1 1
- TMDS A\_TX1- 1 2
- SRN33J-5-GP-U 1 3
- TMDS A\_TX2+ 1 1
- TMDS A\_TX2- 1 2
- SRN33J-5-GP-U 1 3
- TMDS A\_TXC+ 1 1
- TMDS A\_TXC- 1 2
- SRN33J-5-GP-U 1 3

ERN77~ERN80要靠近MXM1

- TPM15 TPAD30
- TPM14 TPAD30
- TPM05 TPAD30
- TPM04 TPAD30
- TPM11 TPAD30
- TPM10 TPAD30
- TPM02 TPAD30
- TPM13 TPAD30

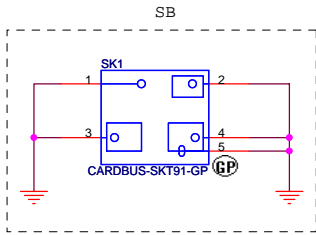
- DVI B HPD
- TMDS B\_TXC+
- TMDS B\_TXC-

<Core Design>

緯創資通 Wistron Corporation  
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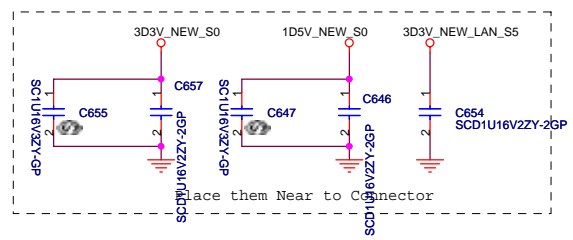
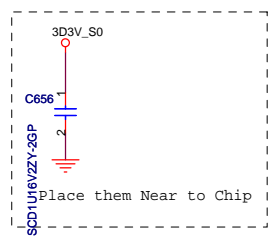
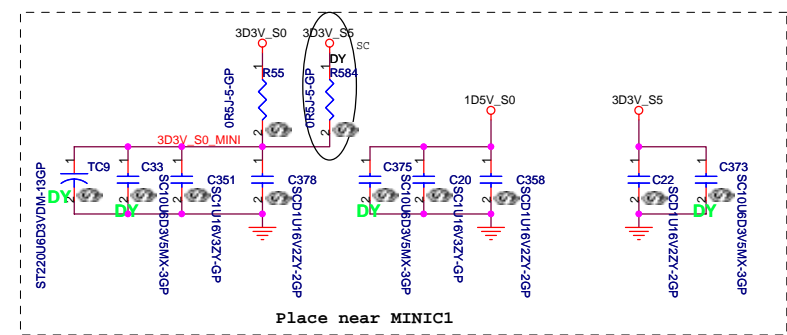
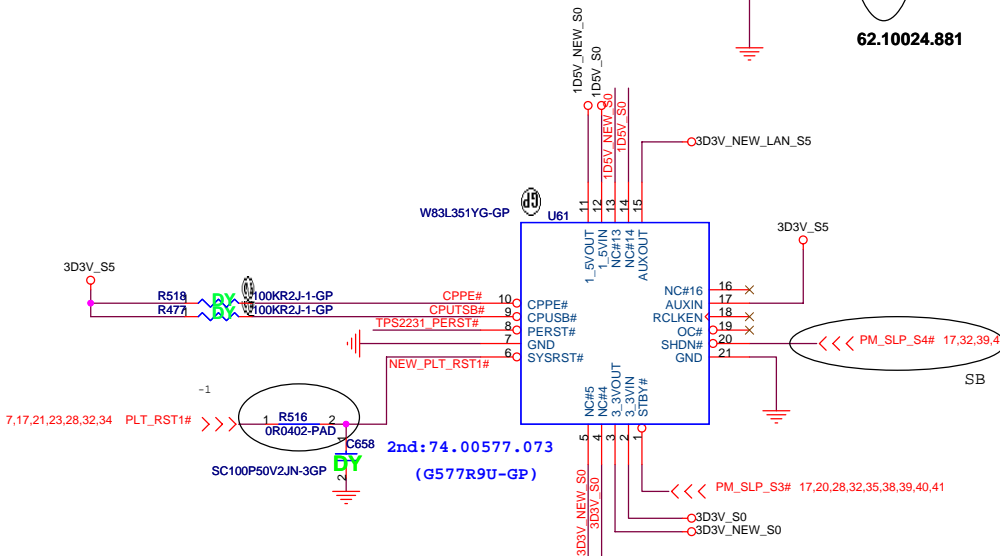
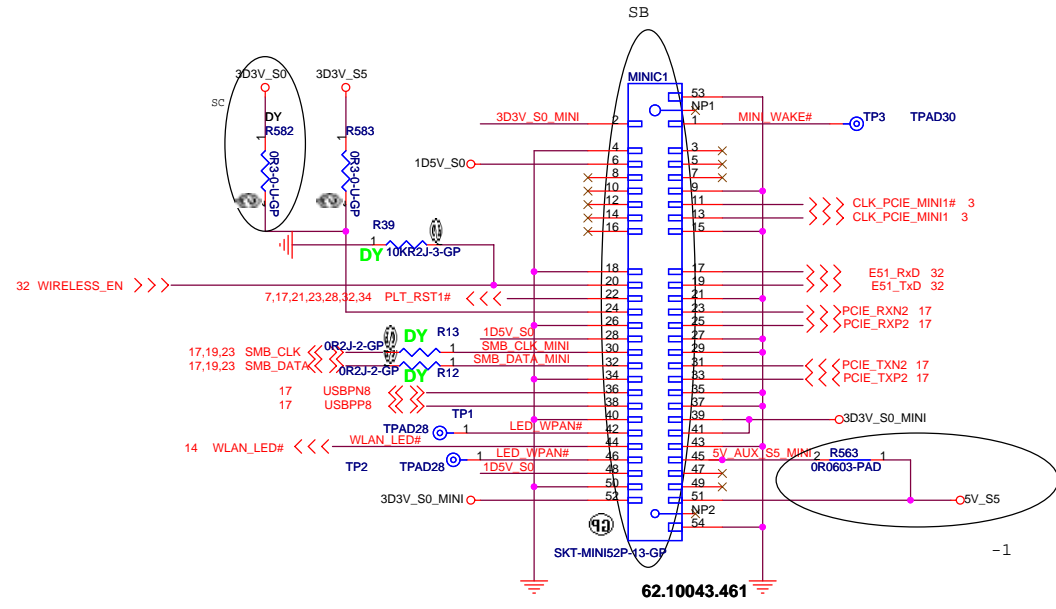
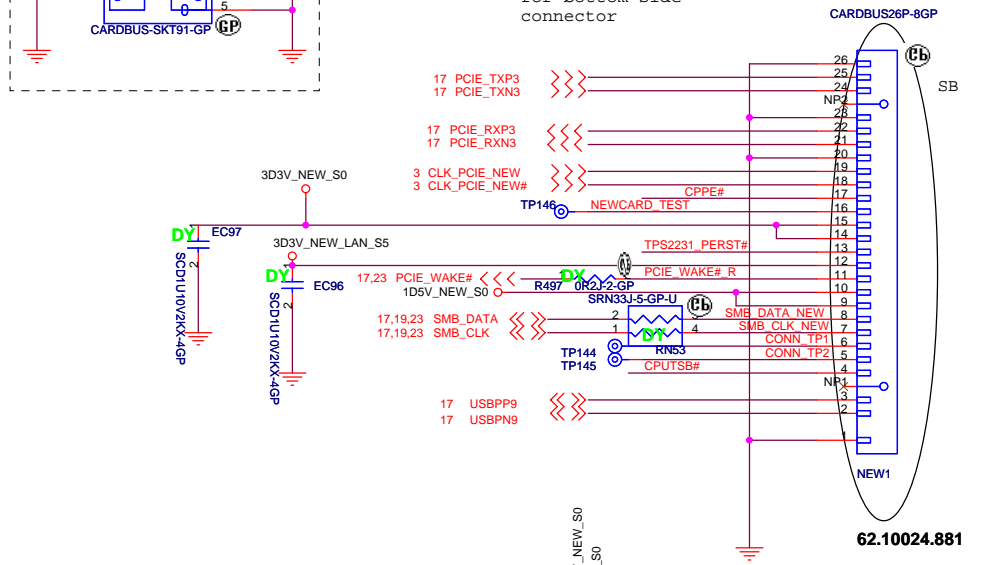
Title		
Graphic MXM CONN		
Size	Document Number	Rev
A3		-1
Date: Monday, February 26, 2007		
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# Mini Card Connector



## NEWCARD Connector

Reserve the symbol for bottom side connector



bom1

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD / NEW CARD**

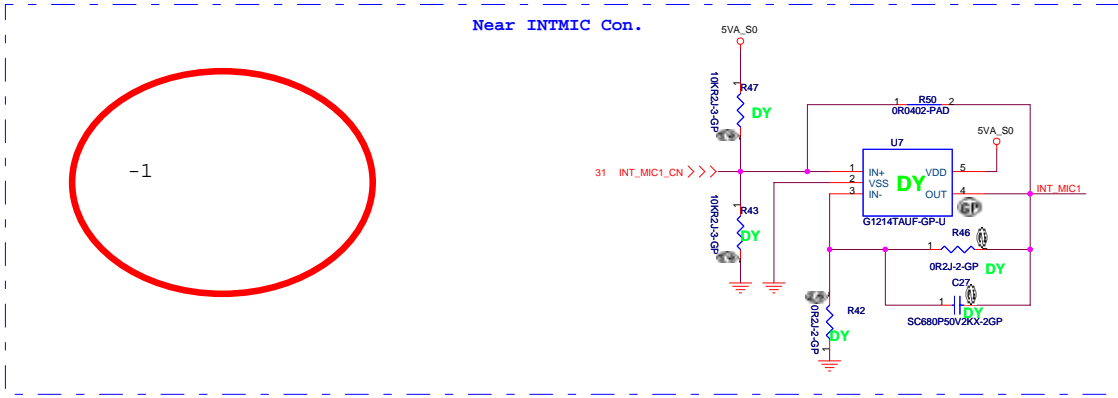
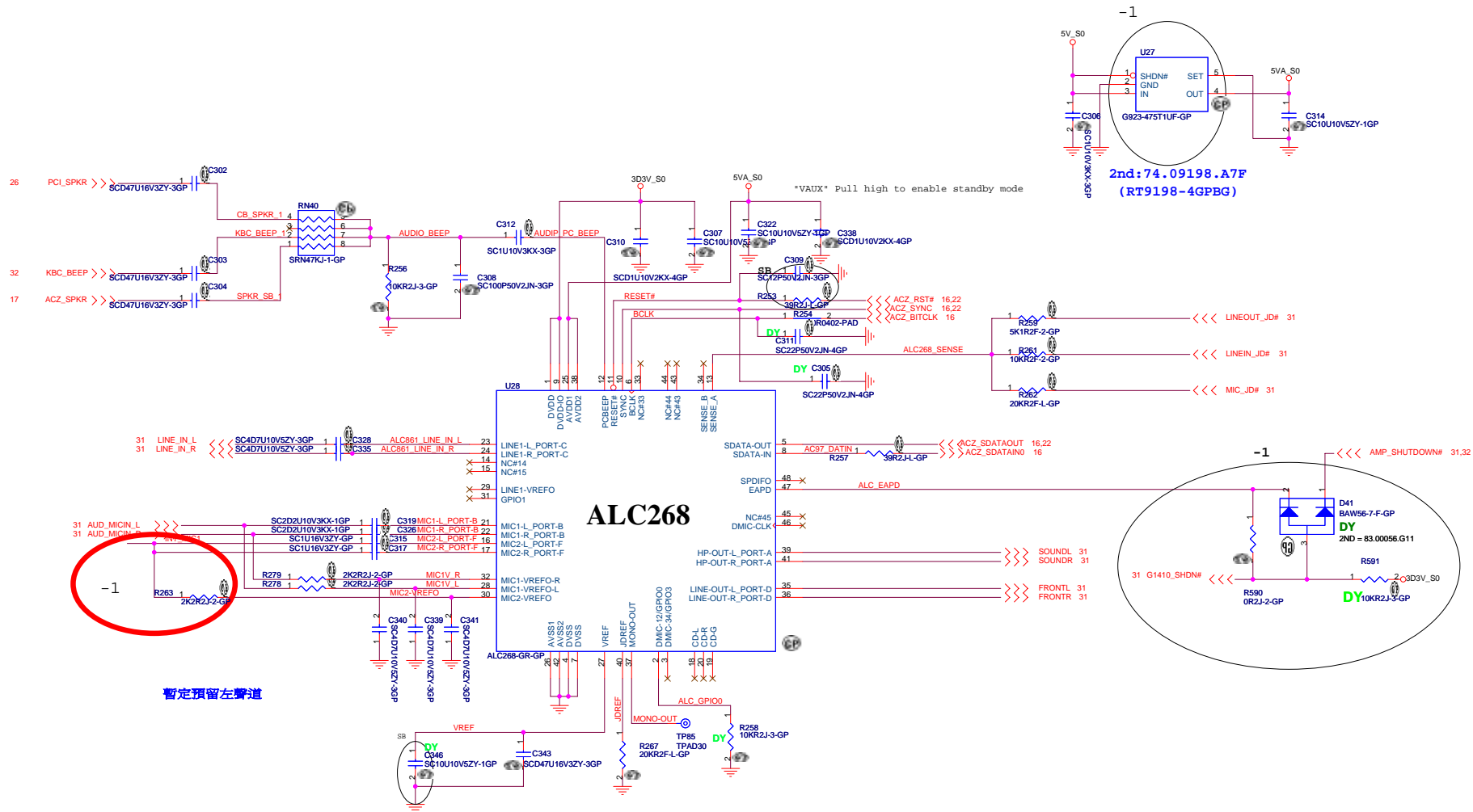
Size: Document Number

Date: Monday, February 26, 2007

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**Columbia/Tangiz**



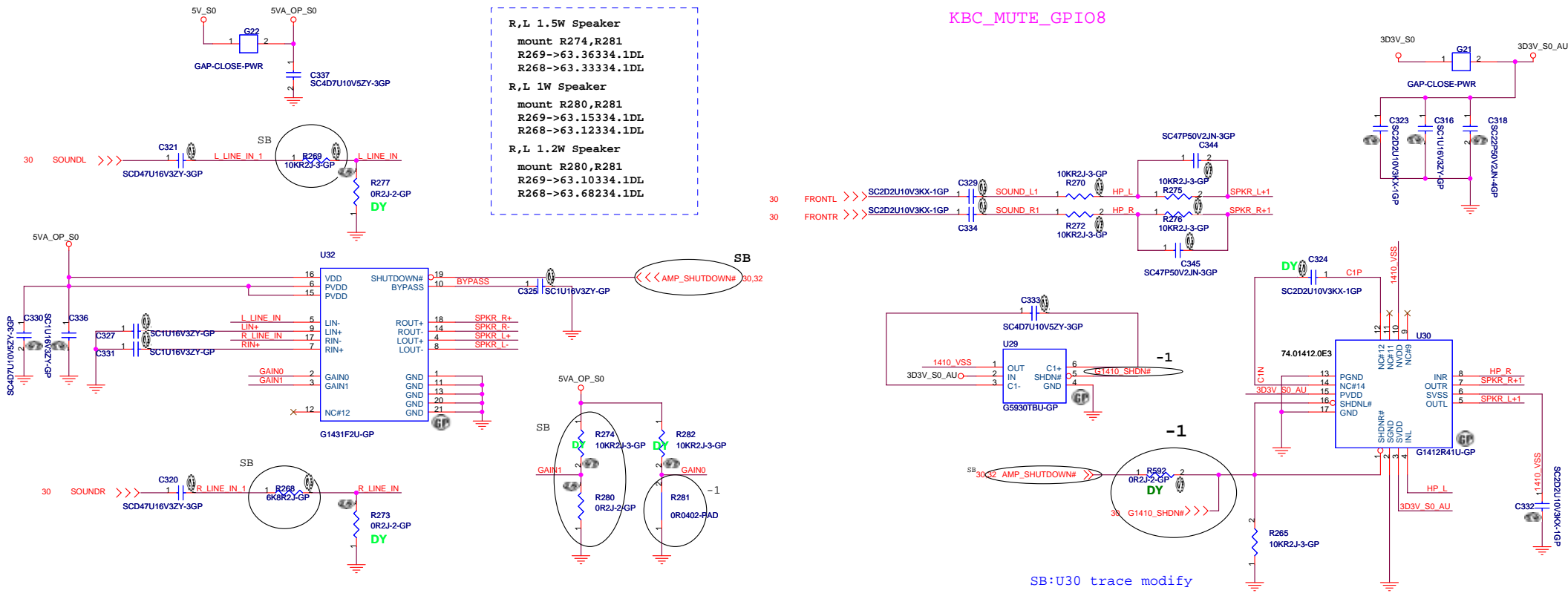
# AUDIO OP AMPLIFIER

R,L 1.5W Speaker  
 mount R274,R281  
 R269->63.36334.1DL  
 R268->63.33334.1DL

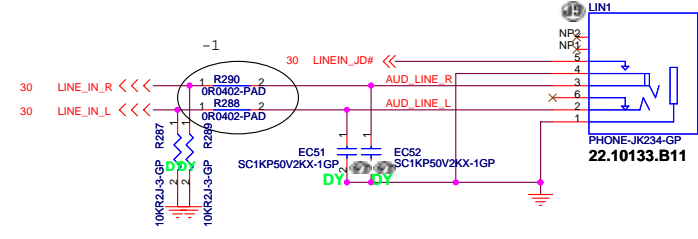
R,L 1W Speaker  
 mount R280,R281  
 R269->63.15334.1DL  
 R268->63.12334.1DL

R,L 1.2W Speaker  
 mount R280,R281  
 R269->63.10334.1DL  
 R268->63.68234.1DL

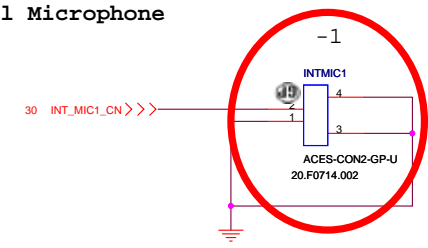
KBC\_MUTE\_GPIO8



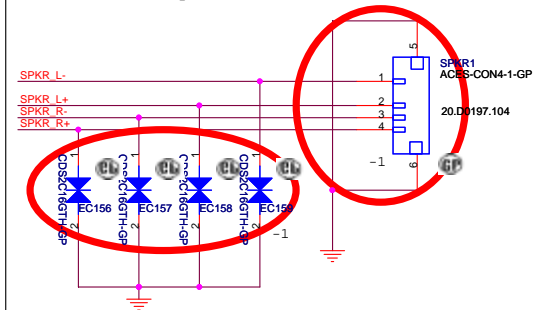
## LINE IN



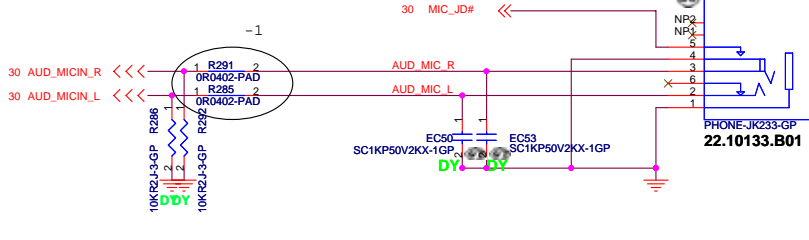
## Internal Microphone



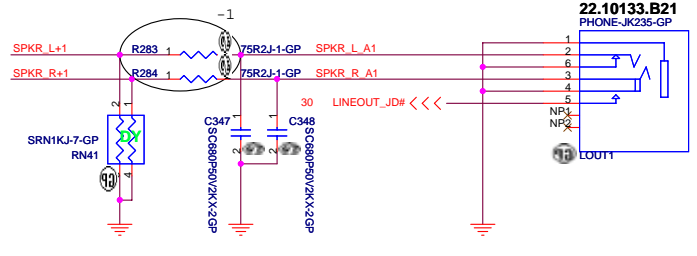
## Internal Speaker



## MIC IN



## LINE OUT



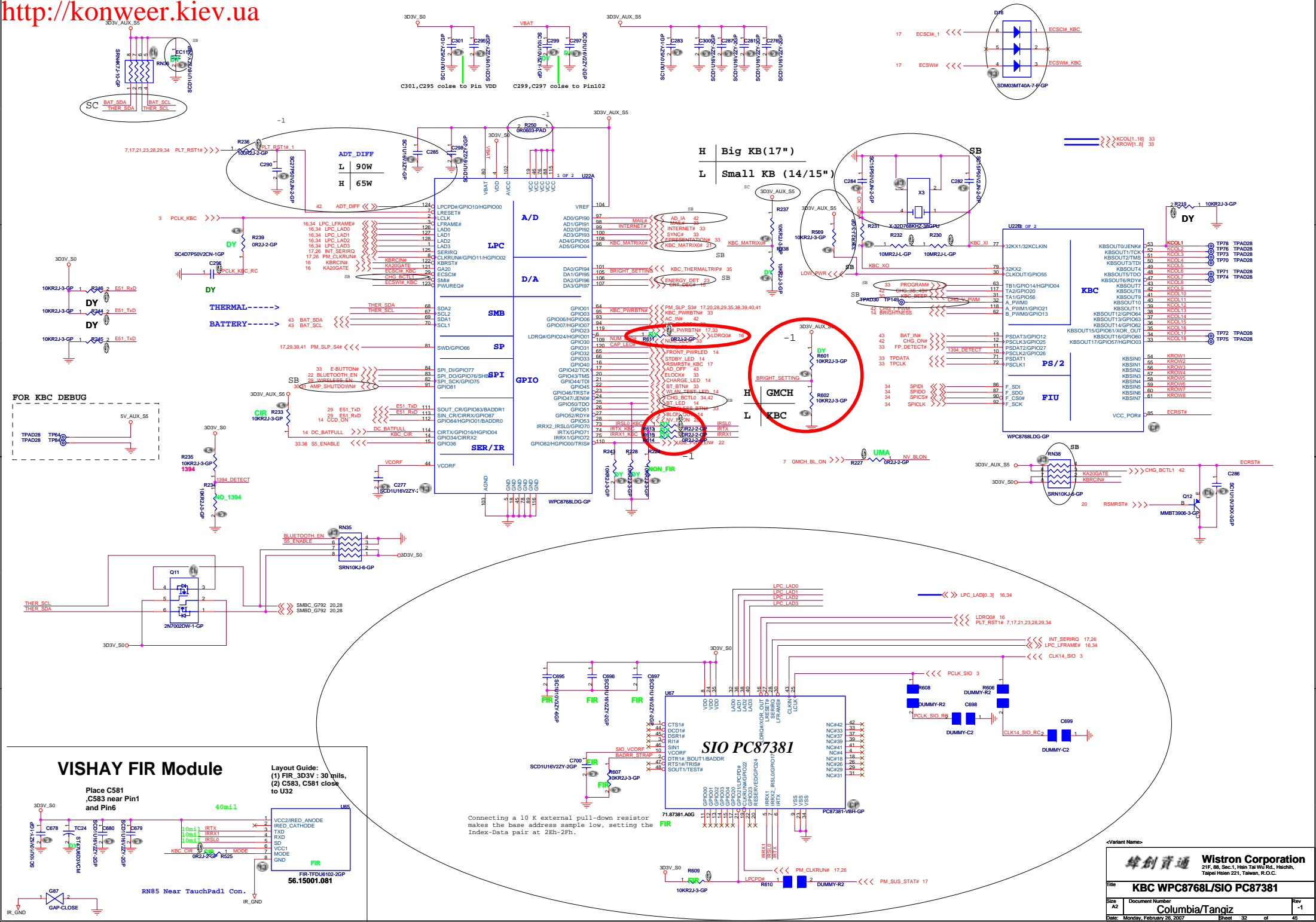
<Variant Name>

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 Taipei Hsien 221, Taiwan, R.O.C.

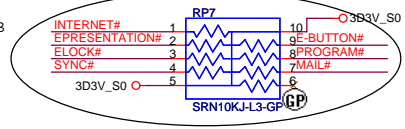
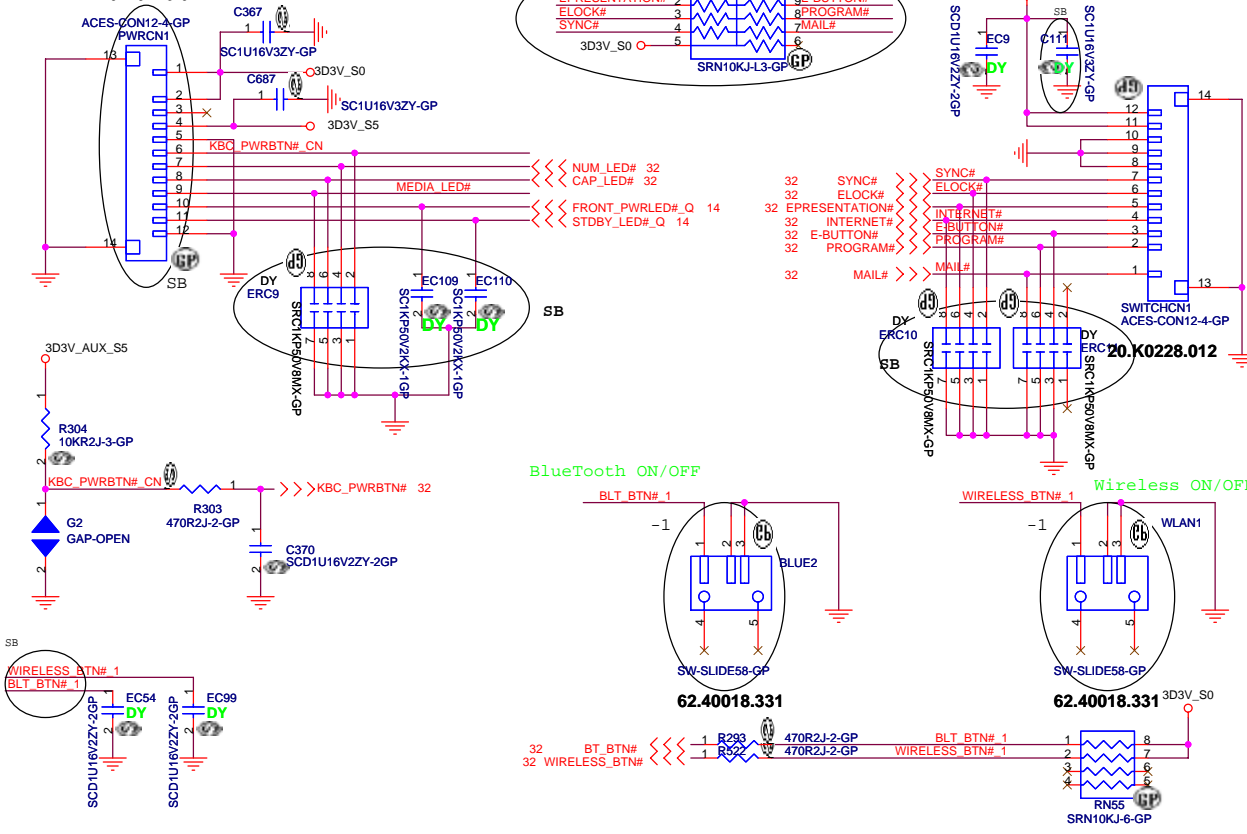
Title: **AUDIO AMP AND JACK**

Size: Document Number      Rev: -1

Date: Monday, February 26, 2007      Sheet 31 of 45

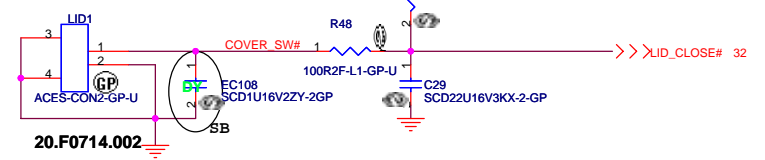


20.K0228.012



### Cover Up Switch

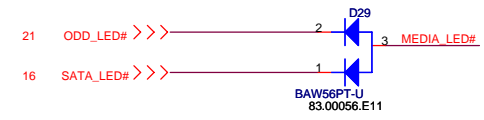
2nd source:20.F00984.002



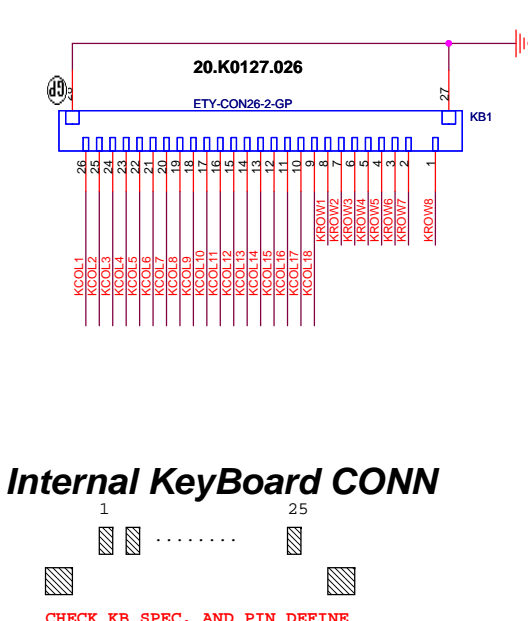
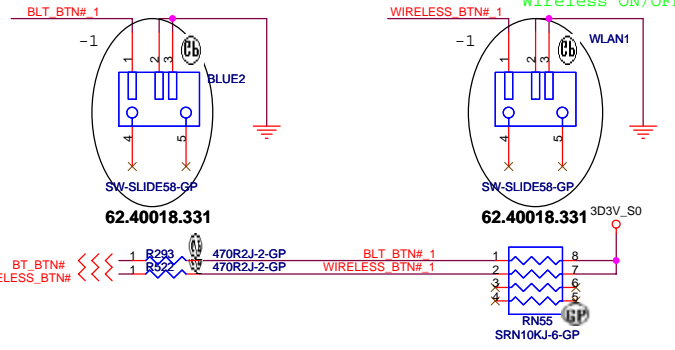
### Check test point

- 3D3V\_AUX\_S5 <--> TP139 TPAD30
- 3D3V\_S5 <--> TP143 TPAD30
- 5V\_S5 <--> TP142 TPAD30
- 17,32 PM\_PWRBTN# <--> TP141 TPAD30
- 4,16,35 H\_PWRGD <--> TP29 TPAD30
- 32,38 SS\_ENABLE <--> TP140 TPAD30
- 4,6 H\_CPURST# <--> TP90 TPAD30

Test Point放在Dimm Door打開可量測處

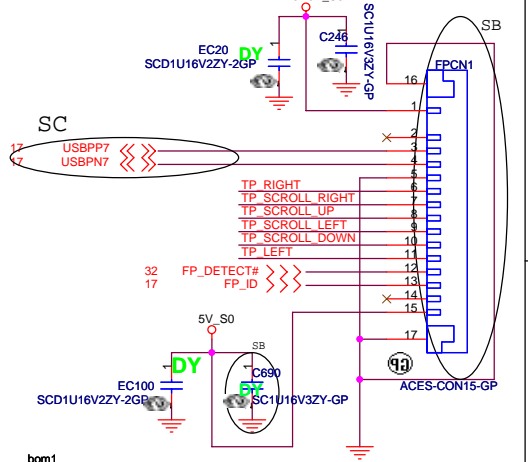
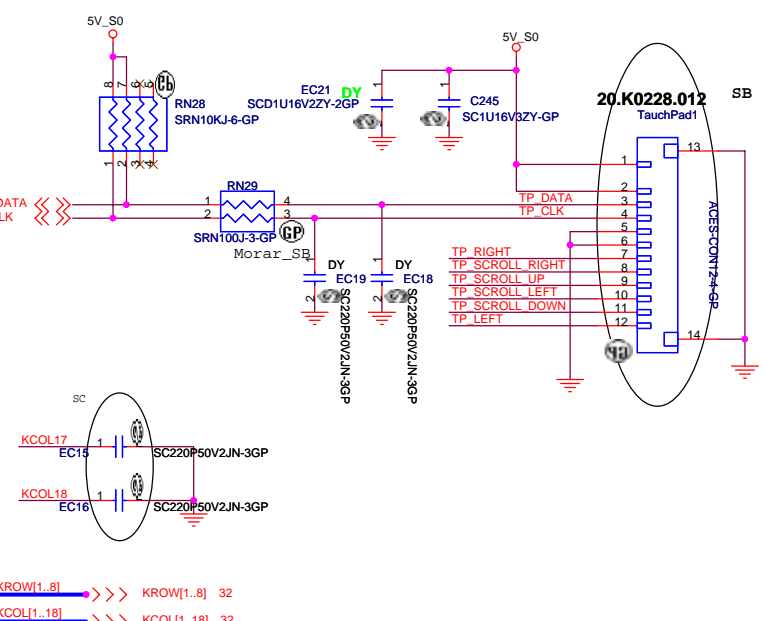


### Bluetooth ON/OFF



### EMI Bypass cap.

KCOL13	EC128	SC220P50V2JN-3GP
KCOL14	EC129	SC220P50V2JN-3GP
KCOL15	EC136	SC220P50V2JN-3GP
KCOL16	EC130	SC220P50V2JN-3GP
KCOL5	EC131	SC220P50V2JN-3GP
KCOL6	EC132	SC220P50V2JN-3GP
KCOL7	EC134	SC220P50V2JN-3GP
KCOL8	EC133	SC220P50V2JN-3GP
KCOL1	EC135	SC220P50V2JN-3GP
KCOL2	EC137	SC220P50V2JN-3GP
KCOL3	EC138	SC220P50V2JN-3GP
KCOL4	EC139	SC220P50V2JN-3GP
KROW8	EC141	SC220P50V2JN-3GP
KROW7	EC140	SC220P50V2JN-3GP
KROW6	EC142	SC220P50V2JN-3GP
KROW5	EC143	SC220P50V2JN-3GP
KROW4	EC144	SC220P50V2JN-3GP
KROW3	EC146	SC220P50V2JN-3GP
KROW2	EC145	SC220P50V2JN-3GP
KROW1	EC147	SC220P50V2JN-3GP
KCOL9	EC148	SC220P50V2JN-3GP
KCOL10	EC148	SC220P50V2JN-3GP
KCOL11	EC148	SC220P50V2JN-3GP
KCOL12	EC151	SC220P50V2JN-3GP
KCOL1	EC150	SC220P50V2JN-3GP



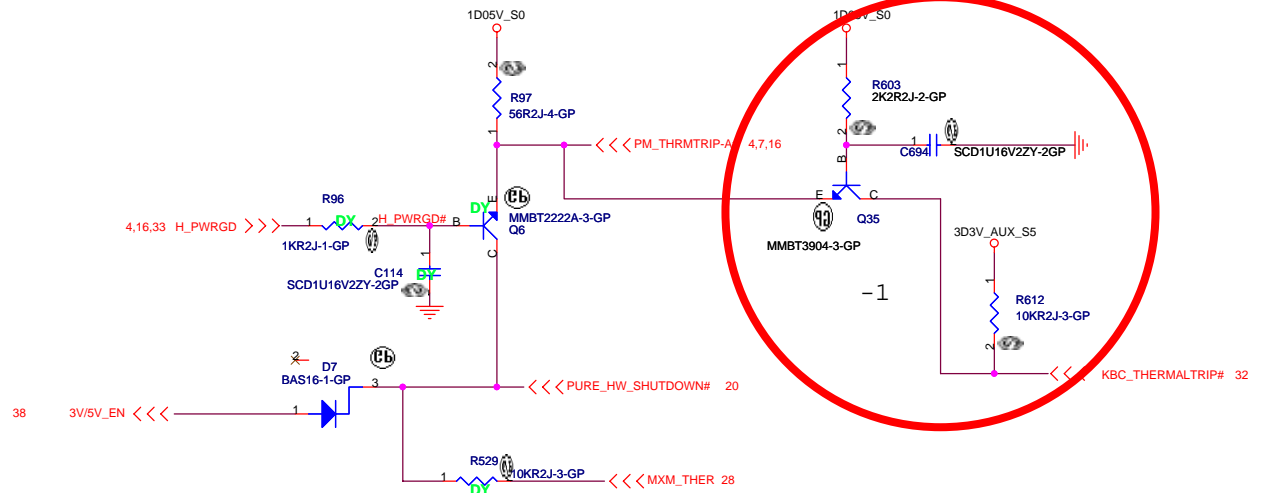
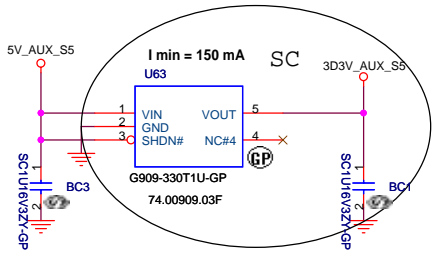
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File: **BUTTONS / KB / TOUCHPAD**

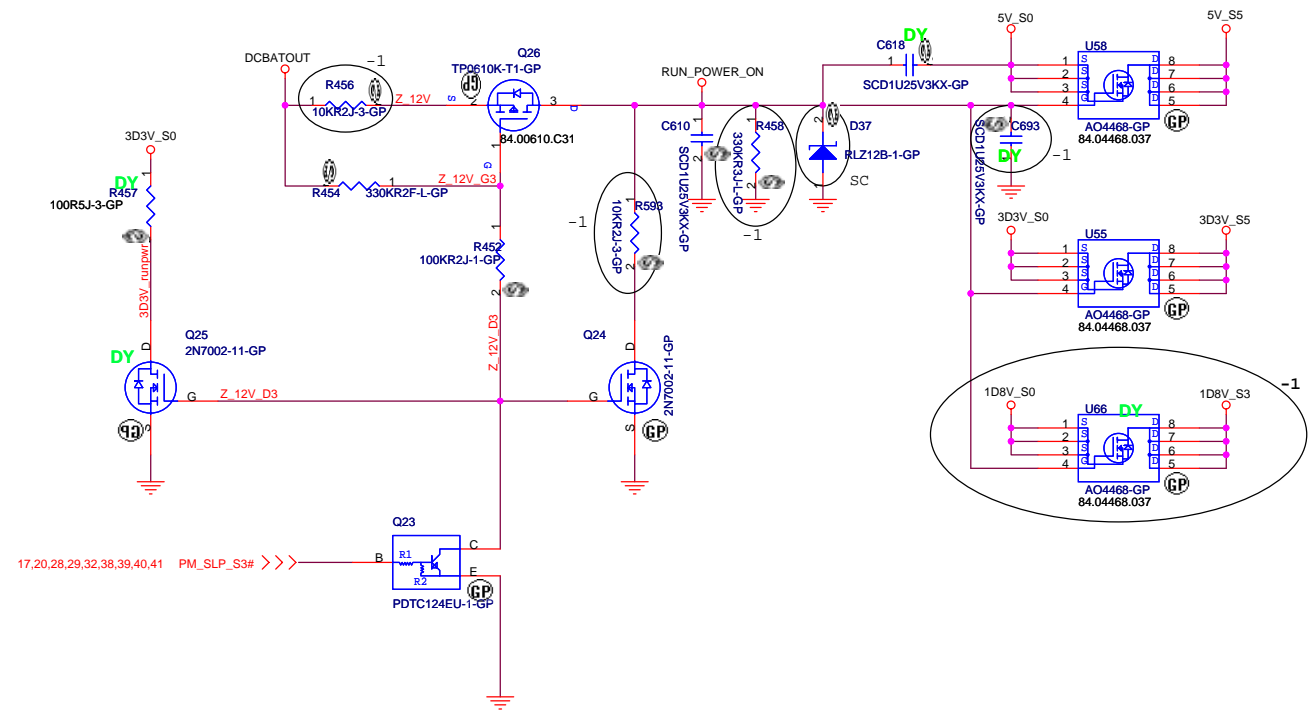
Size: Document Number Rev: -1

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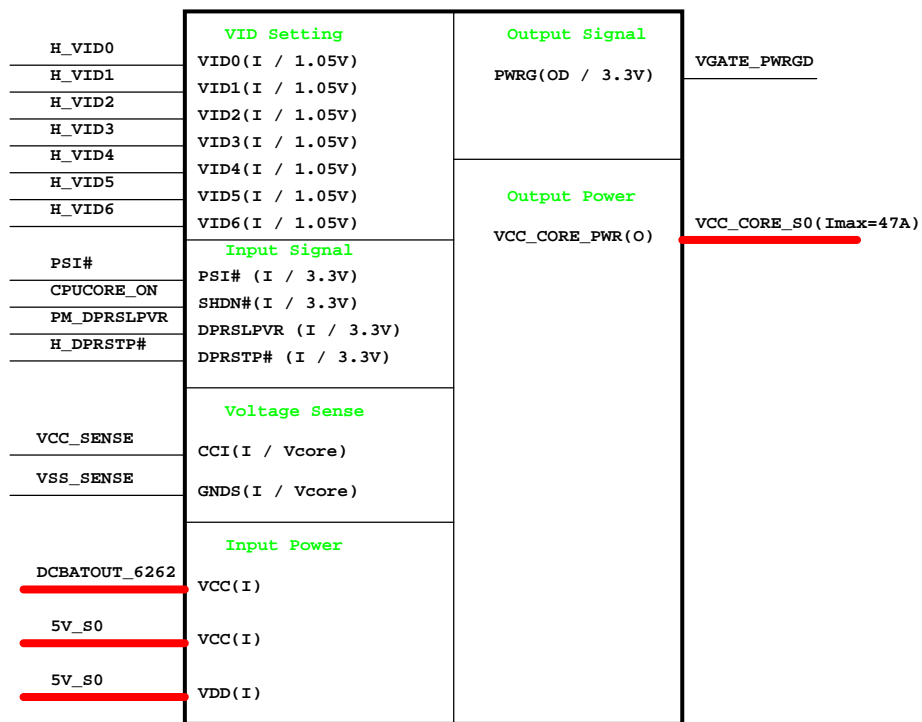




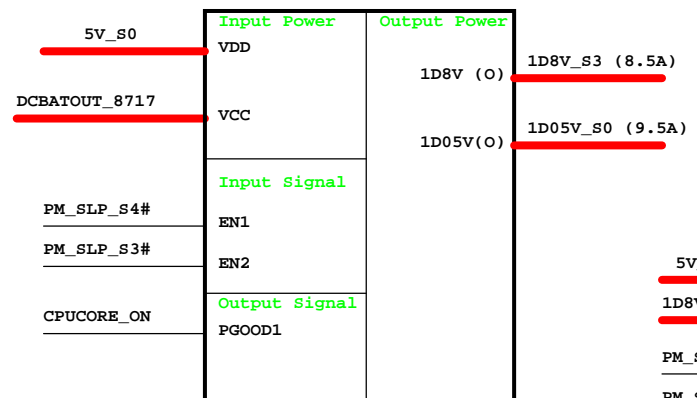
**Run Power**



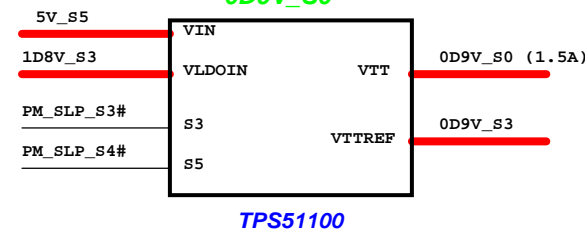
**CPU\_CORE  
MAX8770**



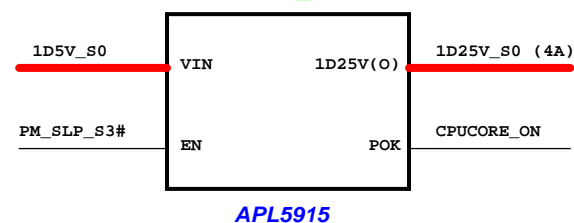
**MAX8717  
1D8V/1D05V**



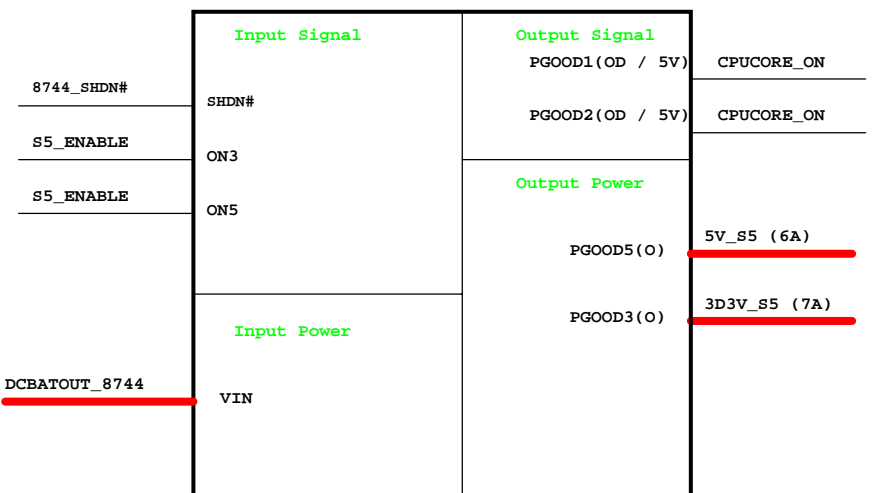
**0D9V\_S0**



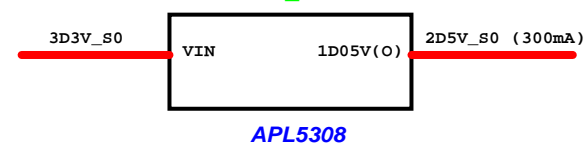
**1D25V\_S0**



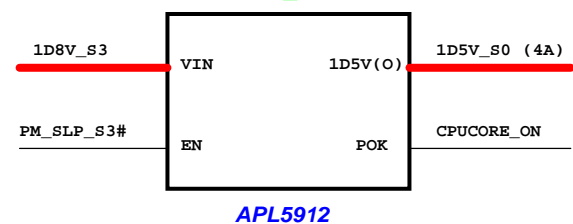
**MAX8744  
5V/3D3V**



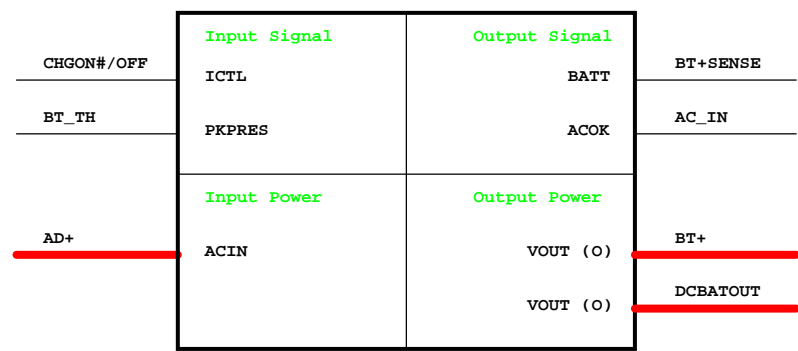
**2D5V\_S0**



**1D5V\_S0**



**Charger ISL6255**

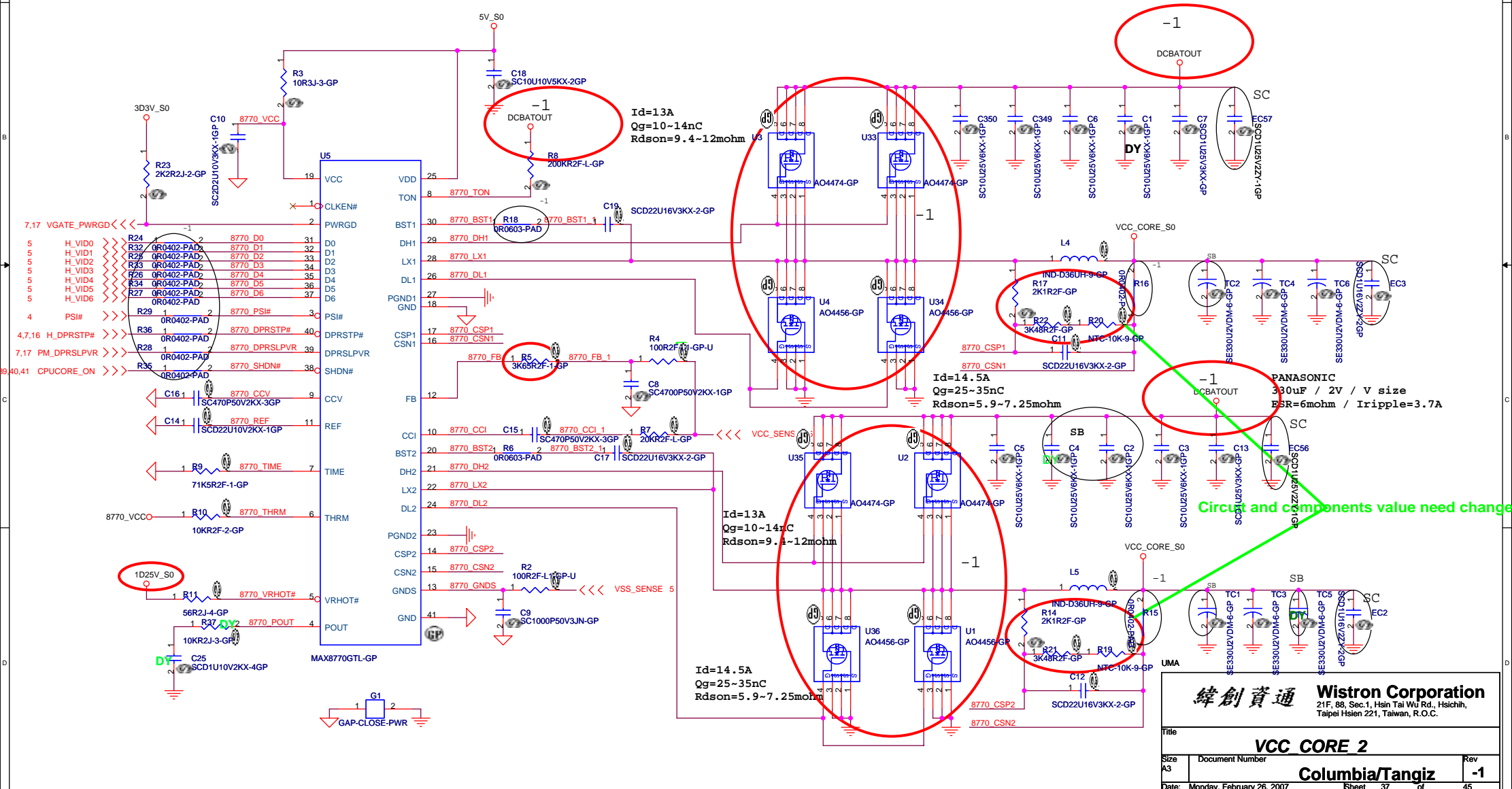


<Variant Name>

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Title: **Power Block Diagram**

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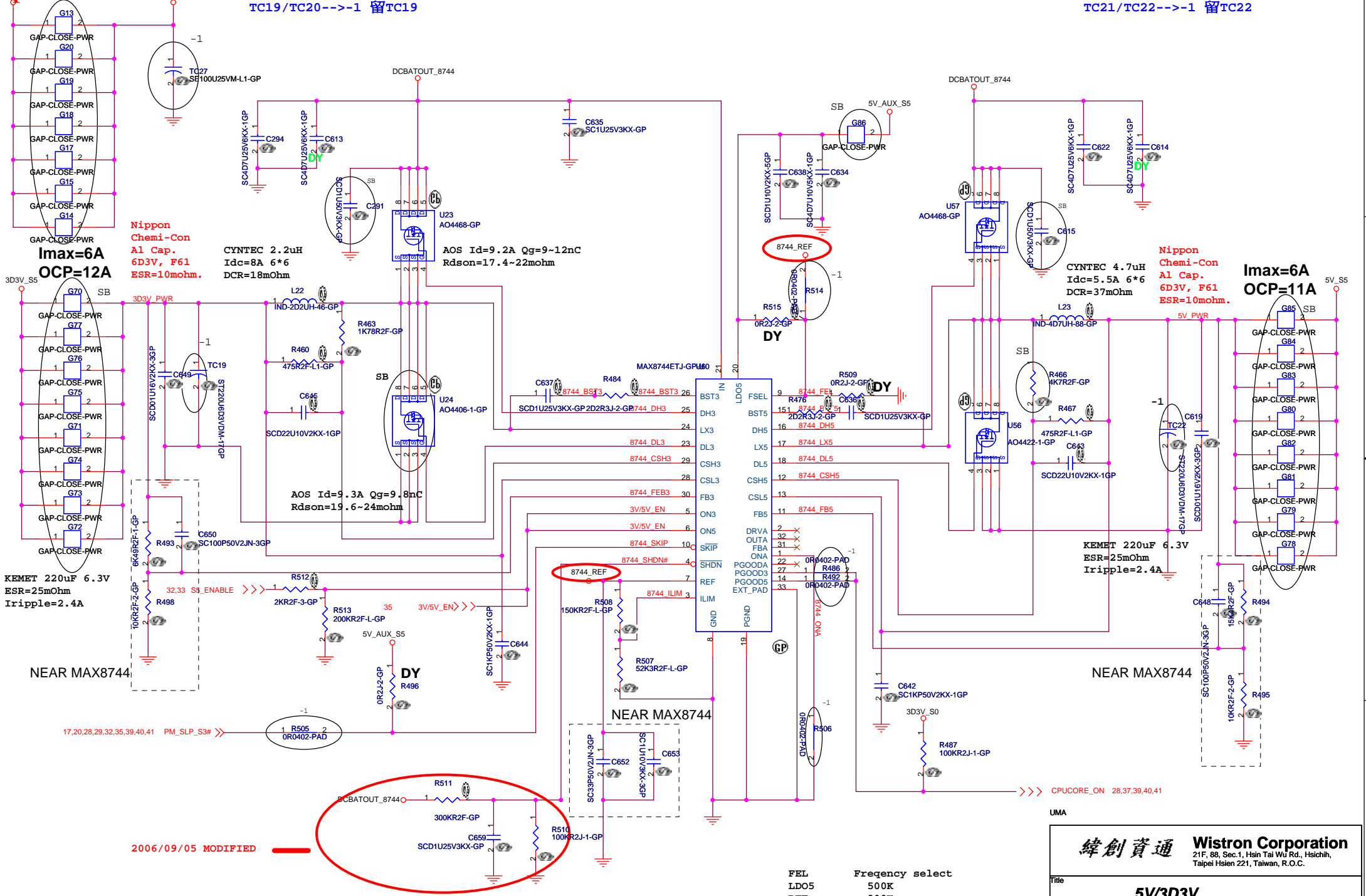
緯創資通 **Wistron Corporation**  
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**Title** VCC CORE 2  
**Size** A3  
**Document Number**  
**Date** Monday, February 26, 2007  
**Sheet** 37 of 45  
**Rev** -1  
**Columbia/Tangiz**

TC19/TC20-->-1 留TC19

TC21/TC22-->-1 留TC22



**Nippon Chemi-Con**  
**Al Cap.**  
**6D3V, F61**  
**ESR=10mohm.**

**CYNTec 2.2uH**  
**Idc=8A 6\*6**  
**DCR=18mOhm**

**AOS Id=9.2A Qg=9~12nC**  
**Rdson=17.4~22mohm**

**AOS Id=9.3A Qg=9.8nC**  
**Rdson=19.6~24mohm**

**CYNTec 4.7uH**  
**Idc=5.5A 6\*6**  
**DCR=37mOhm**

**Nippon Chemi-Con**  
**Al Cap.**  
**6D3V, F61**  
**ESR=10mohm.**

**Imax=6A**  
**OCP=11A**

**Imax=6A**  
**OCP=12A**

**KEMET 220uF 6.3V**  
**ESR=25mOhm**  
**Iripple=2.4A**

**KEMET 220uF 6.3V**  
**ESR=25mOhm**  
**Iripple=2.4A**

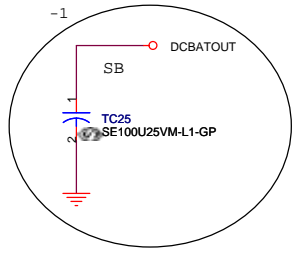
FEL	Frequency select
LDO5	500K
REF	300K
GND	200K

2006/09/05 MODIFIED

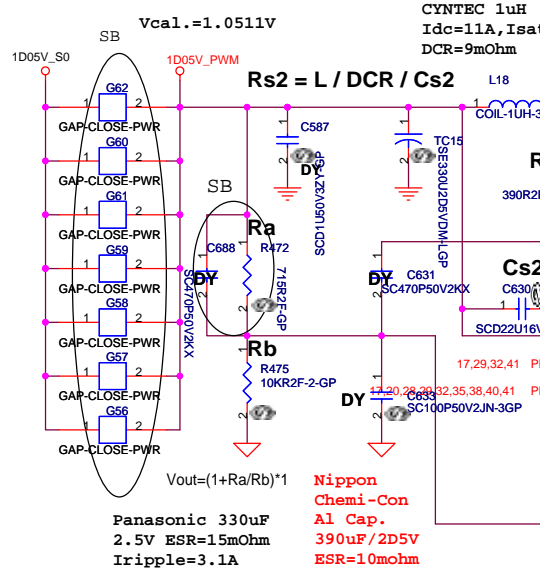
<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title		<b>5V/3D3V</b>	
Size A3	Document Number	<b>Columbia/Tangiz</b>	
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TC15/TC16-->-1 留TC15

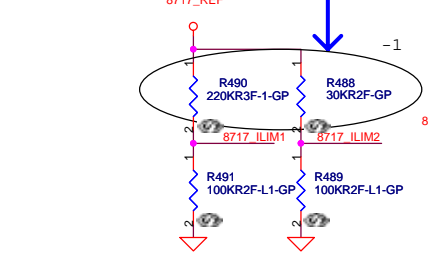
TC17/TC18-->-1 留TC17



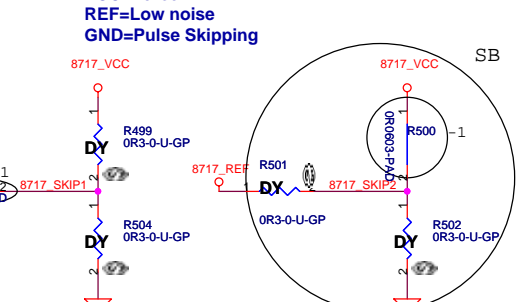
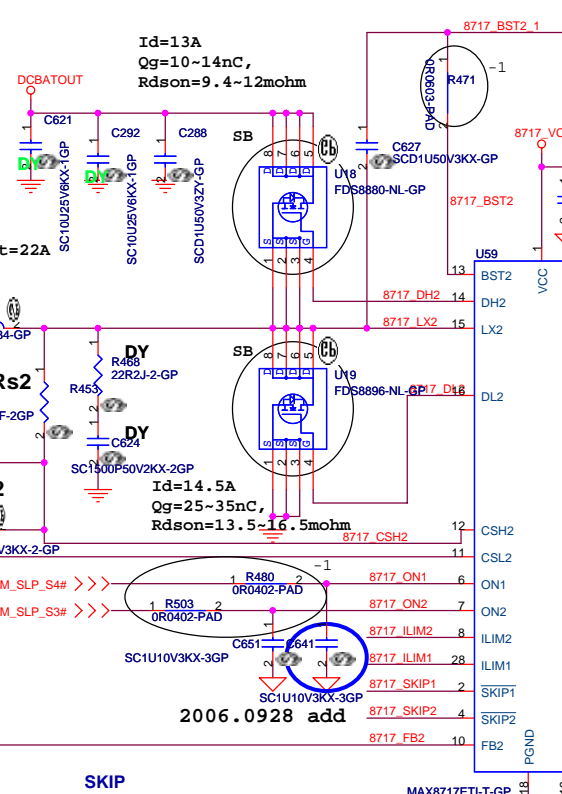
1D05V Iomax=12A  
OCP>19A



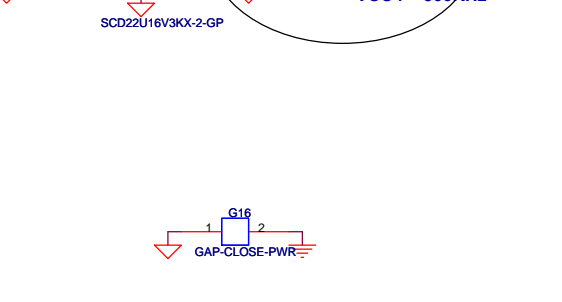
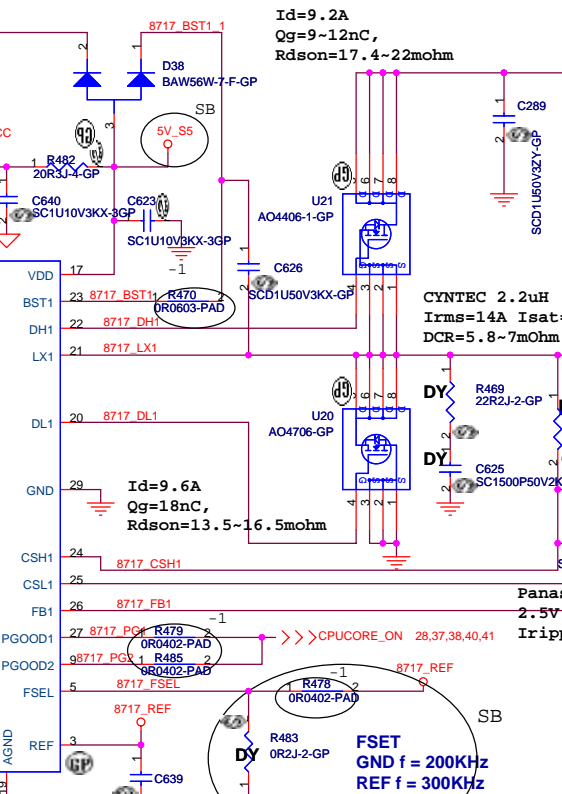
Adjust the current limit threshold from R14, R15



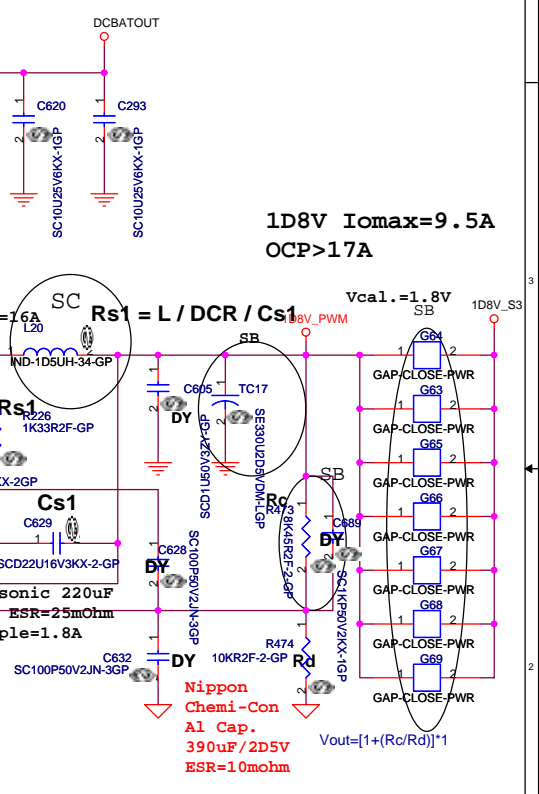
VILIM = 0.5V~2.0V  
Output Current =  
ILIM / 10 / LDCR - di/2



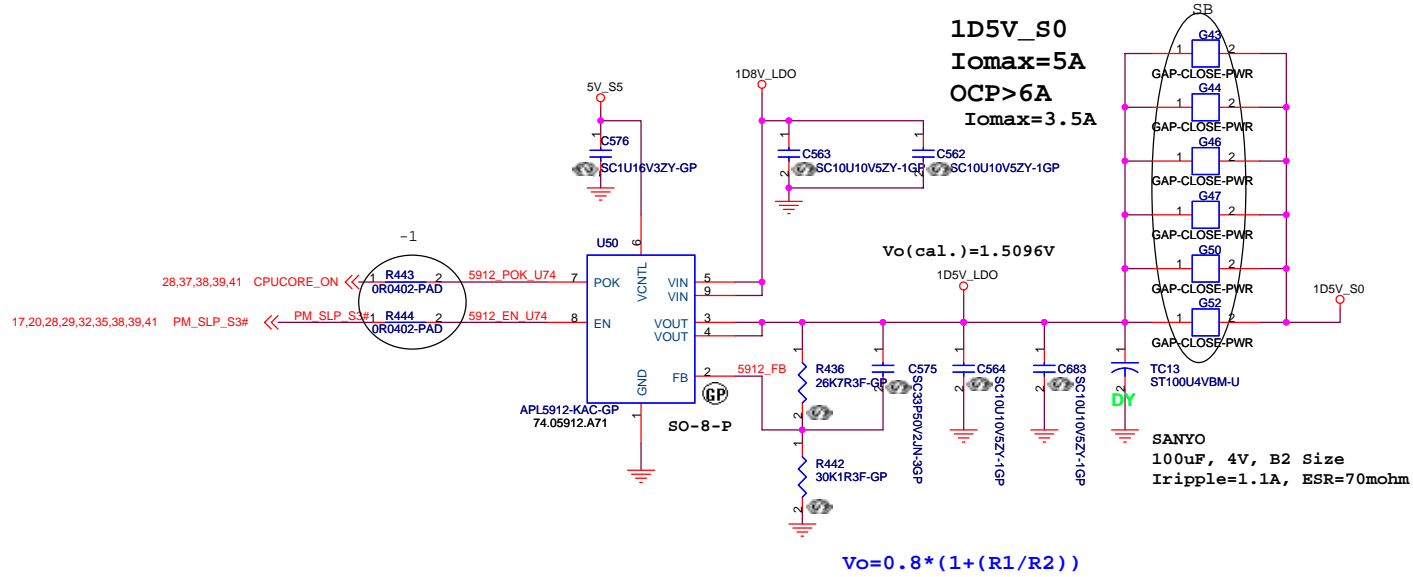
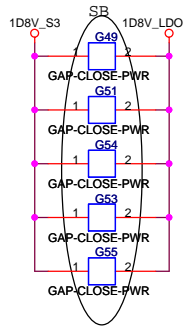
VILIM = 0.5V~2.0V  
Output Current =  
ILIM / 10 / LDCR - di/2



VILIM = 0.5V~2.0V  
Output Current =  
ILIM / 10 / LDCR - di/2



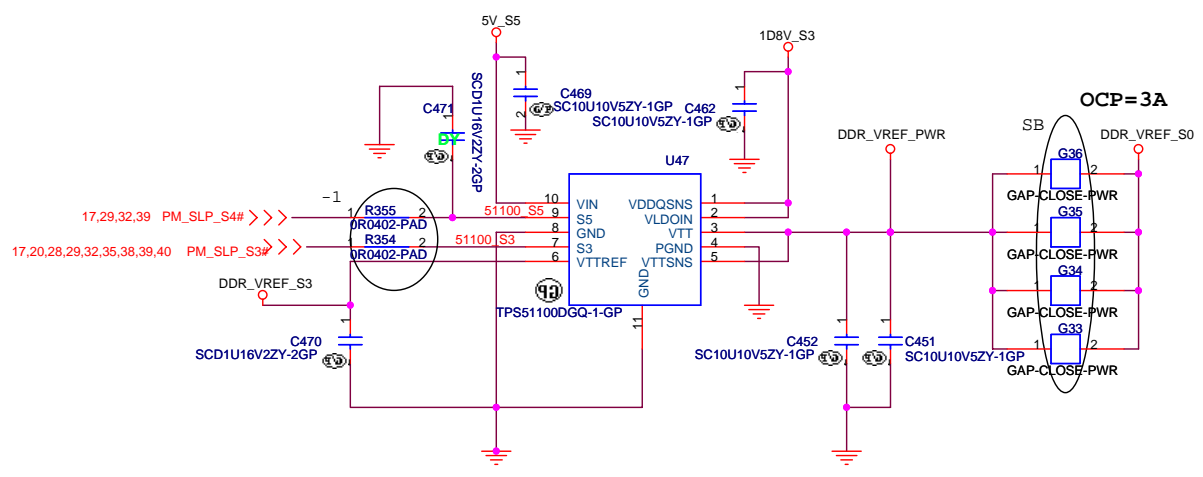
VILIM = 0.5V~2.0V  
Output Current =  
ILIM / 10 / LDCR - di/2



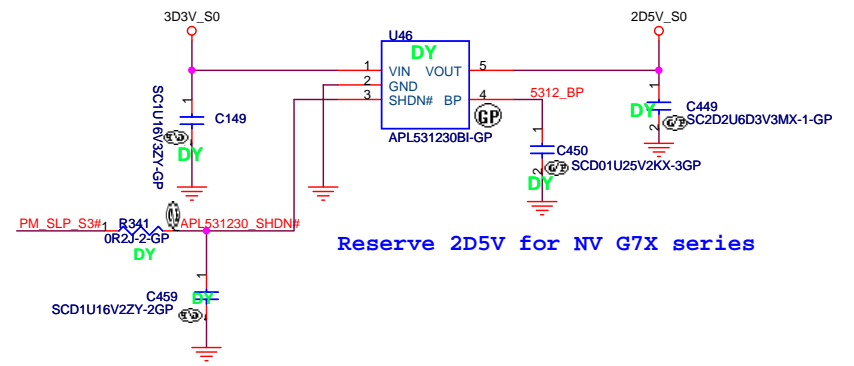
UMA

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>APW5912_1D5V</b>			
Size	Document Number	<b>Columbia/Tangiz</b>	
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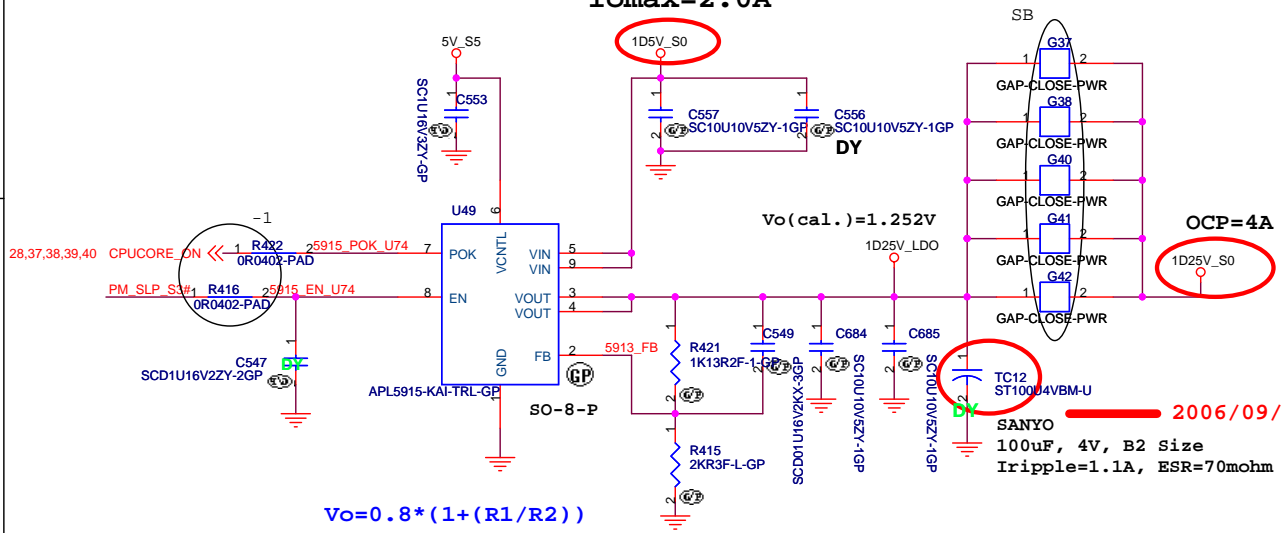
**0D9V\_S3**  
Iomax=1.2A



**2D5V**  
Iomax=130mA



**1D25V\_S0**  
Iomax=2.0A



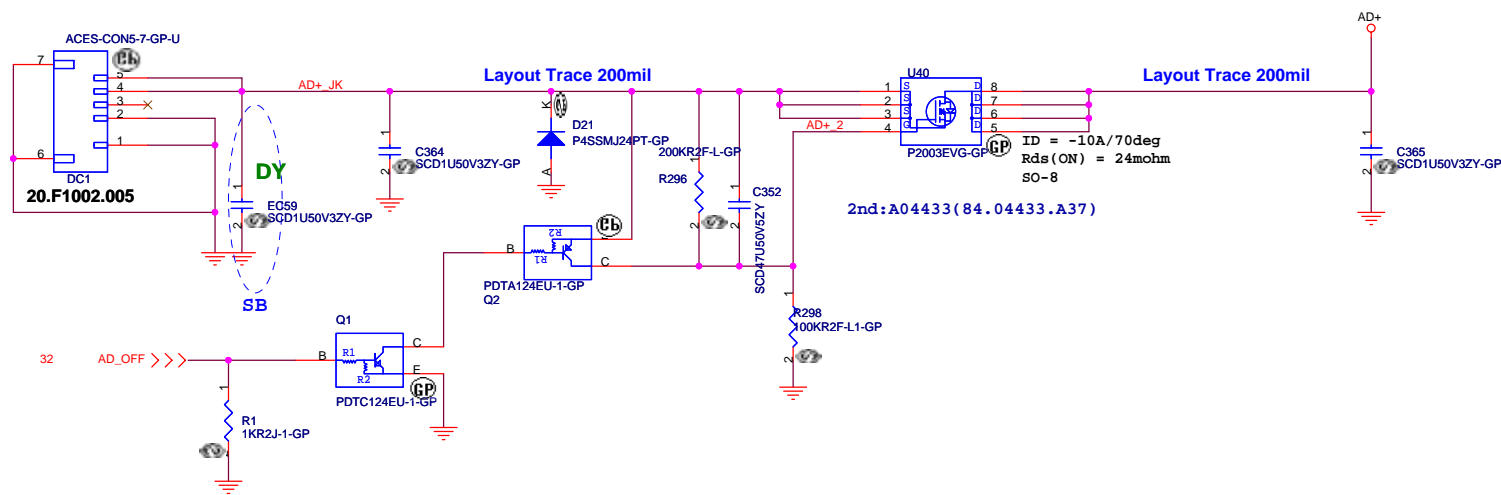
$$V_o = 0.8 * (1 + (R1/R2))$$

UMA

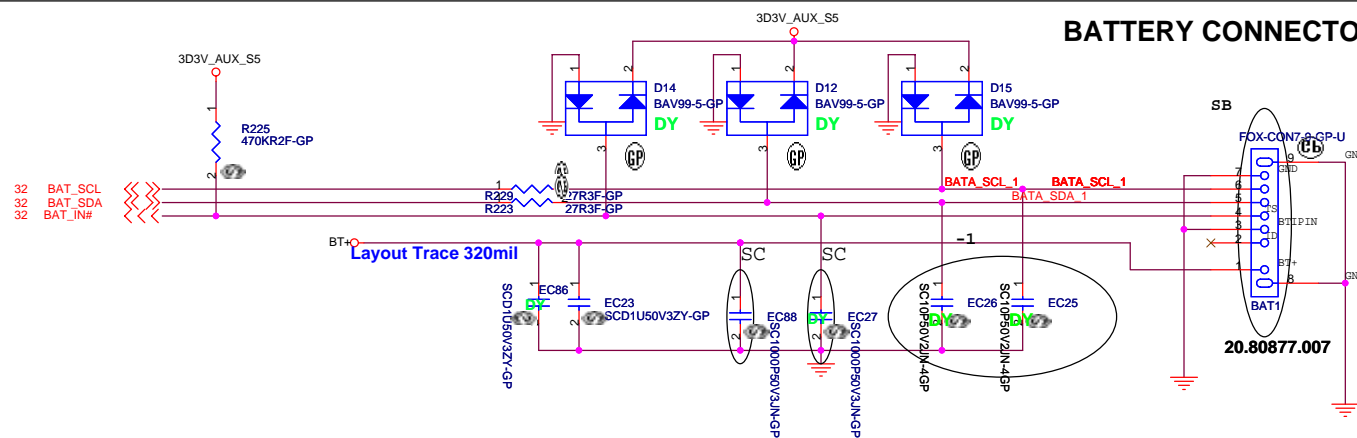
<b>緯創資通 Wistron Corporation</b>		21F, 88, Sec.1, Hsin Tai Wuj Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b>			
<b>1D25V/2D5V//1D05V/0D9V</b>			
Size B	Document Number	Rev	
	<b>Columbia/Tangiz</b>	<b>-1</b>	
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### Adaptor in to generate DCBATOUT



### BATTERY CONNECTOR

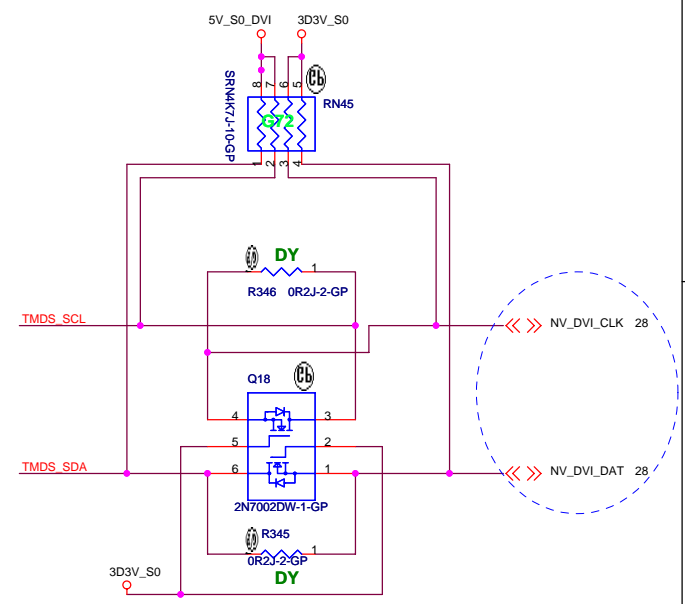
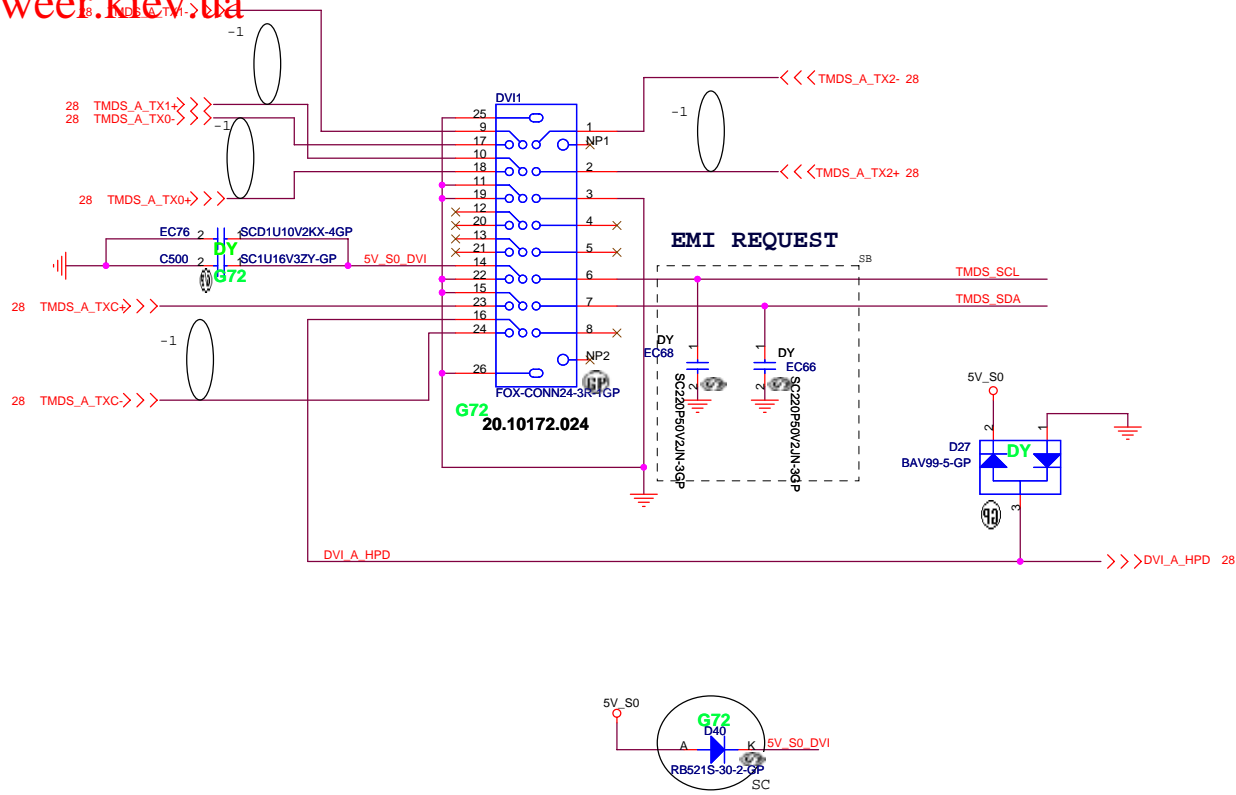


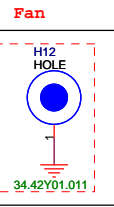
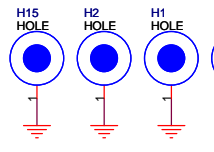
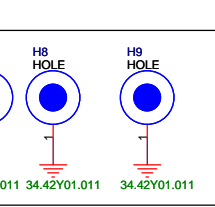
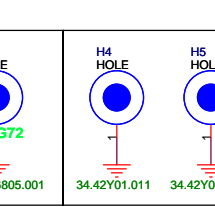
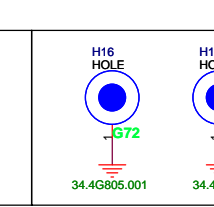
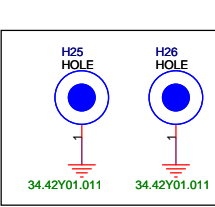
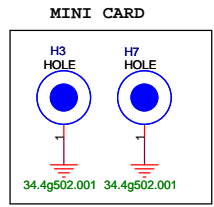
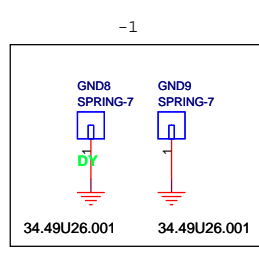
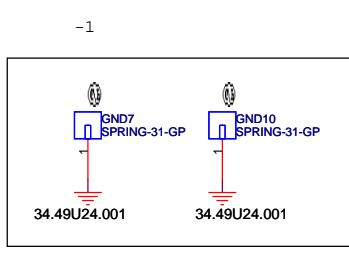
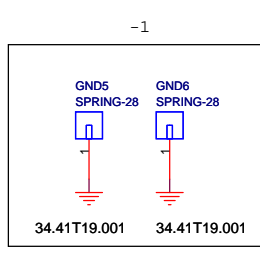
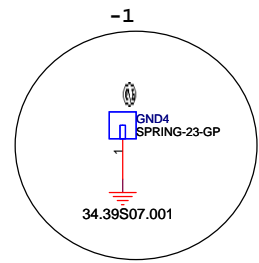
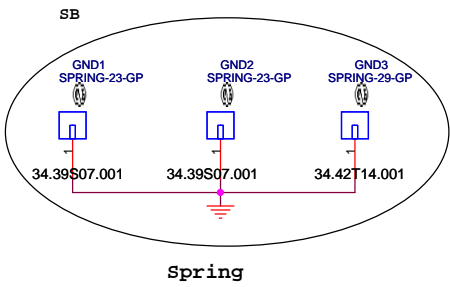
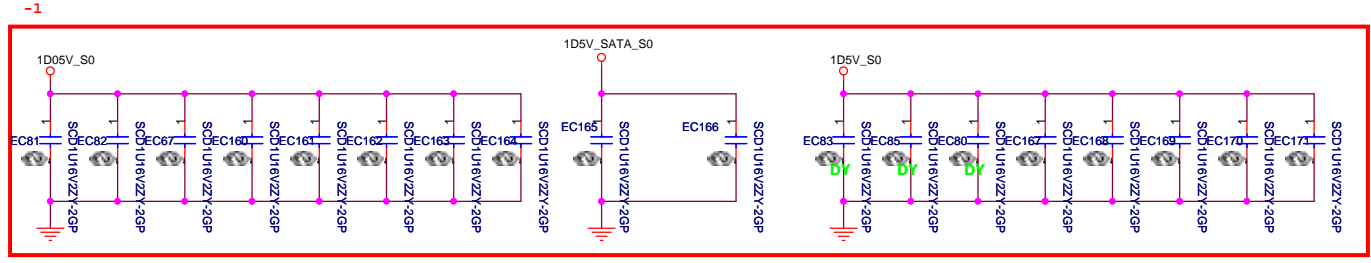
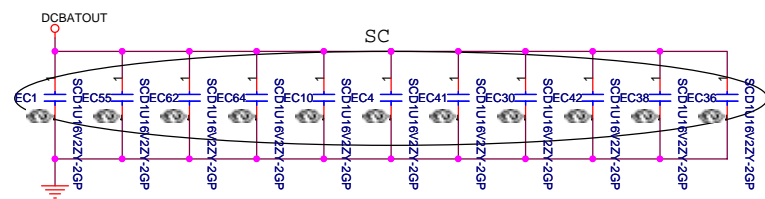
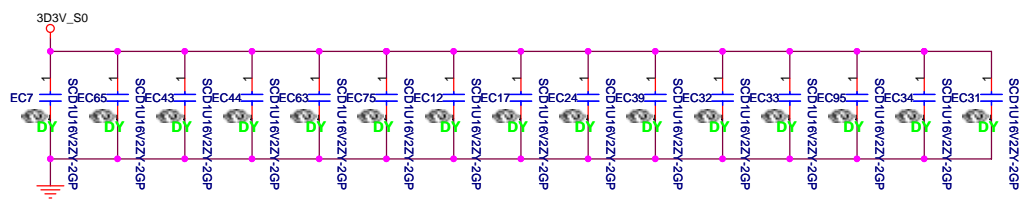
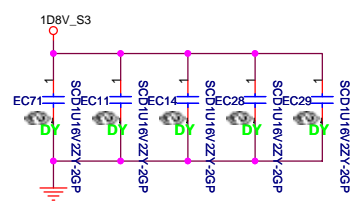
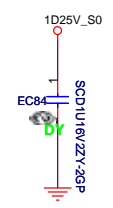
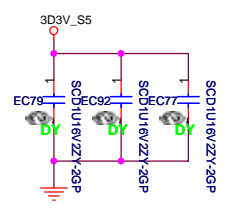
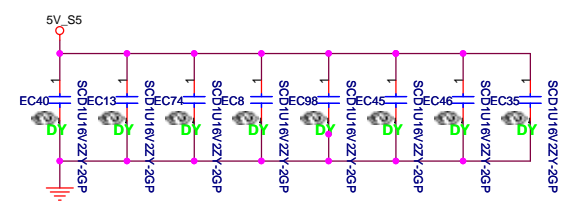
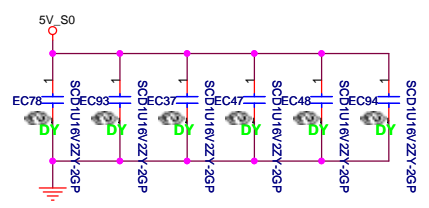
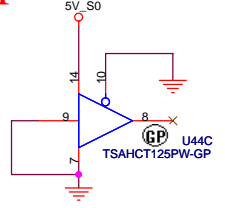
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