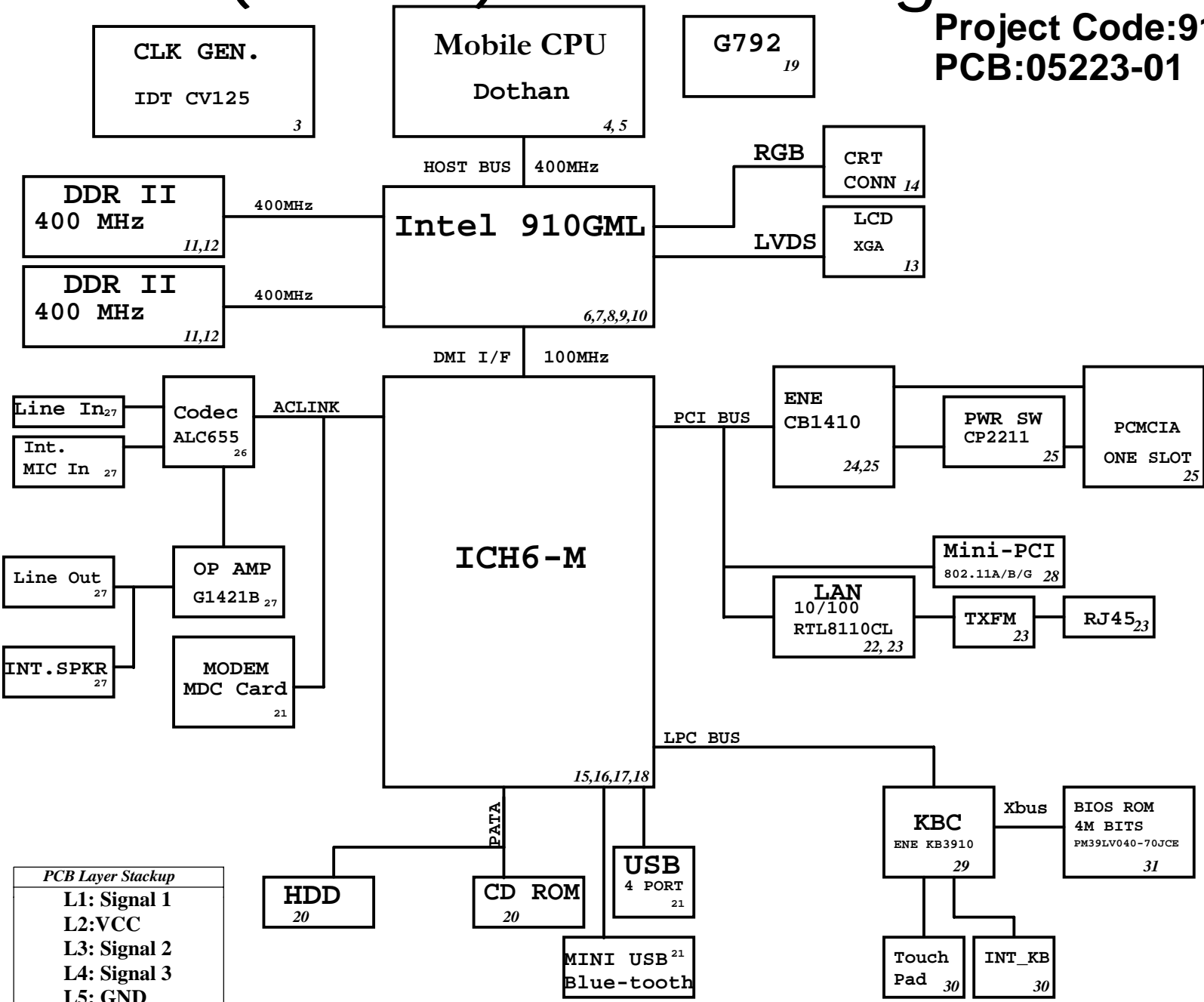


# AG1(Alviso) Block Diagram 2005/11/01

Project Code:91.4G301.001  
PCB:05223-01



**PCB Layer Stackup**

- L1: Signal 1
- L2: VCC
- L3: Signal 2
- L4: Signal 3
- L5: GND
- L6: Signal 4

CPU DC/DC ISL6218CV-T 34	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

SYSTEM DC/DC TPS51120 35	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5
APL5912-LAC APL5308-25AC 36	
INPUTS	OUTPUTS
5V_S5	1D5V_S0
3D3V_S0	2D5V_S0

SYSTEM DC/DC ISL6227 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S3
TPS51100DGQ 37	
INPUTS	OUTPUTS
5V_S5	DDR_VREF DDR_VREF_S3

CHARGER ISL6255 38	
INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title <b>BLOCK DIAGRAM</b>		
Size Custom	Document Number <b>AG1(Alviso)</b>	Rev <b>01</b>
Date: Tuesday, November 01, 2005 Sheet 1 of 40		

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 <b>1 = DMI x4 (Default)</b>
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott <b>1 = Dothan (Default)</b>
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled <b>11 = Normal Operation (Default)</b>
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled <b>1 = Dynamic ODT Enabled (Default)</b>
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1 = SDVO device present

**NOTE:** All strap signals are sampled with respect to the leading edge of the Alviso GMCH FWORX In signal.

### PCI Routing

	IDSEL	IRQ	REQ/GNT
<b>1410</b>	<b>25</b>	<b>B.F.G</b>	<b>0</b>
<b>MiniPCI</b>	<b>21</b>	<b>F</b>	<b>1</b>
<b>LAN</b>	<b>23</b>	<b>E</b>	<b>2</b>

### ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

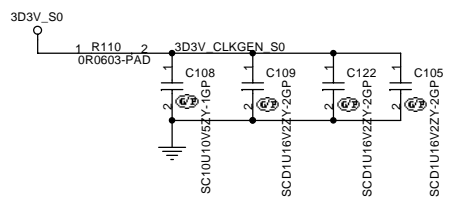
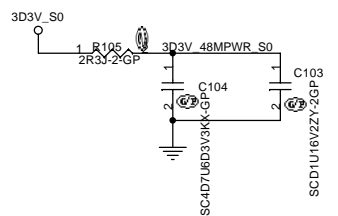
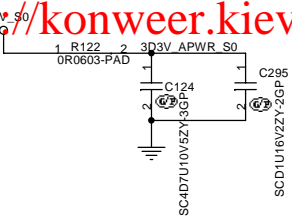
ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]/GPO[17], GNT[6]/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

### ICH6-M IDE Integrated Series Termination Resistors

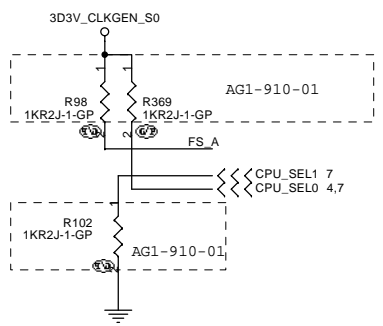
DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

<Core Design>

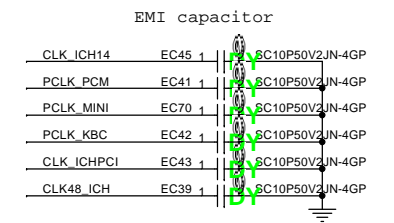
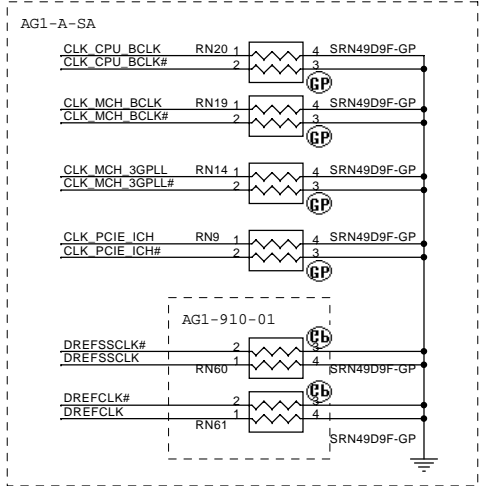
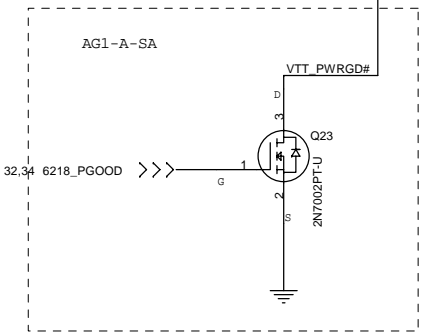
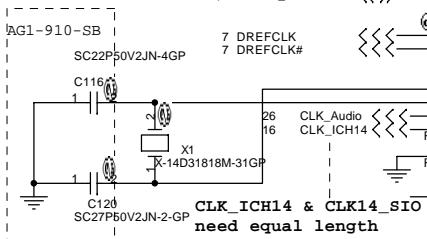
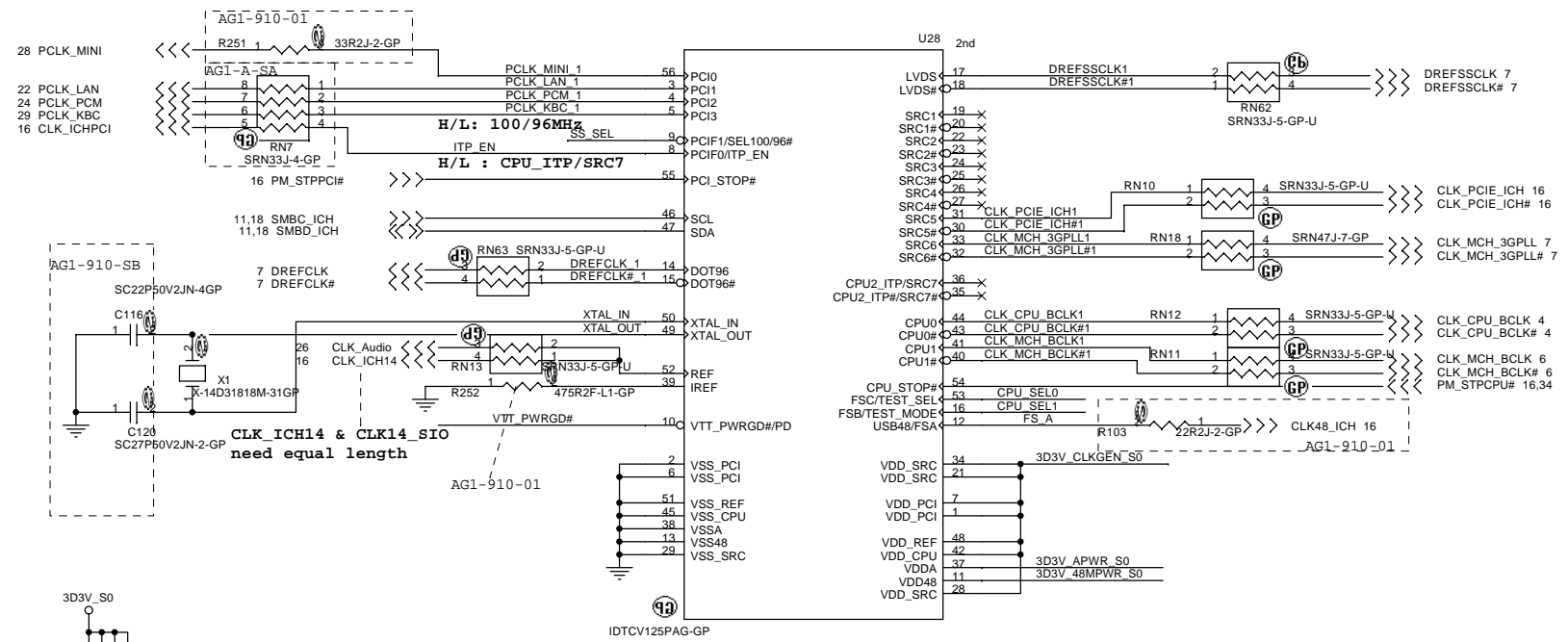
<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
<b>Memo</b>			
Size A3	Document Number <b>AG1(Alviso)</b>	Rev <b>01</b>	
Date: Tuesday, November 01, 2005		Sheet 2	of 40



IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z



FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved



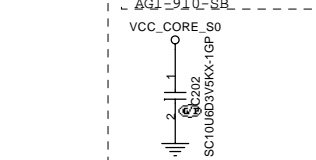
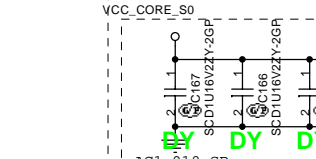
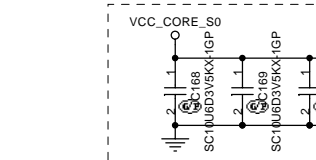
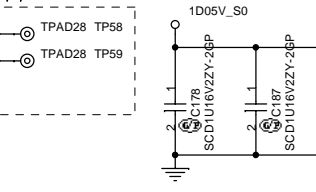
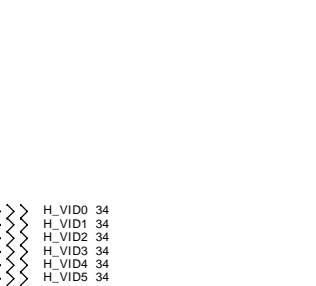
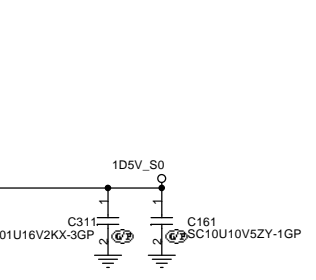
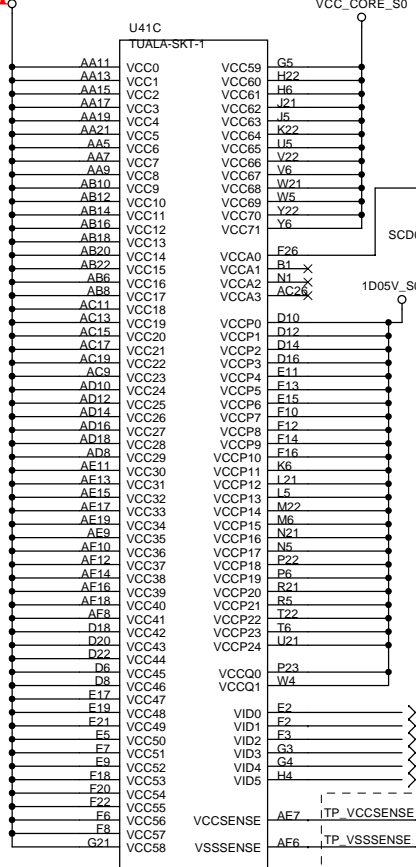
<Core Design>

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Title: **Clock Generator - IDT125**

Size A3	Document Number	Rev <b>01</b>
Date: Friday, October 28, 2005		Sheet 3 of 40

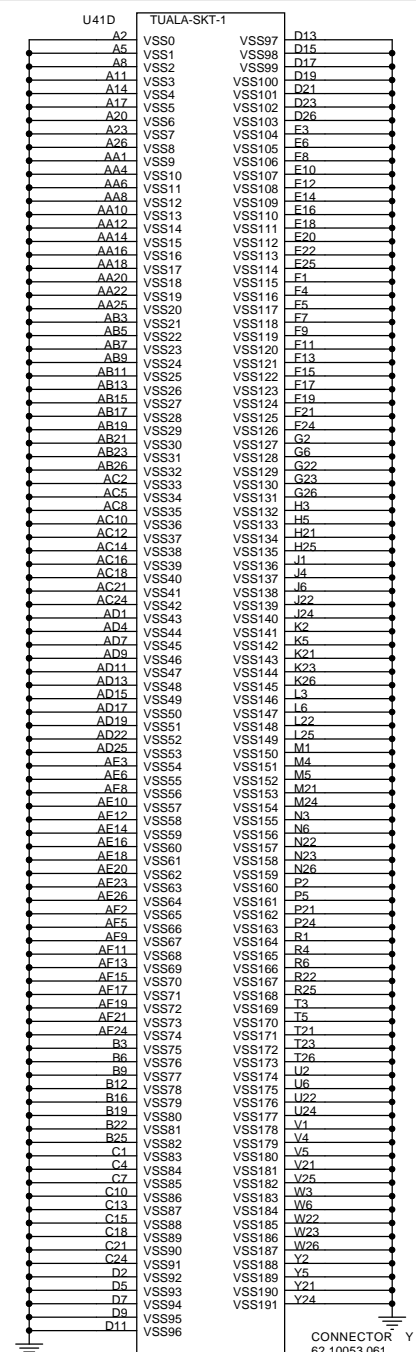
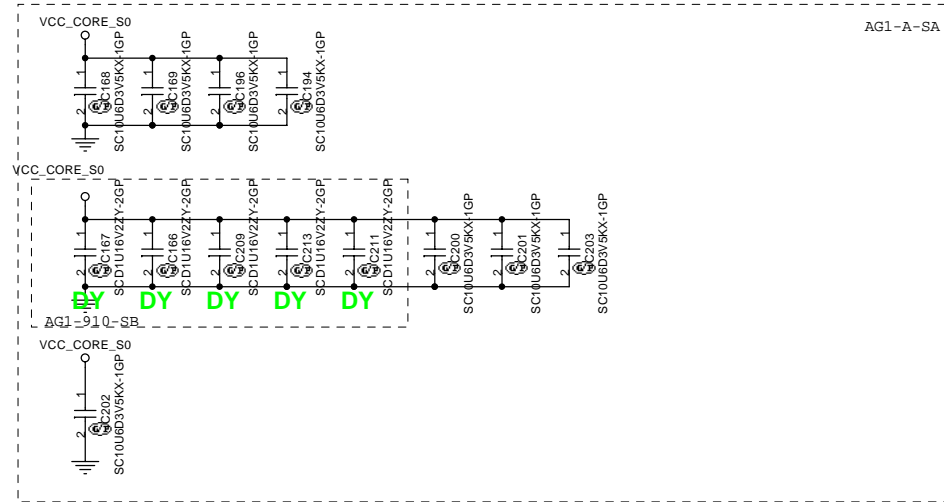




62.10053.061 CONNECTOR Y

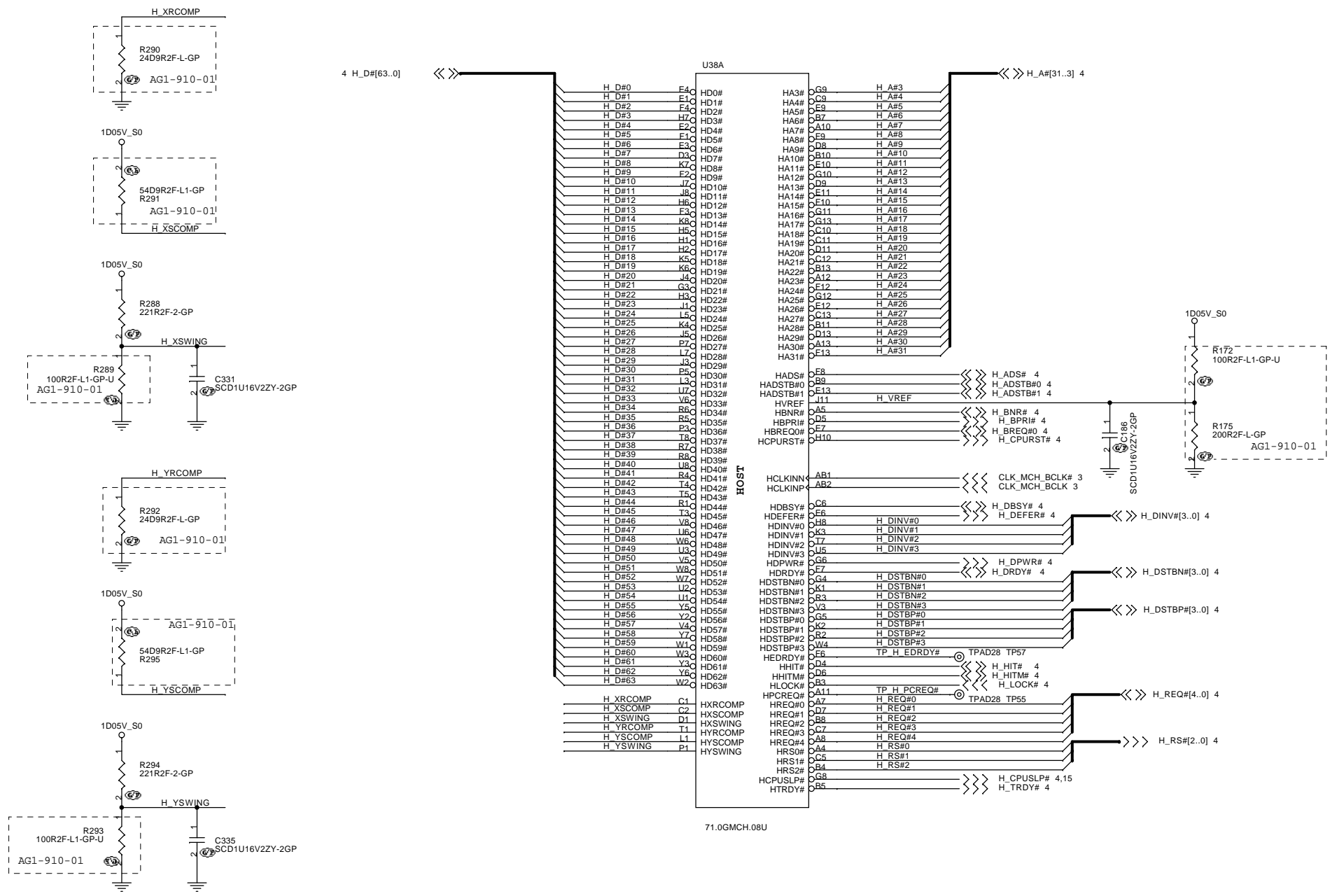
Layout Note: VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note: Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.



<Core Design>

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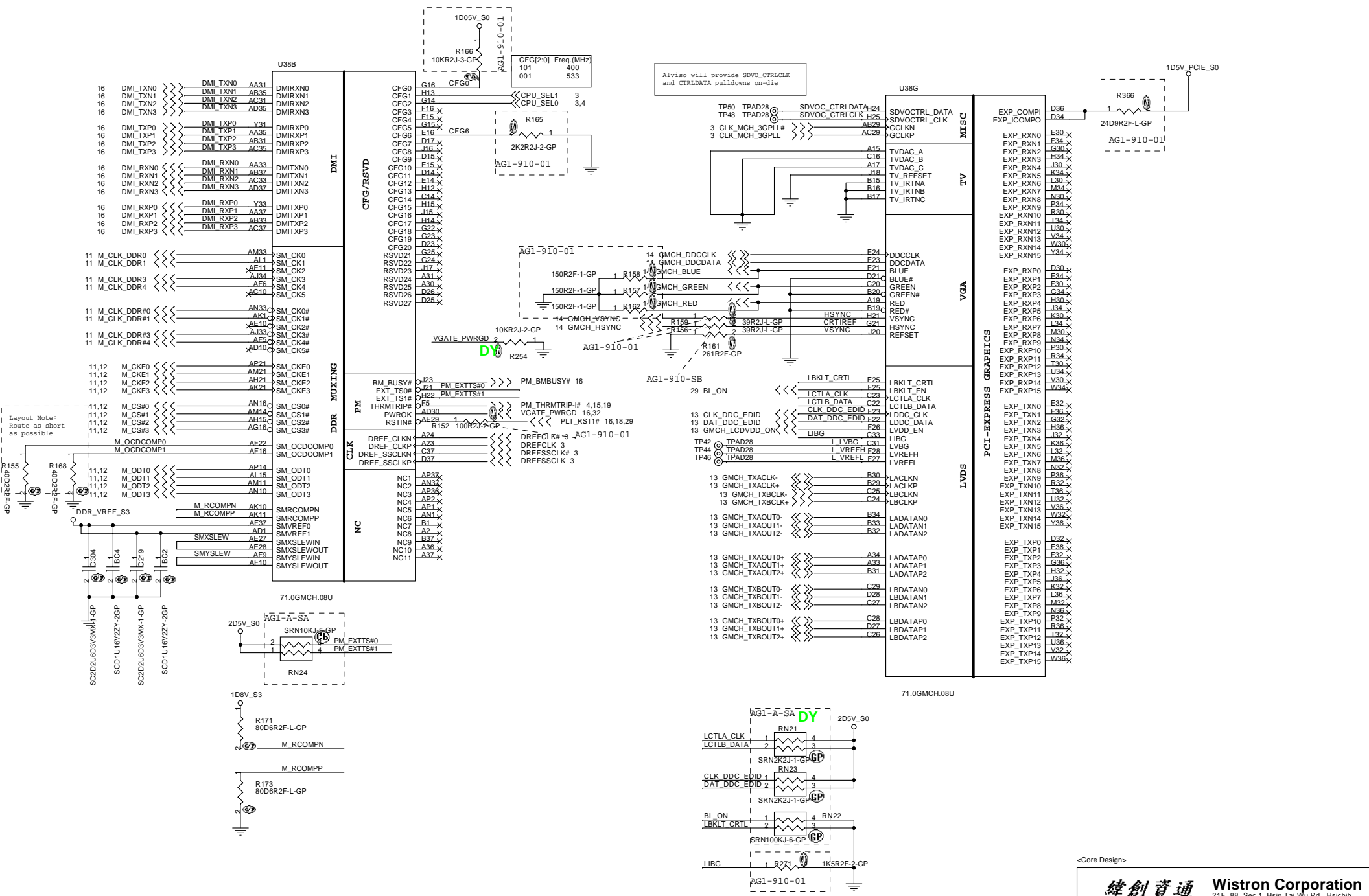
<Core Design>

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Title: **GMCH (1 of 5)**

Size A3	Document Number	Rev
	<b>AG1(Alviso)</b>	<b>01</b>

Date: Tuesday, October 25, 2005 Sheet 6 of 40



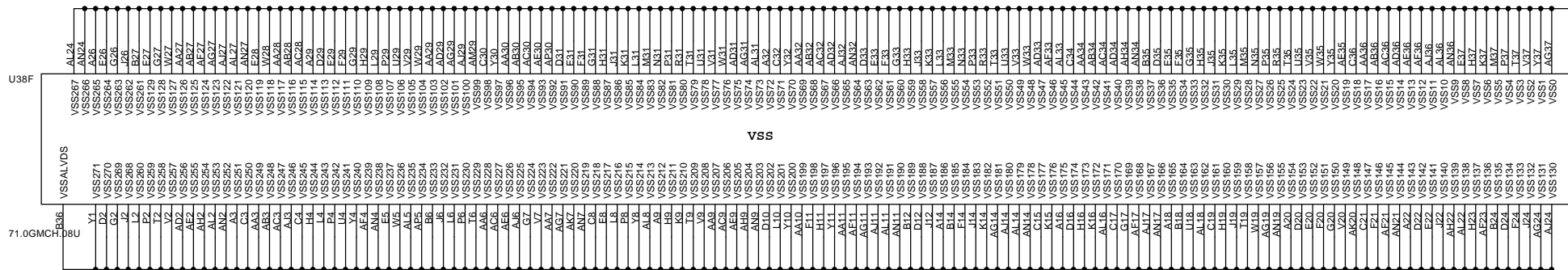
<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

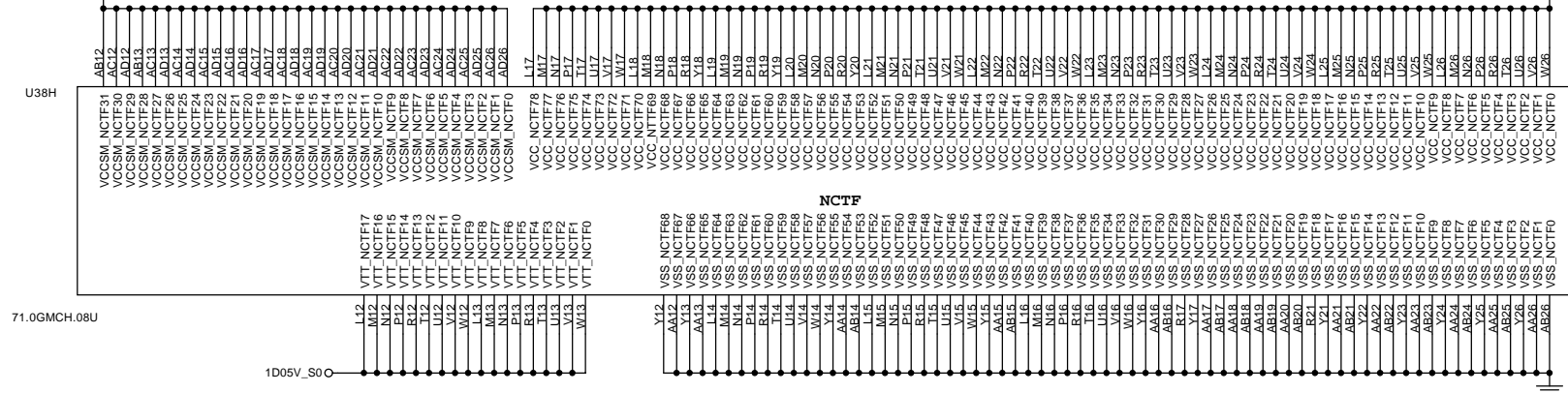
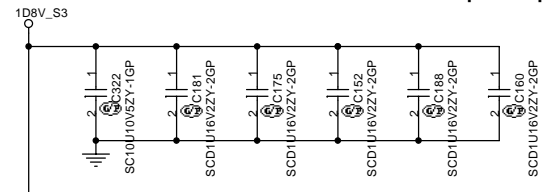
Title			GMCH (2 of 5)		
Size	Document Number			Rev	
Custom	AG1(Alviso)				01
Date:	Tuesday, October 25, 2005	Sheet	7	of	40







Place these Hi-Freq decoupling caps near GMCH



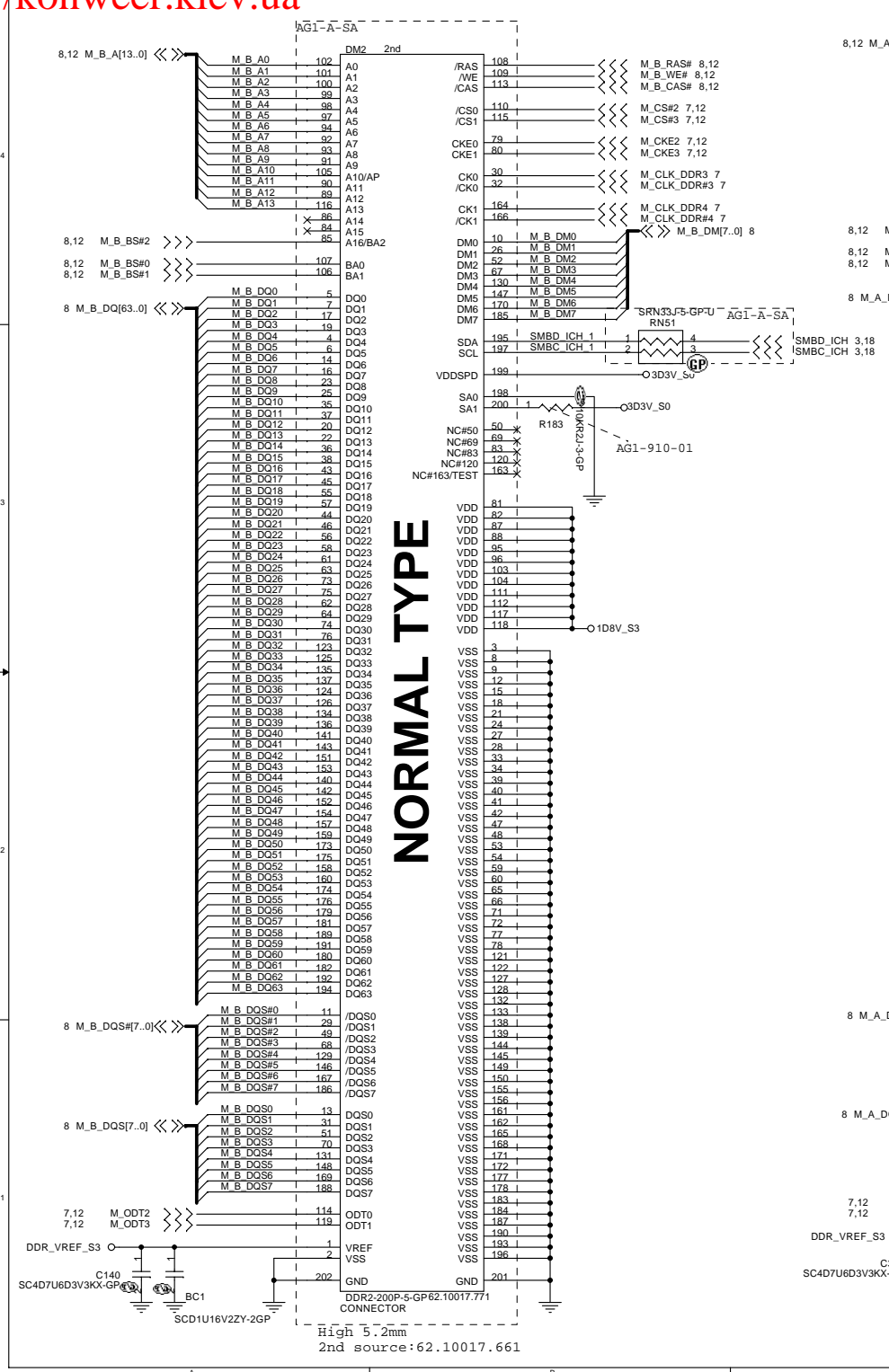
<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

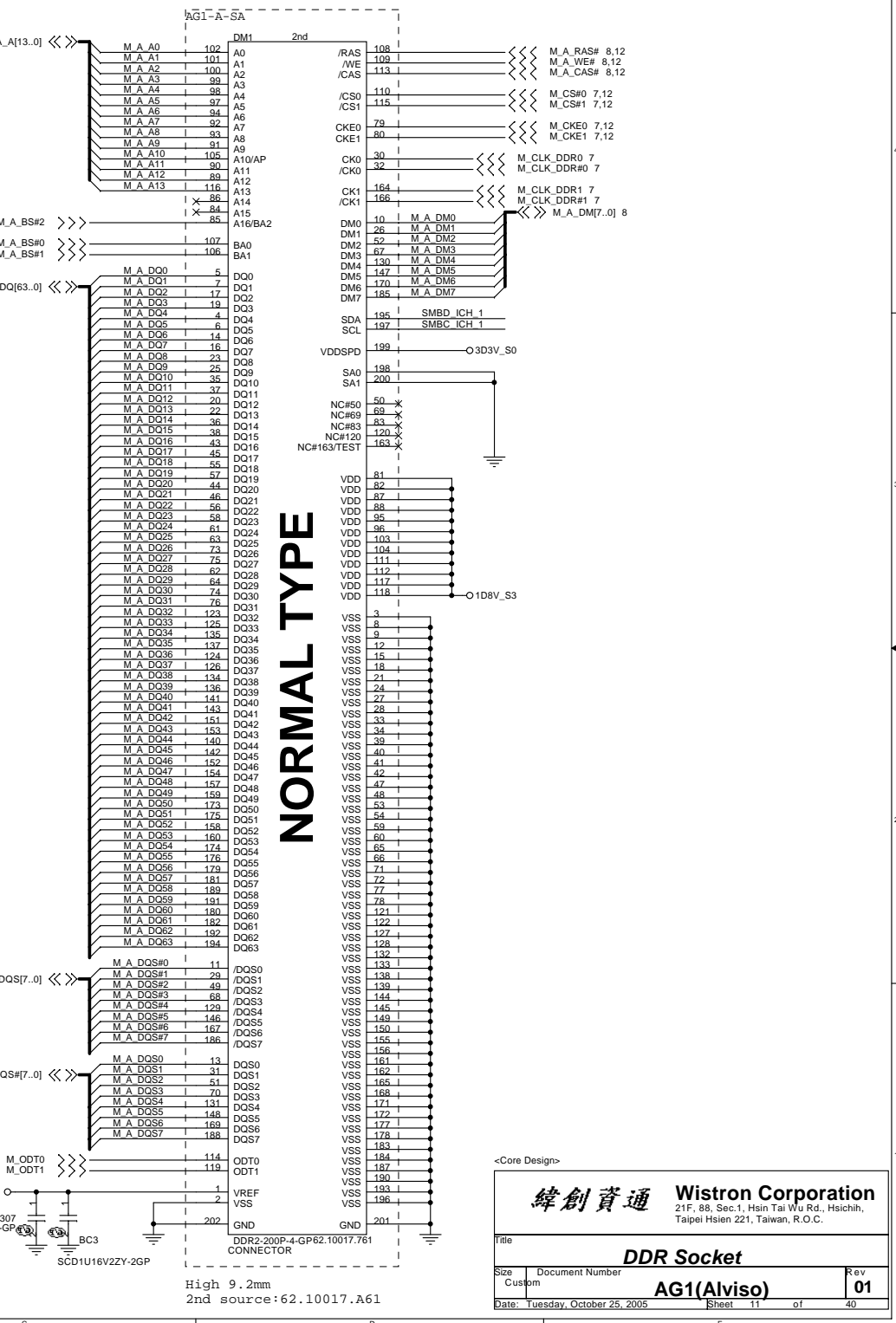
Title: **GMCH (5 of 5)**

Size A3 Document Number **AG1(Alviso)** Rev **01**

Date: Monday, October 17, 2005 Sheet 10 of 40



NORMAL TYPE



NORMAL TYPE

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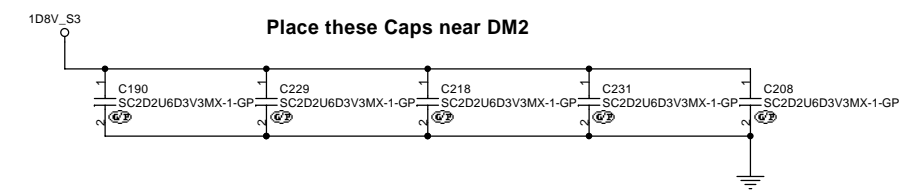
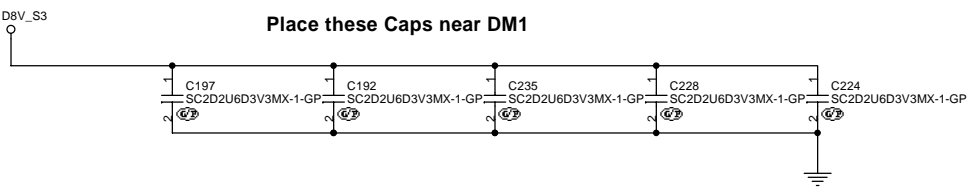
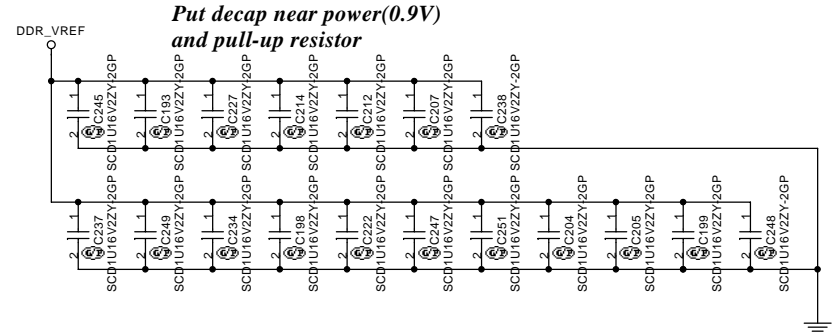
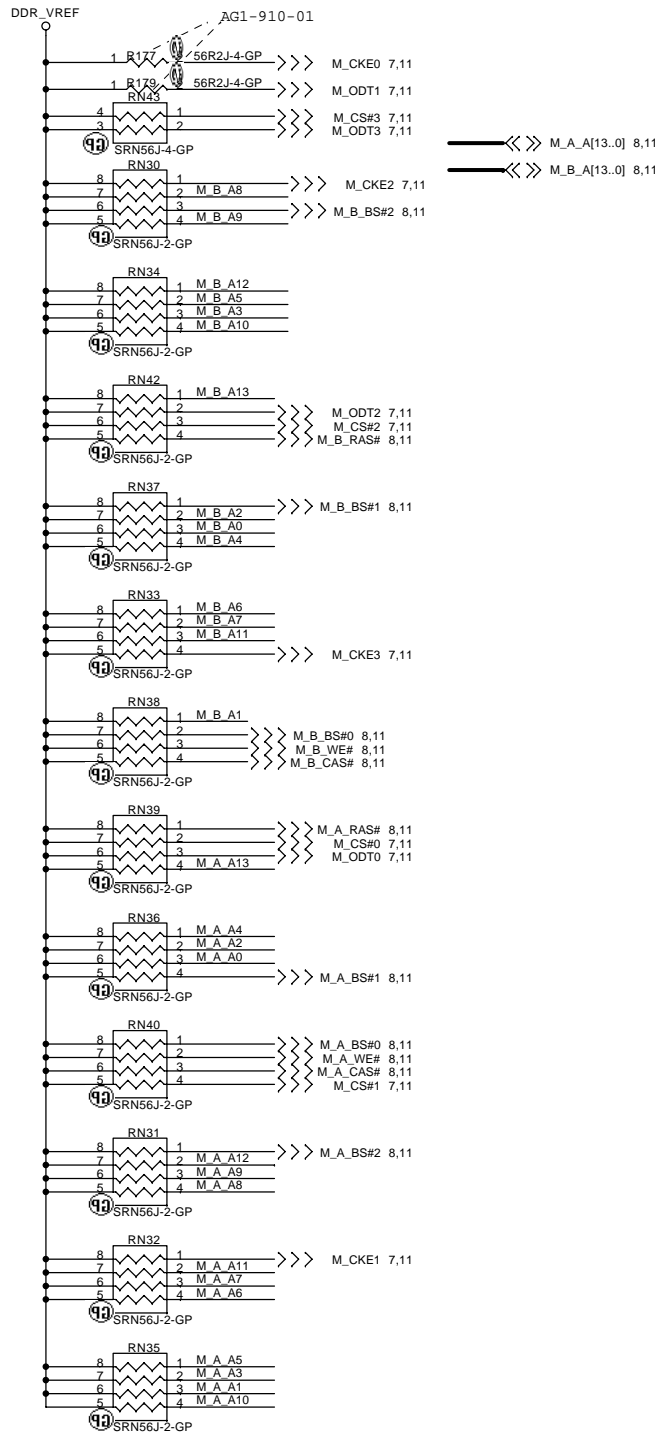
**DDR Socket 221**

File: **AG1(Alviso)** Rev: **01**

Date: Tuesday, October 25, 2005 Sheet 11 of 40

High 5.2mm  
2nd source:62.10017.661

High 9.2mm  
2nd source:62.10017.A61



<Core Design>

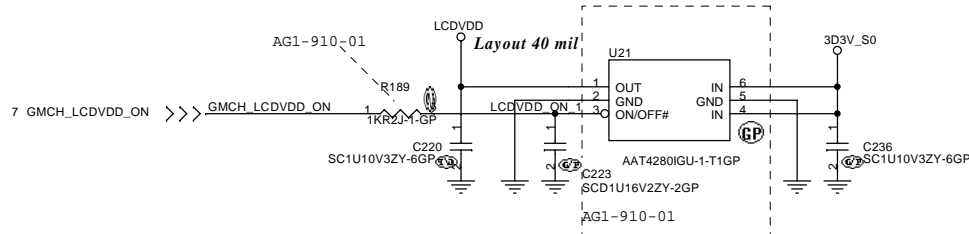
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2 Termination Resistor**

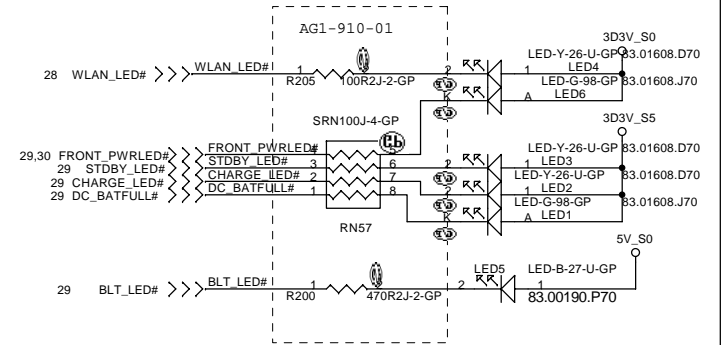
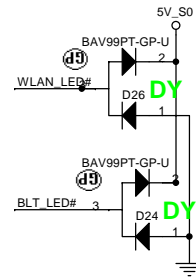
Size: A3 Document Number: **AG1(Alviso)** Rev: **01**

Date: Tuesday, October 25, 2005 Sheet 12 of 40

# LED



## LCD/INVERTER/CCD CONN

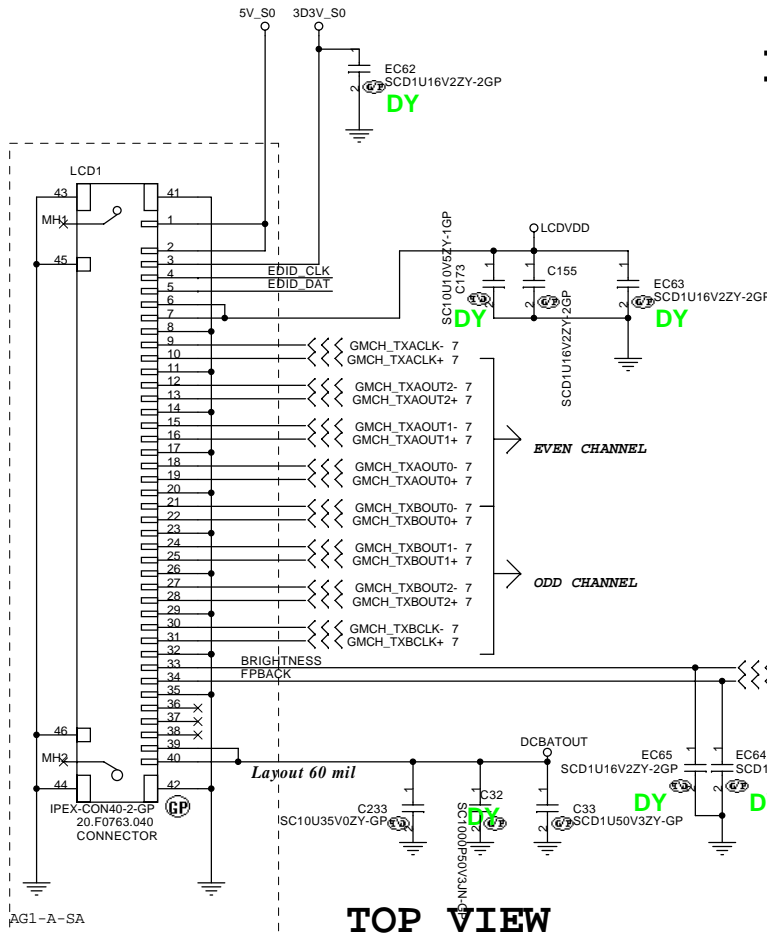


## LED BD CONN

Pin	Symbol
1	5V
2	USB-
3	USB+
4	GND
5	GND

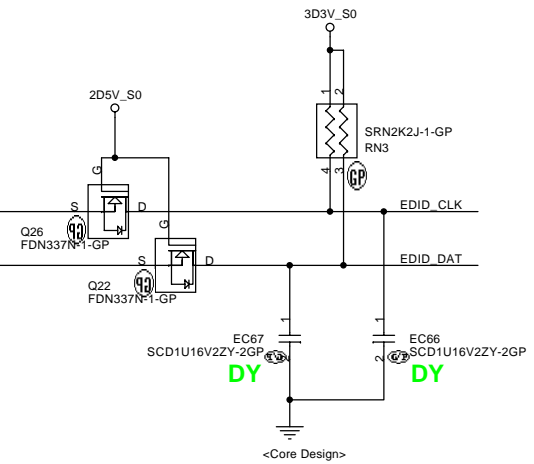
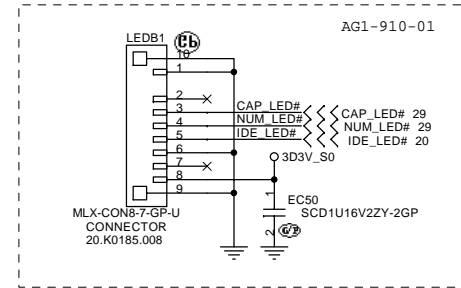
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Pin	Symbol
1	5V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	KCOL19
8	MAIL_LED#
9	STDBY_LED#
10	PWRLED#
11	GND
12	GND



TOP VIEW

LCD



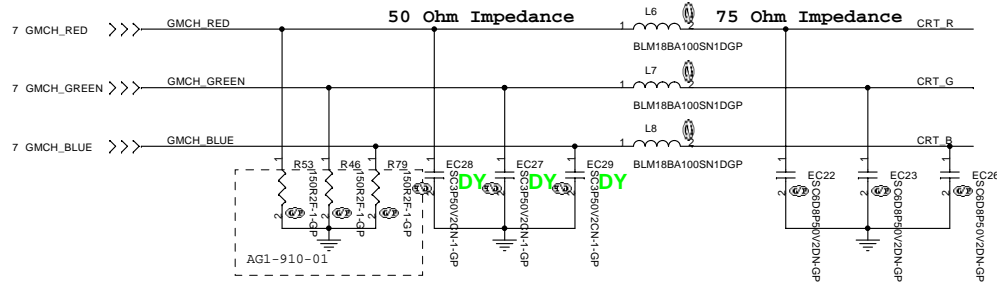
<Core Design>

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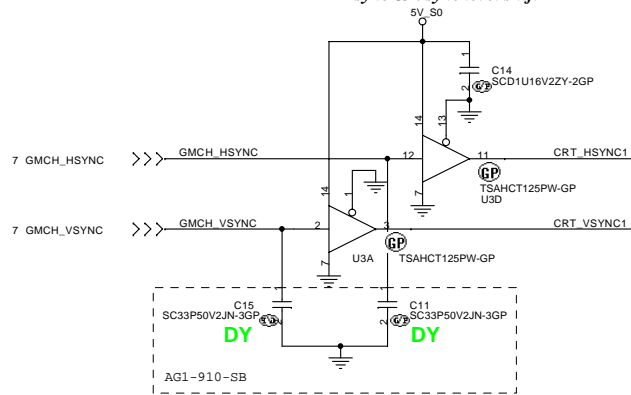
Title		
LCD CONN & LED		
Size	Document Number	Rev
A3	AG1(Alviso)	01
Date: Friday, October 28, 2005	Sheet 13 of	40

# CRT CONNECTOR

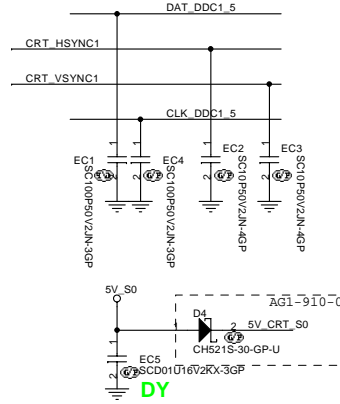
Ferrite bead impedance: 75ohm@100MHz



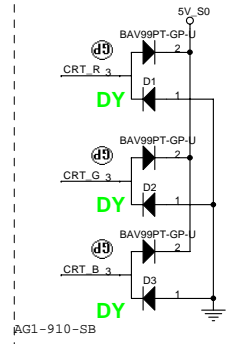
Hsync & Vsync level shift



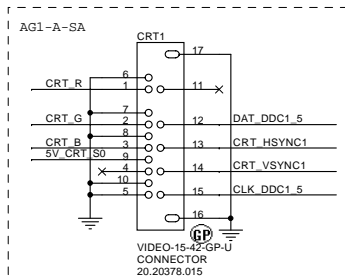
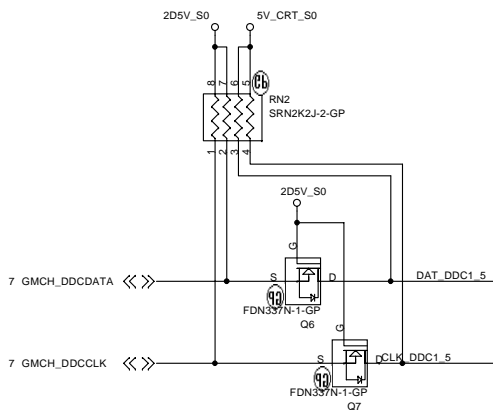
DDC\_CLK & DATA level shift



ESD Protection Diode



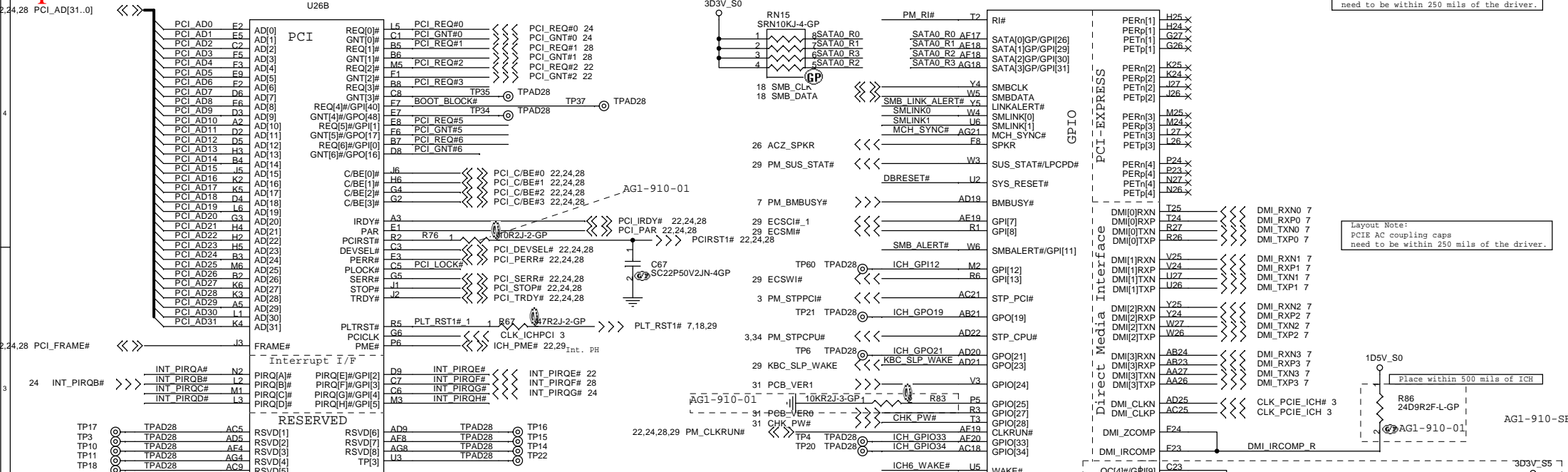
AG1-910-SB



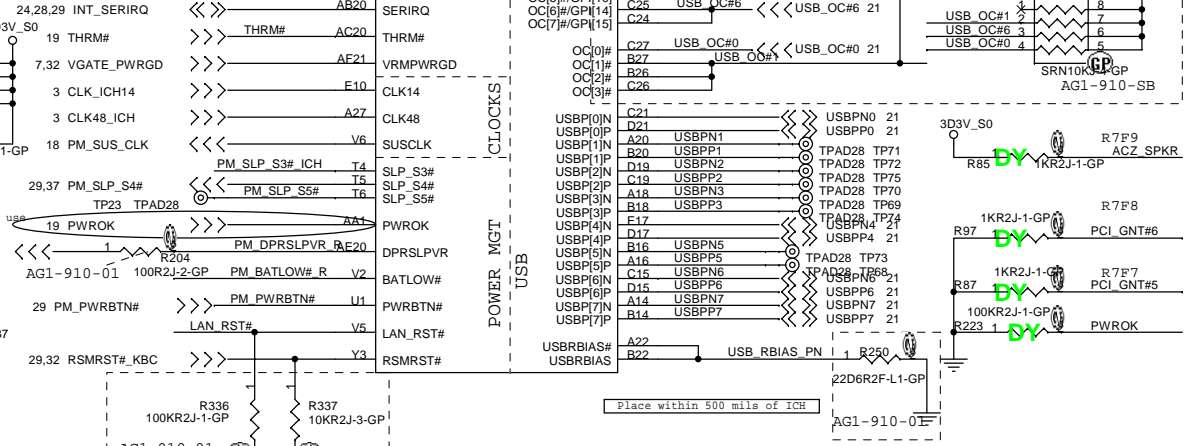
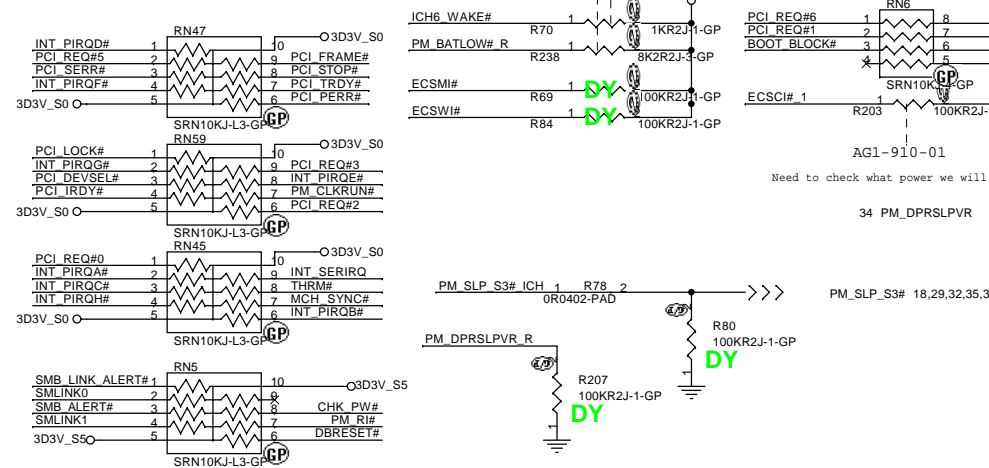
<Core Design>

<b>緯創資通 Wistron Corporation</b>		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>CRT Connector</b>		
Size	Document Number	Rev
Custom	<b>AG1(Alviso)</b>	<b>01</b>
Date: Friday, October 28, 2005	Sheet 14	of 40





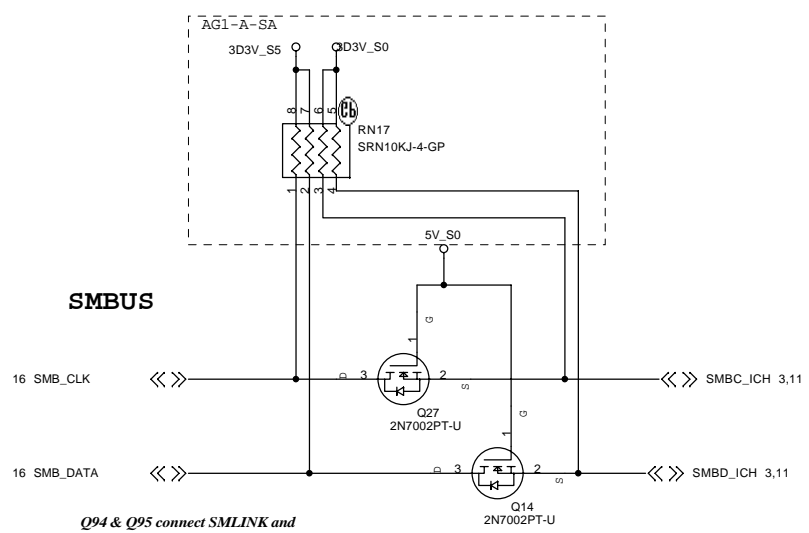
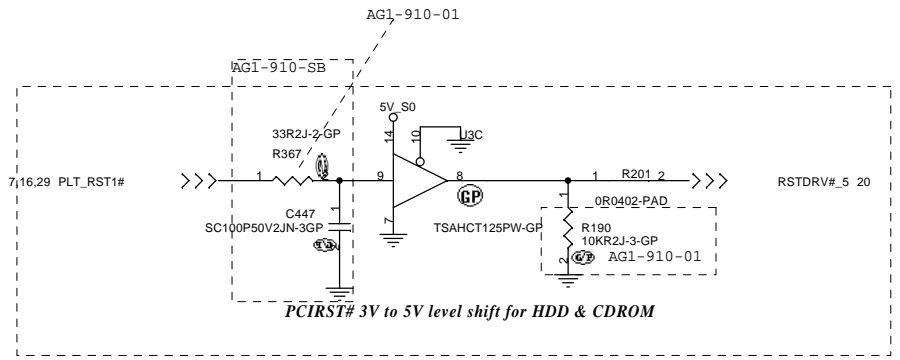
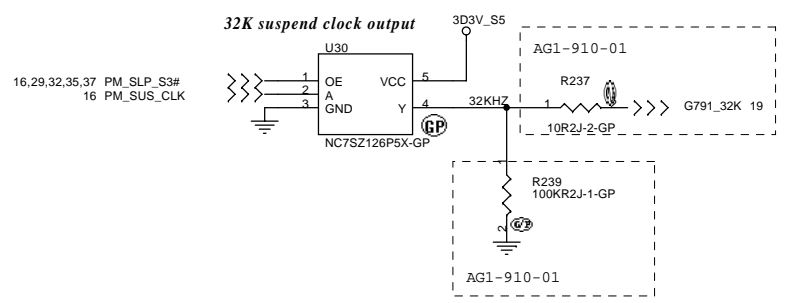
### ICH6 Pullups



### ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF





Q94 & Q95 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

F27	VSS	F4
Y6	VSS	F22
Y27	VSS	F19
Y26	VSS	F17
Y23	VSS	F25
W7	VSS	F19
W25	VSS	E18
W24	VSS	F15
W23	VSS	F14
W1	VSS	D7
V4	VSS	D20
V27	VSS	D18
V26	VSS	D18
V23	VSS	D14
U25	VSS	D13
U24	VSS	D10
U23	VSS	D1
U18	VSS	C4
U13	VSS	C22
I7	VSS	C20
T27	VSS	C18
T26	VSS	C14
T23	VSS	B25
T16	VSS	B24
T15	VSS	B23
T14	VSS	B21
T13	VSS	B19
T12	VSS	B15
T1	VSS	B13
R4	VSS	AG7
R25	VSS	AG3
R24	VSS	AG22
R23	VSS	AG20
R17	VSS	AG17
R16	VSS	AG14
R15	VSS	AG12
R14	VSS	AG1
R13	VSS	AF7
R12	VSS	AF3
R11	VSS	AF26
P22	VSS	AF12
P16	VSS	AF10
P15	VSS	AF1
P14	VSS	AE7
P13	VSS	AE6
P12	VSS	AE25
N7	VSS	AE21
N17	VSS	AE2
N16	VSS	AE12
N15	VSS	AE11
N14	VSS	AE10
N13	VSS	AD6
N12	VSS	AD24
N11	VSS	AD2
N1	VSS	AD18
M4	VSS	AD15
M27	VSS	AD10
M26	VSS	AD1
M23	VSS	AC6
M16	VSS	AC3
M15	VSS	AC26
M14	VSS	AC24
M13	VSS	AC23
M12	VSS	AC22
I25	VSS	AC12
I24	VSS	AC10
I23	VSS	AB9
I15	VSS	AB7
I13	VSS	AB2
K7	VSS	AB19
K27	VSS	AB10
K26	VSS	AB1
K23	VSS	AA4
K1	VSS	AA16
J4	VSS	AA13
J25	VSS	AA11
J24	VSS	A9
J23	VSS	A7
H27	VSS	A4
H26	VSS	A26
H23	VSS	A23
G9	VSS	A21
G7	VSS	A18
G21	VSS	A15
G12	VSS	A12
G1	VSS	A1

<Core Design>

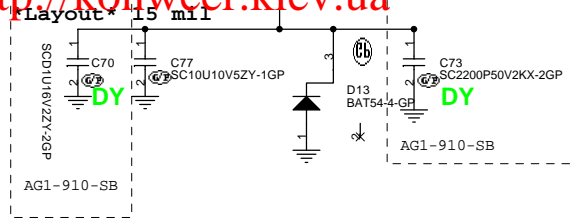
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH6-M (4 of 4)**

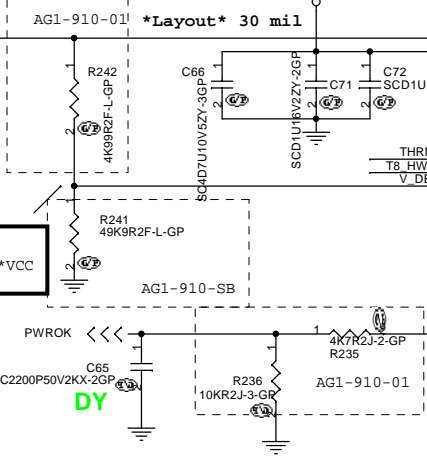
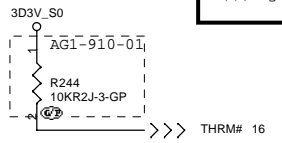
Size A3	Document Number	Rev
	<b>AG1(Alviso)</b>	<b>01</b>

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AM\_VCC

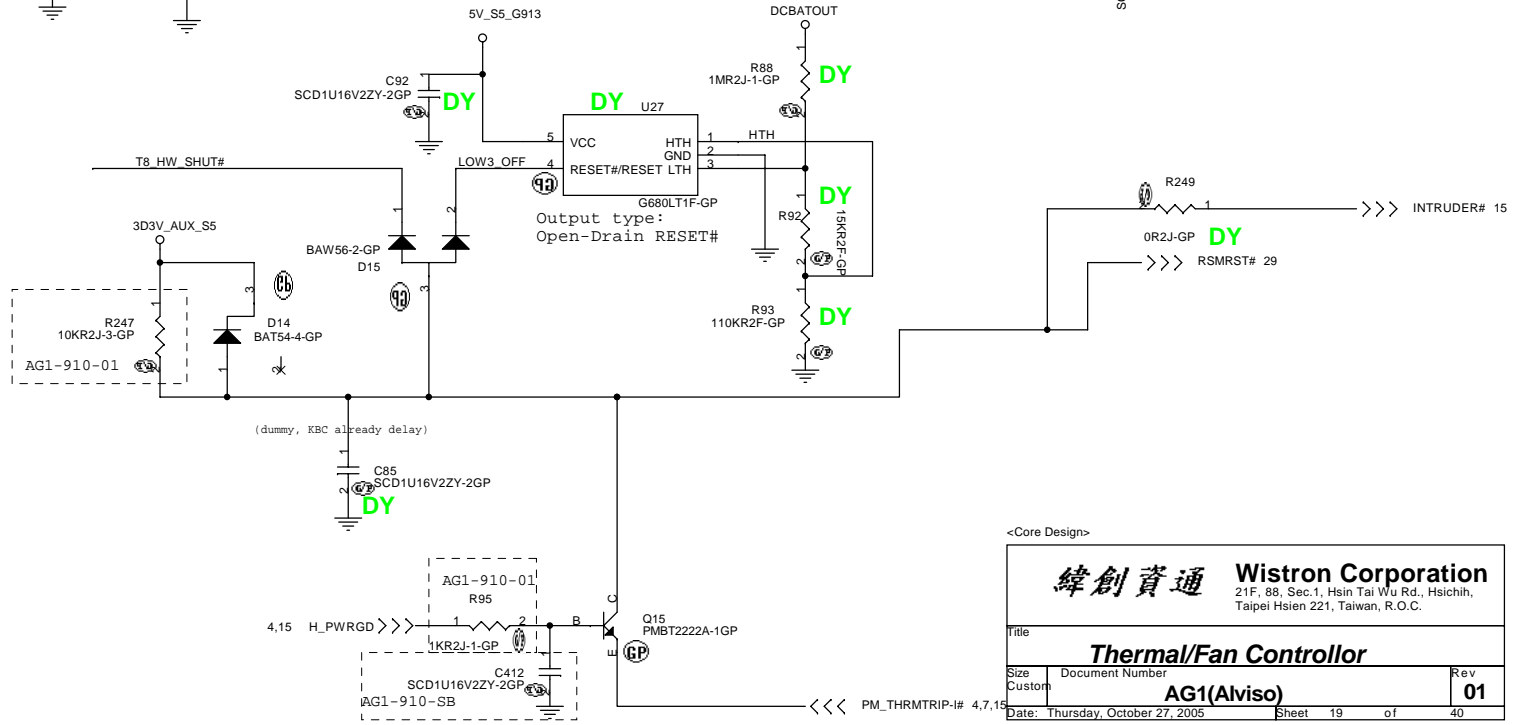


Setting T8 as 100 Degree

$$V\_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$


DXP1:108 Degree  
DXP2:H/W Setting  
DXP3:88 Degree

Place near chip as close as possible



<Core Design>

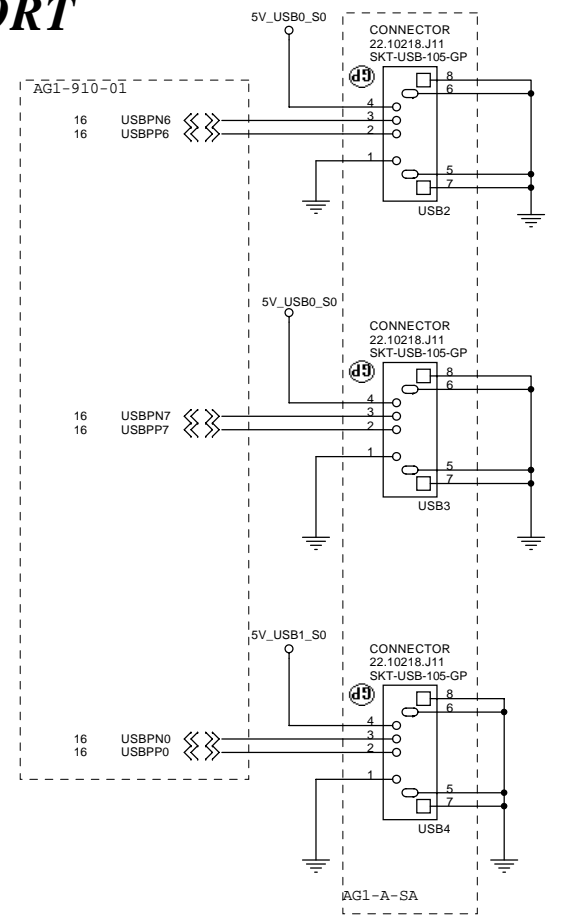
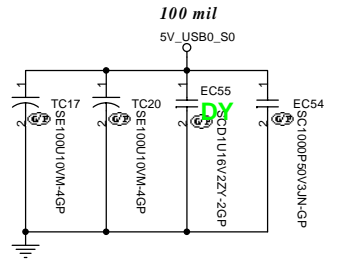
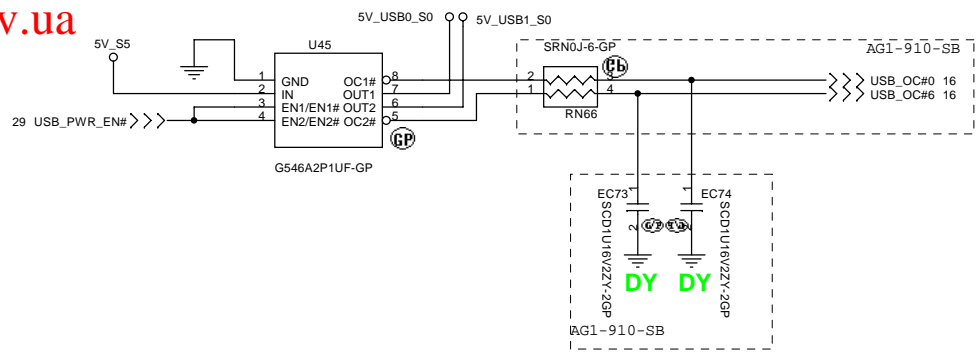
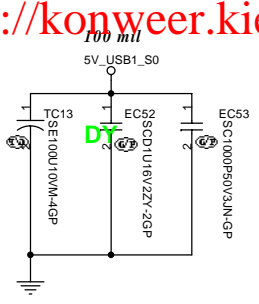
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file  
**Thermal/Fan Controller**

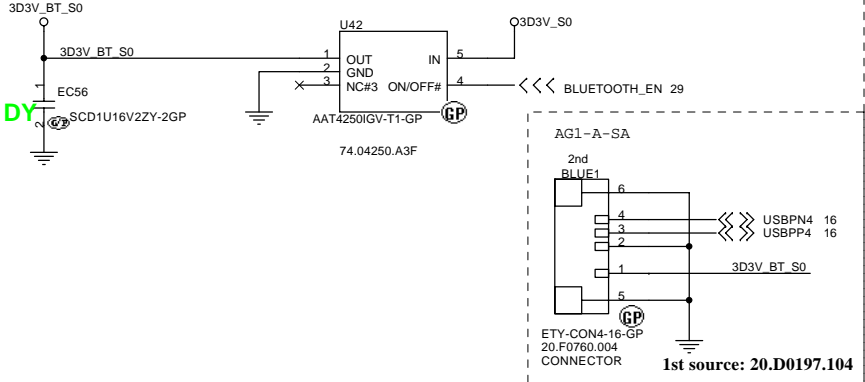
Size Custom	Document Number	Rev
	<b>AG1(Alviso)</b>	<b>01</b>

Date: Thursday, October 27, 2005 Sheet 19 of 40

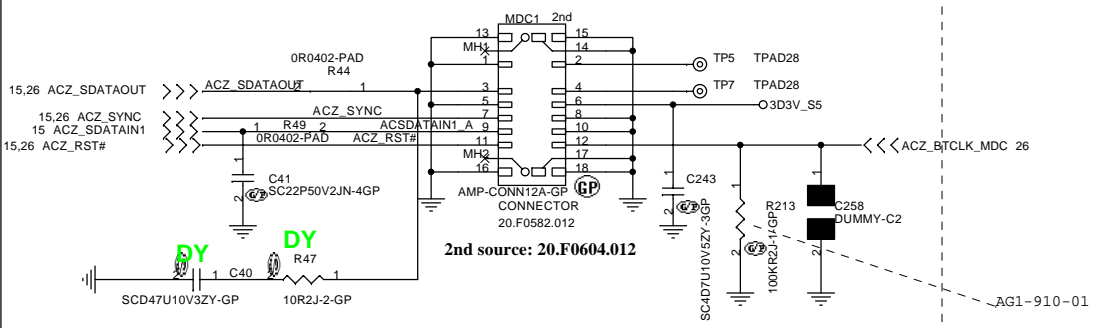




## BLUETOOTH MODULE



## MDC 1.5 CONNECTOR



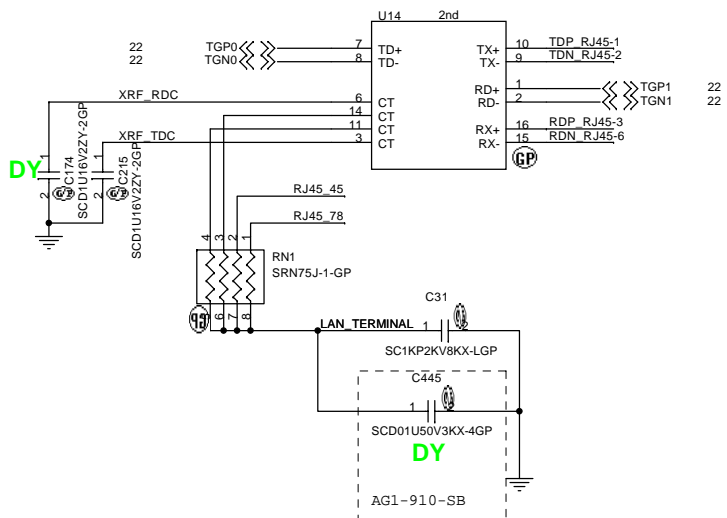
<Core Design>

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Title		
<b>USB / MDC / BLUETOOTH</b>		
Size	Document Number	Rev
A3	<b>AG1(Alviso)</b>	<b>01</b>
Date: Friday, October 28, 2005	Sheet 21 of 40	

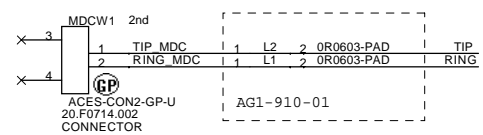


**10/100M Lan Transformer**

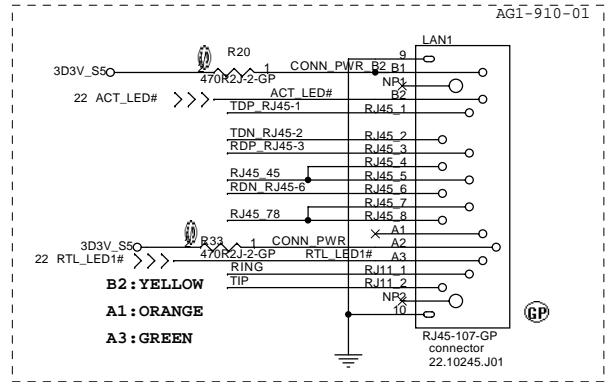


1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

**LAN Connector**



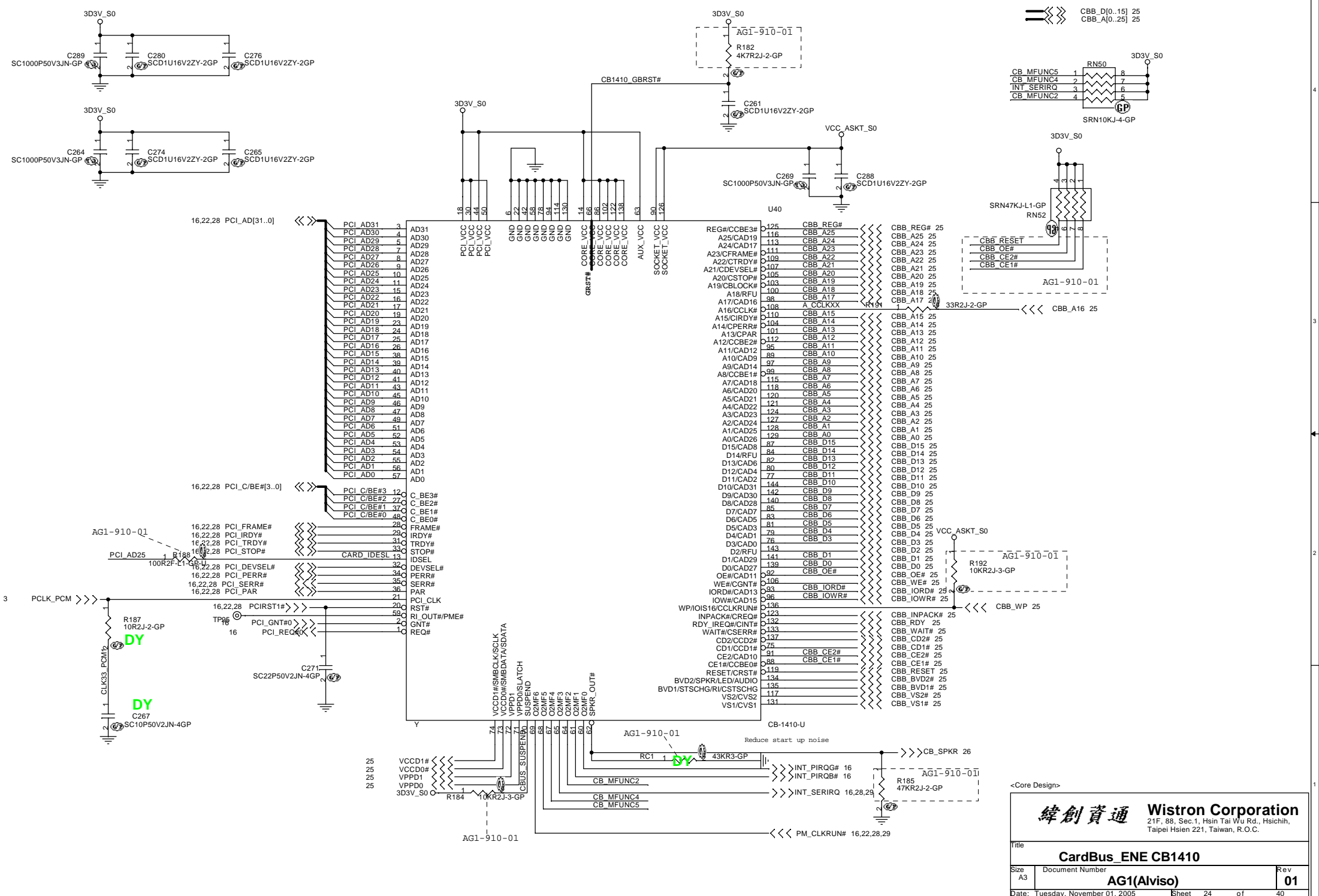
2nd source: 20.D0196.102



- B2 : YELLOW
- A1 : ORANGE
- A3 : GREEN

<Core Design>

<p><b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
Title		
<b>LAN CONN</b>		
Size	Document Number	Rev
A3	<b>AG1(Alviso)</b>	<b>01</b>
Date: Saturday, October 29, 2005		
Sheet 23		of 40

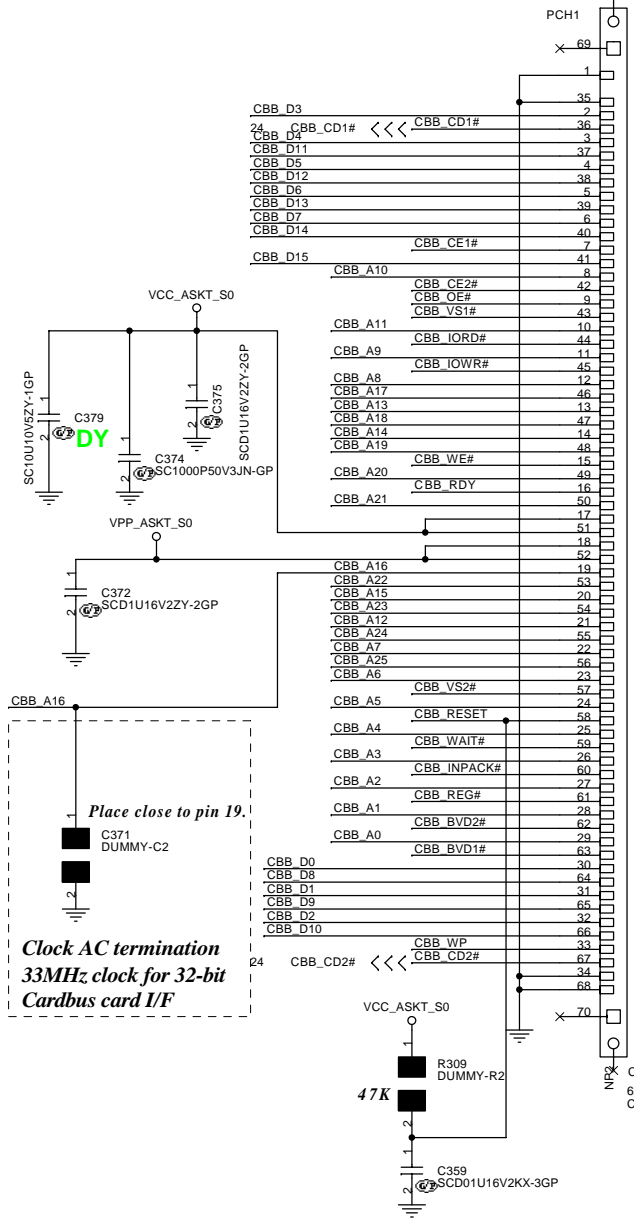


<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

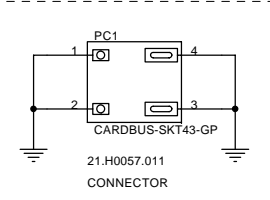
Title		
<b>CardBus_ENE CB1410</b>		
Size	Document Number	Rev
A3	<b>AG1(Alviso)</b>	<b>01</b>
Date:	Tuesday, November 01, 2005	Sheet 24 of 40

**PCMCIA Socket**

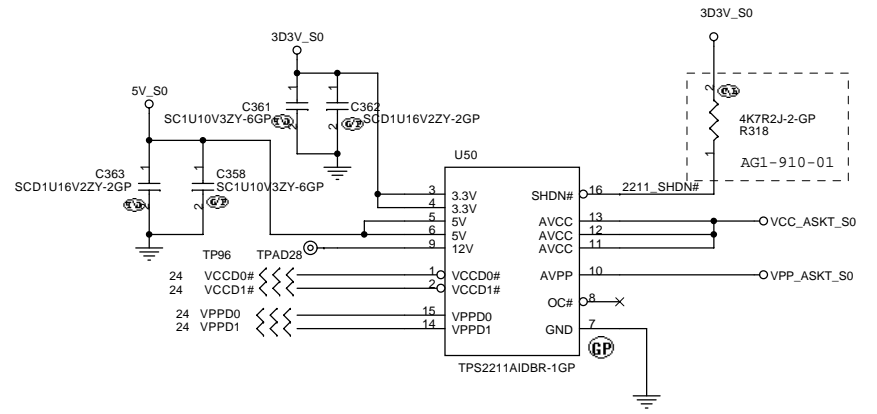


**Cardbus I/F**

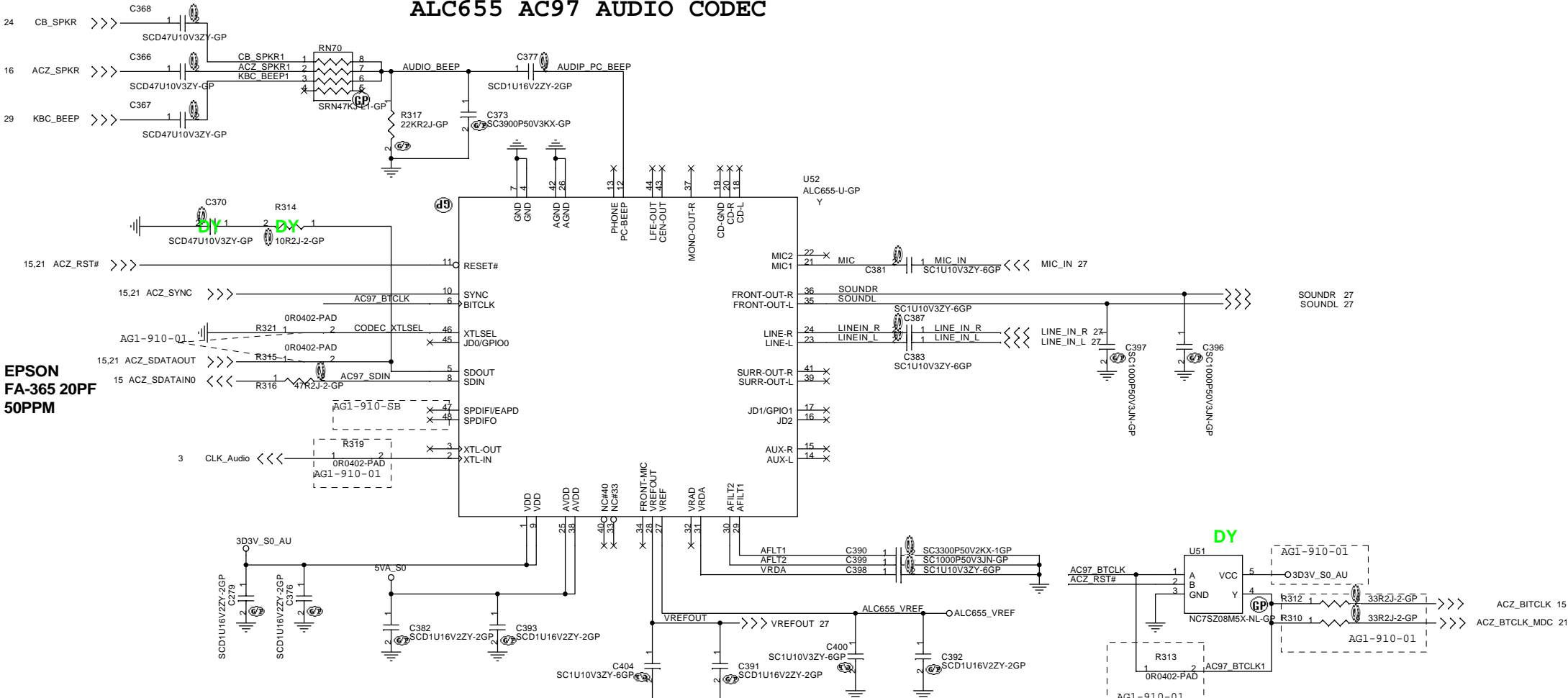
- ≡≡≡ CBB\_D[0..15] 24
- ≡≡≡ CBB\_A[0..25] 24
- ≡≡≡ CBB\_IORD# 24
- ≡≡≡ CBB\_IOWR# 24
- ≡≡≡ CBB\_OE# 24
- ≡≡≡ CBB\_WE# 24
- ≡≡≡ CBB\_REG# 24
- ≡≡≡ CBB\_RDY 24
- ≡≡≡ CBB\_WP 24
- ≡≡≡ CBB\_RESET 24
- ≡≡≡ CBB\_WAIT# 24
- ≡≡≡ CBB\_INPACK# 24
- ≡≡≡ CBB\_CE1# 24
- ≡≡≡ CBB\_CE2# 24
- ≡≡≡ CBB\_BVD1# 24
- ≡≡≡ CBB\_BVD2# 24
- ≡≡≡ CBB\_VS1# 24
- ≡≡≡ CBB\_VS2# 24



**Power switch**



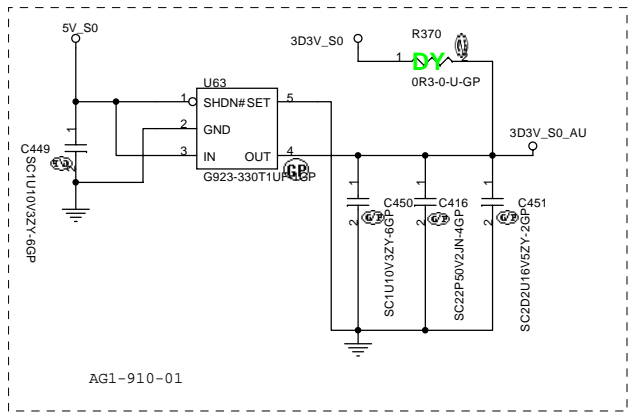
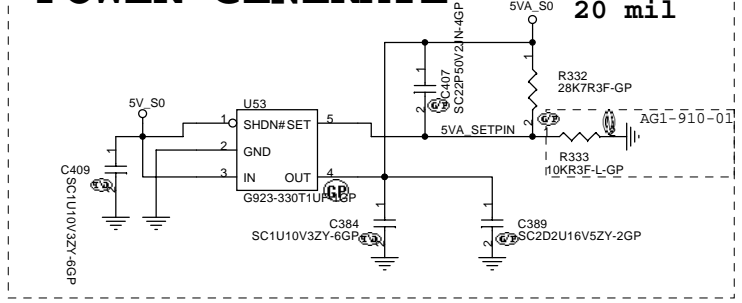
### ALC655 AC97 AUDIO CODEC



EPSON  
FA-365 20PF  
50PPM

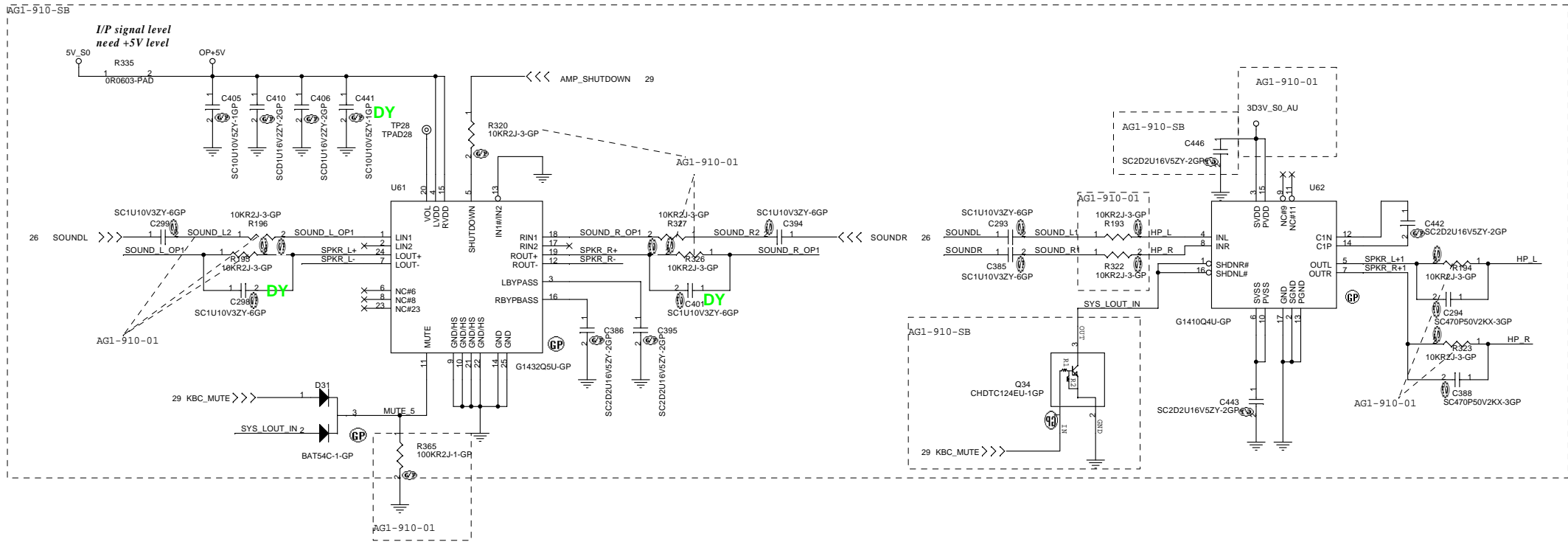
### POWER GENERATE

\*Layout\*  
20 mil

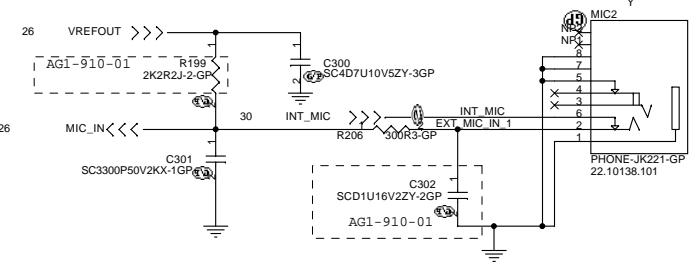


<Core Design>

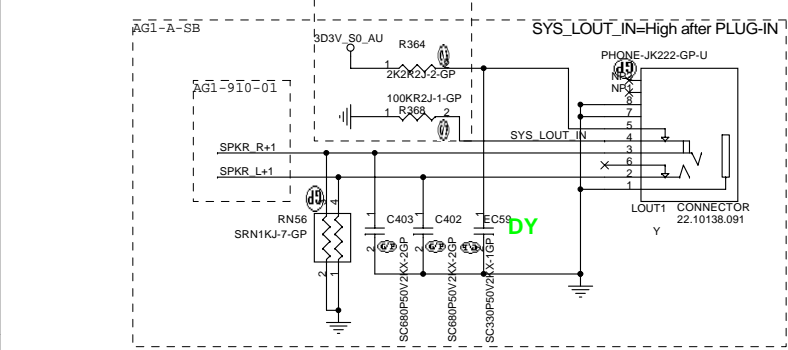
<b>緯創資通 Wistron Corporation</b>		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>AC'97 CODEC - ALC655</b>			
Size A3	Document Number <b>AG1(Alviso)</b>	Rev <b>01</b>	
Date: Tuesday, November 01, 2005		Sheet	26 of 40



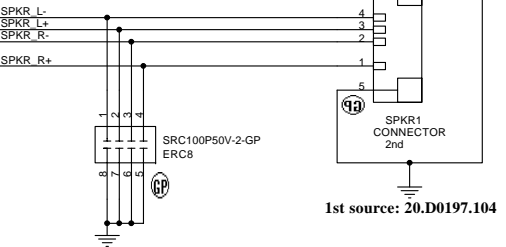
**EXTernal MIC IN**



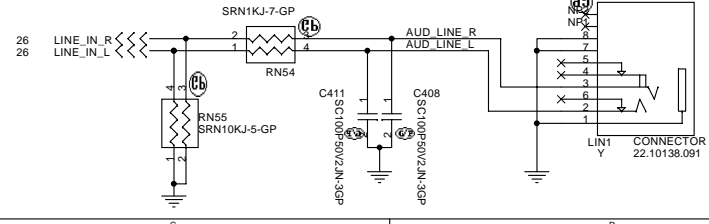
**LINE OUT**



**Internal Speaker**



**LINE IN**



<Core Design>

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Title: **Audio AMP and Jack**

Size: Document Number

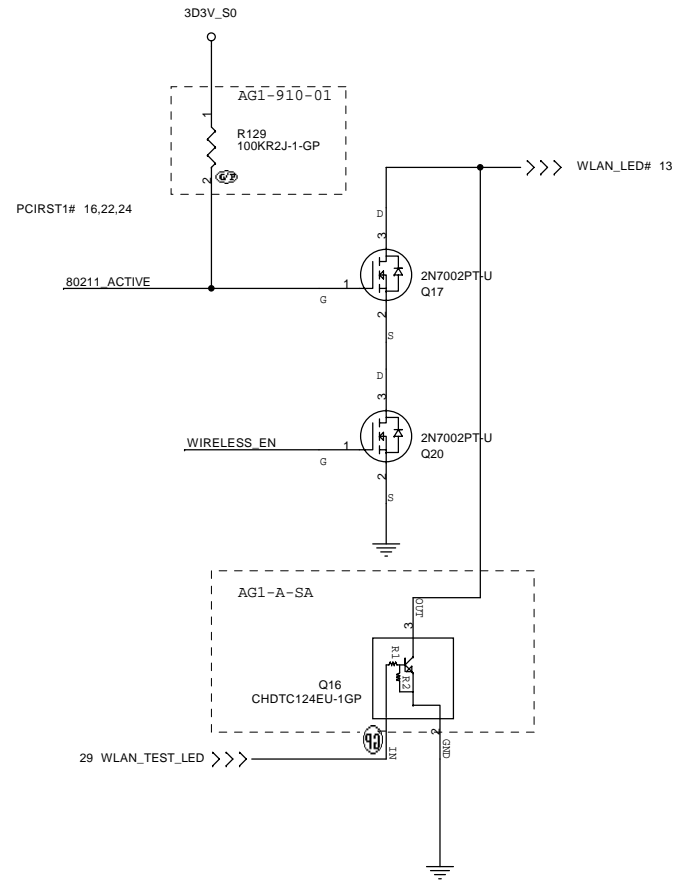
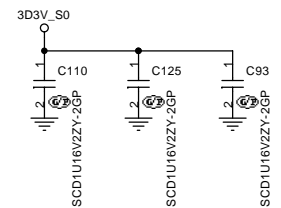
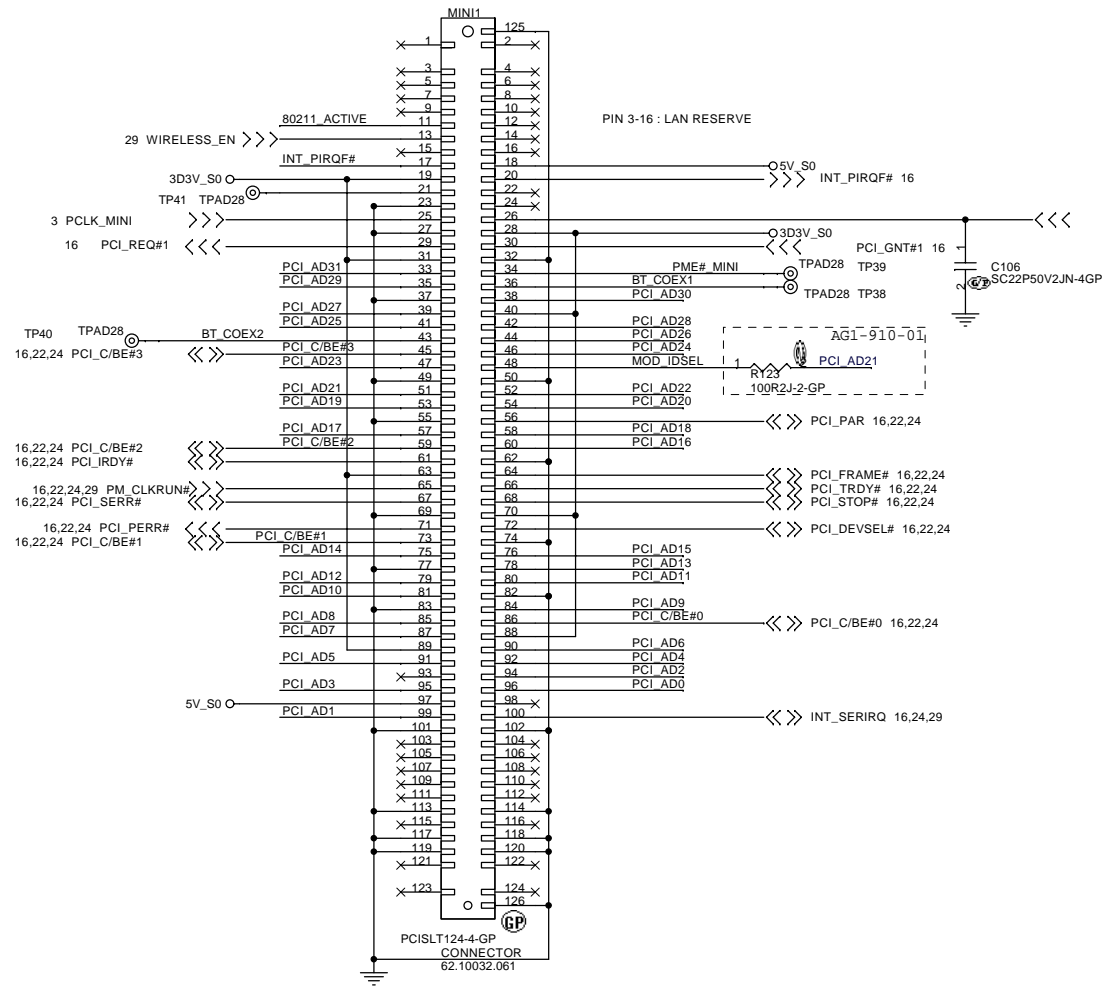
Date: Monday, October 31, 2005

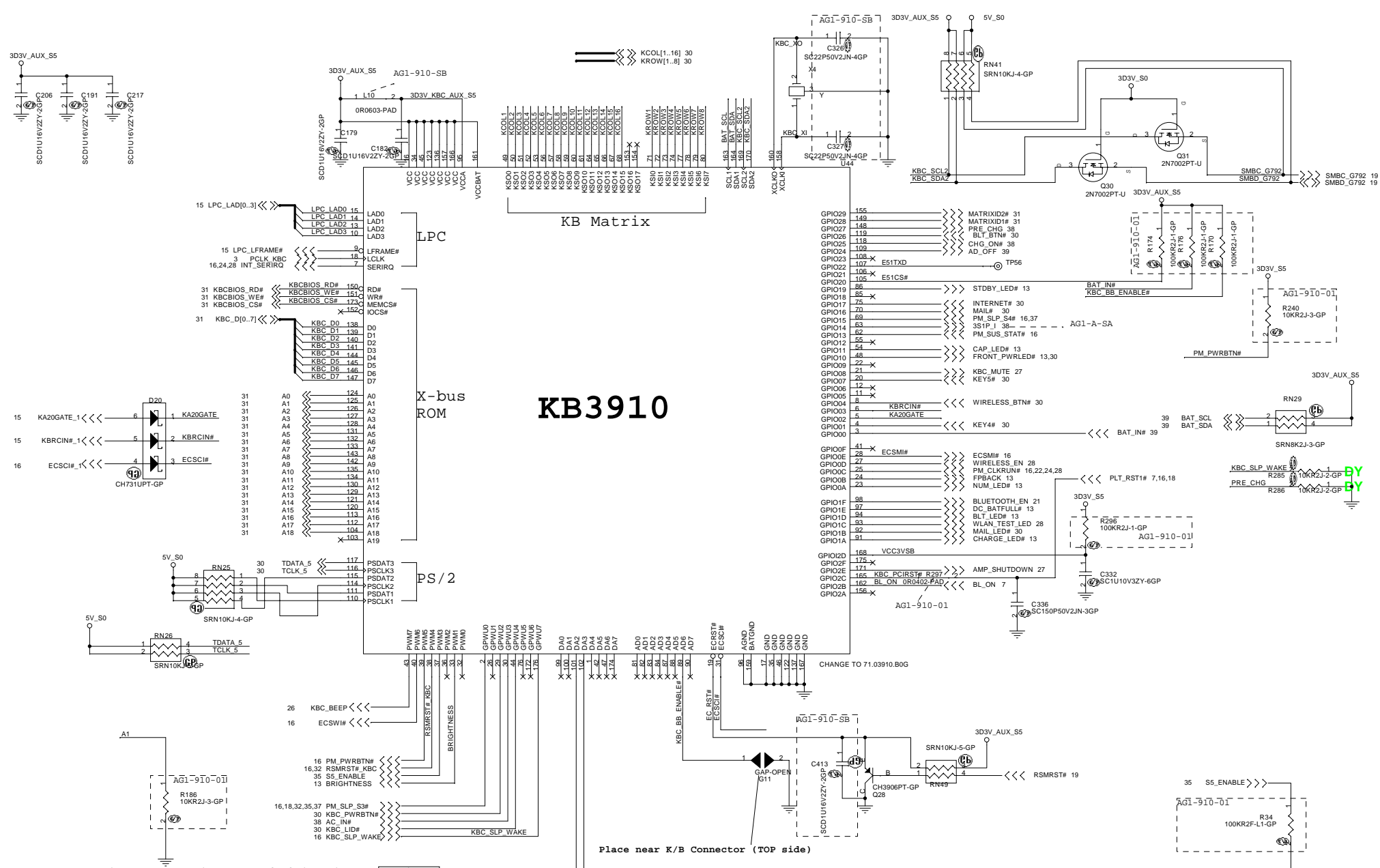
Sheet 27 of 40

Rev 01

**AG1(Alviso)**

16,22,24 PCI\_AD[31..0] <<<





# KB3910

A4 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable  
 A4 for DMRP==>High=Disable,Low=Enable  
 A5 for EMWB==>High=Enable,Low=Disable  
 GPIO05 for clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)  
 GPIO06 for DPLL test mode==> High=Test Mode,Low=Normal operation(Recommended)

Place near K/B Connector (TOP side)

-Core Design-

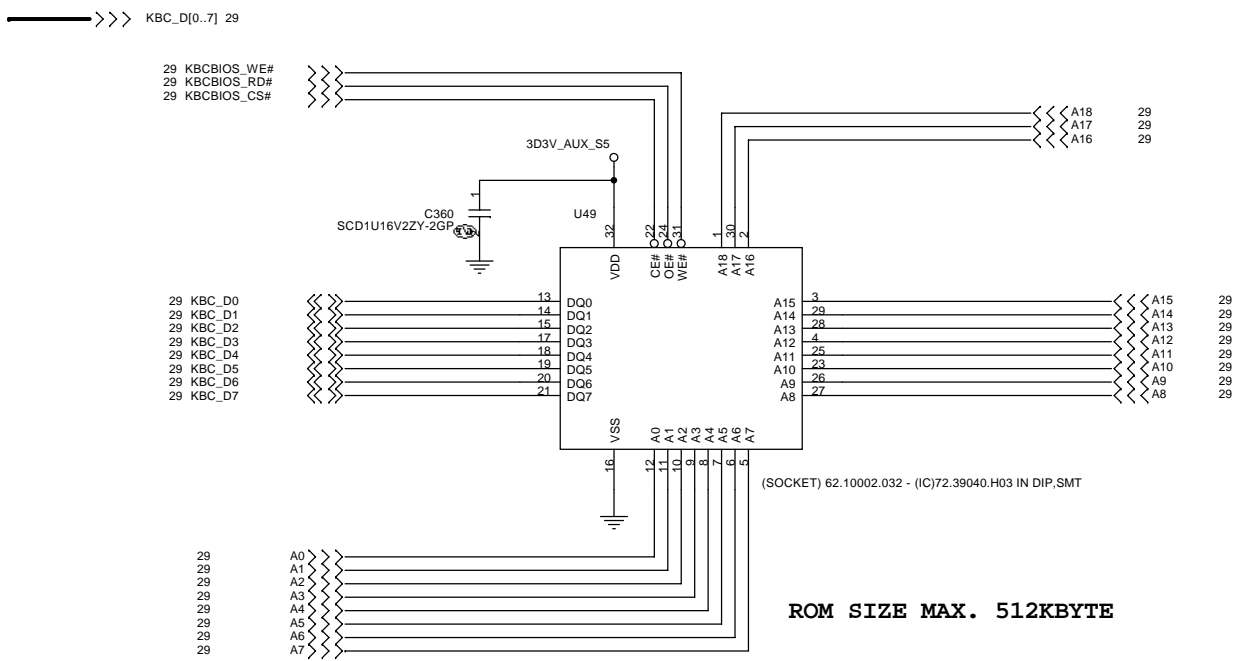
**緯創資通** Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

**KBC ENE**

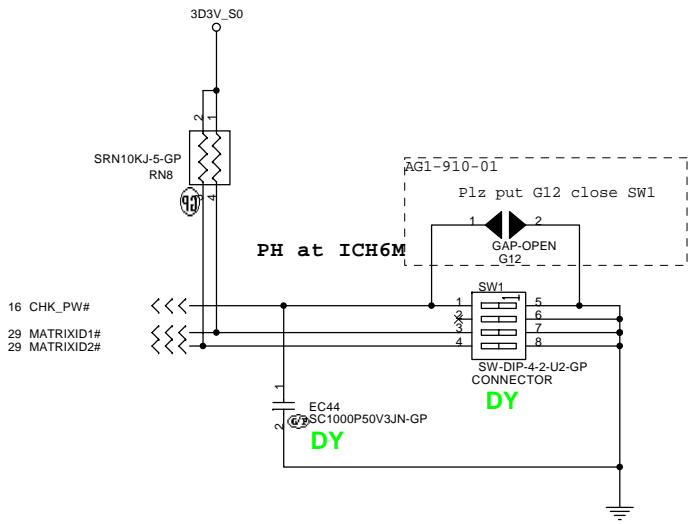
**AG1(Alviso)**

File: \_\_\_\_\_  
 Size: Custom Document Number: \_\_\_\_\_ Rev: **01**  
 Date: Thursday, October 27, 2005 Sheet: 29 of 40



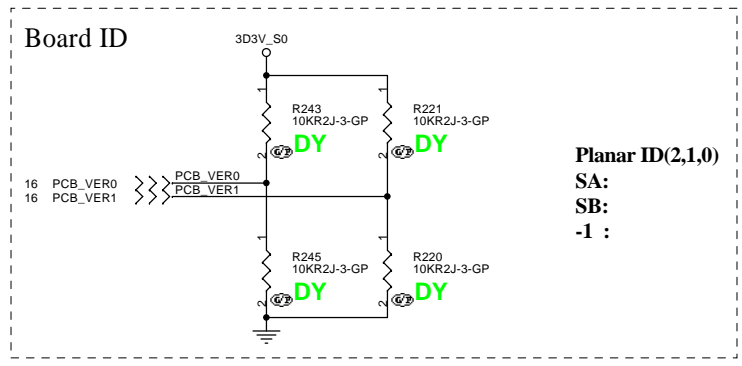


PLCC32 Socket P/N:  
SSKT3262.10002.032  
SSKT32 62.10005.032



Keyboard matrix ( from vendor )

	US	Jap	Eur	Other
Low Bit MATRIXID1#	1	1	0	0
High Bit MATRIXID2#	1	0	1	0



<Core Design>

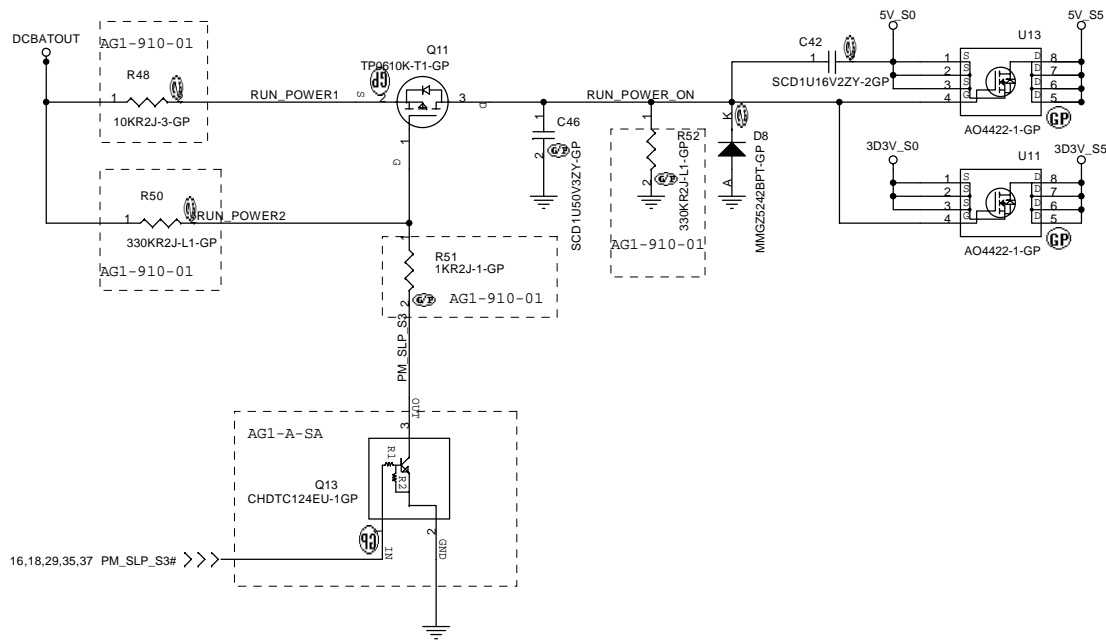
**緯創資通 Wistron Corporation**  
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Title: **BIOS ROM**

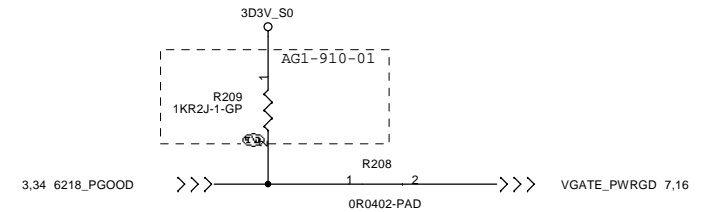
Size A3	Document Number <b>AG1-910</b>	Rev <b>01</b>
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Date: Tuesday, November 01, 2005 Sheet 31 of 40

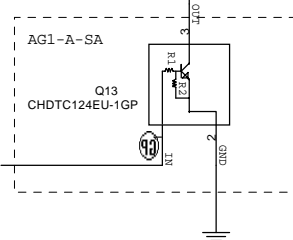
# Run Power



# PWRGD for NB and SB

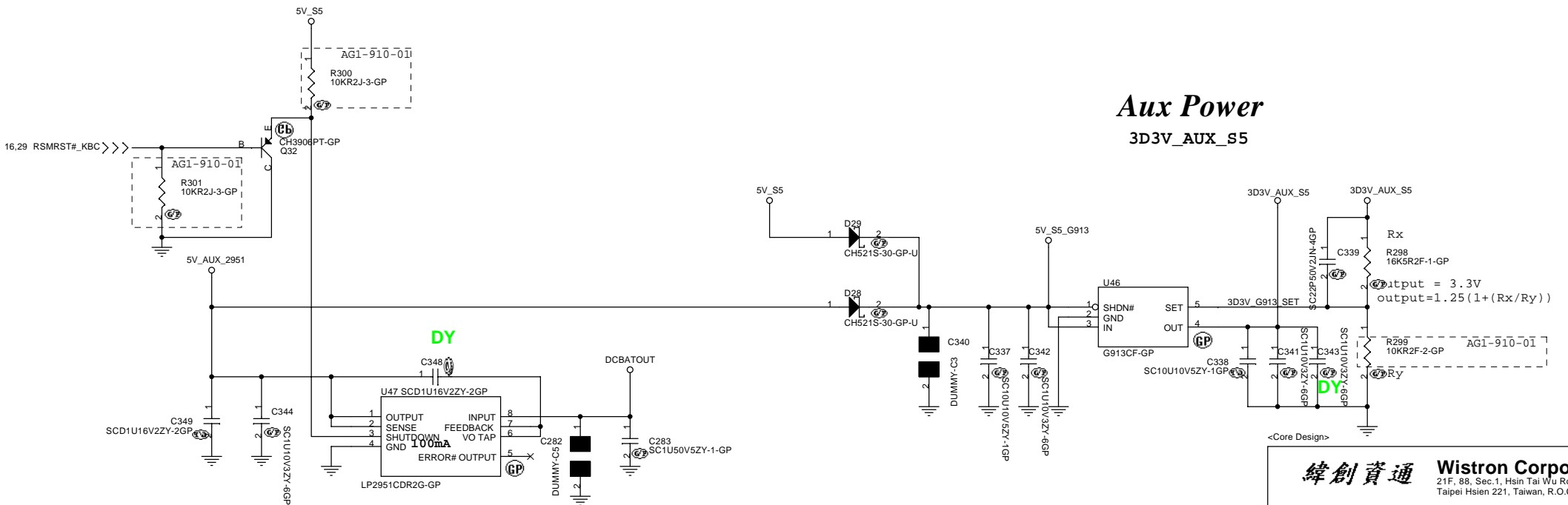


# PWRGD to Turn on CPU\_Core\_Power

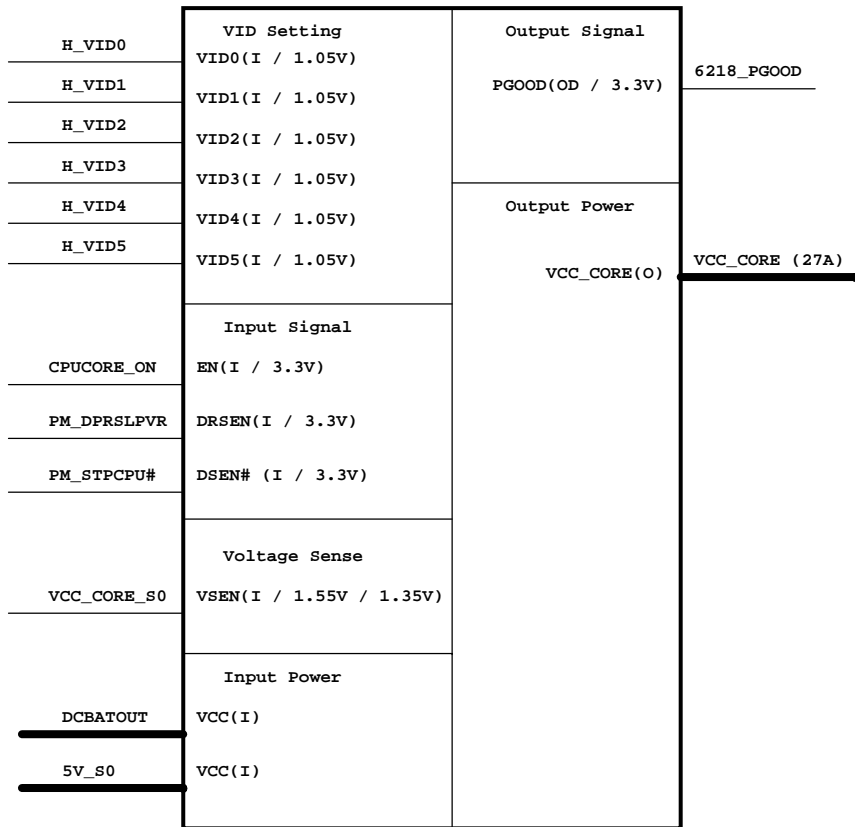


# Aux Power

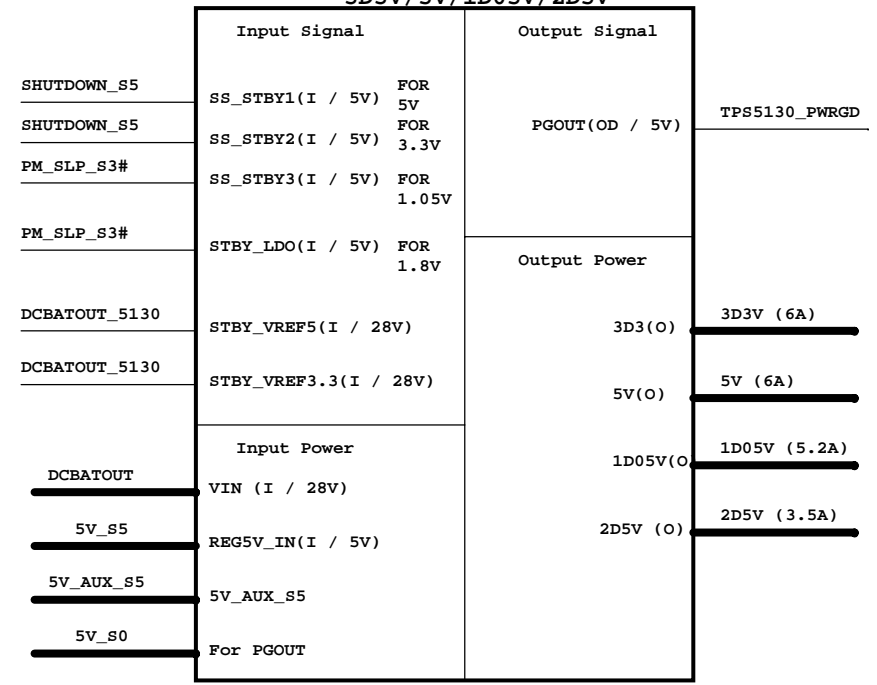
## 3D3V\_AUX\_S5



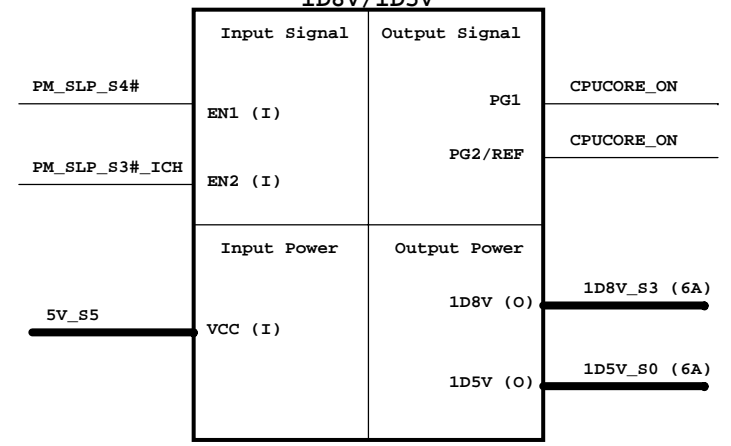
**CPU\_CORE ISL6218CV**



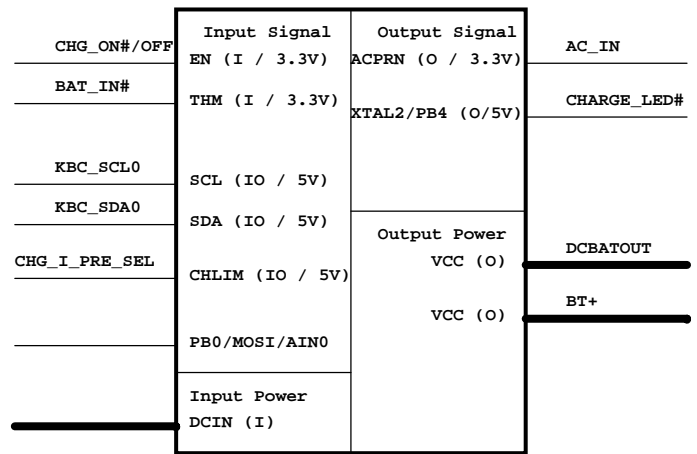
**TPS5130  
3D3V/5V/1D05V/2D5V**



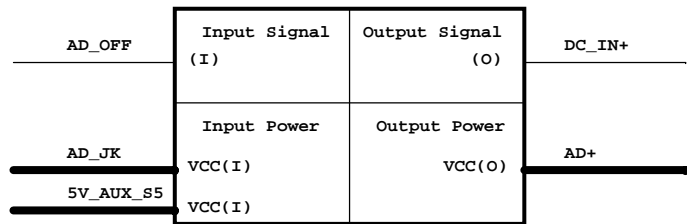
**ISL6227  
1D8V/1D5V**



**Charger\_ISL6255**



**Adapter**



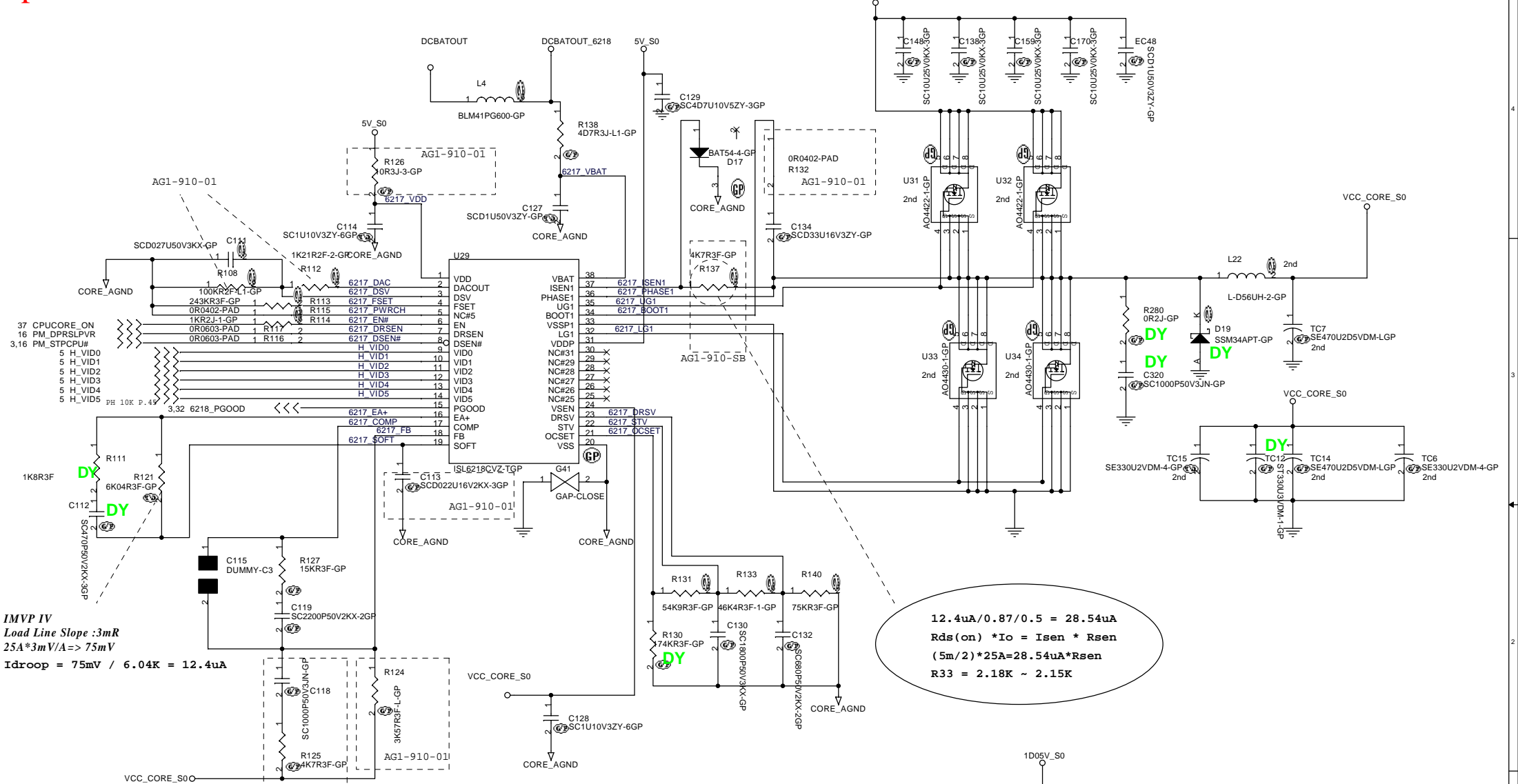
<Core Design>

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Title: **Power Diagram**

Size: A3 Document Number: **AG1(Alviso)** Rev: **01**

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IMVP IV  
Load Line Slope :3mR  
25A\*3mV/A=> 75mV  
Idroop = 75mV / 6.04K = 12.4uA

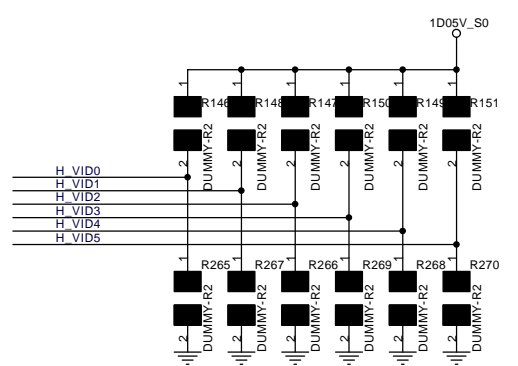
$$12.4\mu\text{A} / 0.87 / 0.5 = 28.54\mu\text{A}$$

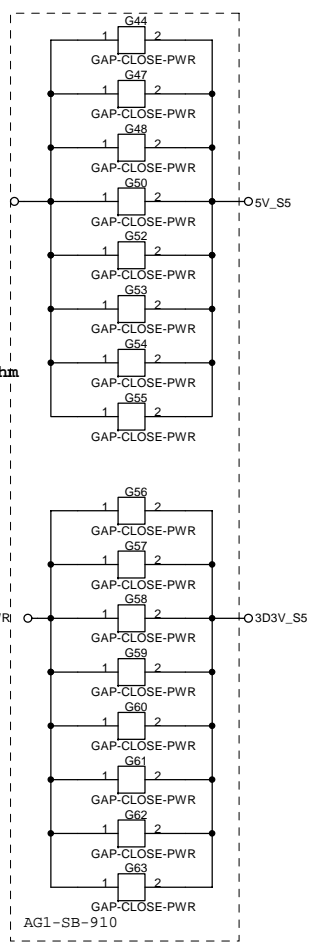
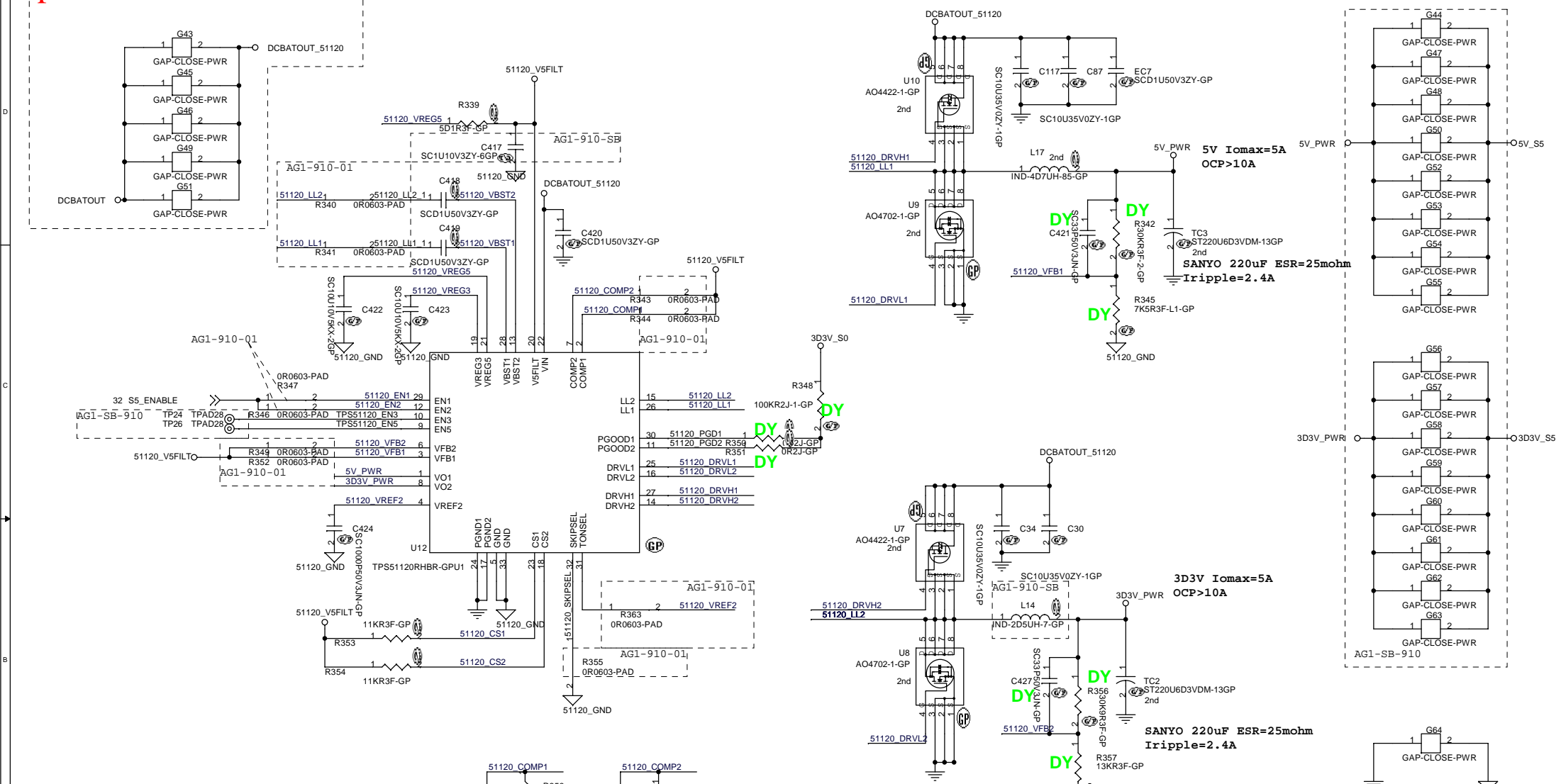
$$R_{ds(on)} * I_o = I_{sen} * R_{sen}$$

$$(5\text{m} / 2) * 25\text{A} = 28.54\mu\text{A} * R_{sen}$$

$$R_{33} = 2.18\text{K} \sim 2.15\text{K}$$

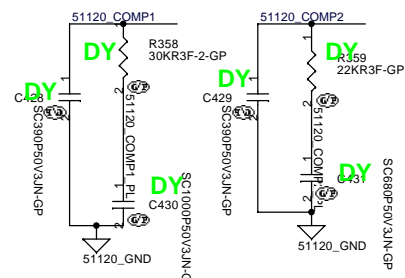
- U12,U14:A04422 84.04422.037  
U13,U15:A04430 84.04430.B37  
R100:3K83R2F
- U12,U14:IRF7413 84.07413.037  
U13,U15:IRF7832-U 84.07832.037  
R100:2K43R2F





$$V_{out} = 1V * (R1 + R2) / R2$$

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	witcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on



**For TPS51120, Vout=5V**

- If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
- If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

**Vout=3.3V**

- If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
- If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

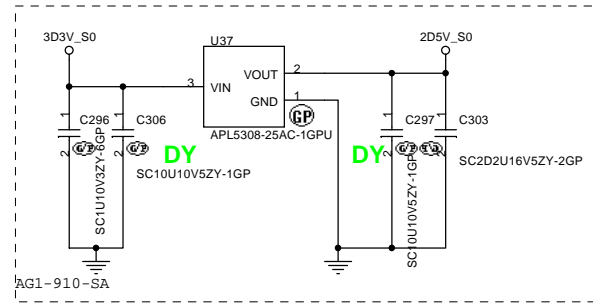
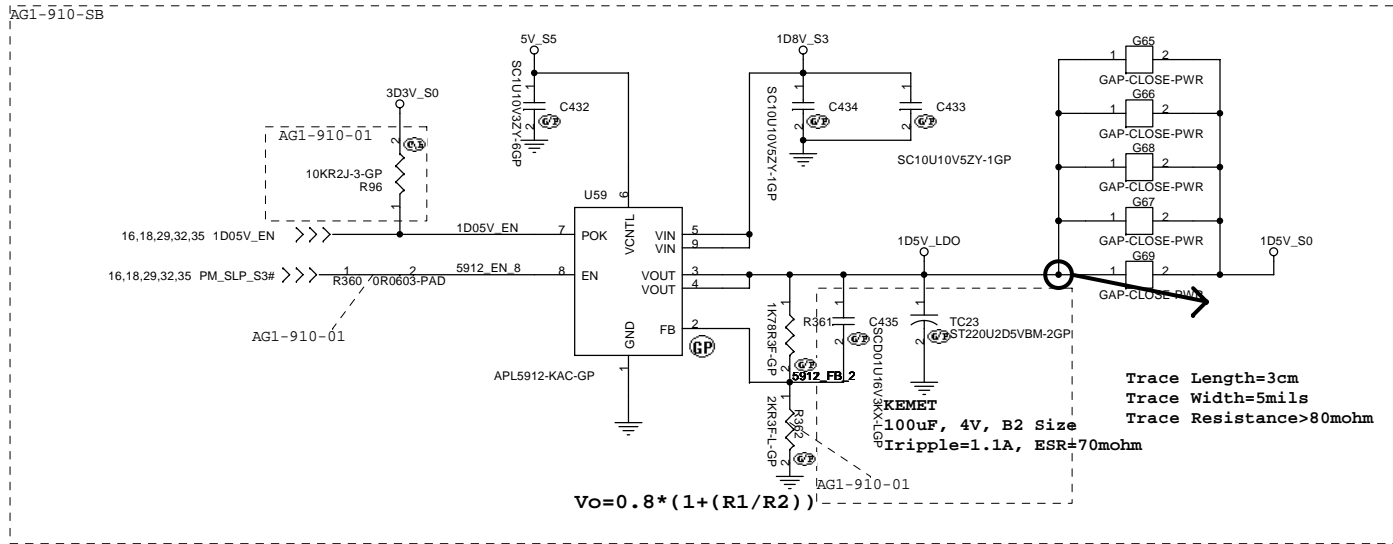
<Core Design>

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File: **TPS51120 3D3V 5V**  
AG1(Alviso)

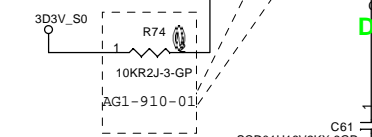
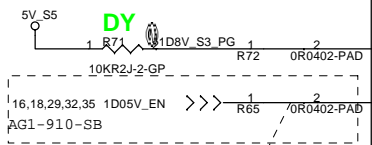
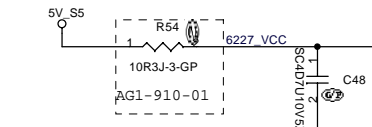
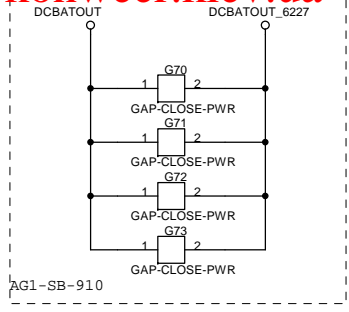
Size A3 Document Number **AG1(Alviso)** Rev **01**

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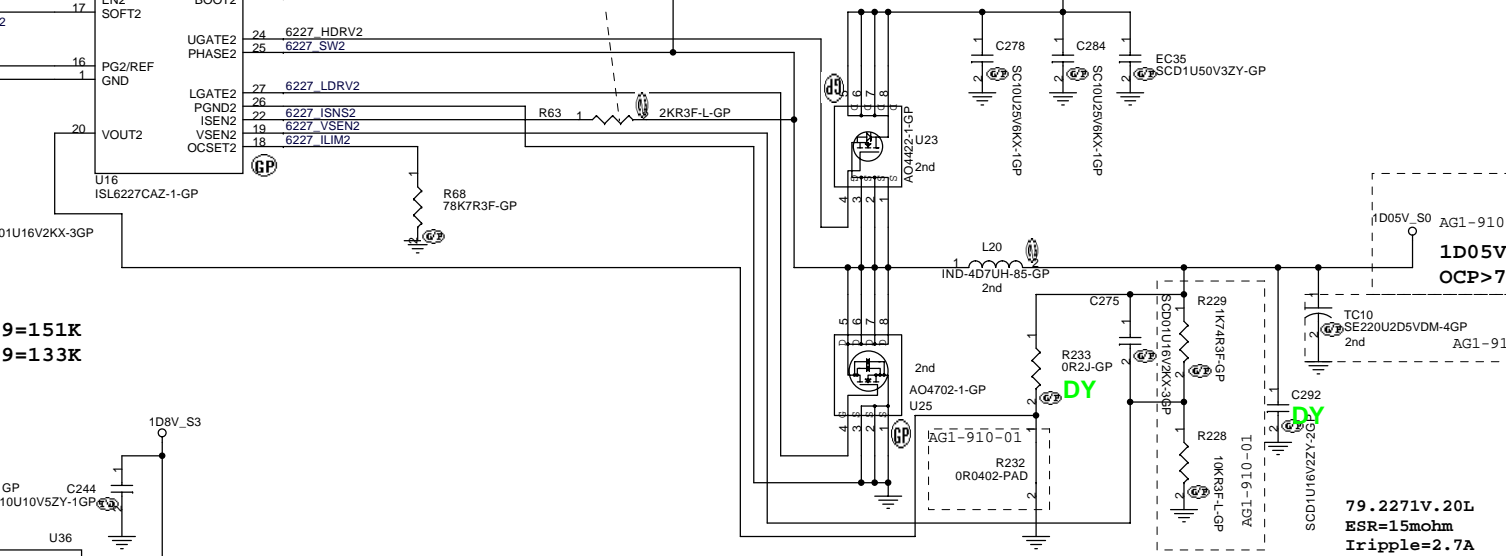
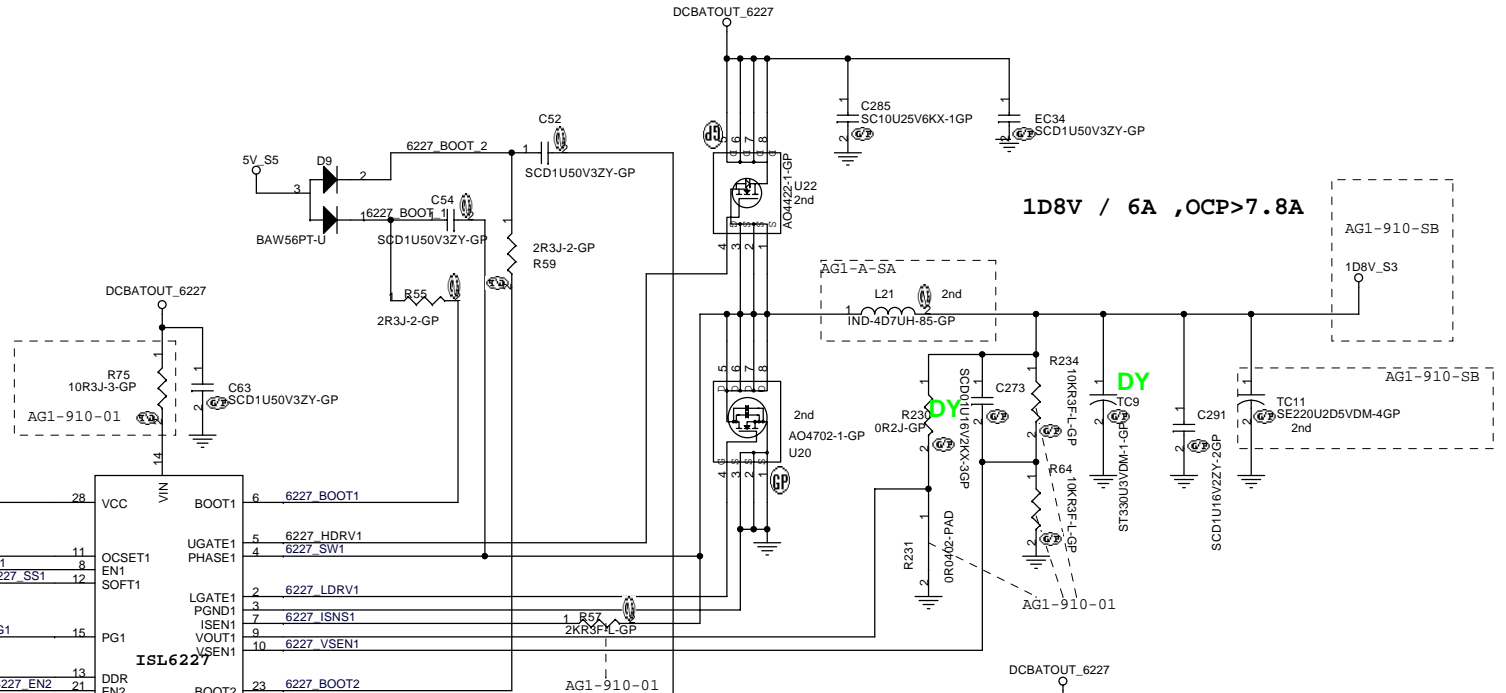
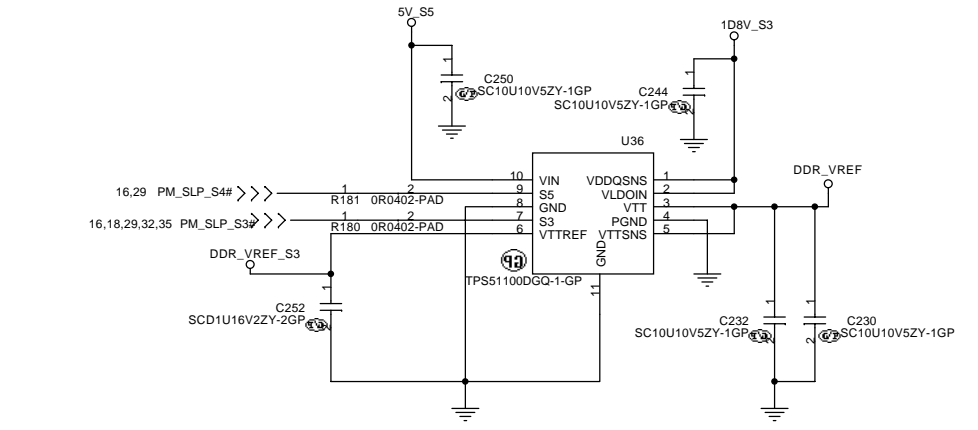
<Core Design>

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Title		
<b>1D5V/2D5V(LDO)</b>		
Size	Document Number	Rev
A3	<b>AG1(Alviso)</b>	<b>01</b>
Date: Monday, October 31, 2005		
Sheet 36 of 40		

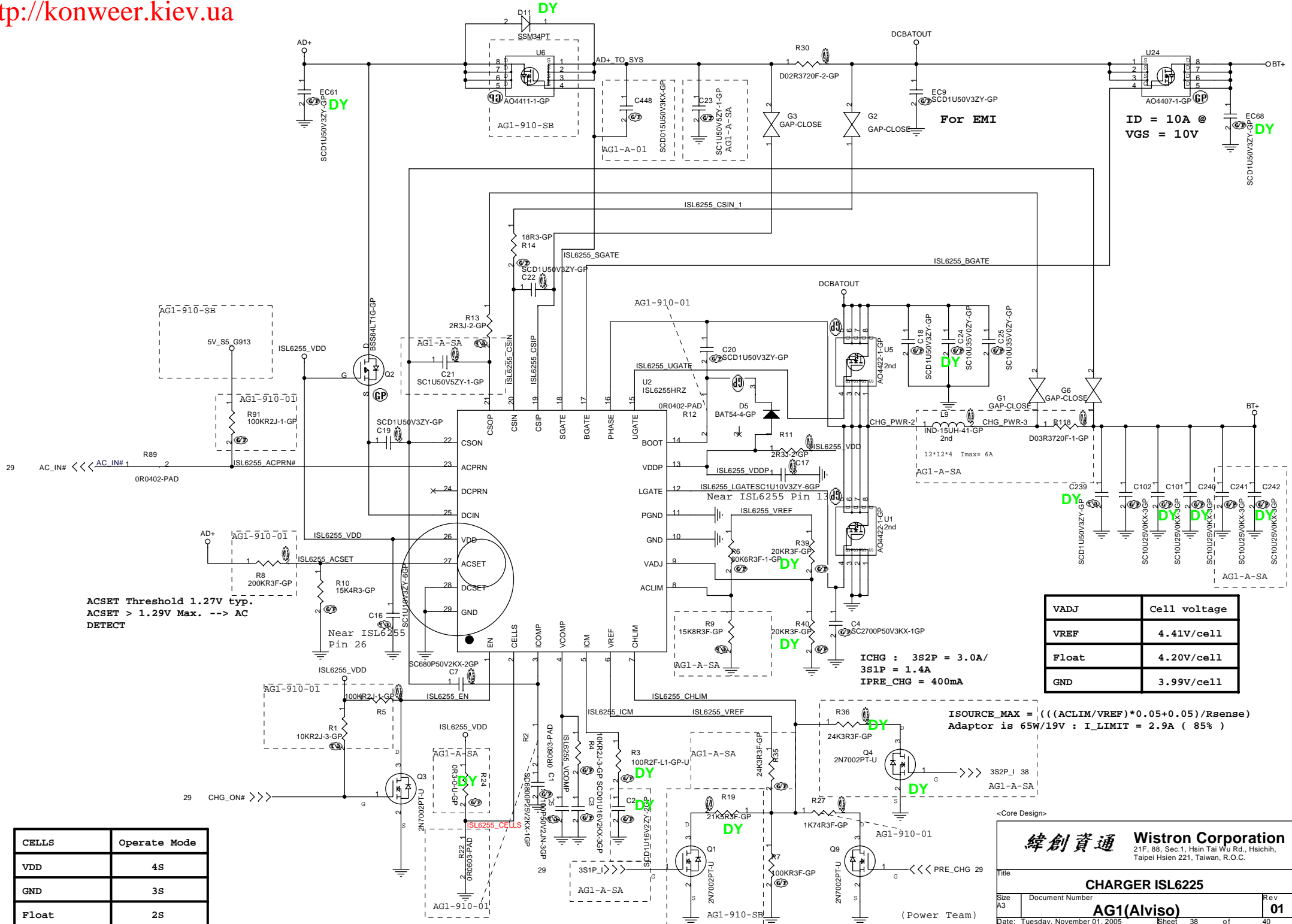


0D9V

**OCP**  
 7.8A=>R169=151K  
 9.0A=>R169=133K



79.2271V.20L  
 ESR=15mohm  
 Tripple=2.7A



ACSET Threshold 1.27V typ.  
 ACSET > 1.29V Max. --> AC  
 DETECT

ICHG : 3S2P = 3.0A/  
 3S1P = 1.4A  
 IPRE\_CHG = 400mA

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

ISOURCE\_MAX = (((ACLIM/VREF)\*0.05+0.05)/Rsense)  
 Adaptor is 65W/19V : I\_LIMIT = 2.9A ( 85% )

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

<Core Design>

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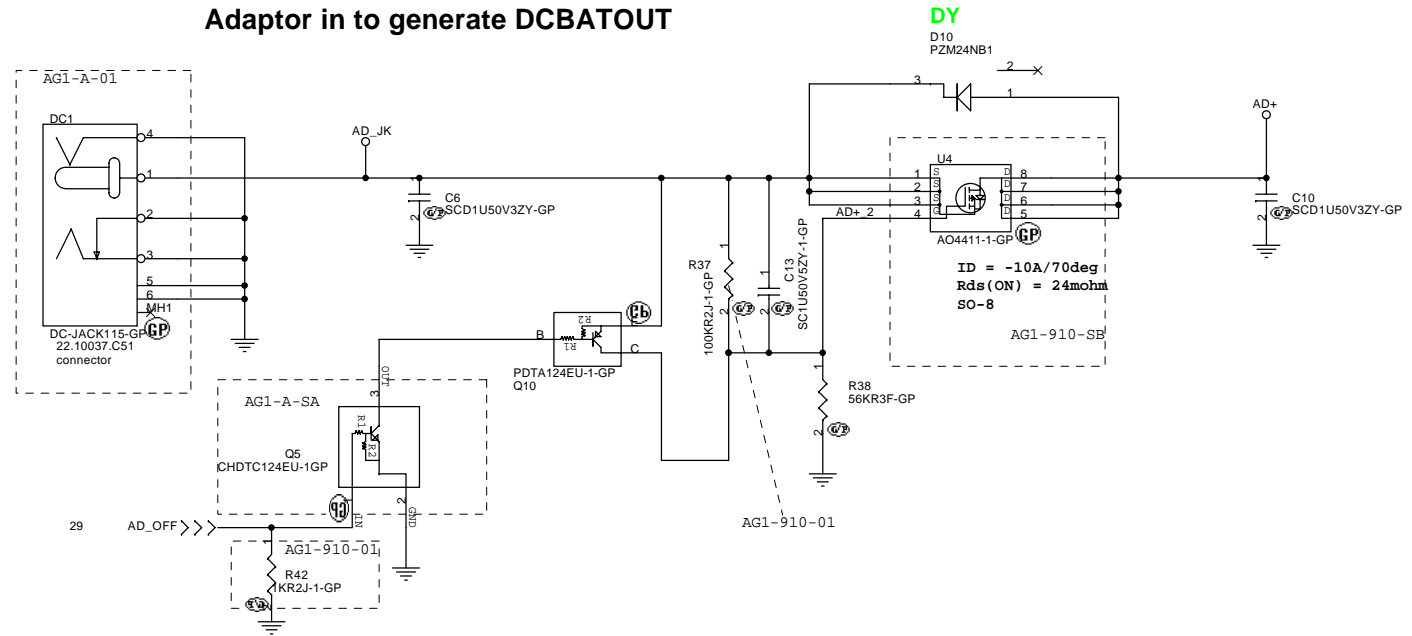
Title: **CHARGER ISL6225**

Size A3 Document Number: **AG1(Alviso)** Rev **01**

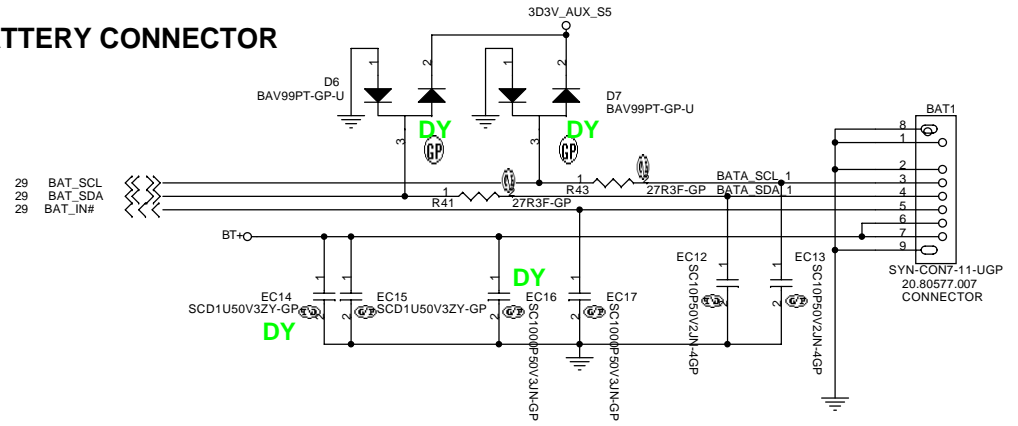
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(Power Team)

### Adaptor in to generate DCBATOUT



### BATTERY CONNECTOR



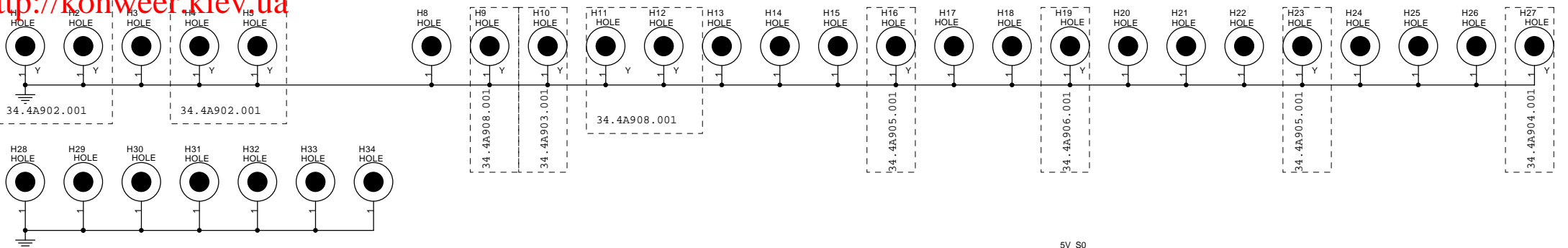
<Core Design>

緯創資通

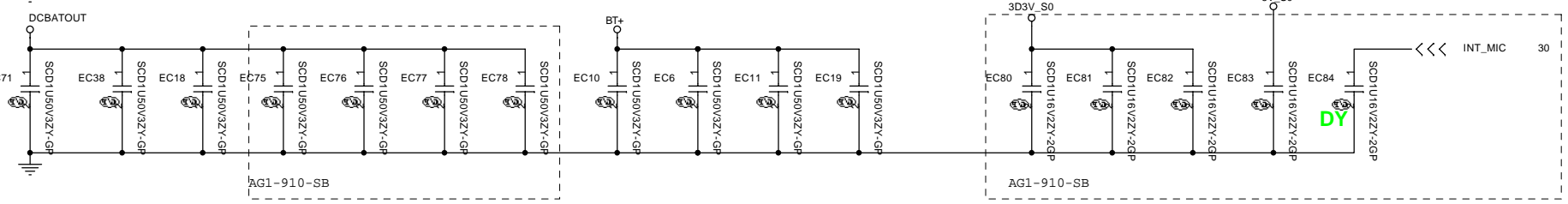
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Title <b>AD/BATT CONN</b>		
Size A3	Document Number <b>AG1(Alviso)</b>	Rev <b>01</b>
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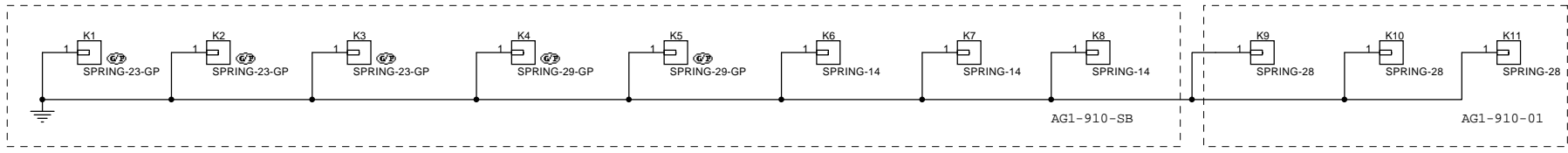
D



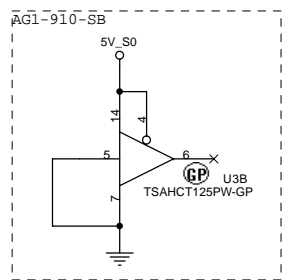
C



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Title: **EMI**

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