

# Compal Confidential

## HBL50 Schematics Document

**Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M  
(With nVIDIA G73M/72MV)**

**2005-11-08**

**REV: 0.3**

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				B	HBL50 LA-2921P	0.3
				Date:	Friday, November 11, 2005	Sheet 1 of 59

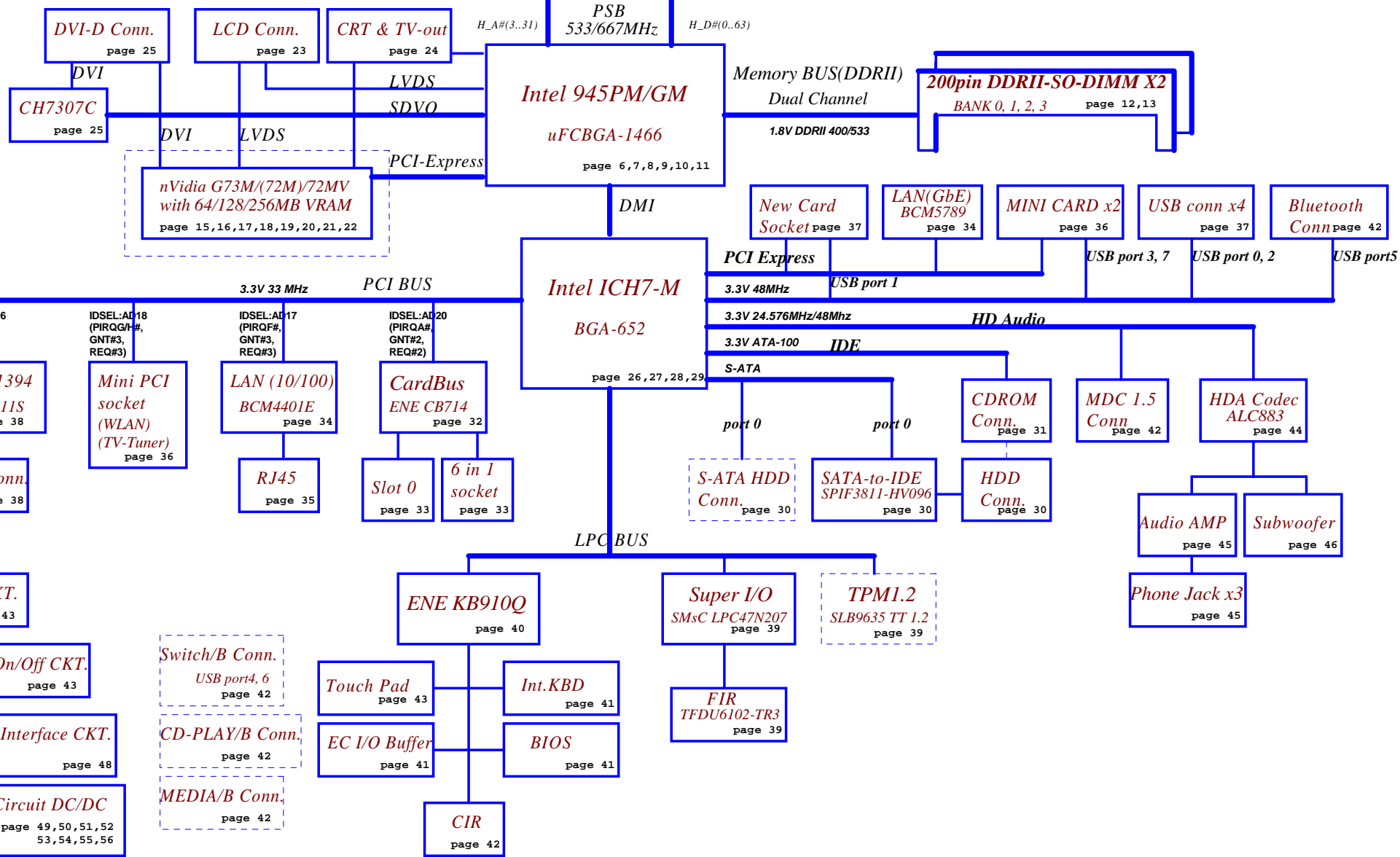
**Model Name : HBL50**  
**File Name : LA-2921**

*Fan Control*  
 page 47

*Yonah*  
*uPGA-478 Package*  
 page 4,5

*Thermal Sensor*  
*F75383M*  
 page 4

*Clock Generator*  
*ICS9LPRS325*  
 page 14



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Size B	Document Number	HBL50 LA-2921P		Rev 0.3
Date:	Friday, November 11, 2005	Sheet	2 of 59	

### Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

### External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

### EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

### EC SM Bus2 address

### ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

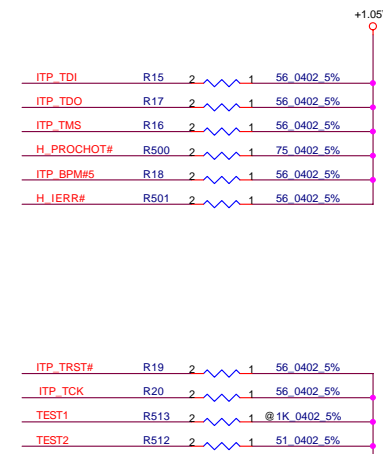
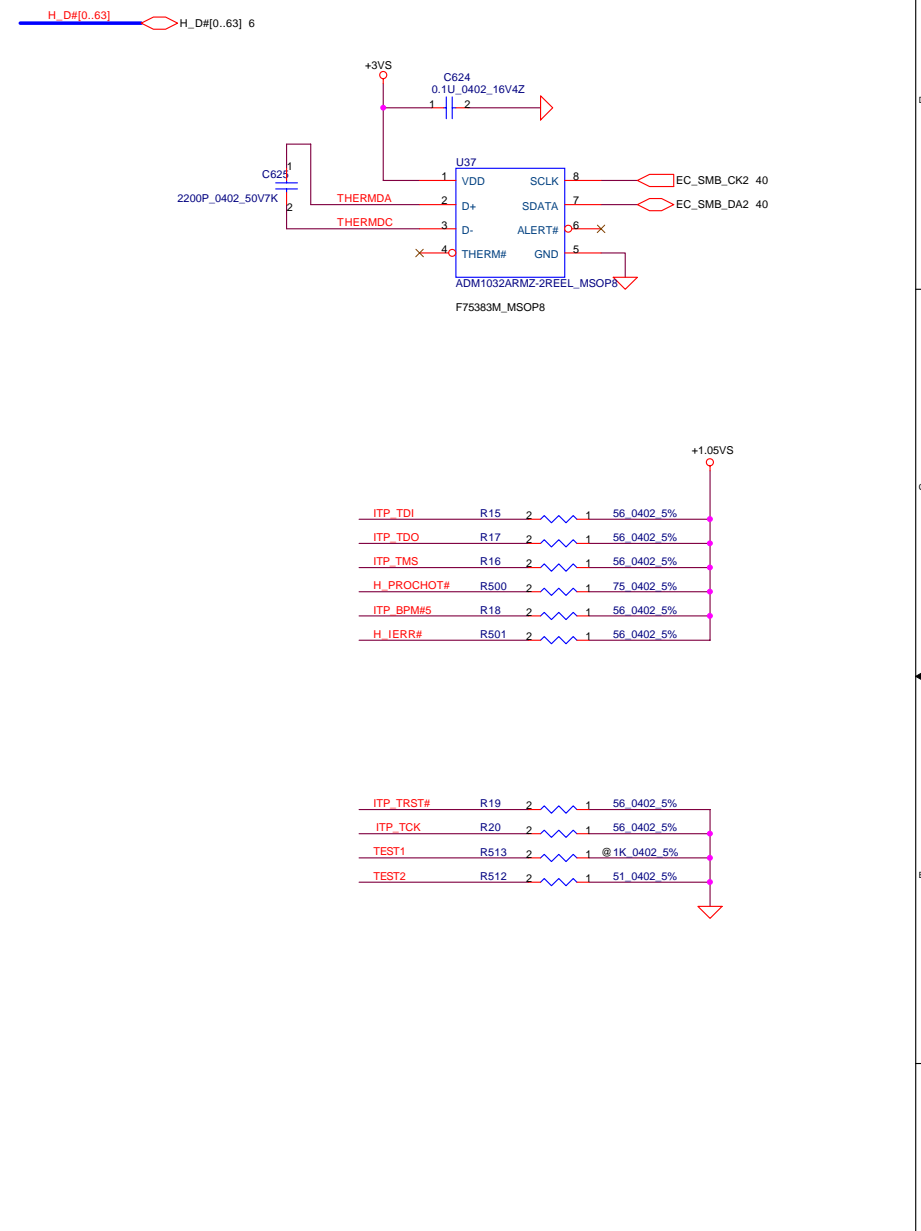
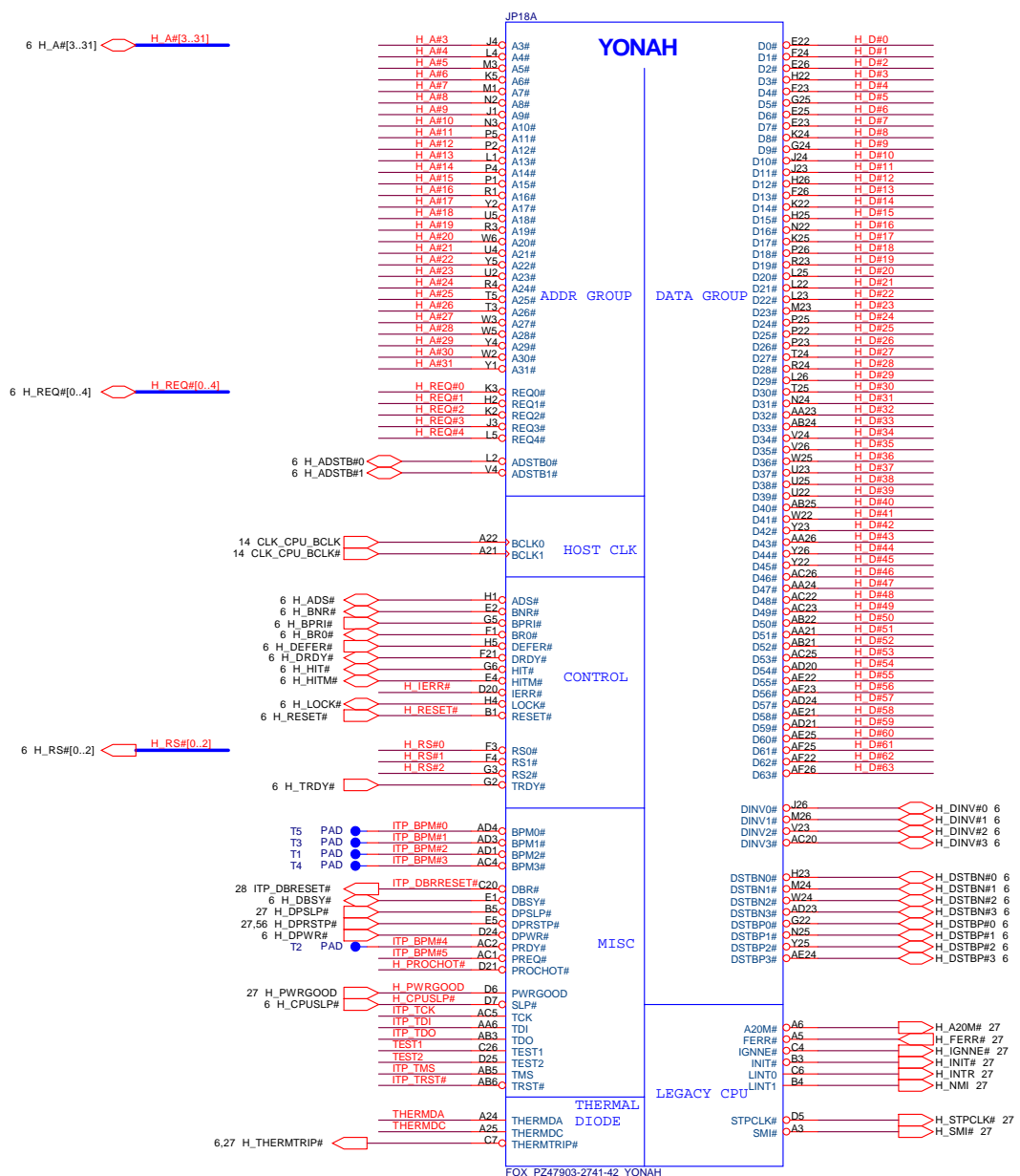
### BTO Option Table

BTO Item	BOM Structure
VGA	PM@ + VGA@
UMA	GM@
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI_CARD1	MINI1@
MINI_CARD2	MINI2@
SATA-to-IDE	3811@
PATA	PATA@
GRAPEVINE	GRA@
G72MV Only	G72@
G73 Only	G73@
VRAM	X76@
VRAM 64M	64@
VRAM 128M	64@+128@
VRAM 256M	64@+128@+256@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
LCM	LCM@
Sub-woofer	SUB@

### SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

5789&5787	8789@
4401&5789	0189@
VP1020	VP1020@
INTERNAL MIC	INTMIC@
1394	1394@
SATA HDD	SATA@

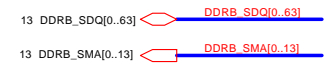
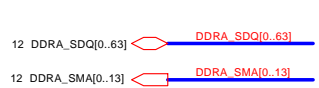


**Layout Note:**  
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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				Date:	Friday, November 11, 2005
				Sheet	4 of 59
				Rev	0.3







U40D

U40E

DDR SYS MEMORY A

DDR SYS MEMORY B

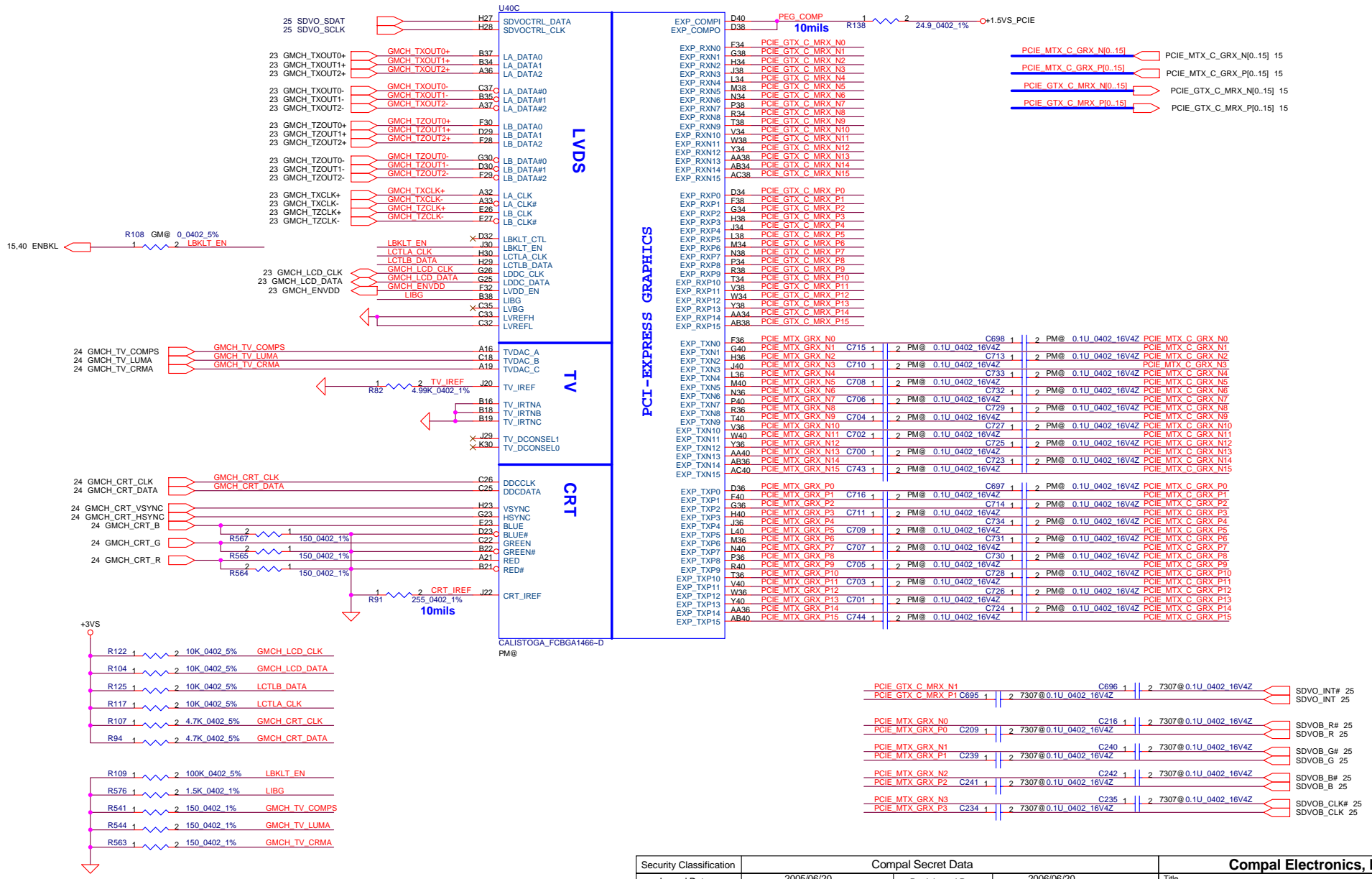
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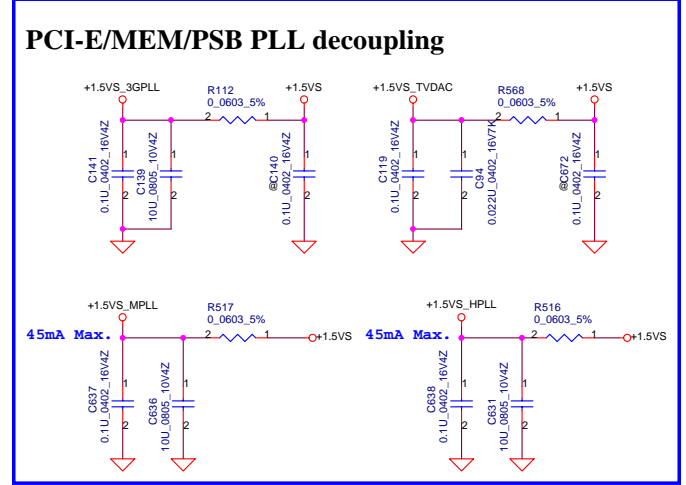
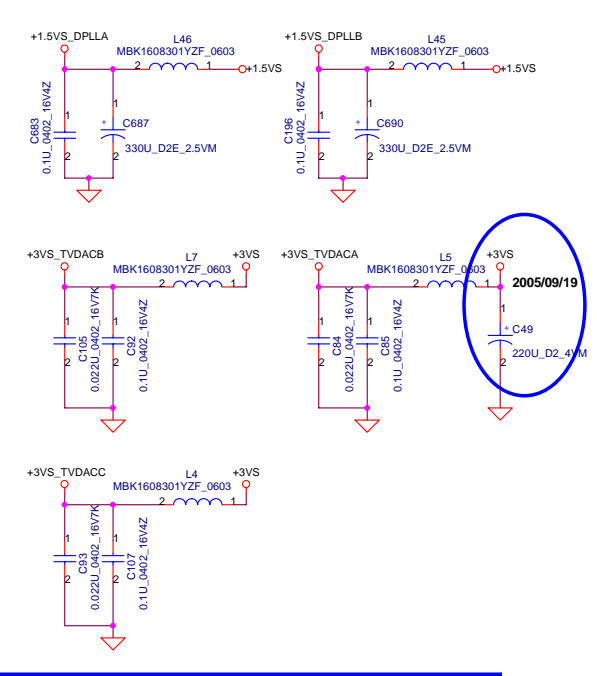
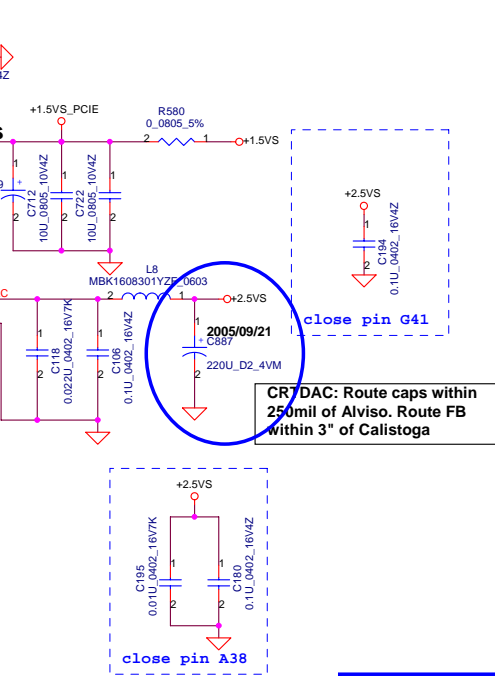
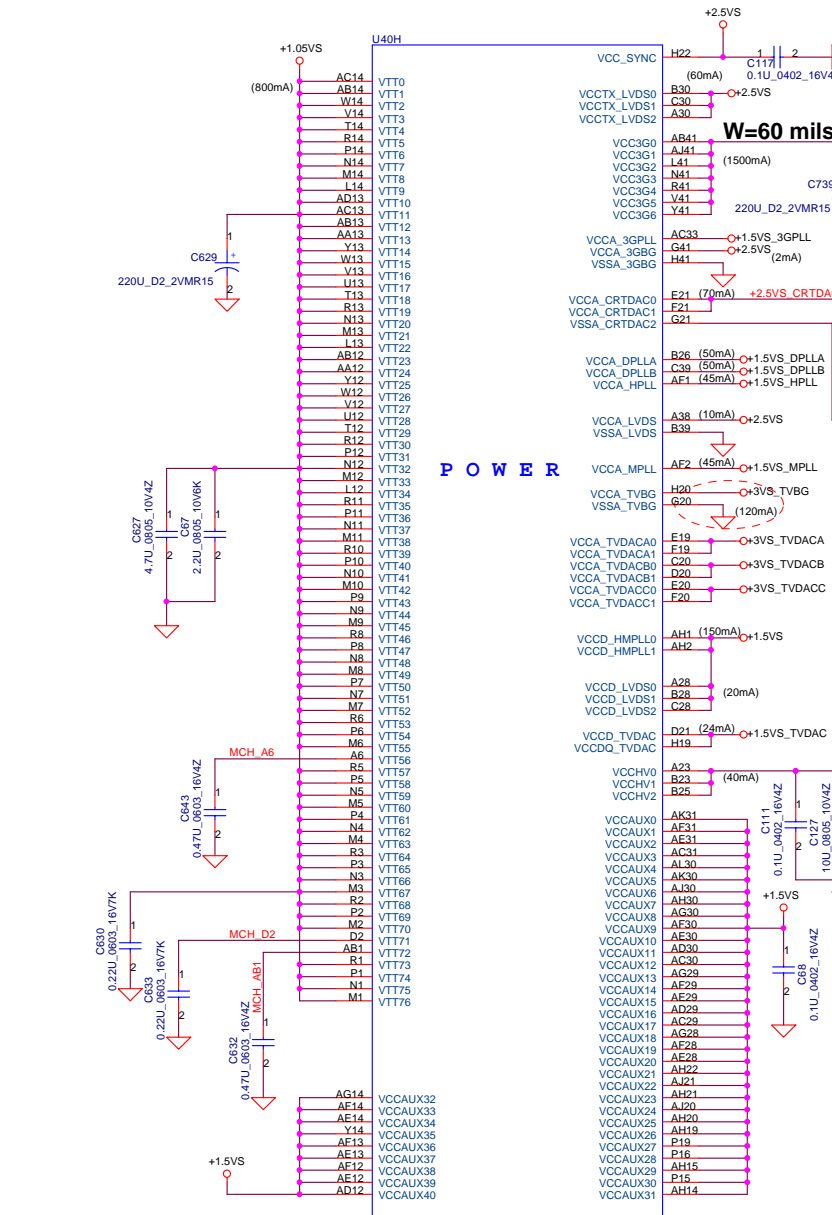
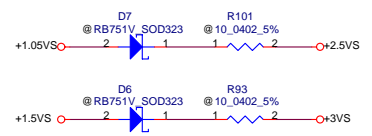
CALISTOGA\_FCBGA1466-D  
PM@

CALISTOGA\_FCBGA1466-D  
PM@

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Document Number			Rev	0.3
HBL50 LA-2921P				
Date:	Friday, November 11, 2005	Sheet	7	of 59



Security Classification		Compal Secret Data		Title	
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				B	HBL50 LA-2921P
				Date:	Friday, November 11, 2005
				Sheet	8 of 59
				Rev	0.3
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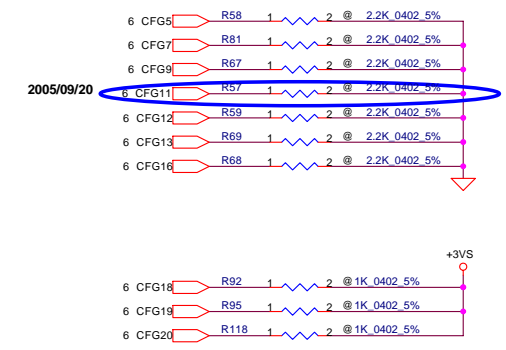
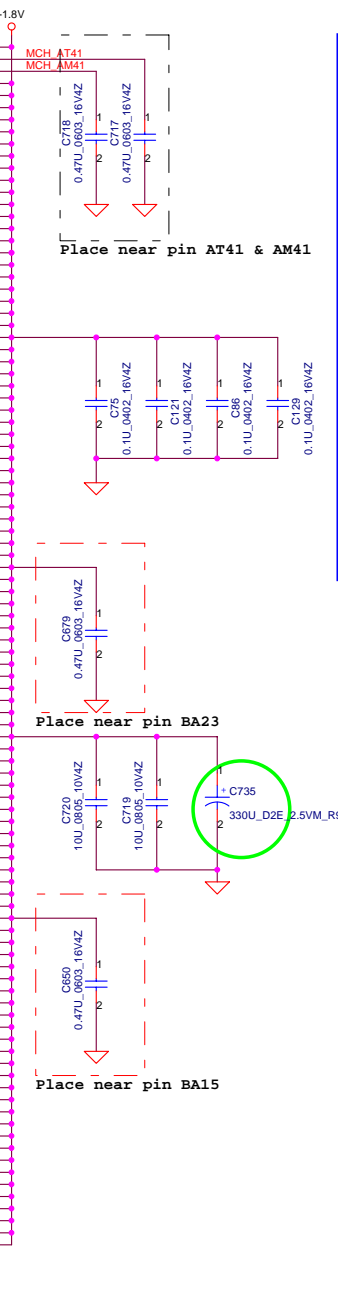
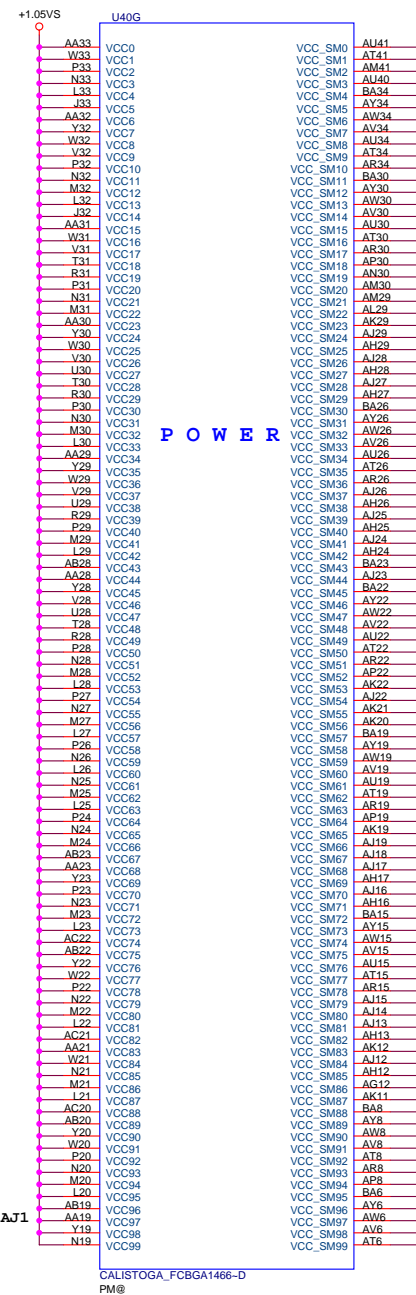
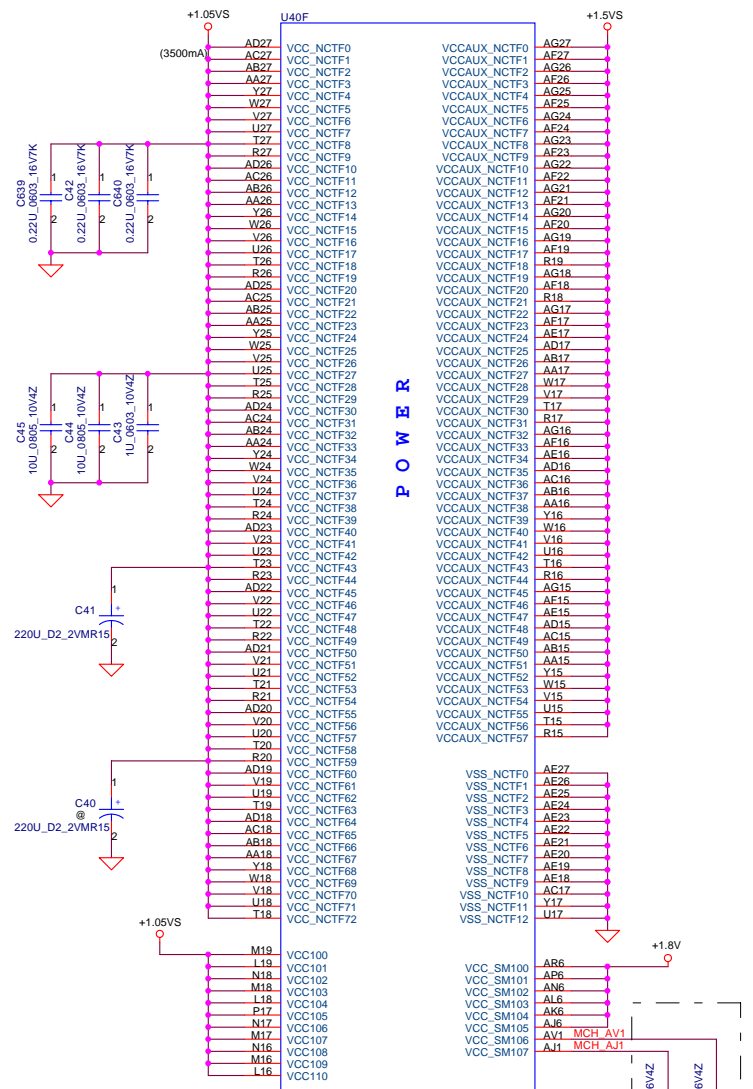
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Size B	Document Number	Rev		
	HBL50 LA-2921P	0.3		
Date:	Friday, November 11, 2005	Sheet	9 of 59	

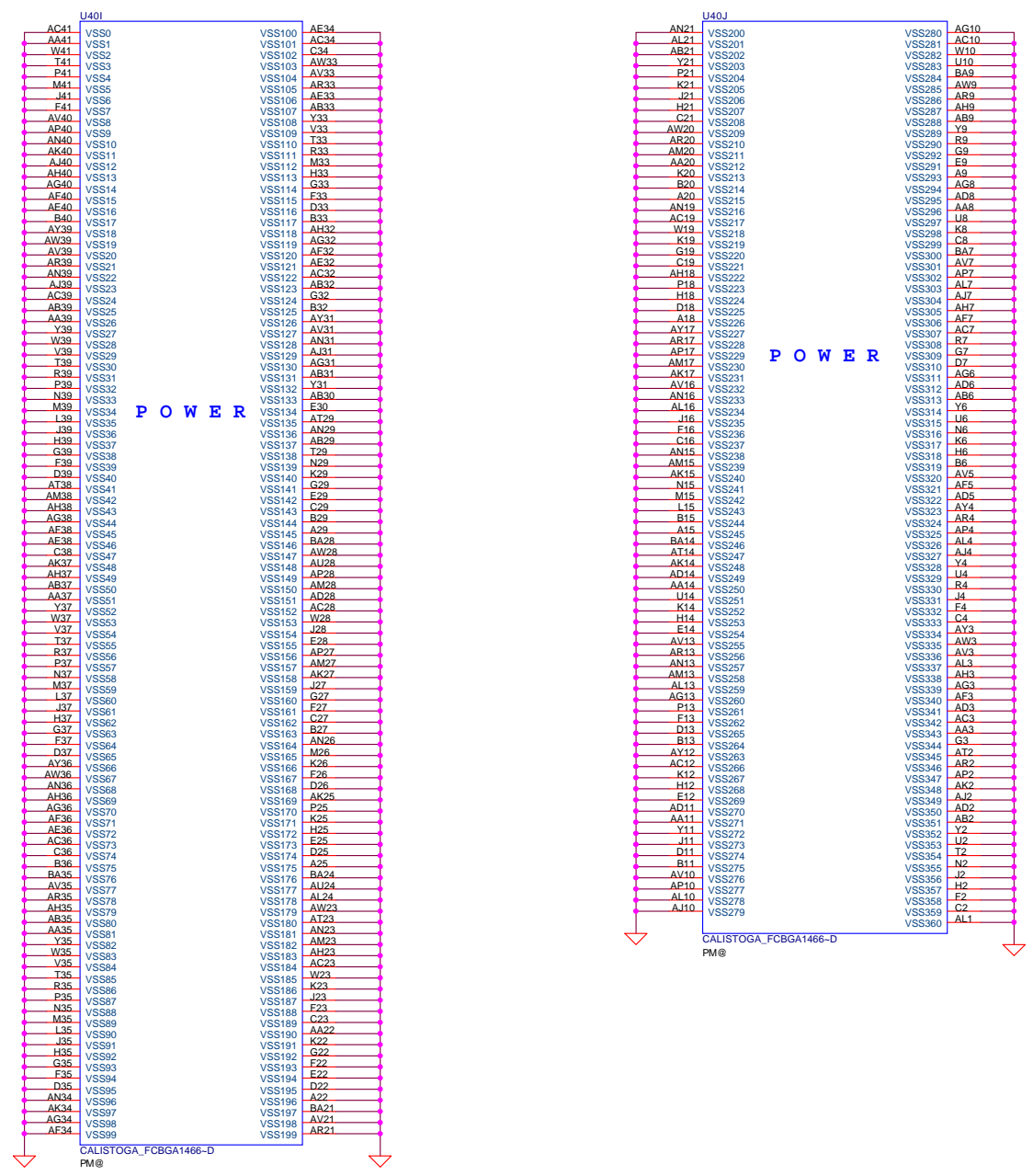
Strap Pin Table

CFG[3:17] have internal pull up  
CFG[19:18] have internal pull down

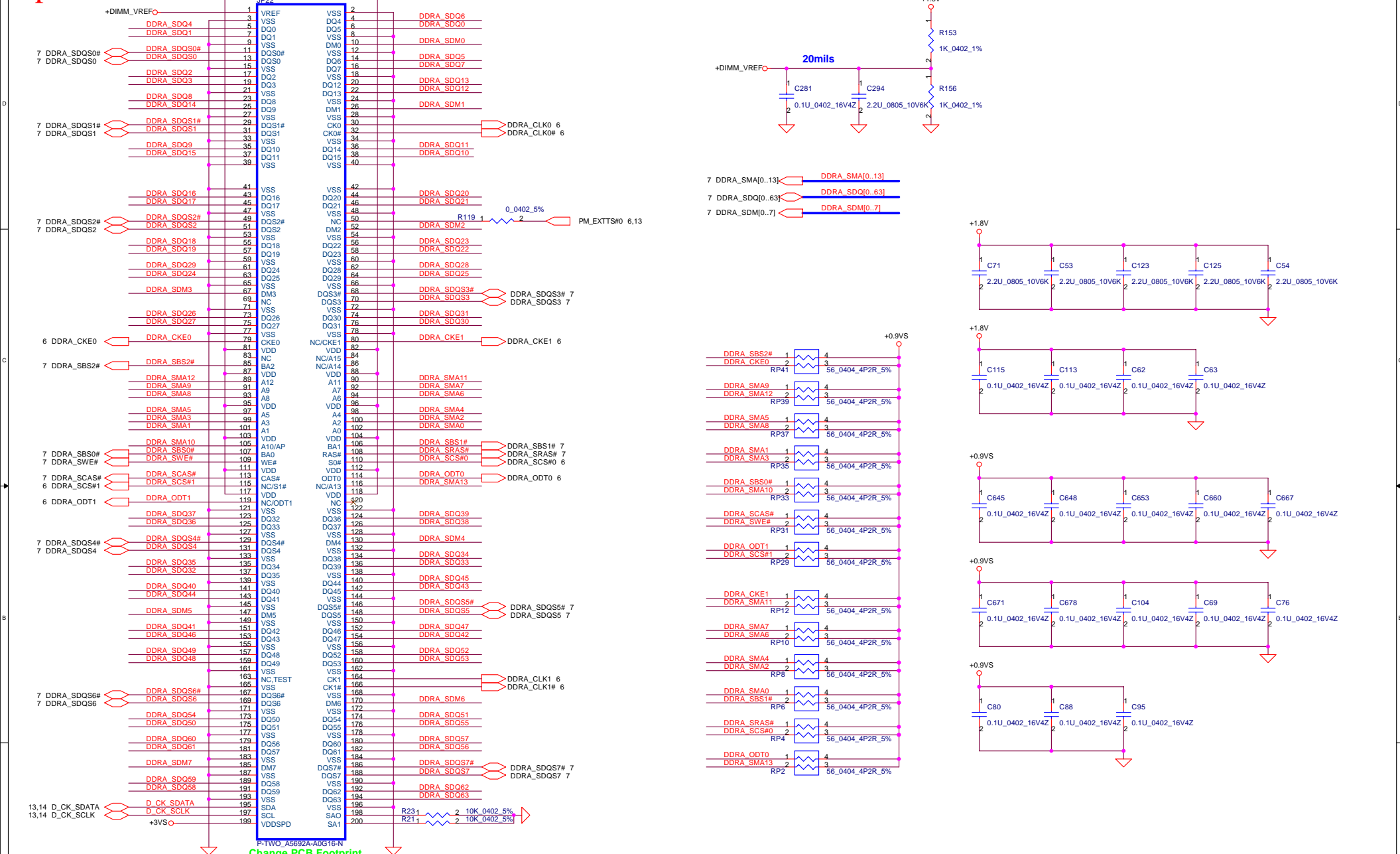
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation*(Default)
CFG11	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



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Size	Document Number	Rev		
B	HBL50 LA-2921P	0.3		
Date:	Friday, November 11, 2005	Sheet	10	of 59

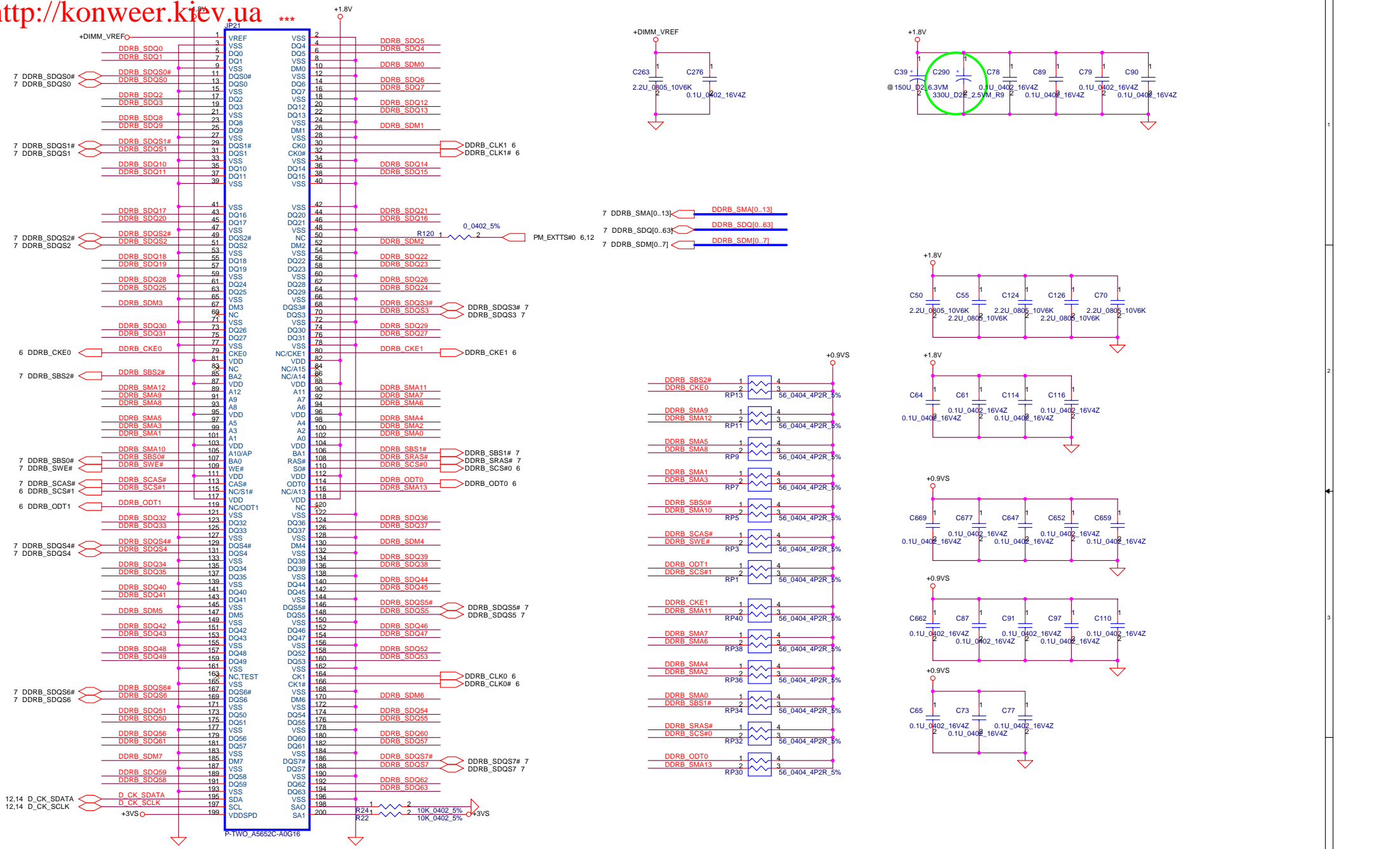


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				Rev 0.3 Sheet 11 of 59



**DIMM0 STD H:9.2mm (BOT)**

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Date:	Friday, November 11, 2005	Sheet	12 of 59	



DIMM1 STD H:5.2mm (BOT)

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				0.3
Date: Friday, November 11, 2005				Sheet 13 of 59

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz 1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

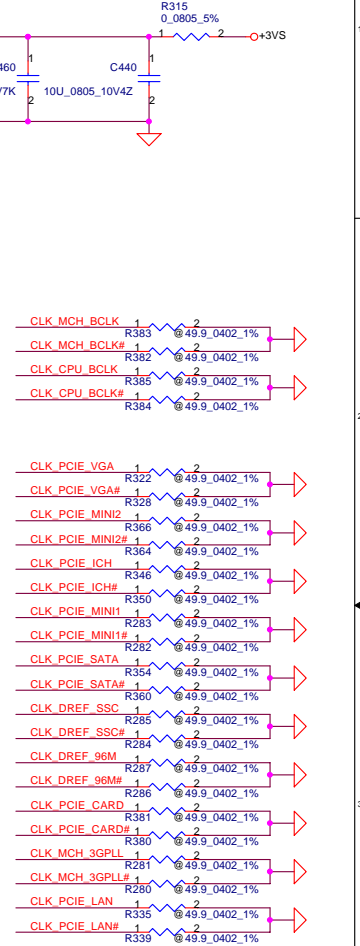
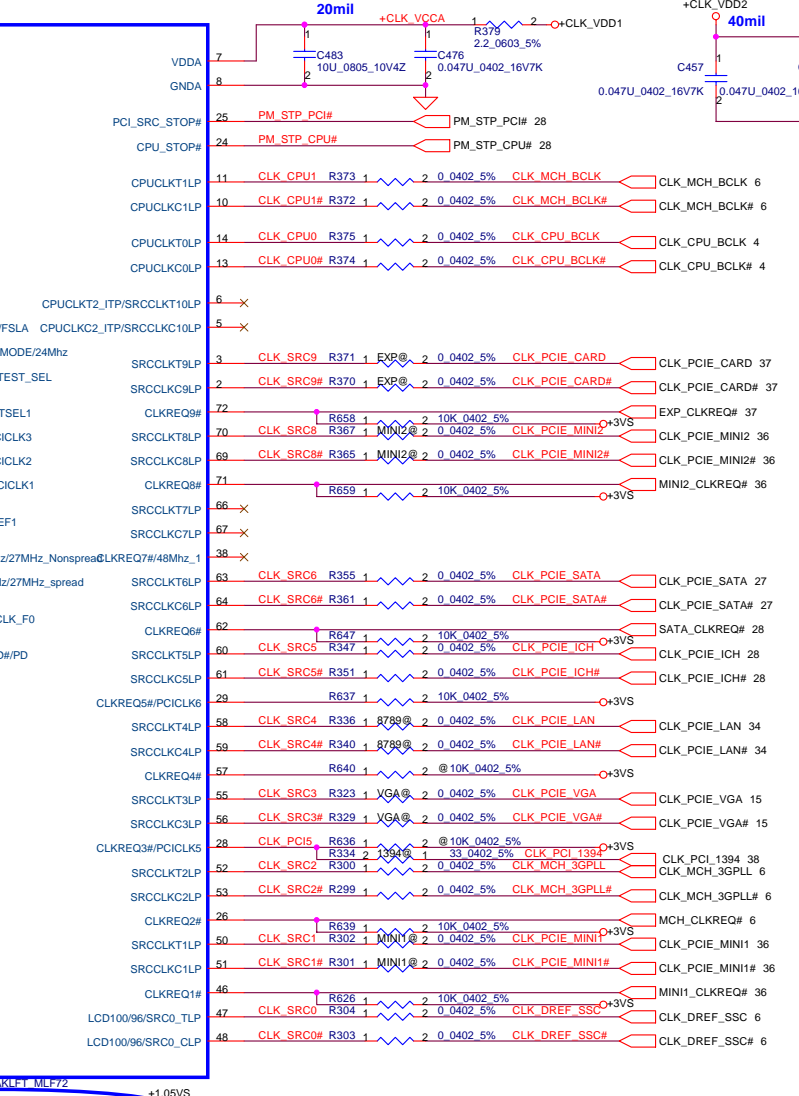
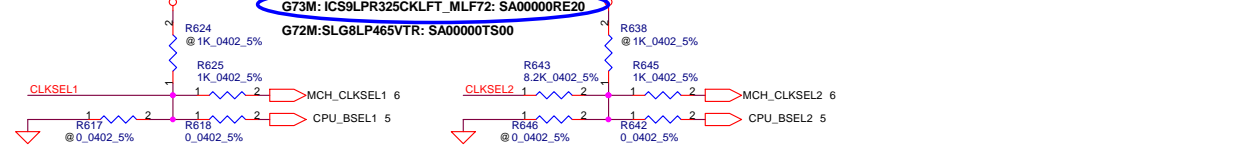
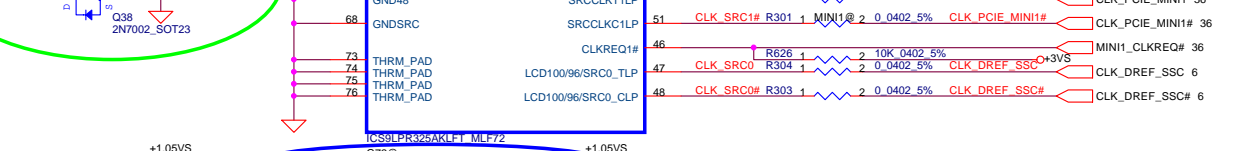
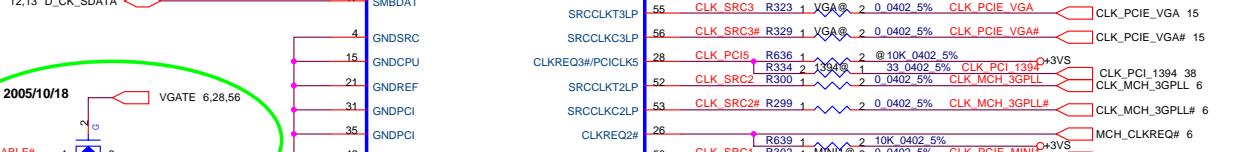
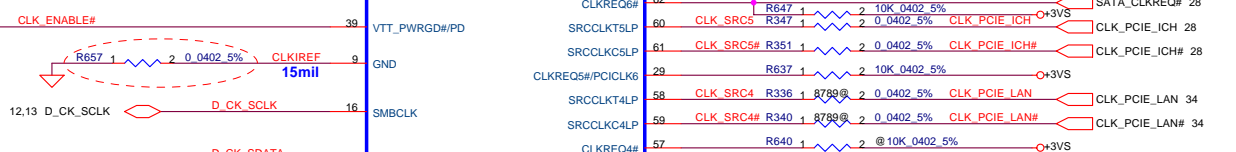
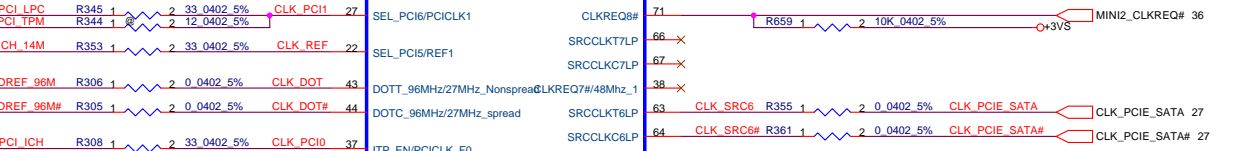
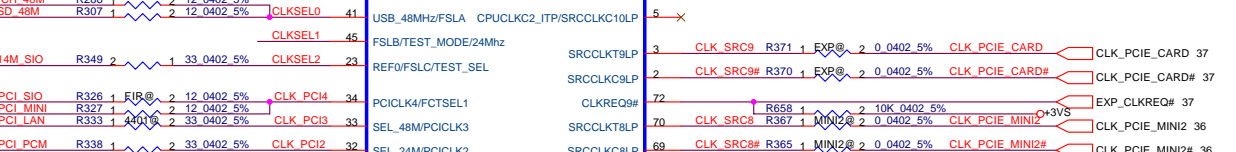
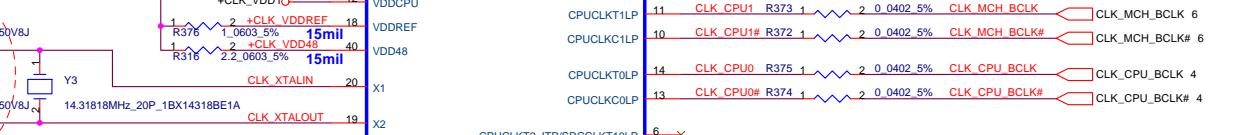
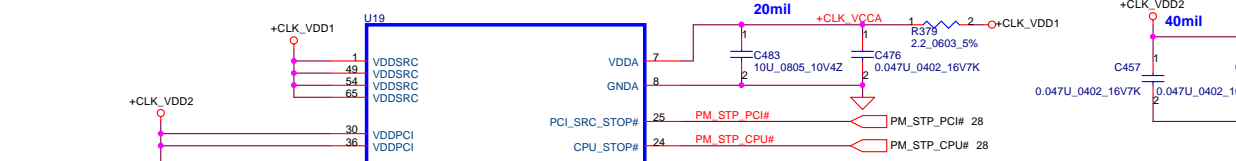
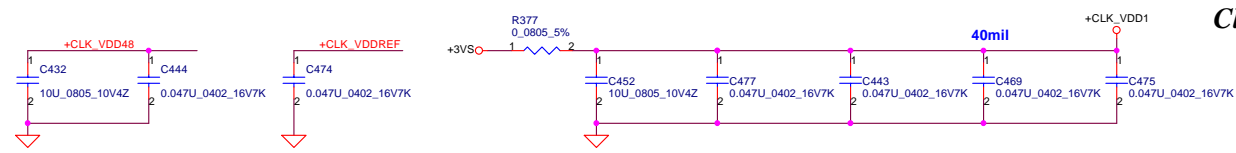
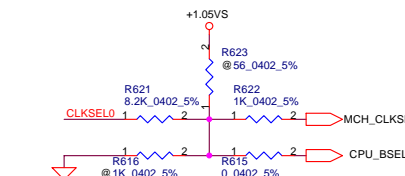
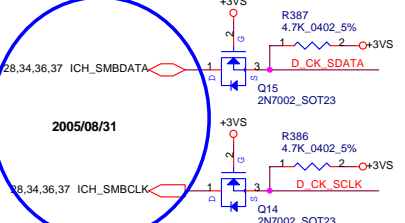
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\*\*SEL\_PCI6/PCICLK1=0=CLKREQ5#

\*\*SEL\_PCI5=1=PCICLK5  
ITP\_EN/PCICLK\_F0=0=SRC pair

CLK\_REF  
R712 10K\_0402\_5%

CLK\_PCI#  
R711 10K\_0402\_5%  
2005/08/31

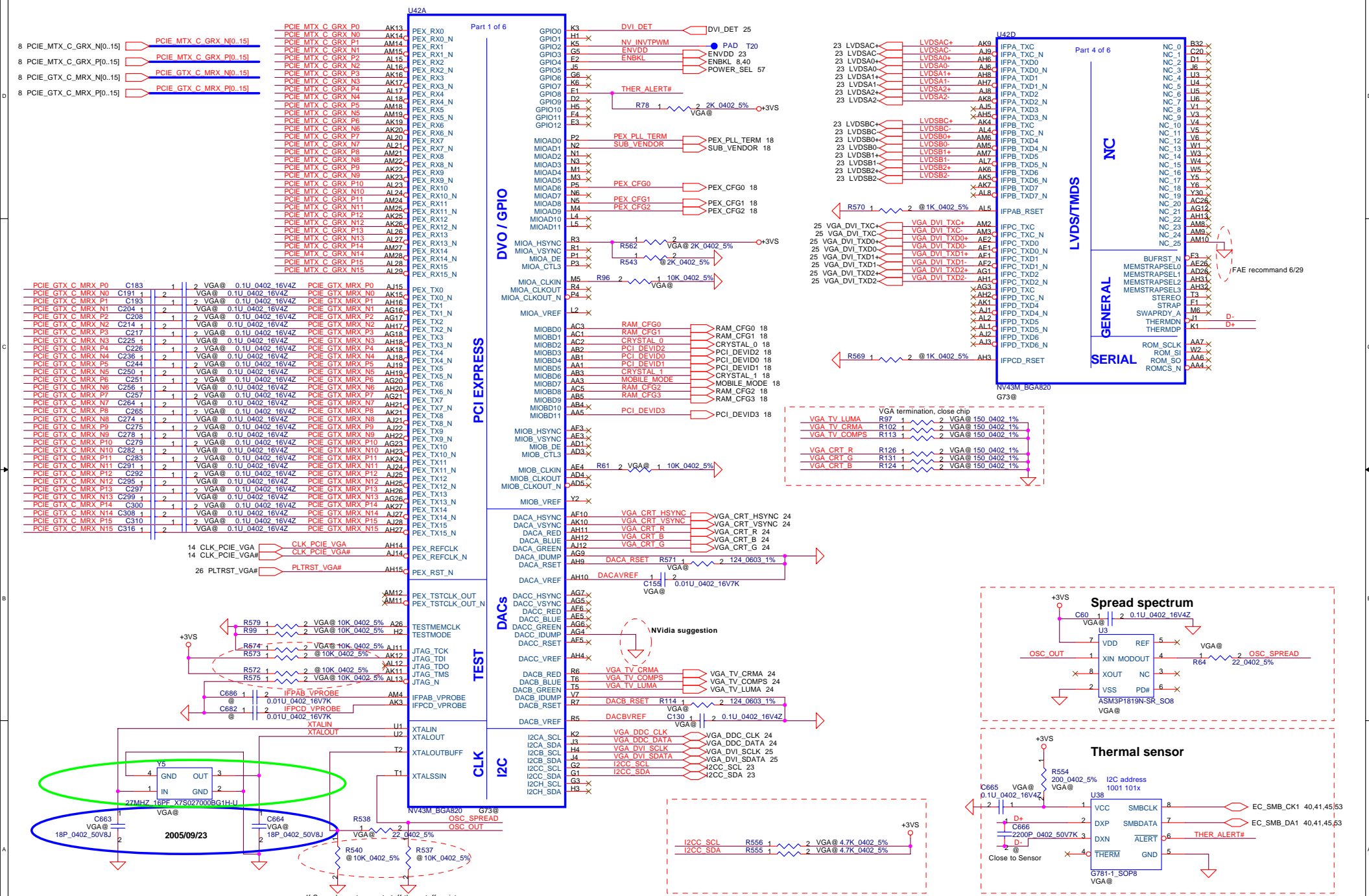
CLK\_ENABLE#  
R620 10K\_0402\_5%  
2005/10/18



Security Classification	Compal Secret Data	
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		2006/06/20

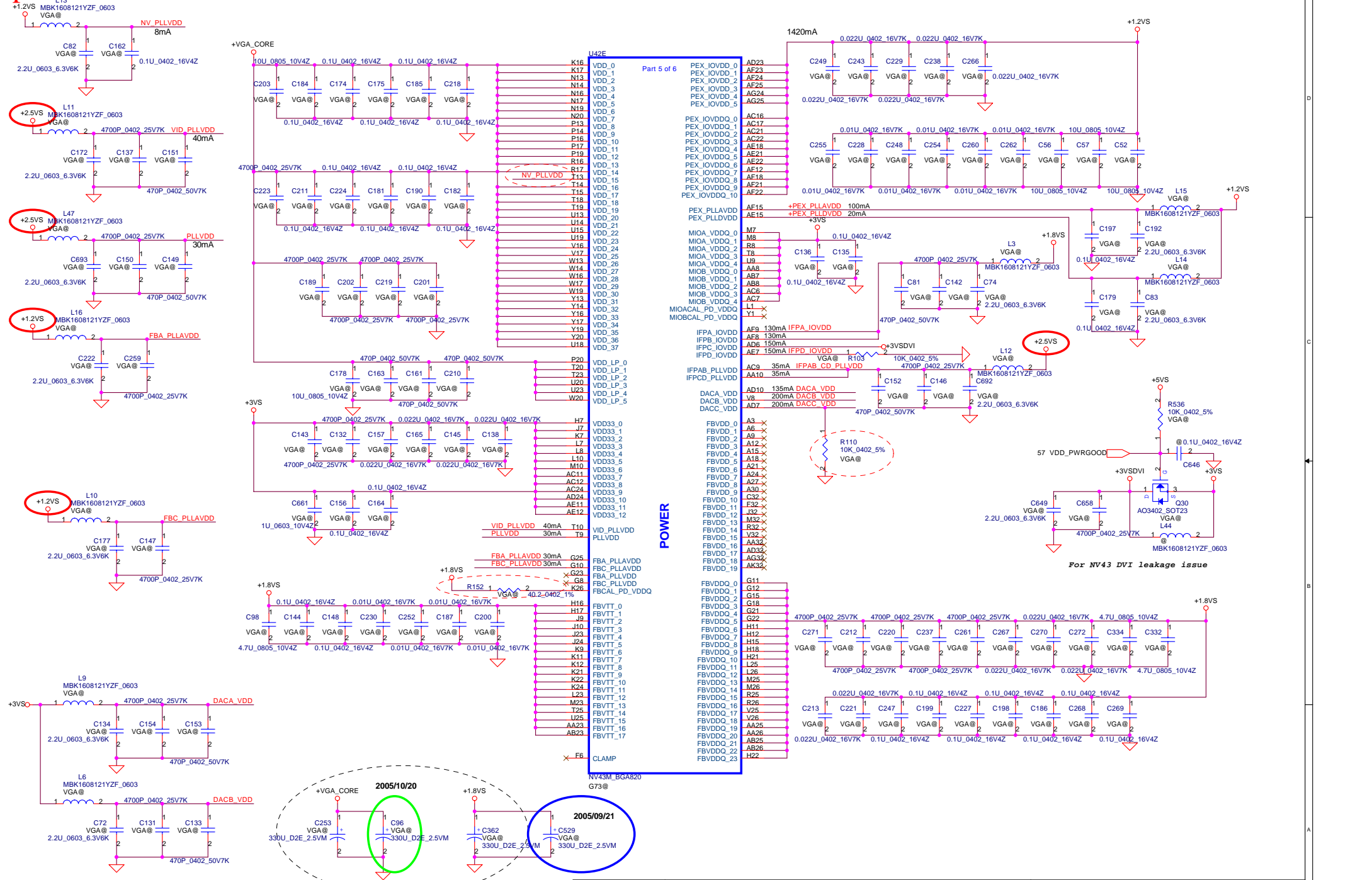
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Clock Generator			
Size	Document Number		Rev
B	HBL50 LA-2921P		0.3
Date:	Friday, November 11, 2005	Sheet	14 of 59



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Issued Date	2005/06/20	Deciphered Date	2006/06/20	G72/G73 Main	
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				B	0.3
				Date:	Friday, November 11, 2005
				Sheet	15 of 59

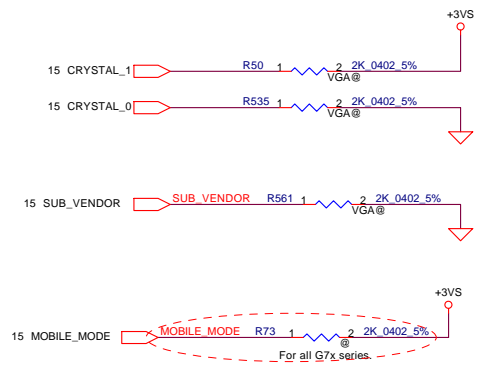
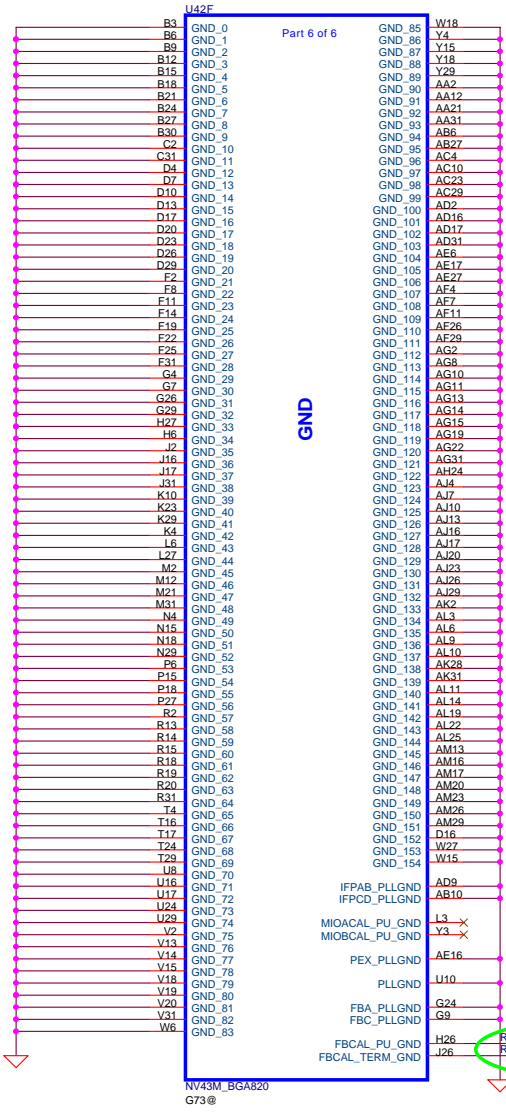




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		2006/06/20

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Compal Electronics, Inc.		
Title		
G72/G73 Power		
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3
Date:	Friday, November 11, 2005	Sheet 17 of 59

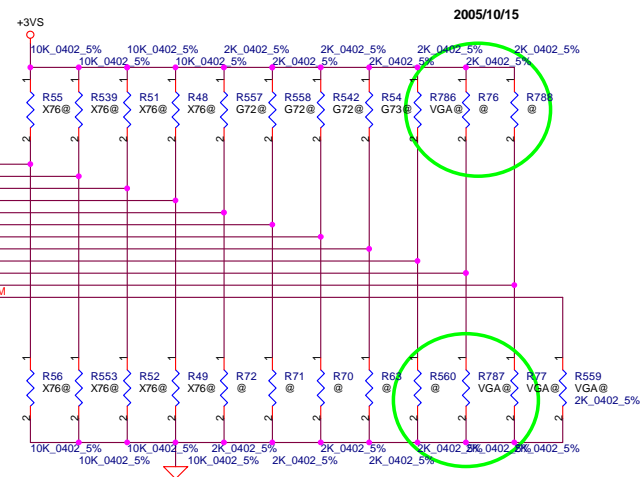


G73M : SA00000QZ00  
 G72M : SA00000QY00  
 G72MV : SA00000QY20

STRAPS	PIN	DESCRIPTION	Value	Value
CRYSTAL[1:0]	MIOBD[6,2]	27MHz=10, 14.318MHz=01, 13.5MHz=00	10	
ROM_TYPE[1:0]	MIOBD [11:10]	Parallel=00, SERIAL M25P10=01, Serial SST45VF=10	01	
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD [9,8,6]	Recommended for G7x	010	
RAM_CFG[3:0]	MIOAD[5:2]	16Mx16x4 1.8V (128bit G73M)	0001	Samsung
		16Mx16x4 1.8V (128bit G73M)	0011	Hynix
		16Mx16x4 1.8V (64bit G73M)	1001	Samsung
		16Mx16x4 1.8V (64bit G73M)	1011	Hynix
		16Mx16x4 1.8V (64bit G72MV)	0001	Samsung
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxxx8 G72M-0x01D8	1000	
		G72MV-0x01D7 TBD/TBD	0111	
MOBILE_MODE	MIOBD7	For NV44M/G7x		0

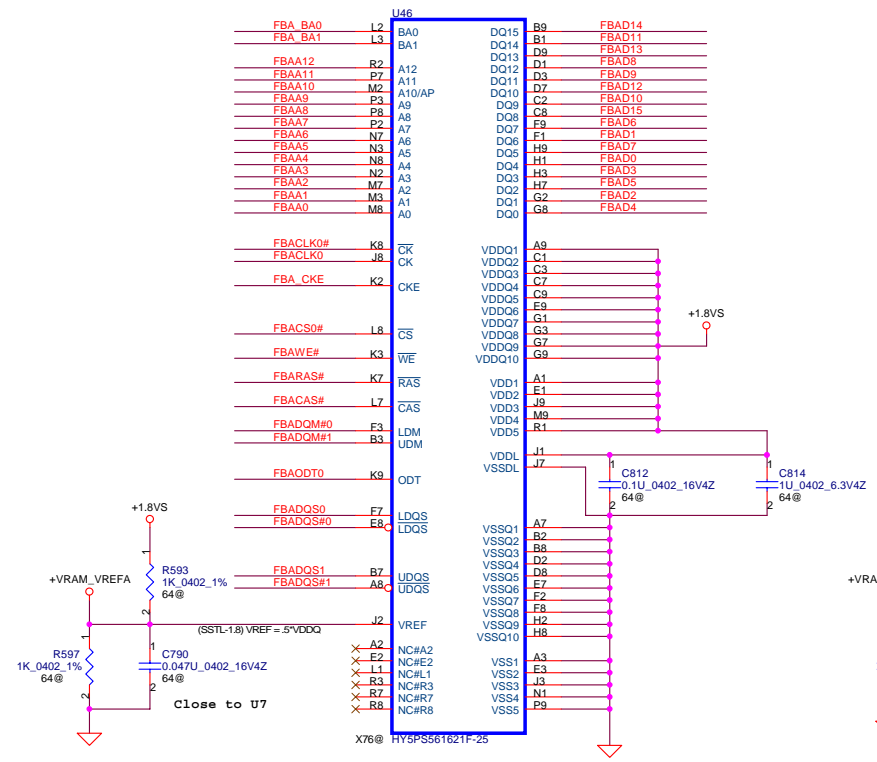
RAM\_CFG[1:0]  
 (Manufacture)  
 (01=Sam, 10=Inf, 11=Hyn)  
 RAM\_CFG[2] (0=16M or 1=32M)  
 RAM\_CFG[3] (Bandwidth 0=Full, 1=Half)

Bandwidth	RAM Type	Vendor
FULL R49	32M R51	Samsung R553, R55
HALF R48	16M R52	Hynix R539, R55 Infineon R553, R56

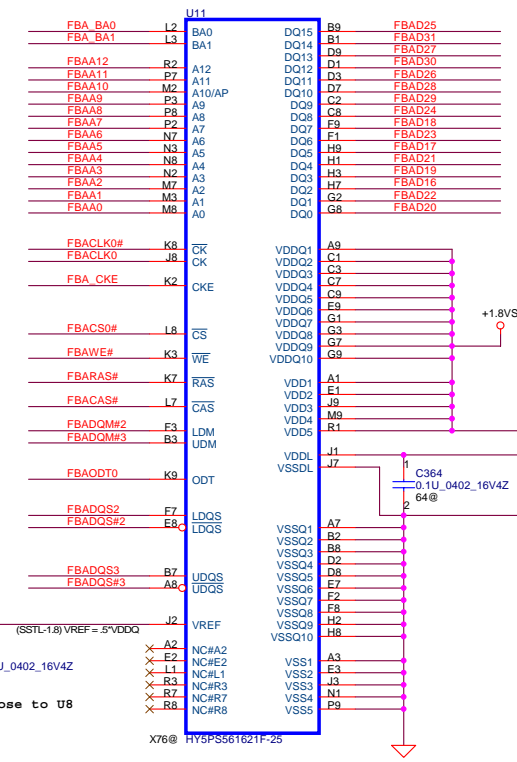


Package	Infineon GDDR2(400): SA00000S800 (HYB18T256161AF-25)	Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)
(10*12.5)	Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)
(11*13)	Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)	Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)
(8*13)		

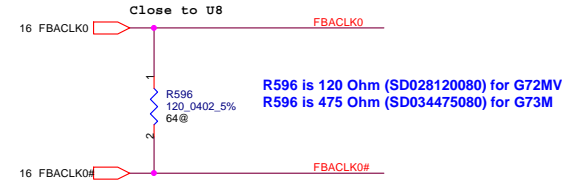
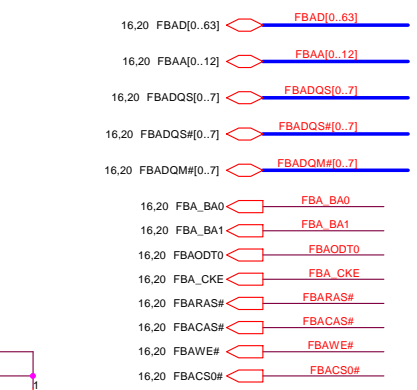
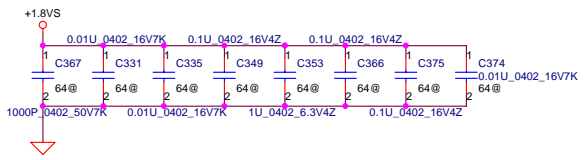
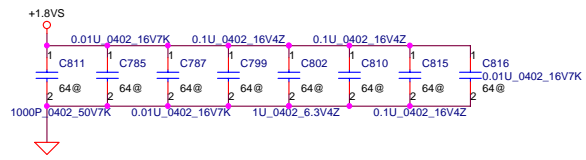
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title
				G72/G73 GND & STRAP
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			Document Number	Rev
			HBL50 LA-2921P	0.3
			Date: Friday, November 11, 2005	Sheet 18 of 59



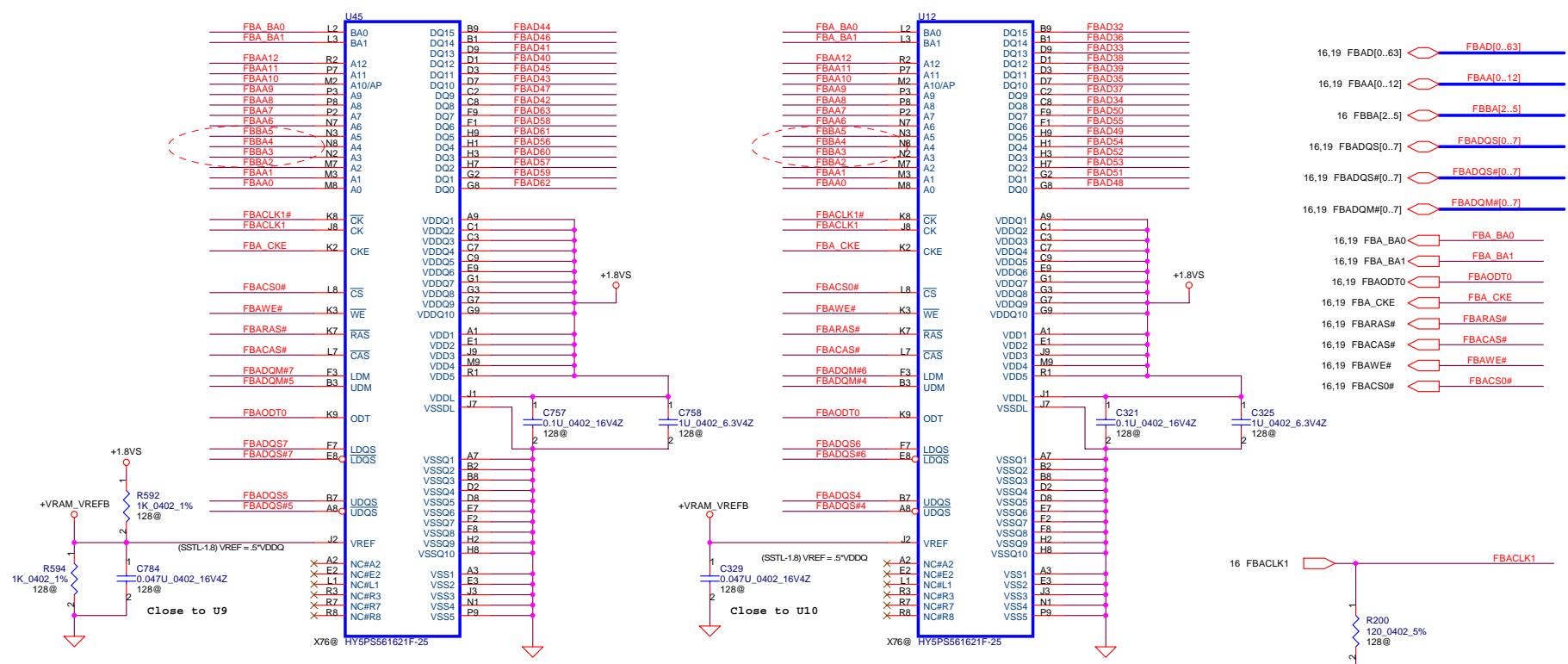
DDR2 BGA MEMORY



DDR2 BGA MEMORY

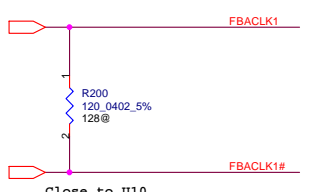
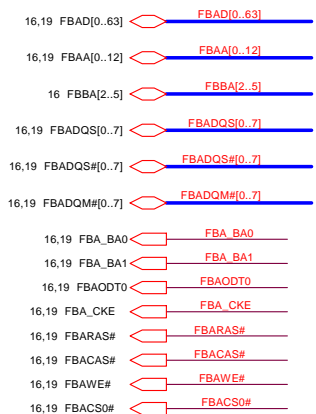


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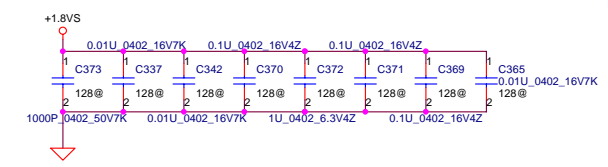
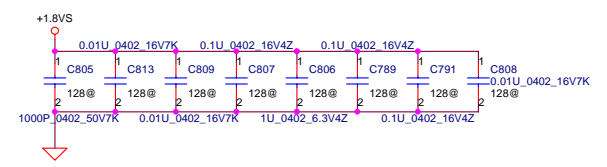


DDR2 BGA MEMORY

DDR2 BGA MEMORY

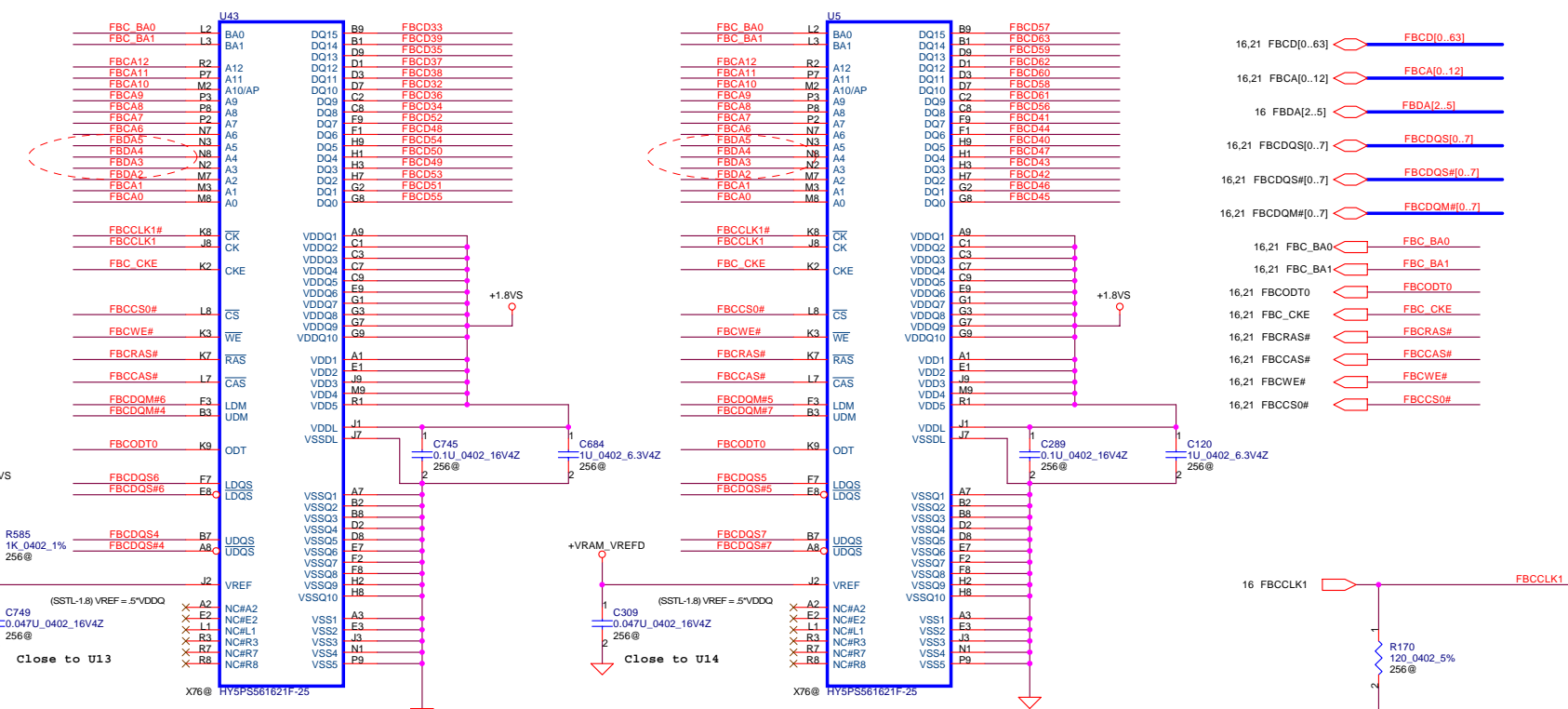


R200 is 120 Ohm (SD028120080) for G72MV  
R200 is 481 Ohm (SD00000CA80) for G73M



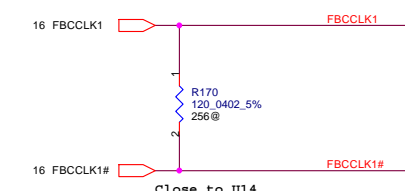
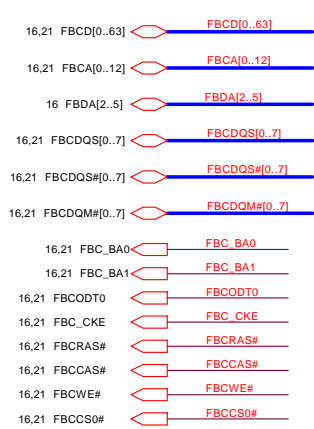
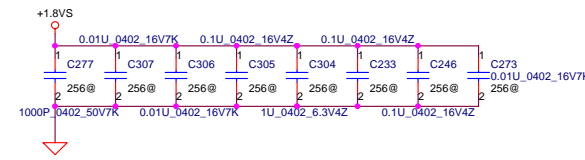
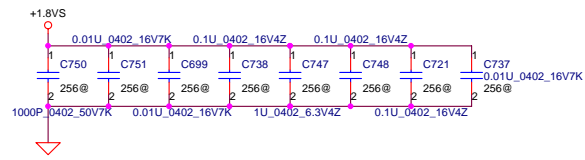
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				Document Number HBL50 LA-2921P
				Rev 0.3
				Date: Friday, November 11, 2005   Sheet 20 of 59





DDR2 BGA MEMORY

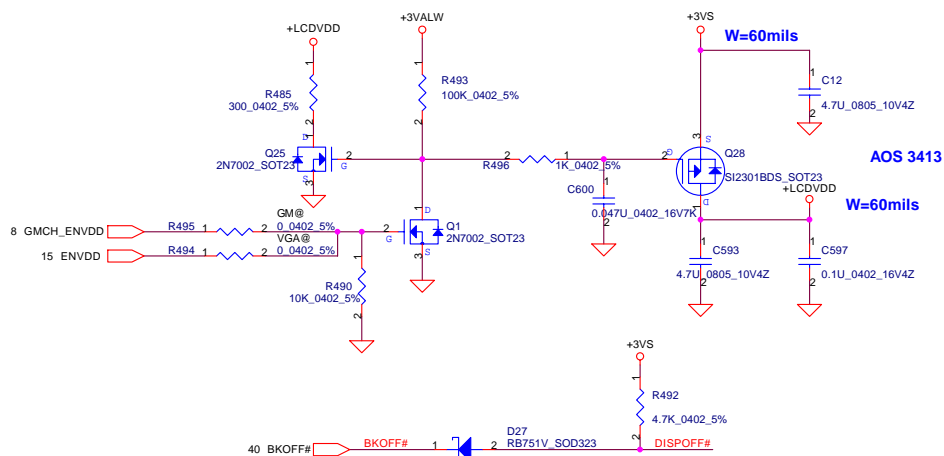
DDR2 BGA MEMORY



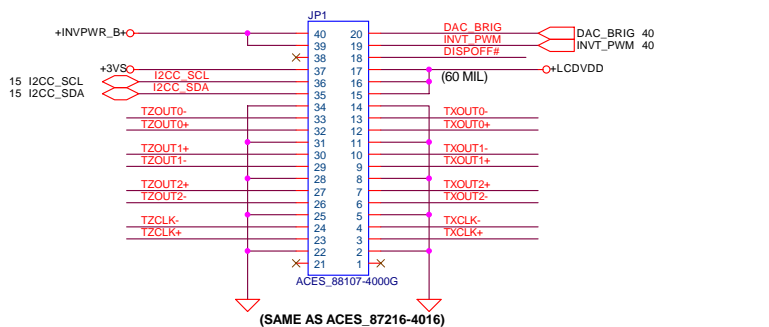
R170 is 120 Ohm (SD028120080) for G72MV  
R170 is 481 Ohm (SD00000CA80) for G73M

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Date: Friday, November 11, 2005			Sheet 22 of 59	Rev 0.3

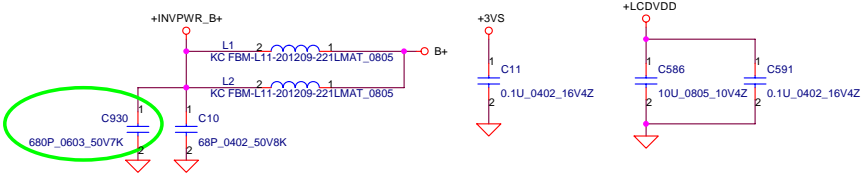
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

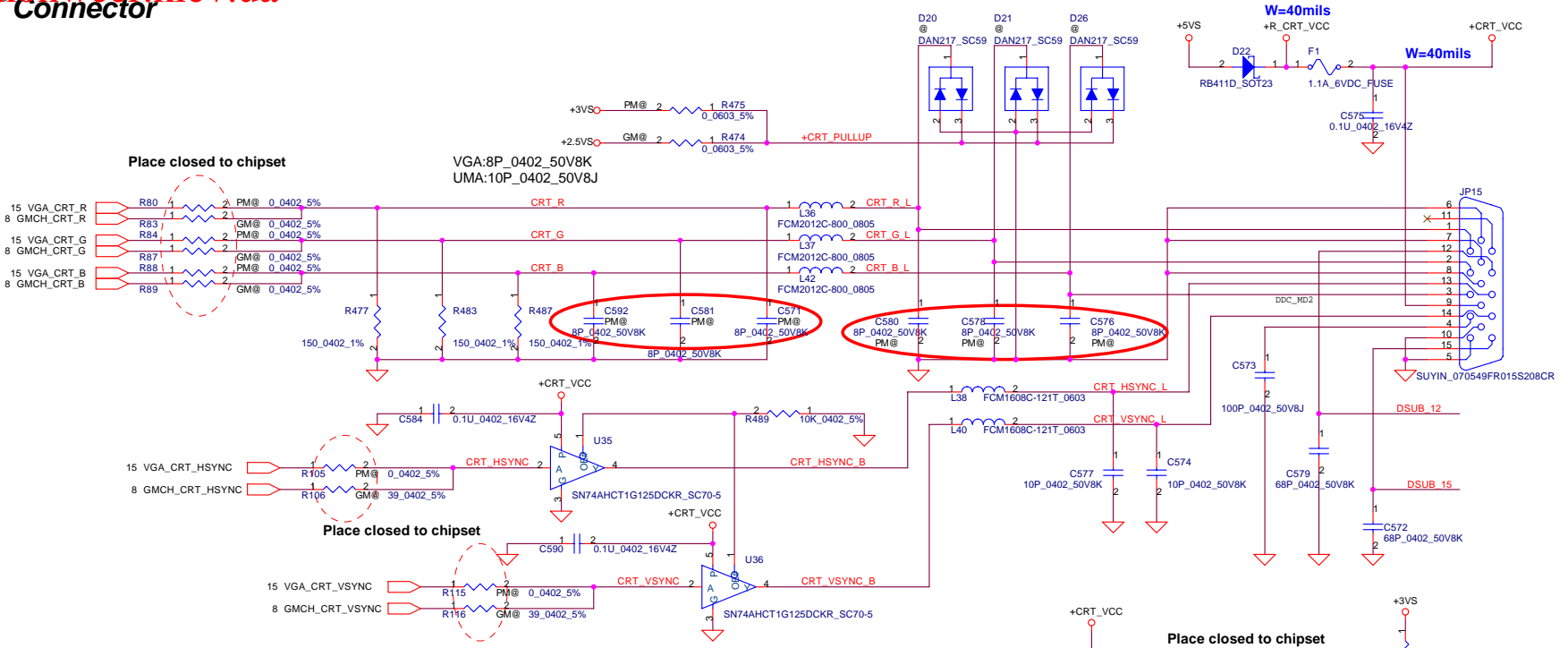


(SAME AS ACES\_87216-4016)

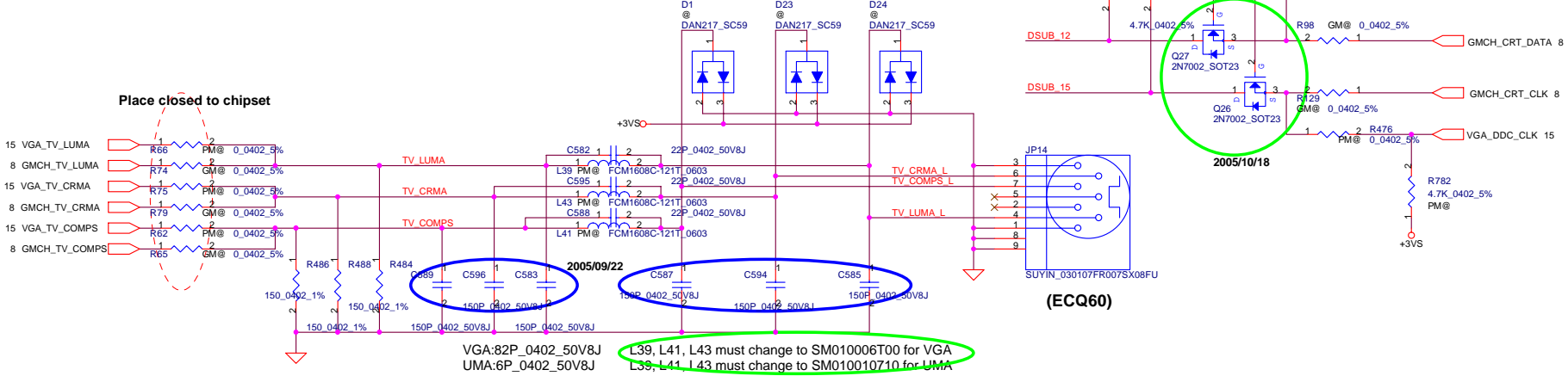


TXOUT0-	R25	1	2	VGA@ 0.0402 5%	LVDSA0-	LVDSA0-	15
TXOUT0+	R26	1	2	VGA@ 0.0402 5%	LVDSA0+	LVDSA0+	15
TXOUT1-	R27	1	2	VGA@ 0.0402 5%	LVDSA1-	LVDSA1-	15
TXOUT1+	R28	1	2	VGA@ 0.0402 5%	LVDSA1+	LVDSA1+	15
TXOUT2-	R29	1	2	VGA@ 0.0402 5%	LVDSA2-	LVDSA2-	15
TXOUT2+	R30	1	2	VGA@ 0.0402 5%	LVDSA2+	LVDSA2+	15
TXCLK-	R31	1	2	VGA@ 0.0402 5%	LVDSAC-	LVDSAC-	15
TXCLK+	R32	1	2	VGA@ 0.0402 5%	LVDSAC+	LVDSAC+	15
TZOUT0-	R33	1	2	VGA@ 0.0402 5%	LVDSB0-	LVDSB0-	15
TZOUT0+	R34	1	2	VGA@ 0.0402 5%	LVDSB0+	LVDSB0+	15
TZOUT1-	R35	1	2	VGA@ 0.0402 5%	LVDSB1-	LVDSB1-	15
TZOUT1+	R36	1	2	VGA@ 0.0402 5%	LVDSB1+	LVDSB1+	15
TZOUT2-	R37	1	2	VGA@ 0.0402 5%	LVDSB2-	LVDSB2-	15
TZOUT2+	R38	1	2	VGA@ 0.0402 5%	LVDSB2+	LVDSB2+	15
TZCLK-	R39	1	2	VGA@ 0.0402 5%	LVDSBC-	LVDSBC-	15
TZCLK+	R40	1	2	VGA@ 0.0402 5%	LVDSBC+	LVDSBC+	15
I2CC_SCL	R41	1	2	GM@ 0.0402 5%	GMCH_LCD_CLK	GMCH_LCD_CLK	8
I2CC_SDA	R42	1	2	GM@ 0.0402 5%	GMCH_LCD_DATA	GMCH_LCD_DATA	8
TXOUT0-	R509	1	2	GM@ 0.0402 5%	GMCH_TXOUT0-	GMCH_TXOUT0-	8
TXOUT0+	R508	1	2	GM@ 0.0402 5%	GMCH_TXOUT0+	GMCH_TXOUT0+	8
TXOUT1-	R507	1	2	GM@ 0.0402 5%	GMCH_TXOUT1-	GMCH_TXOUT1-	8
TXOUT1+	R506	1	2	GM@ 0.0402 5%	GMCH_TXOUT1+	GMCH_TXOUT1+	8
TXOUT2-	R505	1	2	GM@ 0.0402 5%	GMCH_TXOUT2-	GMCH_TXOUT2-	8
TXOUT2+	R504	1	2	GM@ 0.0402 5%	GMCH_TXOUT2+	GMCH_TXOUT2+	8
TXCLK-	R503	1	2	GM@ 0.0402 5%	GMCH_TXCLK-	GMCH_TXCLK-	8
TXCLK+	R502	1	2	GM@ 0.0402 5%	GMCH_TXCLK+	GMCH_TXCLK+	8
TZOUT0-	R525	1	2	GM@ 0.0402 5%	GMCH_TZOUT0-	GMCH_TZOUT0-	8
TZOUT0+	R524	1	2	GM@ 0.0402 5%	GMCH_TZOUT0+	GMCH_TZOUT0+	8
TZOUT1-	R523	1	2	GM@ 0.0402 5%	GMCH_TZOUT1-	GMCH_TZOUT1-	8
TZOUT1+	R522	1	2	GM@ 0.0402 5%	GMCH_TZOUT1+	GMCH_TZOUT1+	8
TZOUT2-	R521	1	2	GM@ 0.0402 5%	GMCH_TZOUT2-	GMCH_TZOUT2-	8
TZOUT2+	R520	1	2	GM@ 0.0402 5%	GMCH_TZOUT2+	GMCH_TZOUT2+	8
TZCLK-	R519	1	2	GM@ 0.0402 5%	GMCH_TZCLK-	GMCH_TZCLK-	8
TZCLK+	R518	1	2	GM@ 0.0402 5%	GMCH_TZCLK+	GMCH_TZCLK+	8

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Date: Friday, November 11, 2005				Sheet 23 of 59

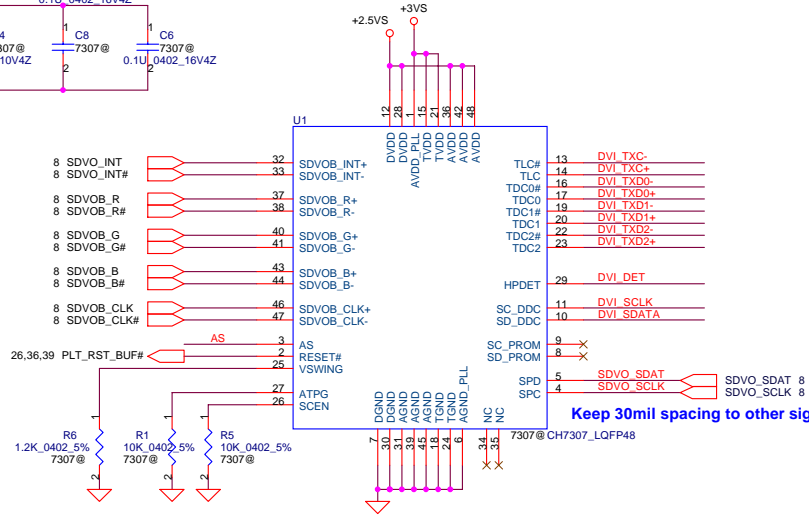
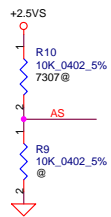
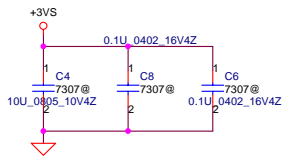
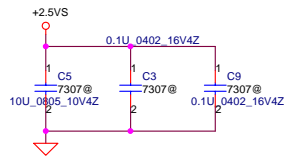


**TV-OUT Conn.**



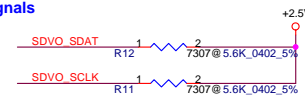
2005/09/22  
 L39, L41, L43 must change to SM010006T00 for VGA  
 L39, L41, L43 must change to SM010010710 for UMA

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				B	HBL50 LA-2921P
				Date:	Friday, November 11, 2005
				Sheet	24 of 59
				Rev	0.3

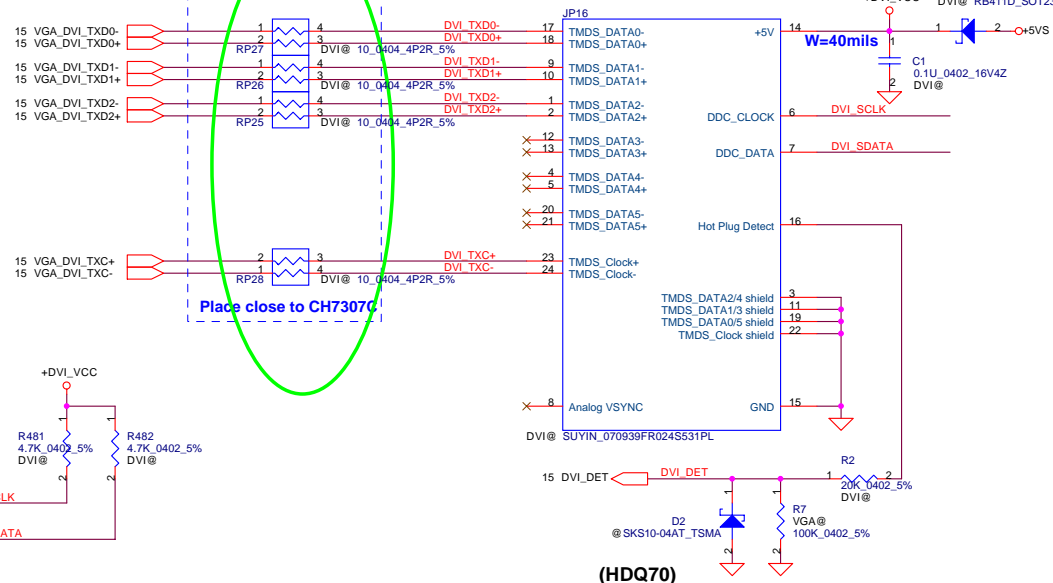


BOM structure	DVI from SDVO	DVI from Discrete VGA
7307@	Stuff	No_Stuff
VGA@	No_Stuff	Stuff
@	No_Stuff	No_Stuff

Keep 30mil spacing to other signals



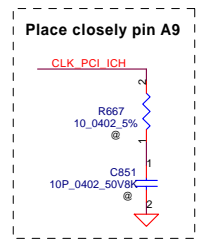
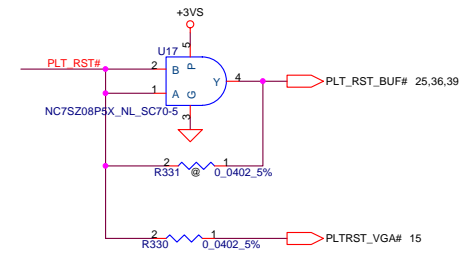
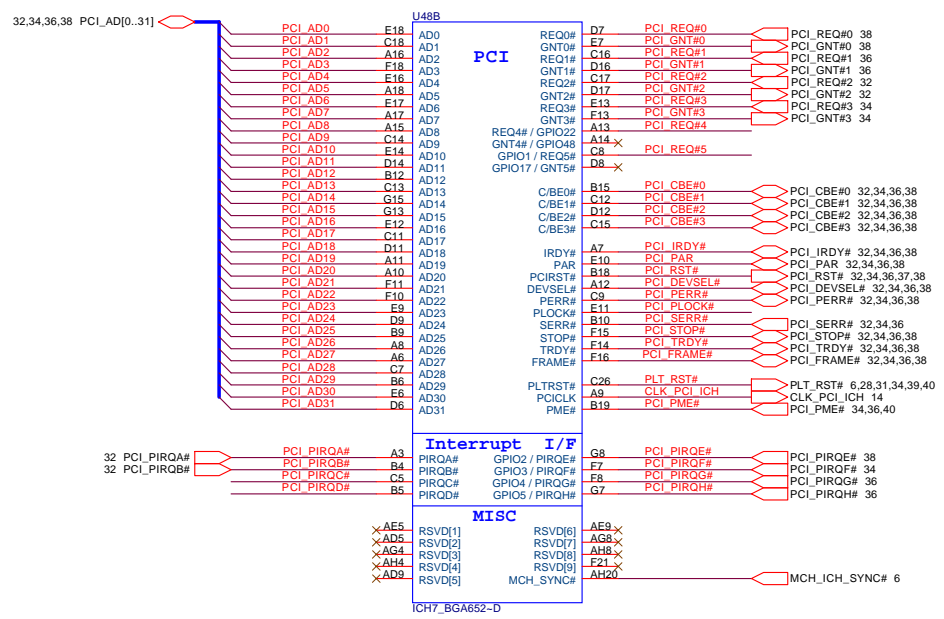
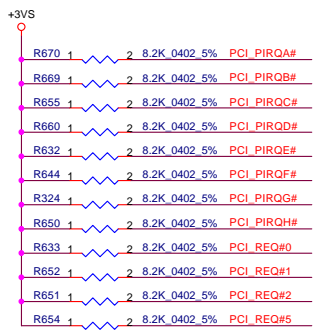
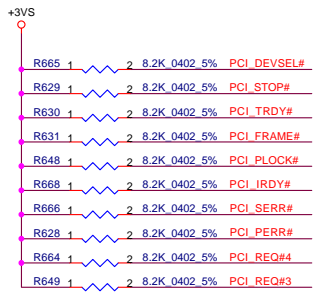
### DVI-D Connector



(HDQ70)

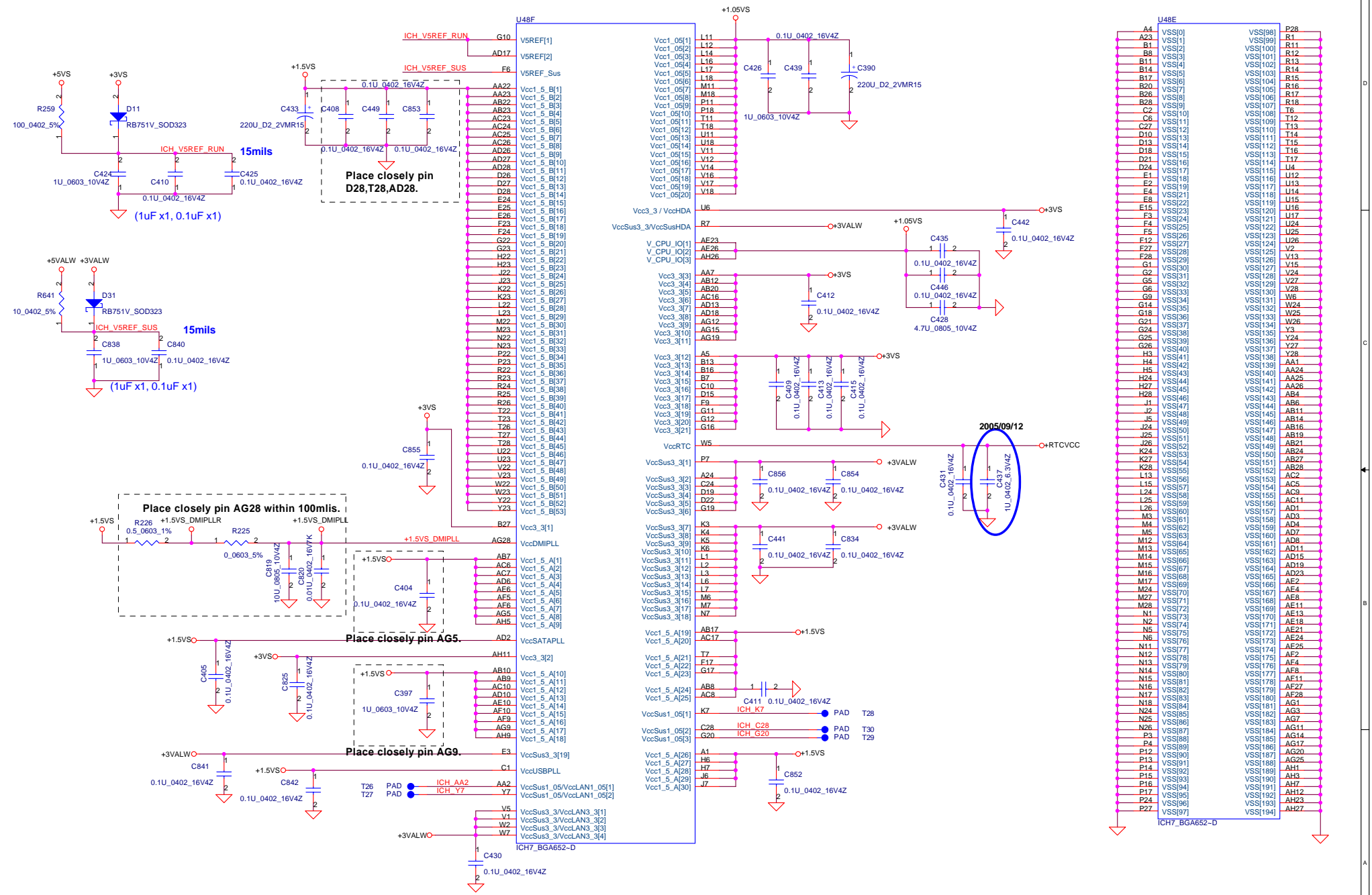
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title		
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Size B	Document Number	HBL50 LA-2921P		Rev	0.3	
Date:	Friday, November 11, 2005	Sheet	25 of 59			

ICH7M(B-0) (QK65) [QS]:SA00000V160  
 ICH7M-DH(B-0) (QK17) [QS]:SA00000JK60

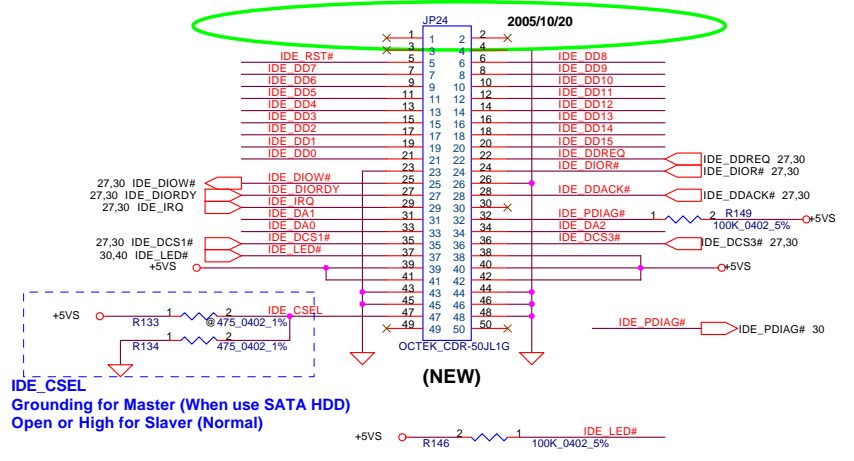
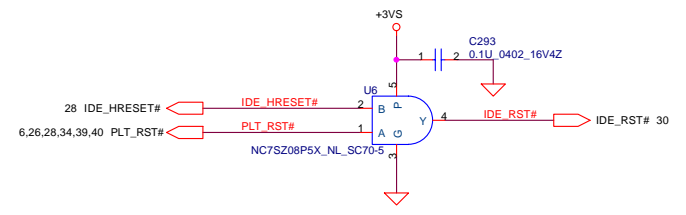
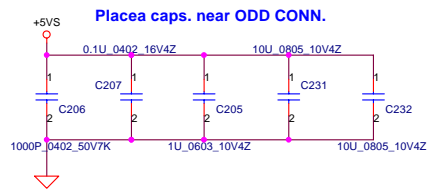




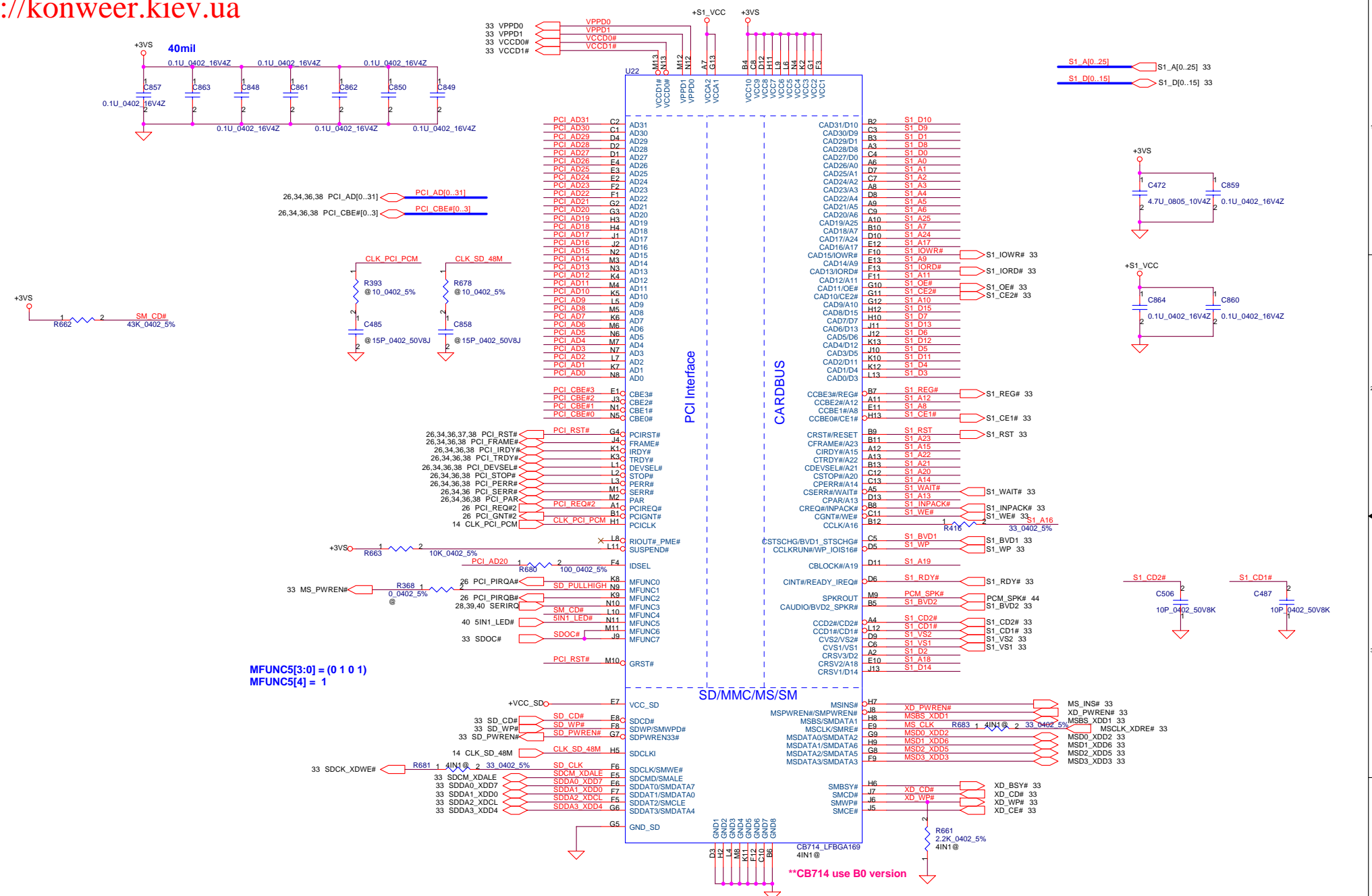








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Date: Friday, November 11, 2005			Sheet 31 of 59	



CB714 P/N: SA007140B50  
 CB1410 P/N: SA014100310

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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Cardbus Controller CB714
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Date:	Friday, November 11, 2005	Sheet	32 of 59	Rev 0.3

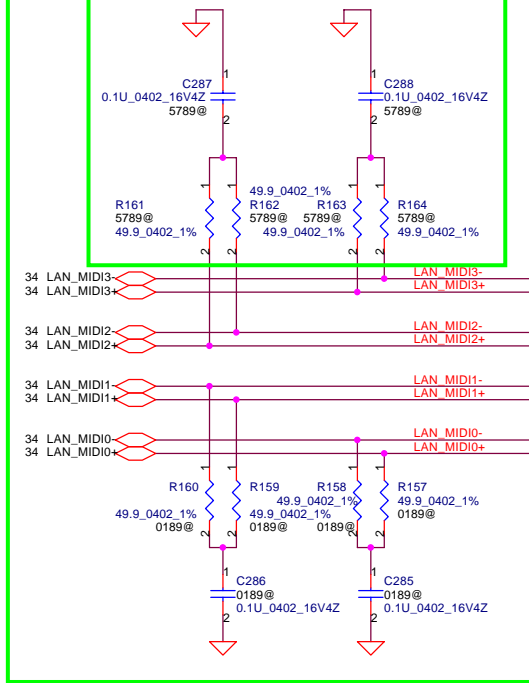




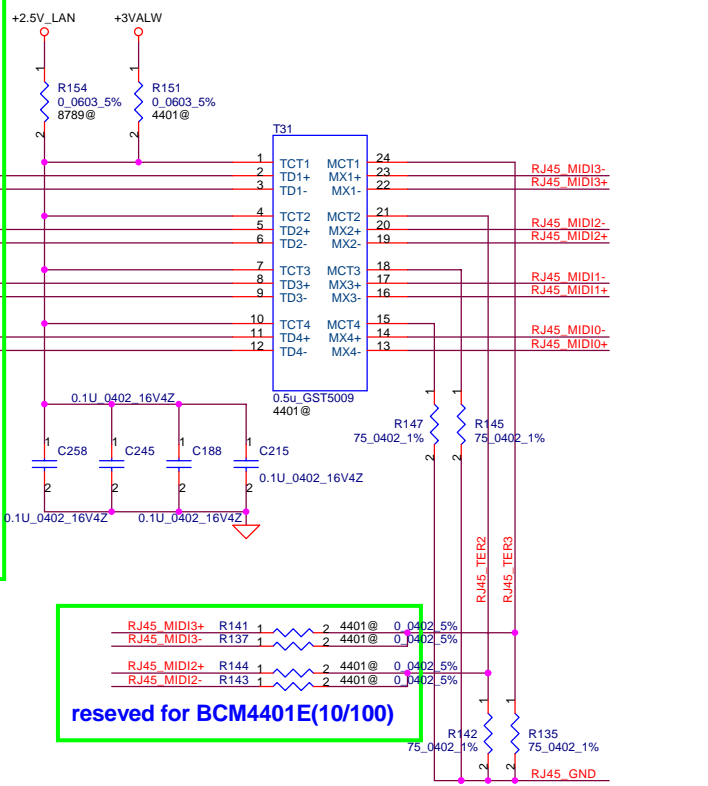
# LAN BCM4401E/ BCM5789

Place these components colsed to LAN chip

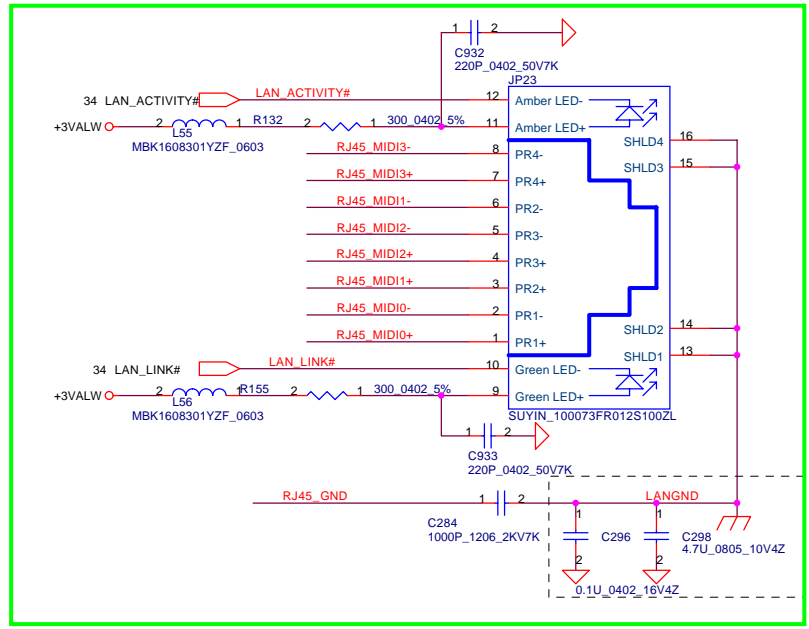
unpop when use BCM4401E(10/100)



GbE Transformer: GST5009 (SP050005610)  
10/100 Transformer : TST1284-LF (SP050001X10)



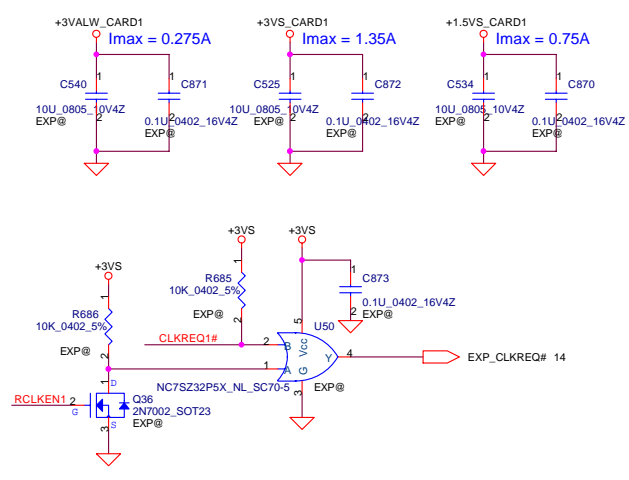
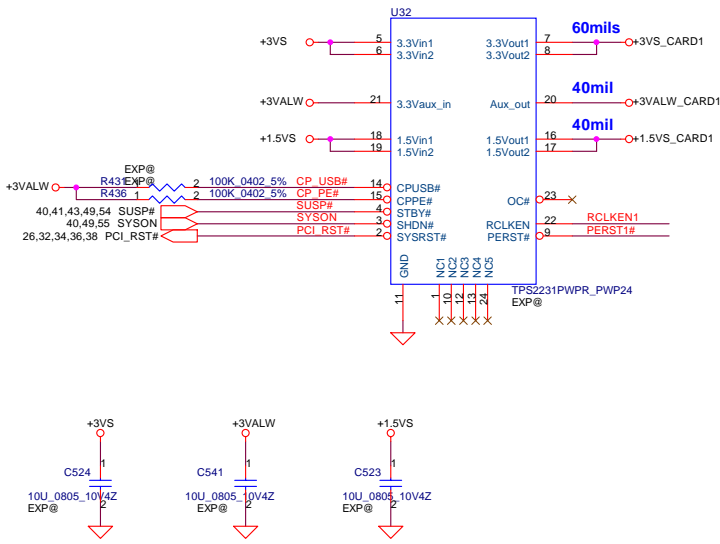
reused for BCM4401E(10/100)



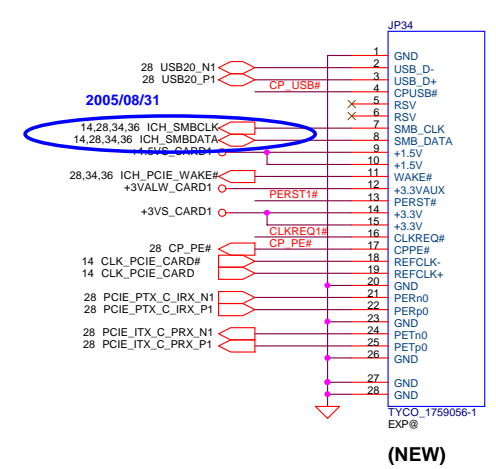
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	
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Size	Document Number	Rev		0.3	
B	HBL50 LA-2921P				
Date:	Friday, November 11, 2005	Sheet	35	of	59



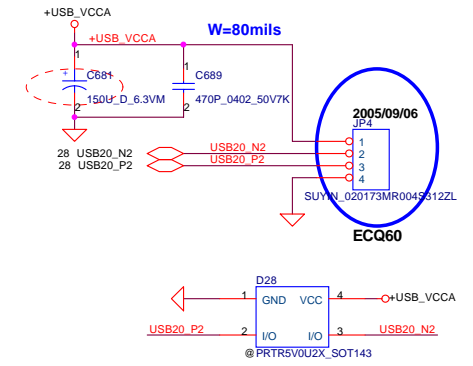
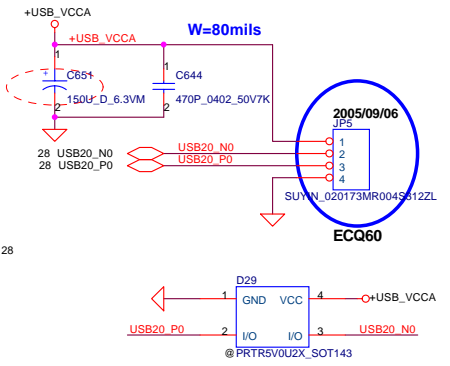
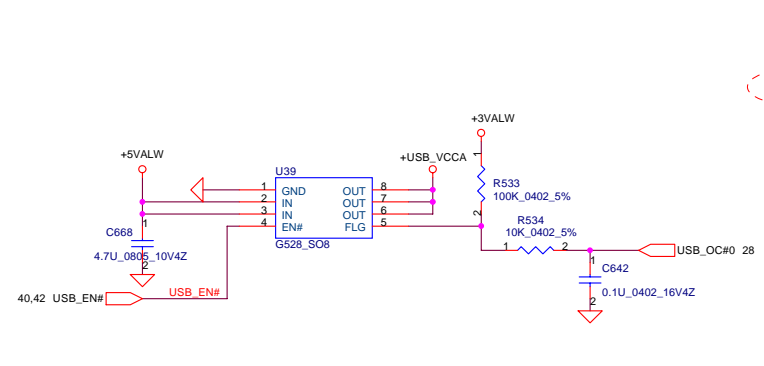
### New Card Power Switch



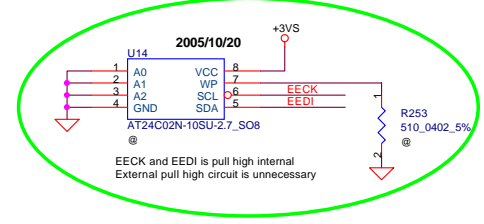
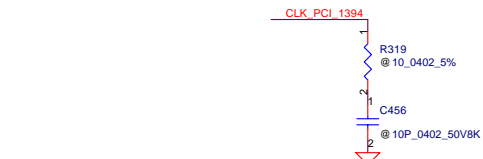
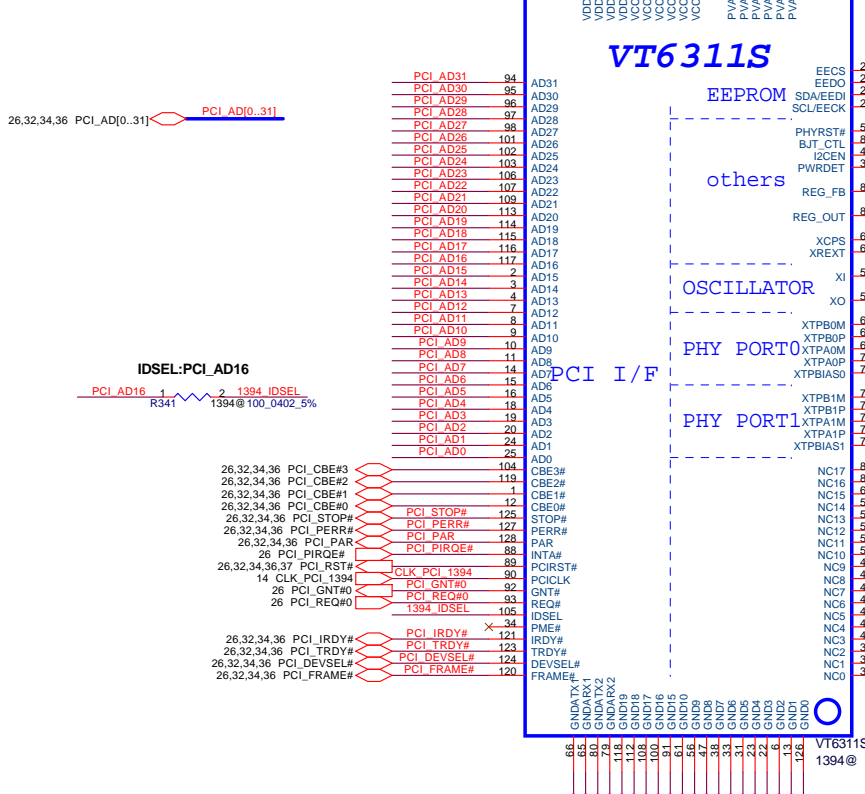
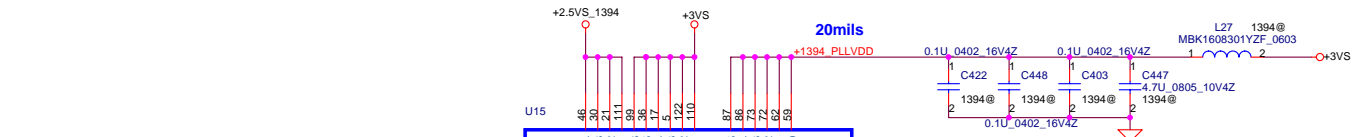
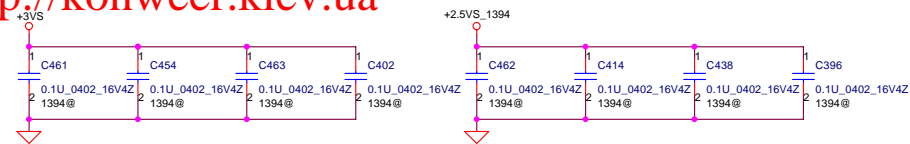
### New Card Socket (Left)



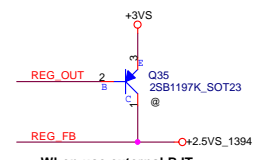
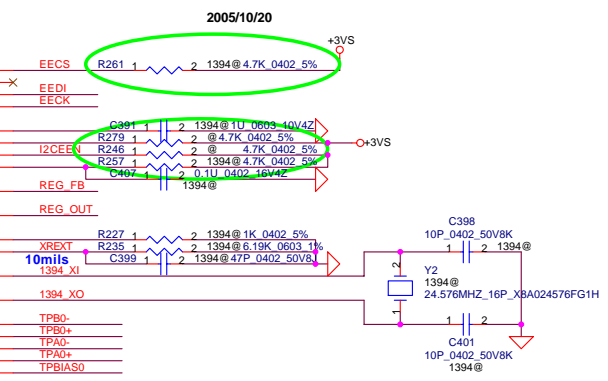
### USB CONN. 1 & 2



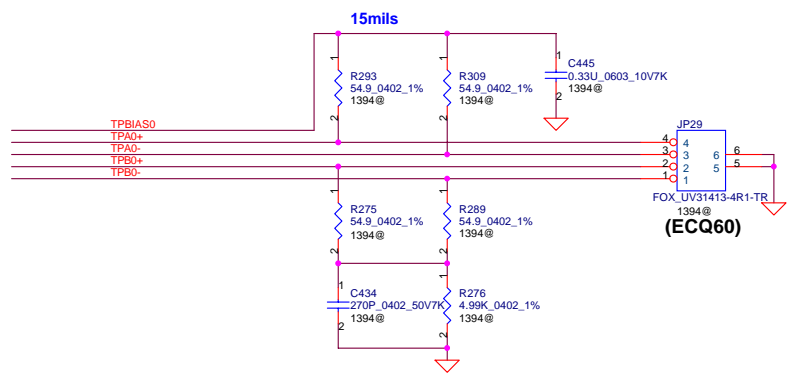
Security Classification	Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	NEW CARD SOCKET
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Date: Friday, November 11, 2005			Document Number	Rev 0.3
Sheet 37 of 59			HBL50 LA-2921P	



When use external EEPROM  
Populate U14, R246, R253  
Un-populate R261

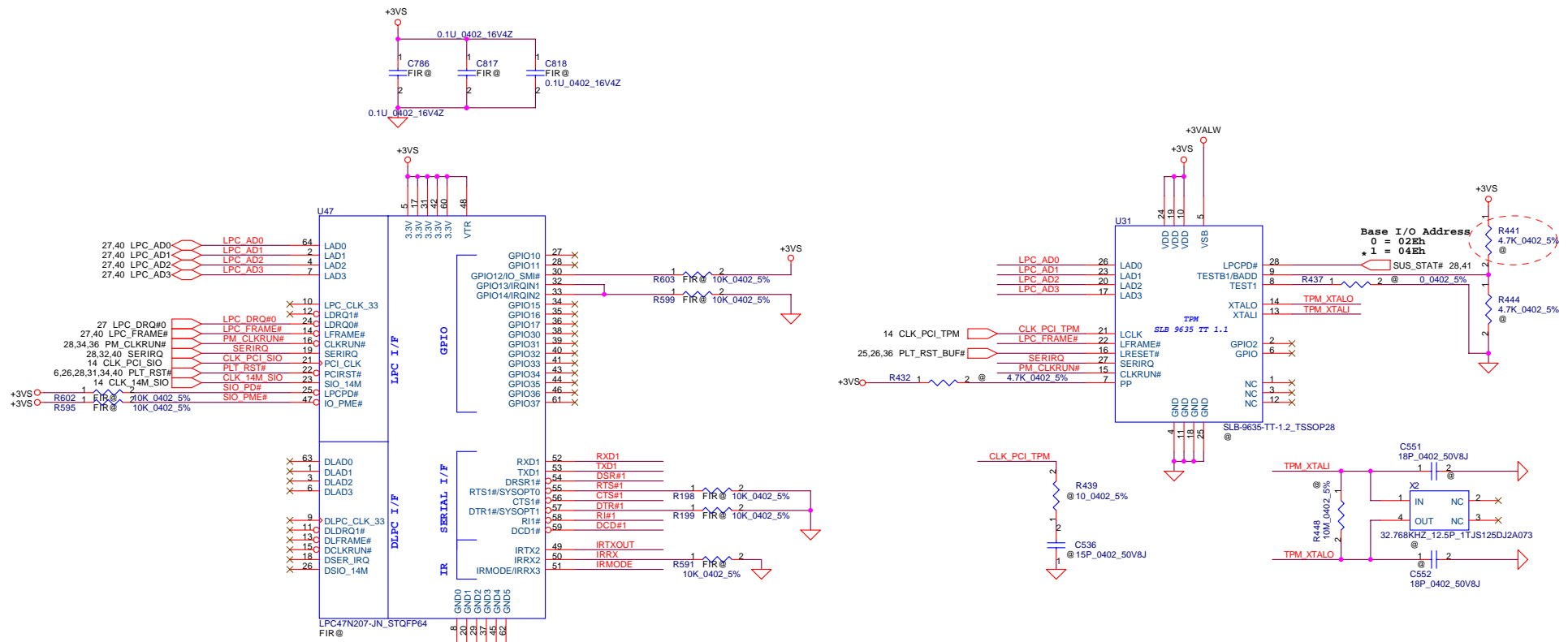


When use external BJT  
Populate Q35, R279

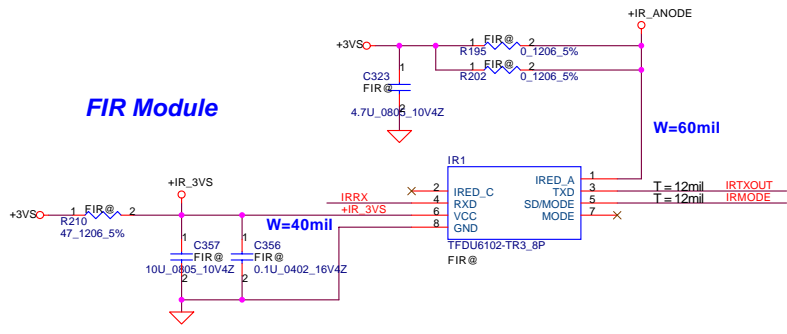


(ECQ60)

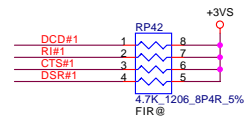
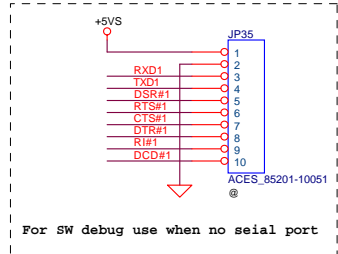
Security Classification		Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	IEEE1394 VIA VT6311S	
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				B	HBL50 LA-2921P
				Date:	Friday, November 11, 2005
				Sheet	38 of 59



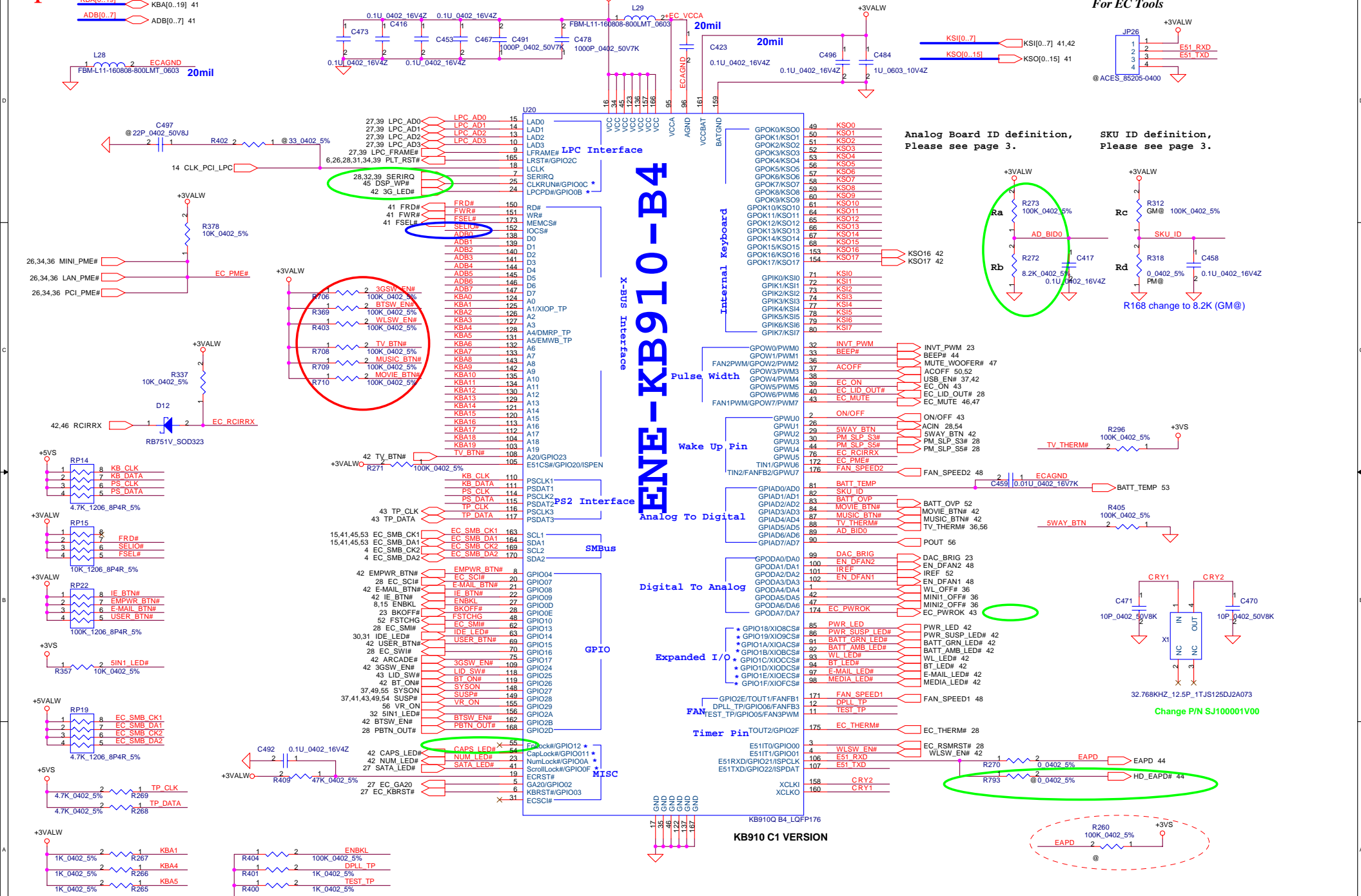
**FIR Module**



Place on the BOT side (near MINIPCI conn.)



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Size B	Document Number	Rev. 0.3		Date:
	Friday, November 11, 2005	Sheet	39 of 59	



For EC Tools

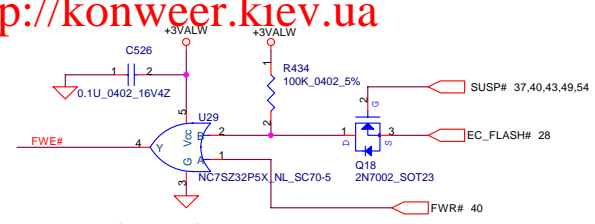
Analog Board ID definition, Please see page 3.

SKU ID definition, Please see page 3.

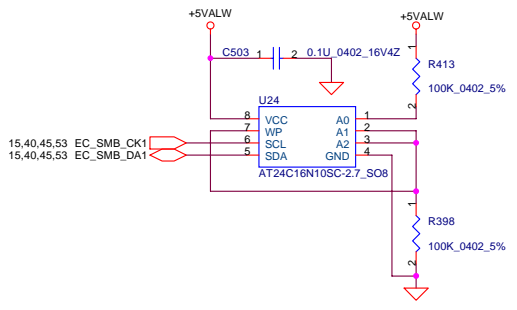
# ENE-KB910-B4

## KB910 C1 VERSION

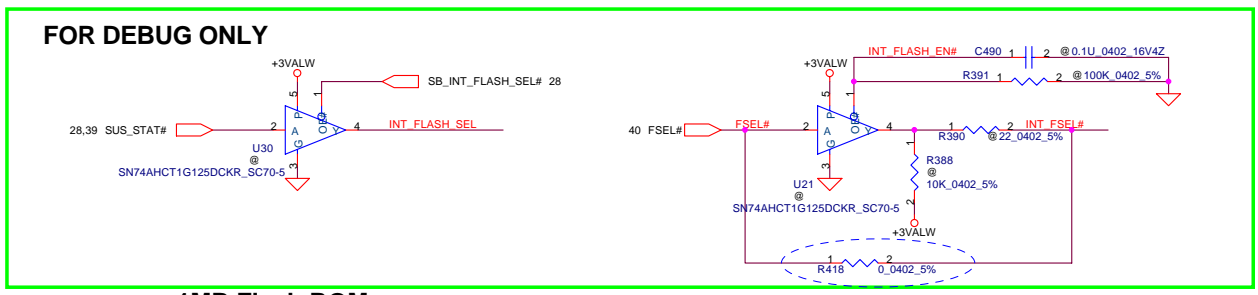
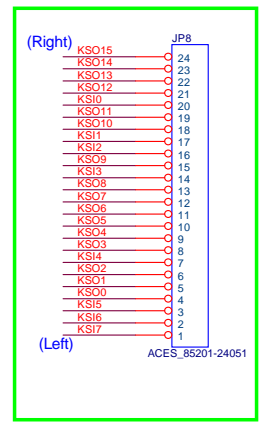
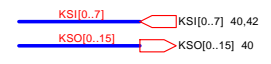
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	EC ENE KB910	
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Size	Document Number	Date		Friday, November 11, 2005	Sheet 40 of 59
HBL50 LA-2921P		Rev		0.3	



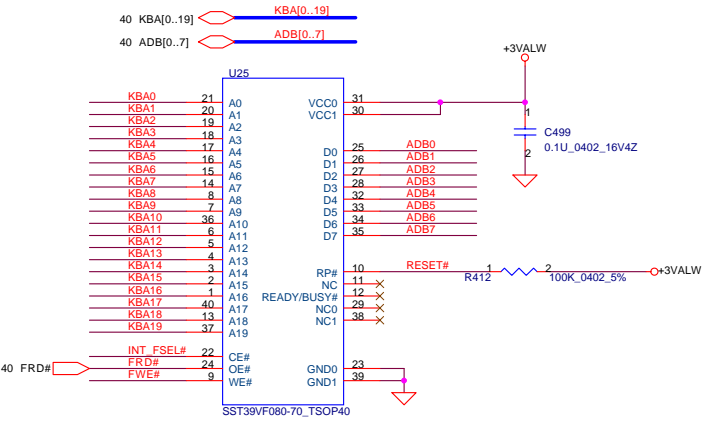
Check PCB Footprint



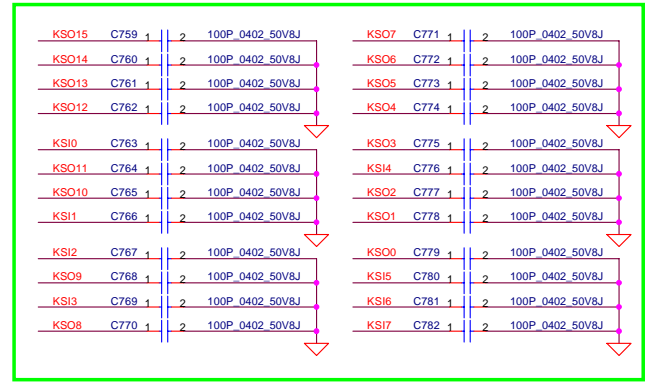
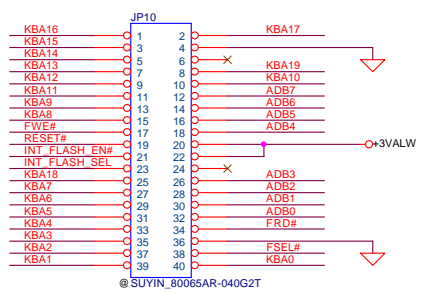
INT\_KBD Conn.



1MB Flash ROM

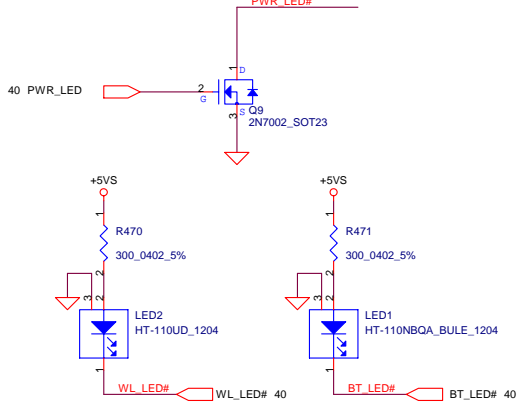
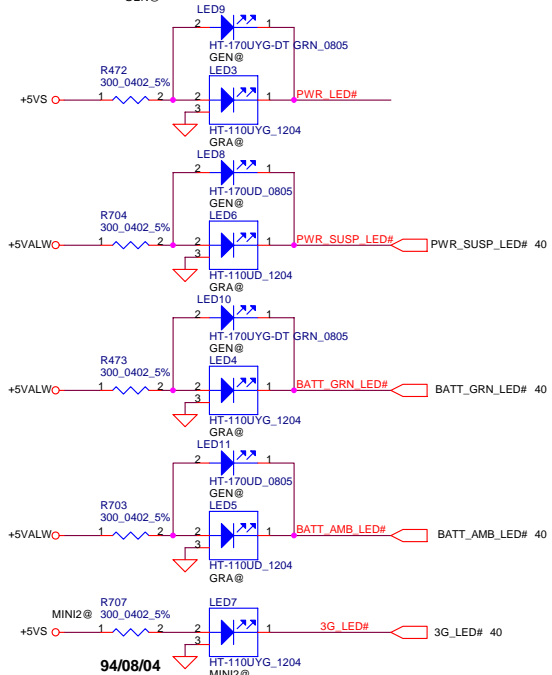
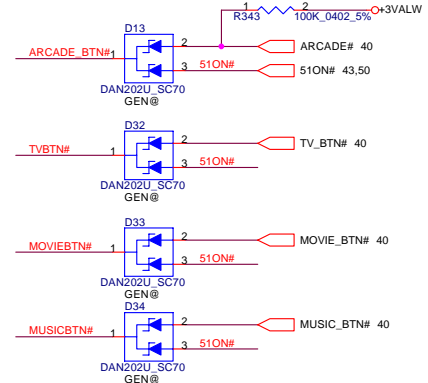
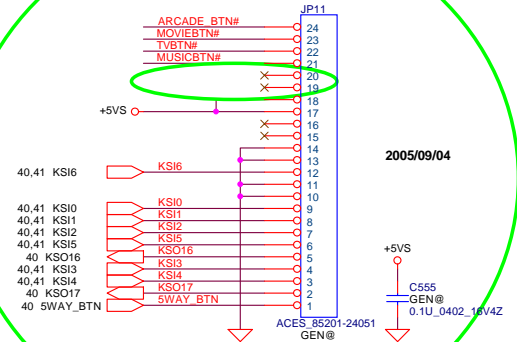


1MB ROM Socket

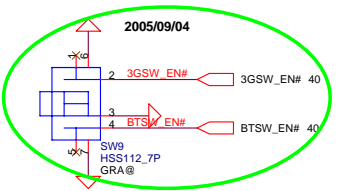


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Size	Document Number	Rev		Date	
B	HBL50 LA-2921P	0.3		Friday, November 11, 2005	
		Sheet	41	of	59

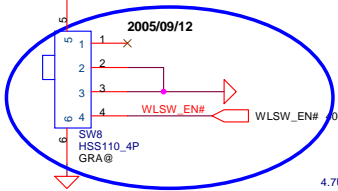
To CD-PLAY/B Conn.



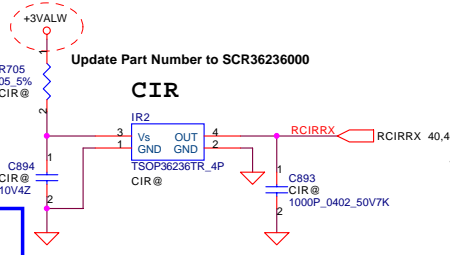
BT\_SW & 3G\_SW



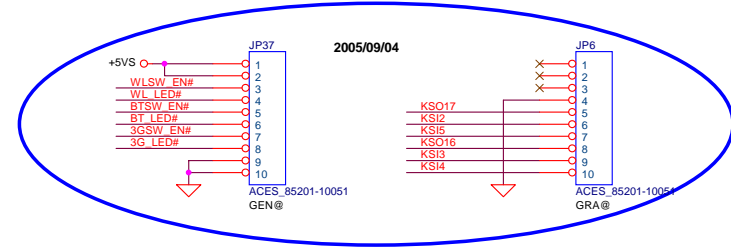
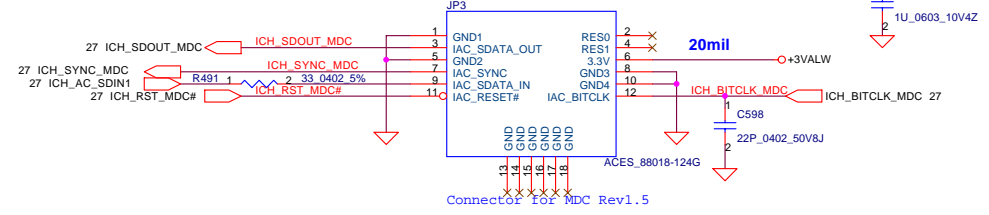
WL\_SW



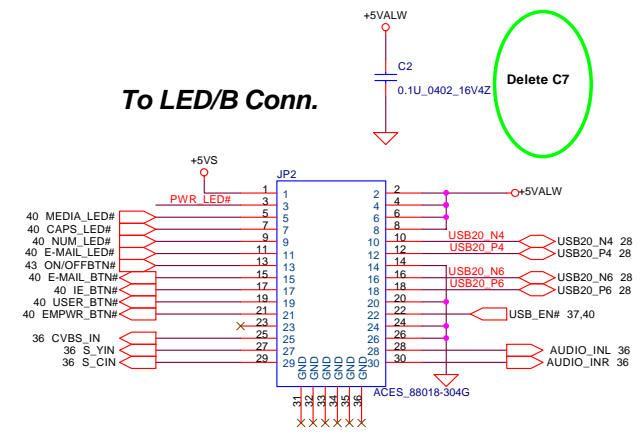
Geneva		Grapevine	
KSO10	VOL_UP	KSO16	PLAY
KSI1	RIGHT	KSI2	STOP
KSI2	PLAY	KSI3	NEXT
KSI3	STOP	KSI4	VOL_UP
KSI4	NEXT	KSI5	VOL_DOWN
KSI5	REV	KSI6	RECORD
KSI6	RECORD		



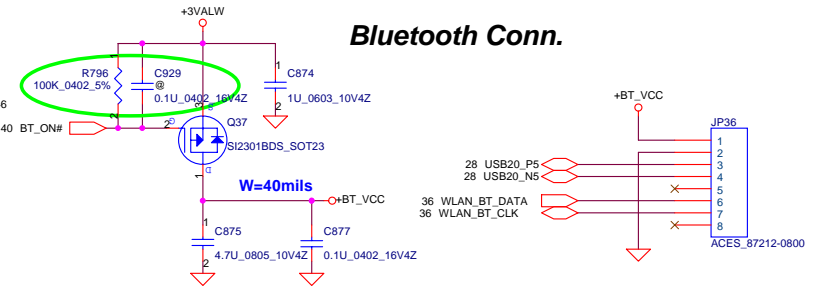
MDC Conn.



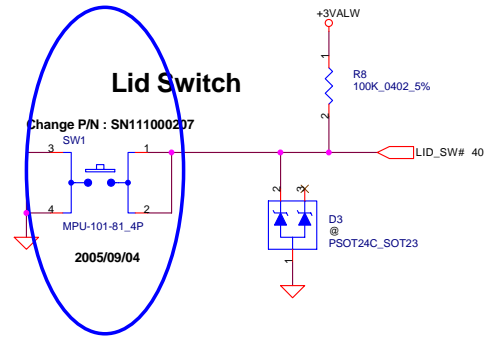
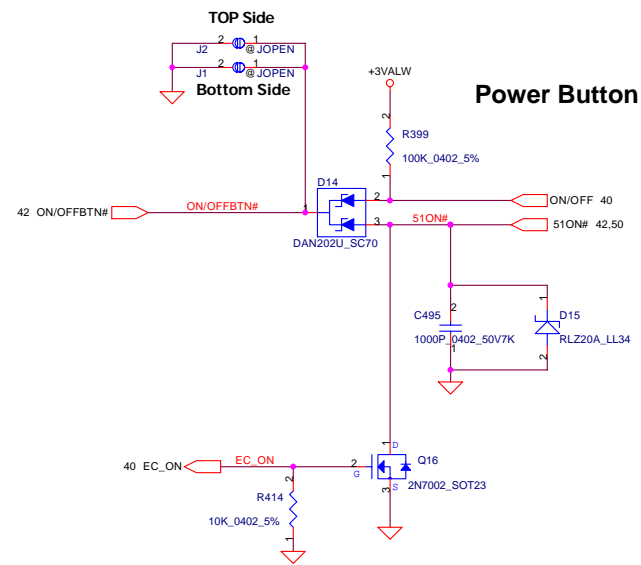
To LED/B Conn.



Bluetooth Conn.

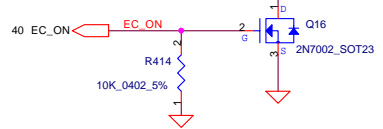
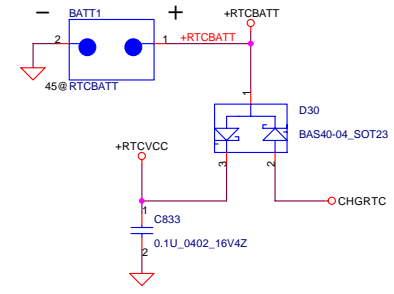


ON/OFF switch

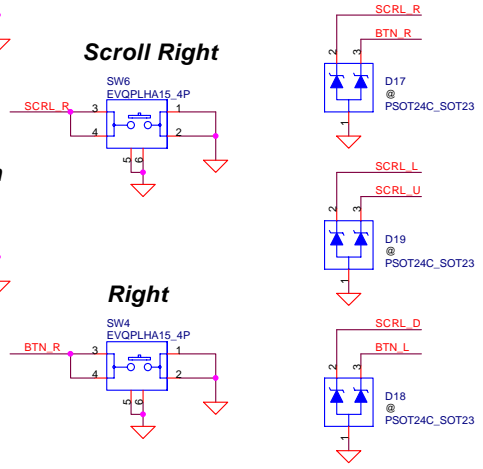
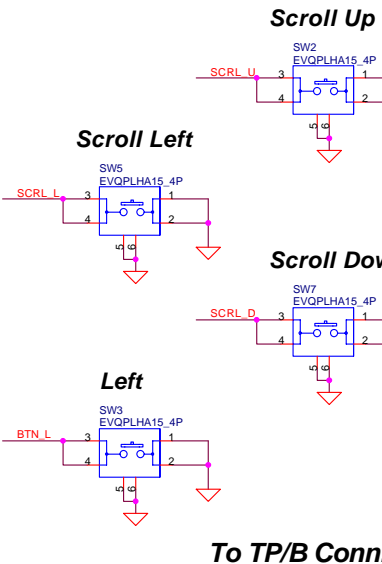
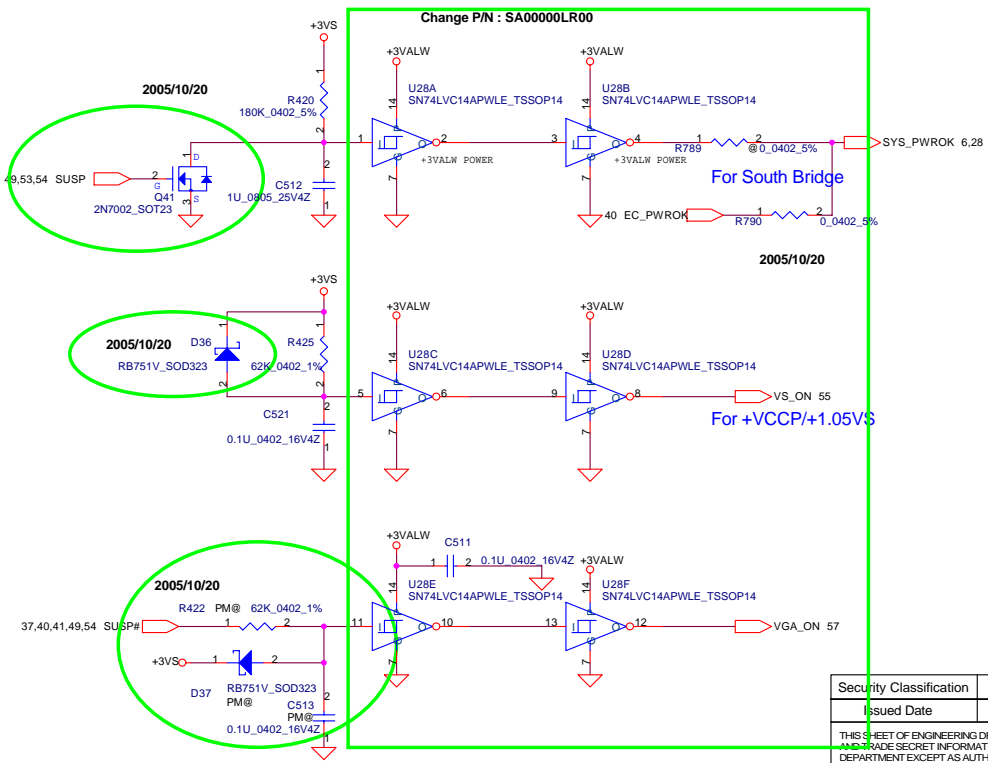


Change BATT1 P/N : SP093PA0200 (Panasonic)  
SP093MX0000 (MAXELL)

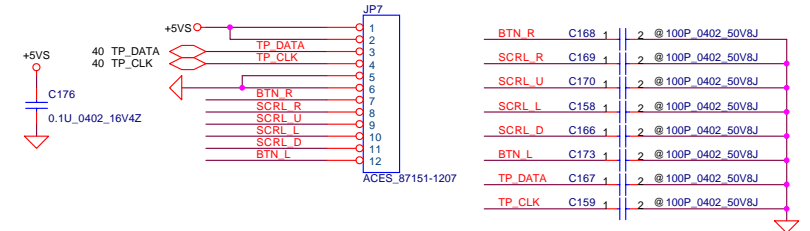
RTC Battery



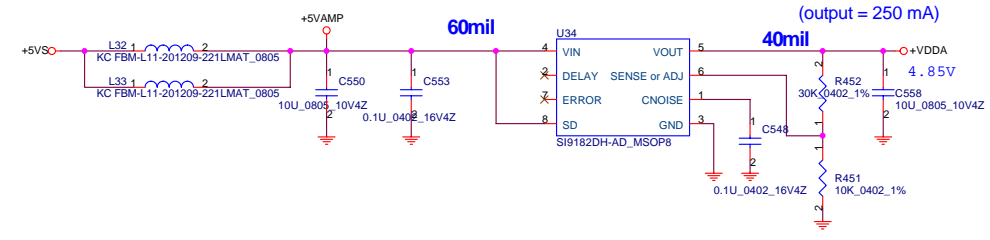
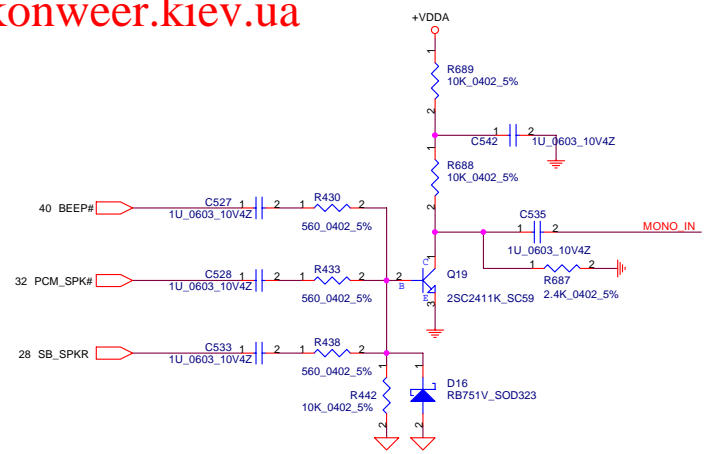
Power ON Circuit



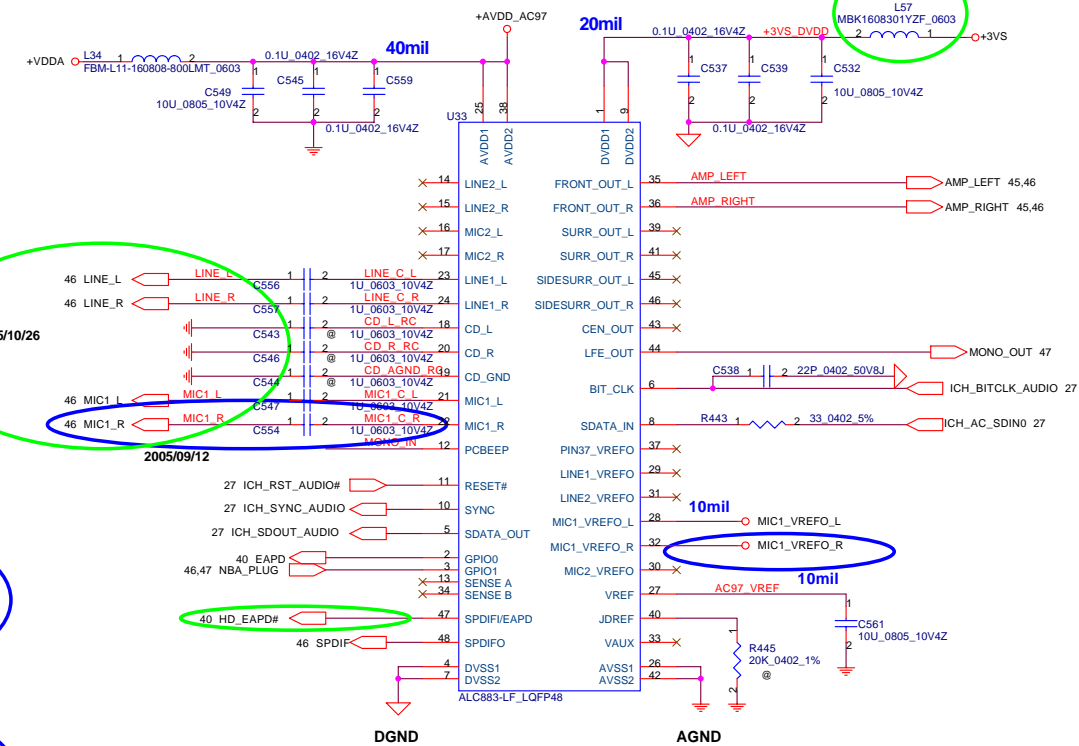
To TP/B Conn.



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Date: Friday, November 11, 2005			Sheet	43 of 59

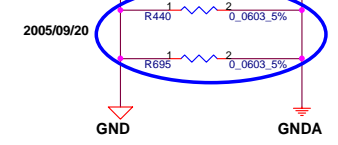
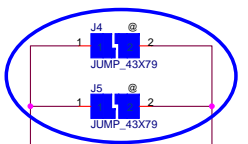


### HD Audio Codec

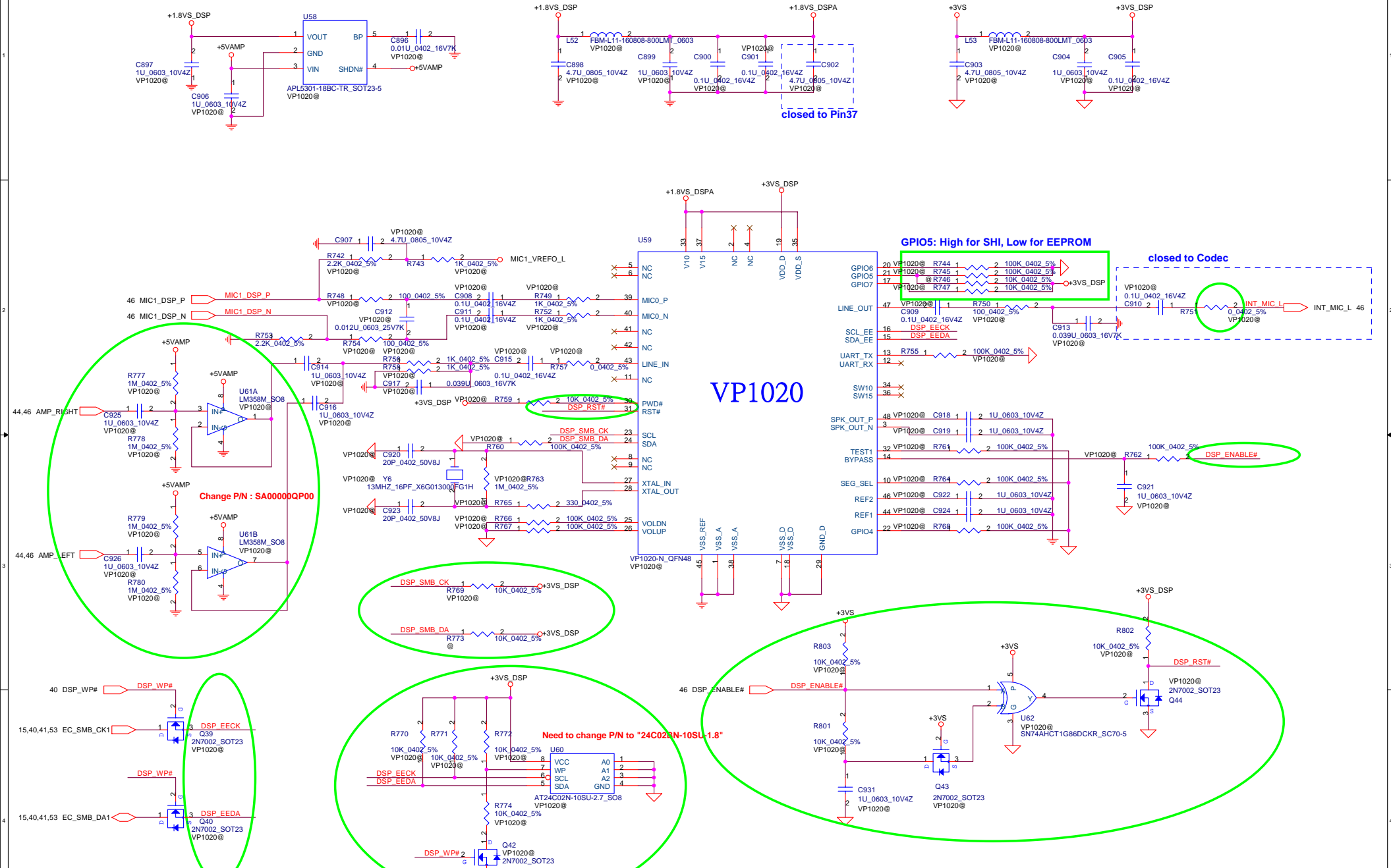


2005/10/26

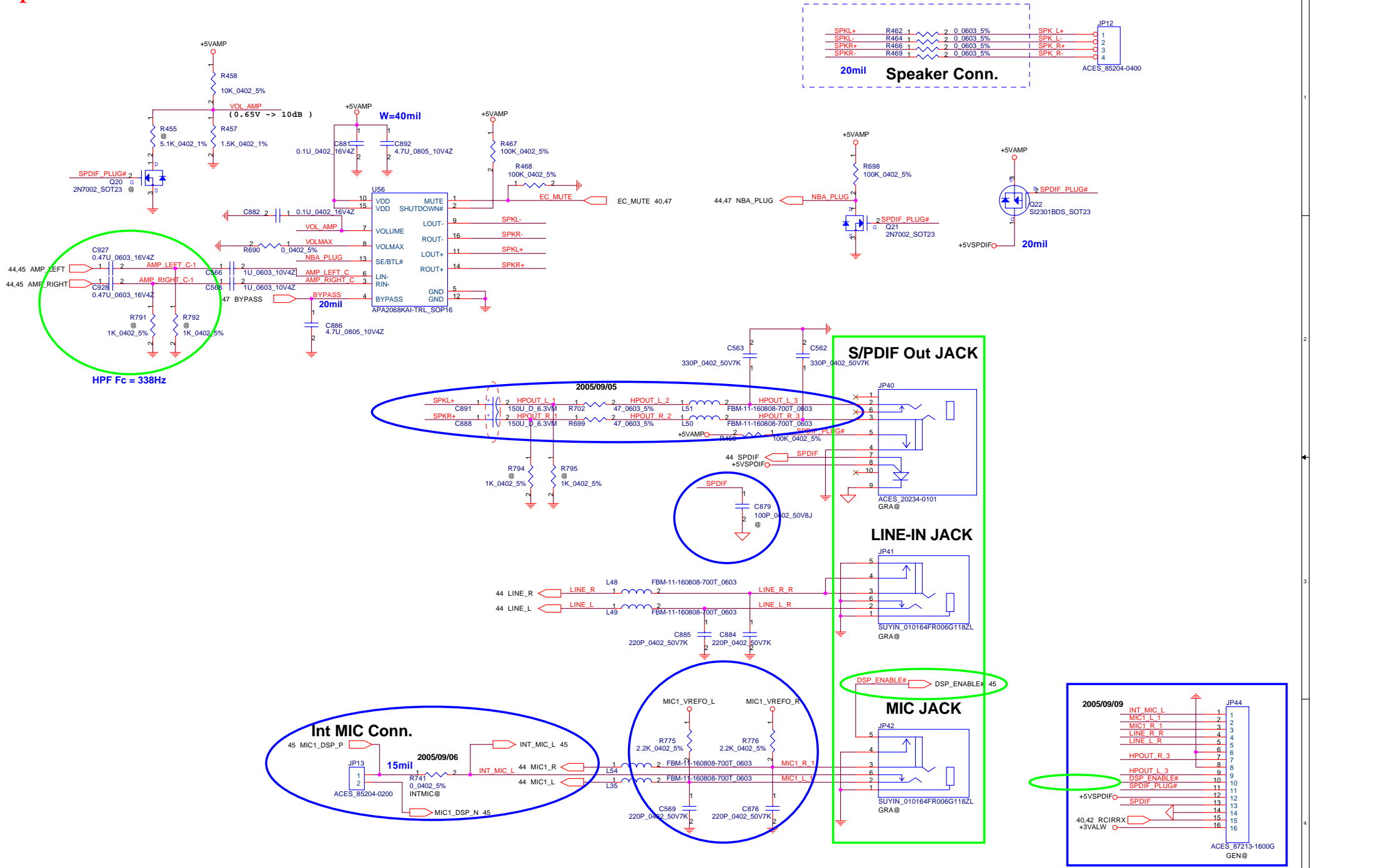
2005/09/12



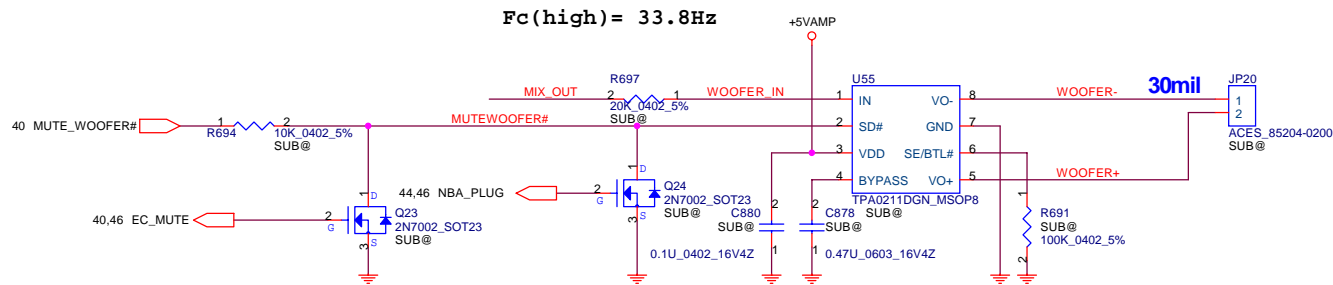
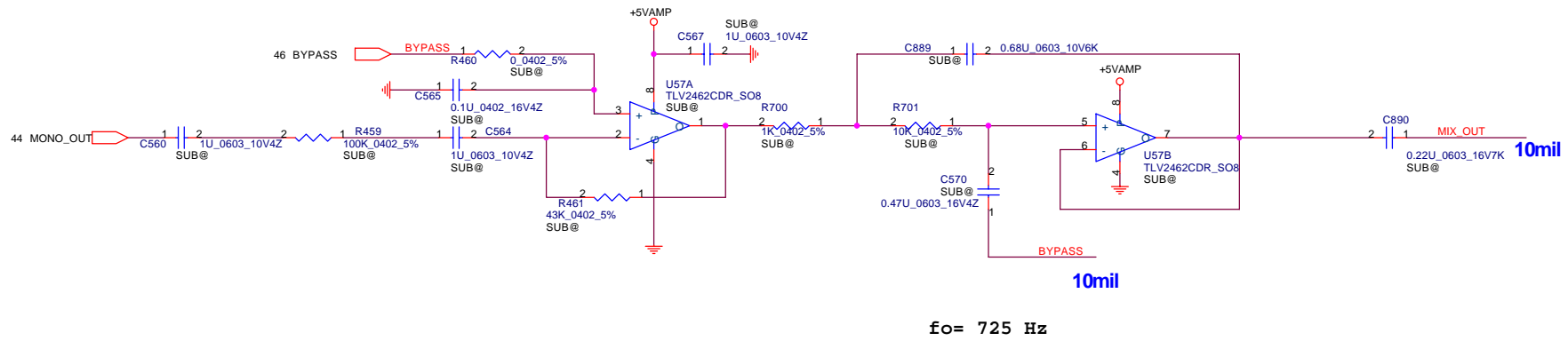
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	HD Audio Codec ALC883
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Date: Friday, November 11, 2005			Sheet 44 of 59	Rev 0.3



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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Echo Cancellation	
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				Date: Friday, November 11, 2005	Sheet 45 of 59

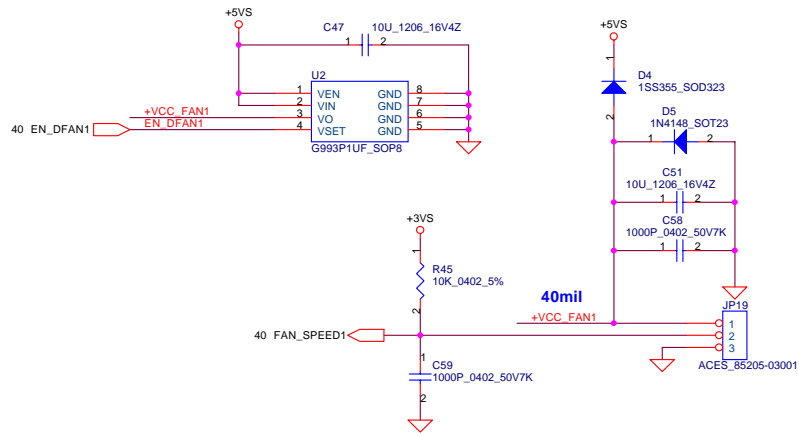


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Compal Electronics, Inc.			Amplifier & Audio Jack	
Size	Document Number		Rev	
B	HBL50 LA-2921P		0.3	
Date:	Friday, November 11, 2005	Sheet	46	of 59

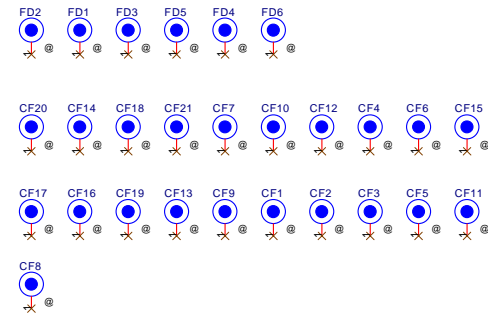
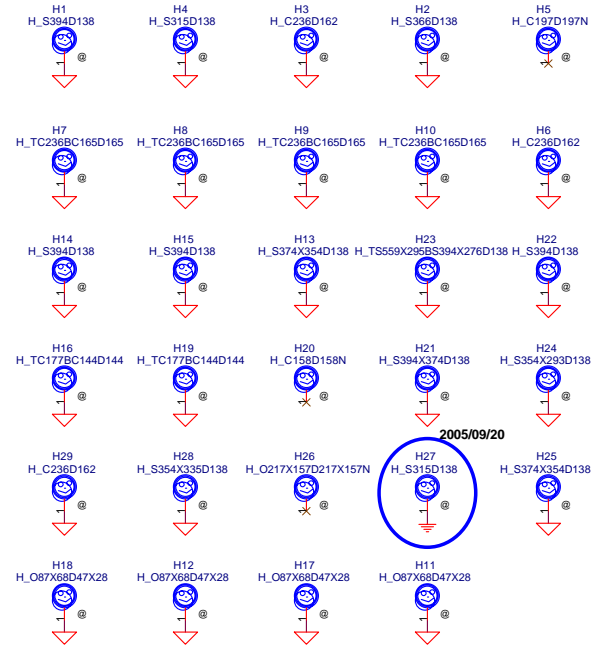
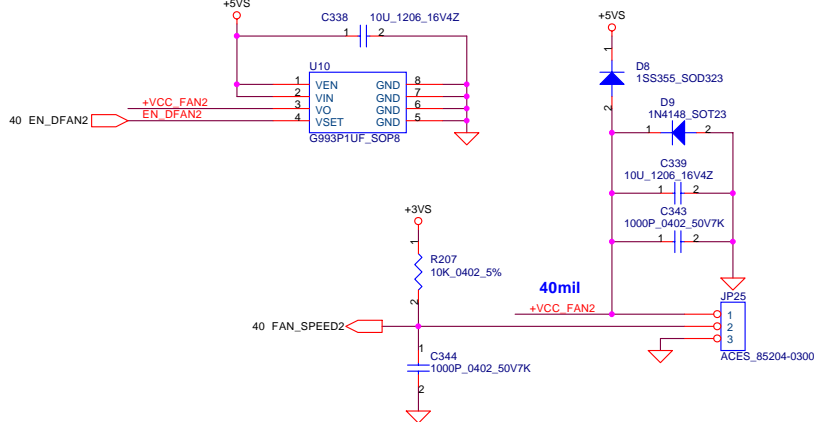


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Size	Document Number			Rev	
B	HBL50 LA-2921P			0.3	
Date:	Friday, November 11, 2005			Sheet	47 of 59

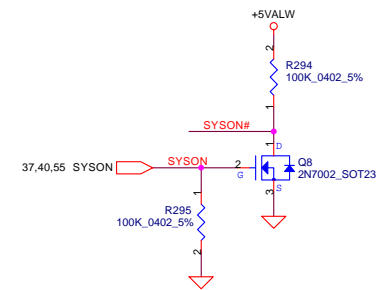
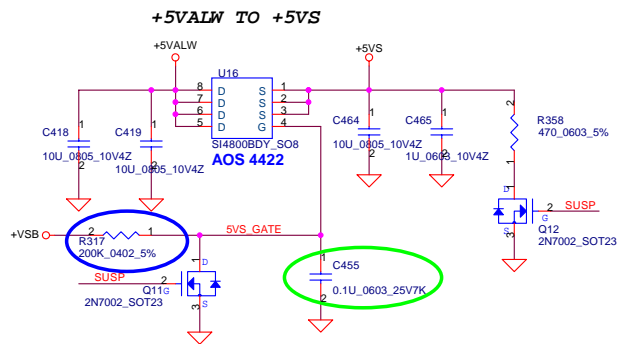
### FAN1 Conn



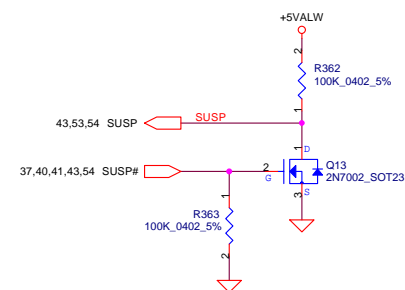
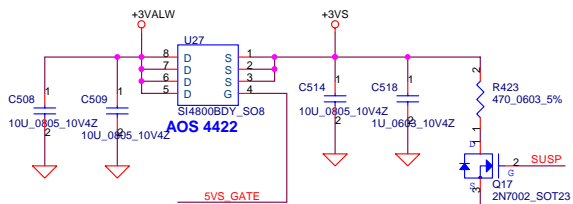
### FAN2 Conn



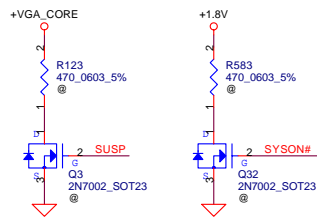
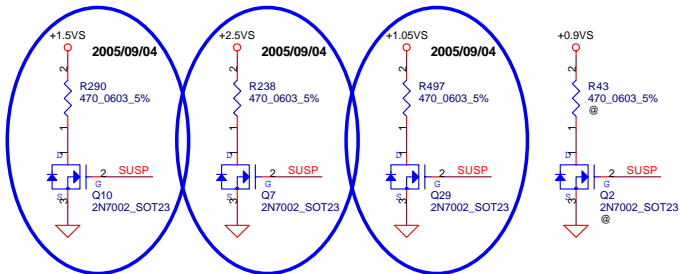
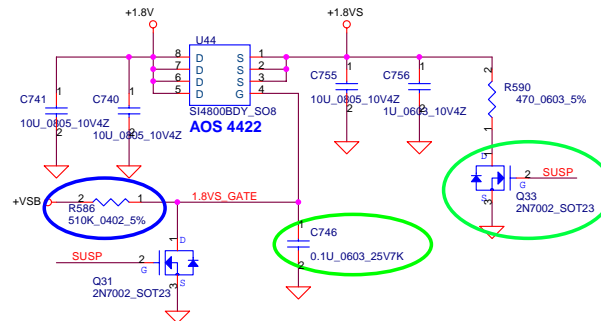
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Size	B	Date:	Friday, November 11, 2005	Rev. 0.3
		Sheet	48	of 59



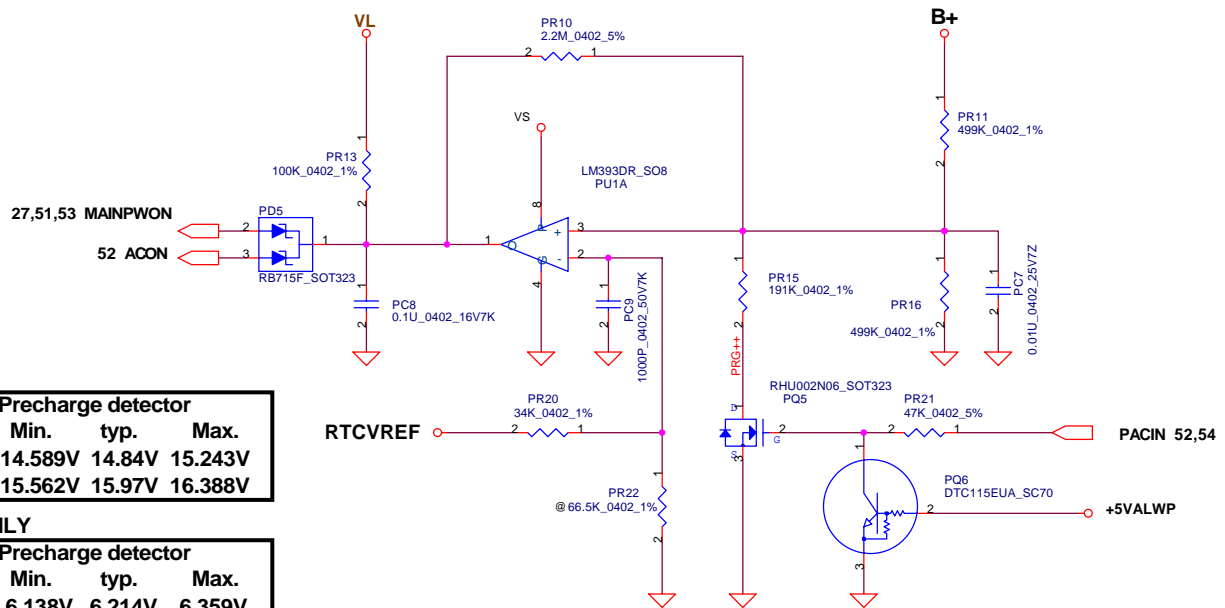
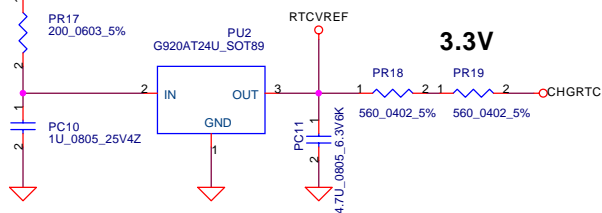
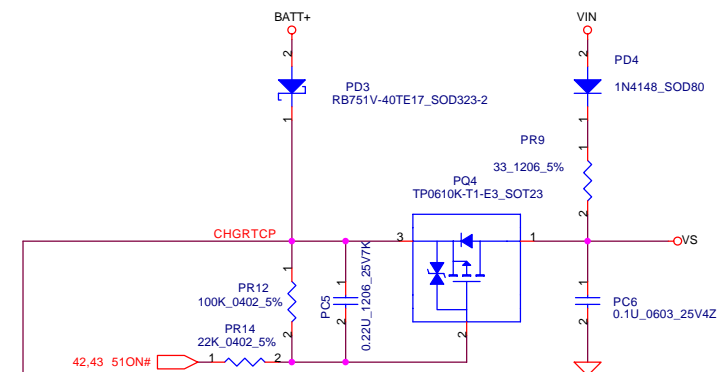
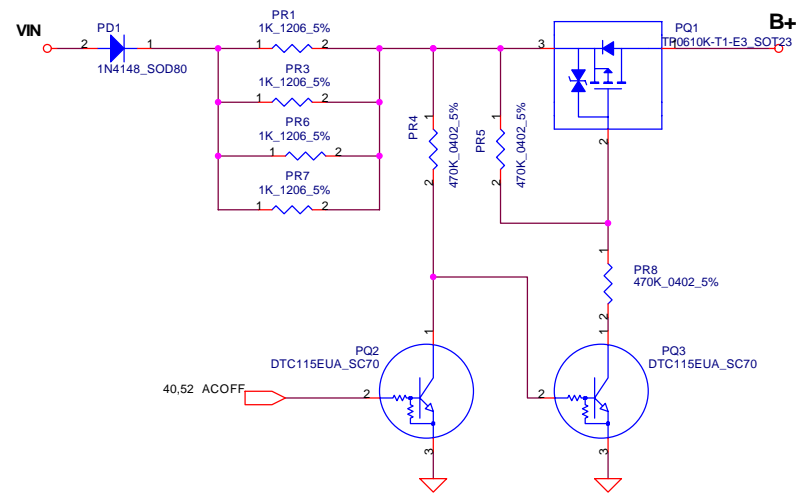
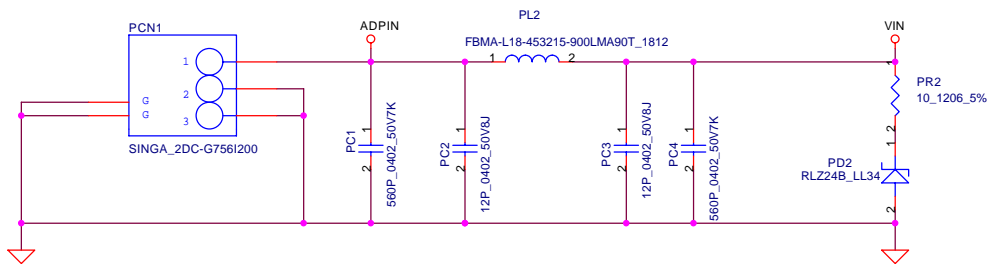
**+3VALW TO +3VS**



**+1.8V to +1.8VS**



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Document Number			Rev	
HBL50 LA-2921P			0.3	
Date: Friday, November 11, 2005				Sheet 49 of 59

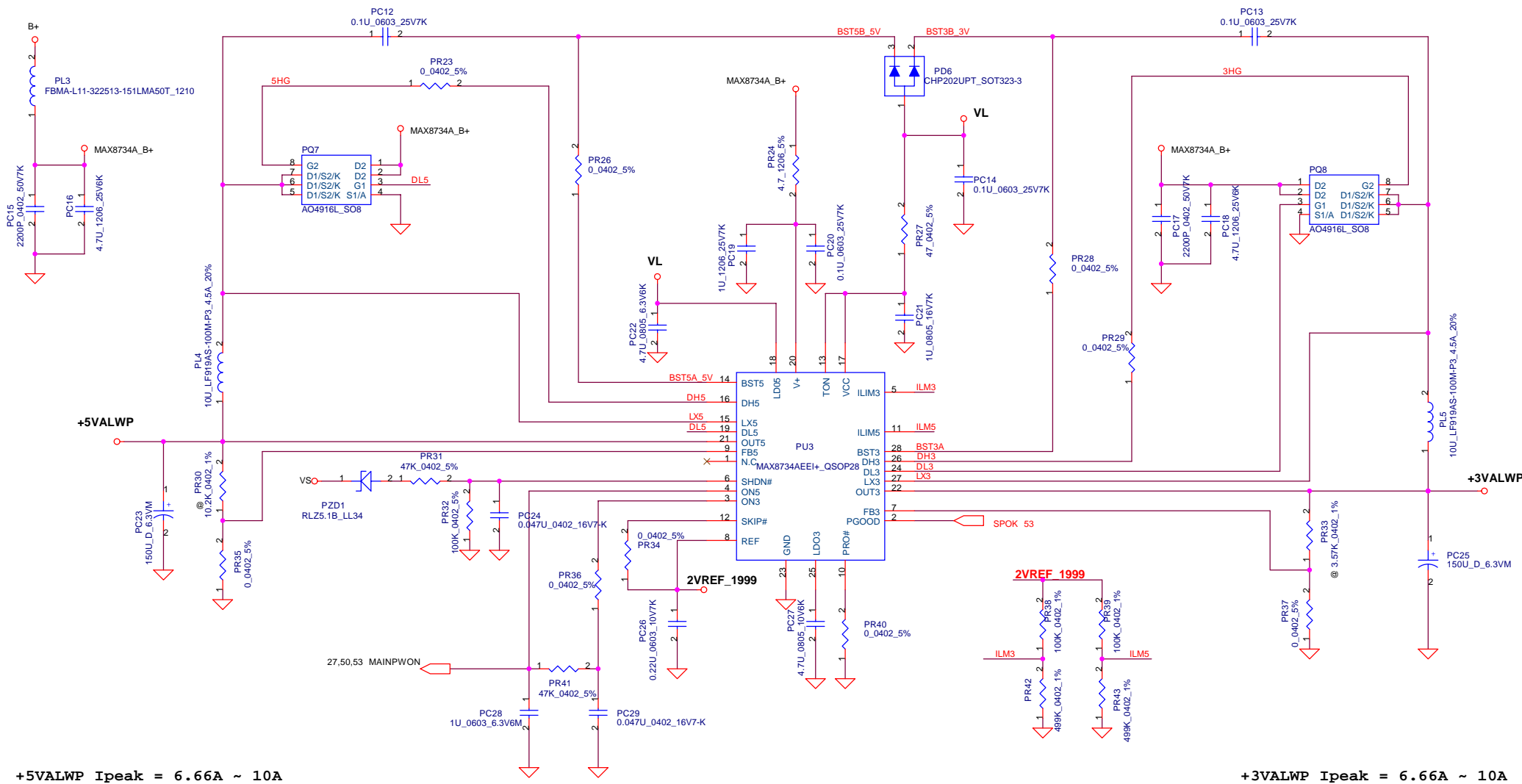


ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

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				HBL50 LA-2921P
				Rev 0.2
				Date: Friday, November 11, 2005
				Sheet 50 of 59

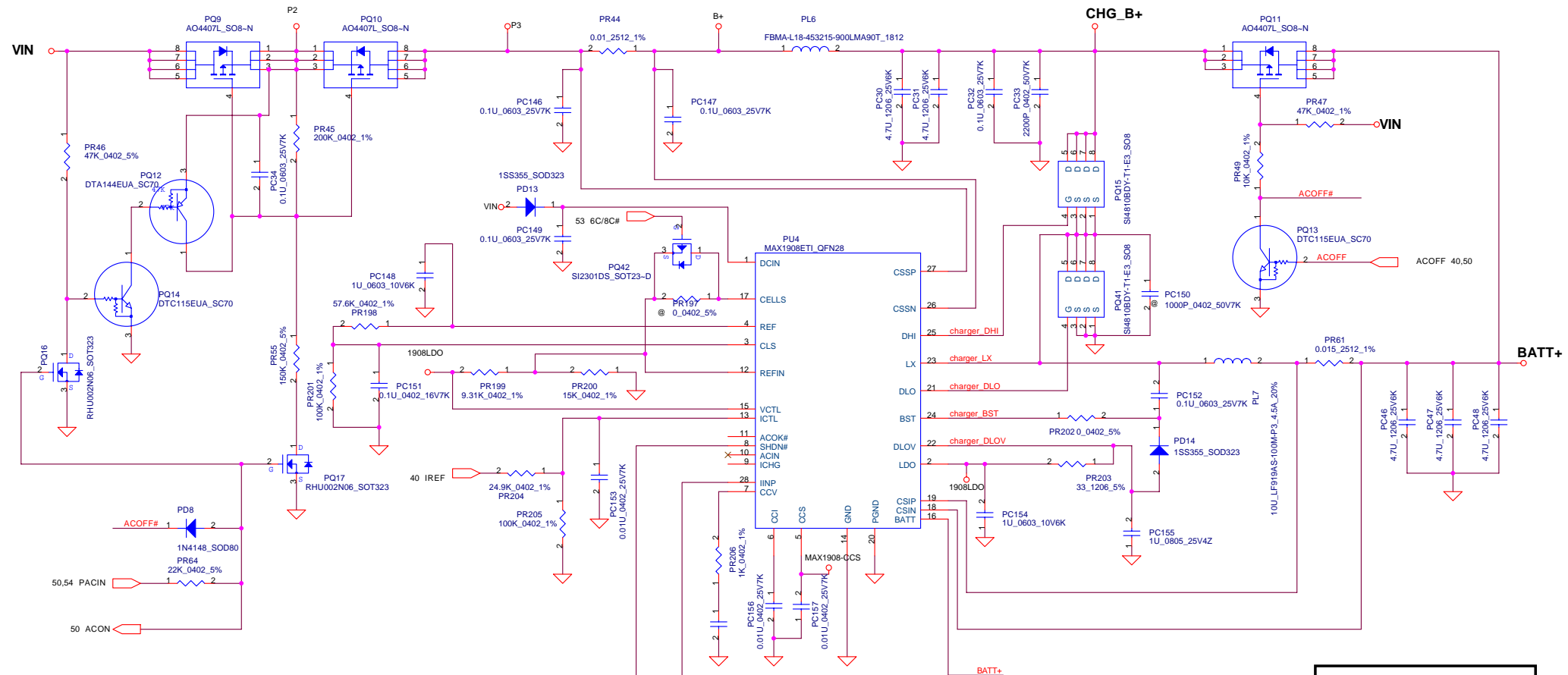


+5VALWP Ipeak = 6.66A ~ 10A

+3VALWP Ipeak = 6.66A ~ 10A

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Size	Document Number	HBL50 LA-2921P		Rev	0.2
Date:	Friday, November 11, 2005	Sheet	51	of	59

I<sub>adp</sub>=0~4.74A(90W)



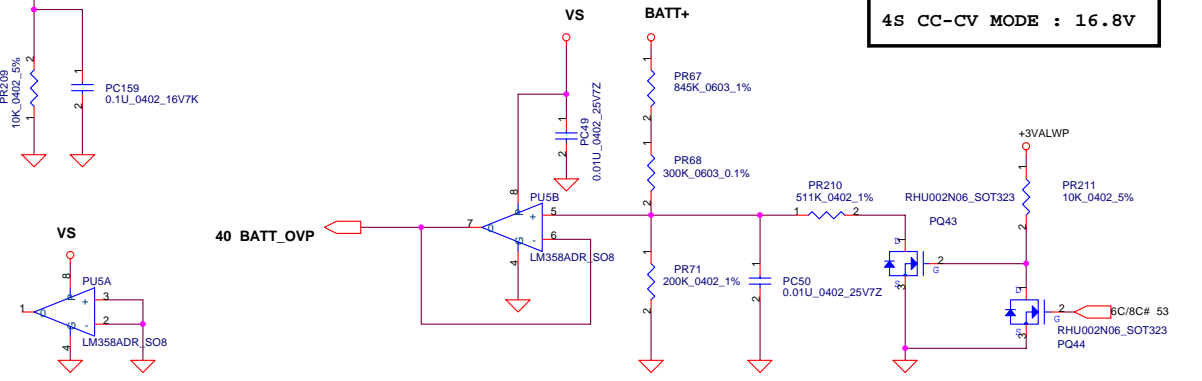
Charge voltage  
4S CC-CV MODE : 16.8V

LI-4S : 17.8V--BATT-OVP=1.9758V  
BATT-OVP=0.111\*BATT+

IREF=0.832\*Icharge  
IREF=0.73~3.3V

2P4S: 4800mAh/cell  
0.8C=3.84A

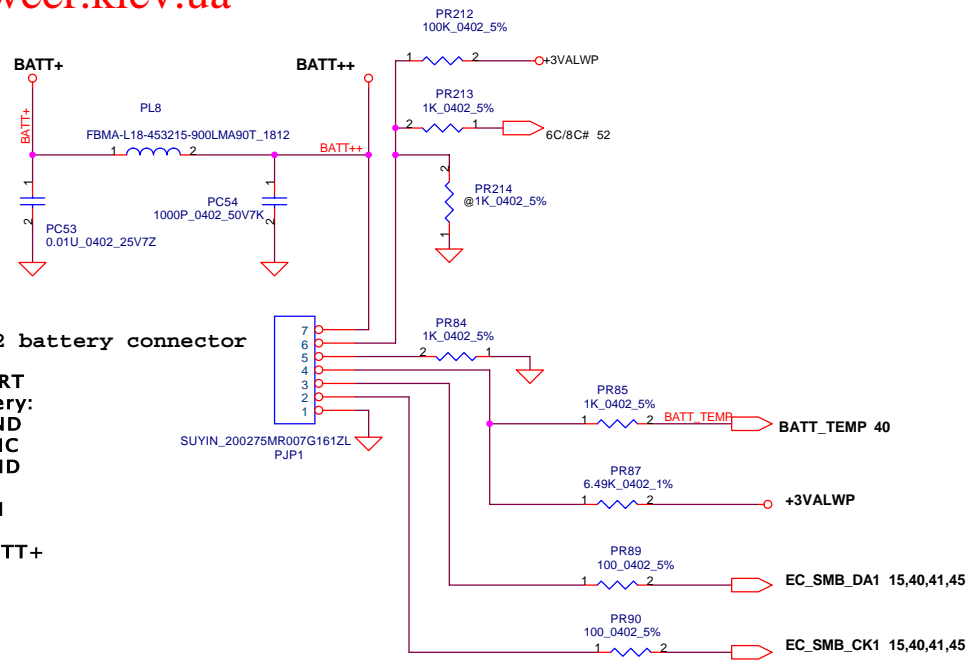
OVP voltage :  
LI-3S : 17.8V---BATT-OVP=1.9758V  
BATT-OVP=0.111\*BATT+



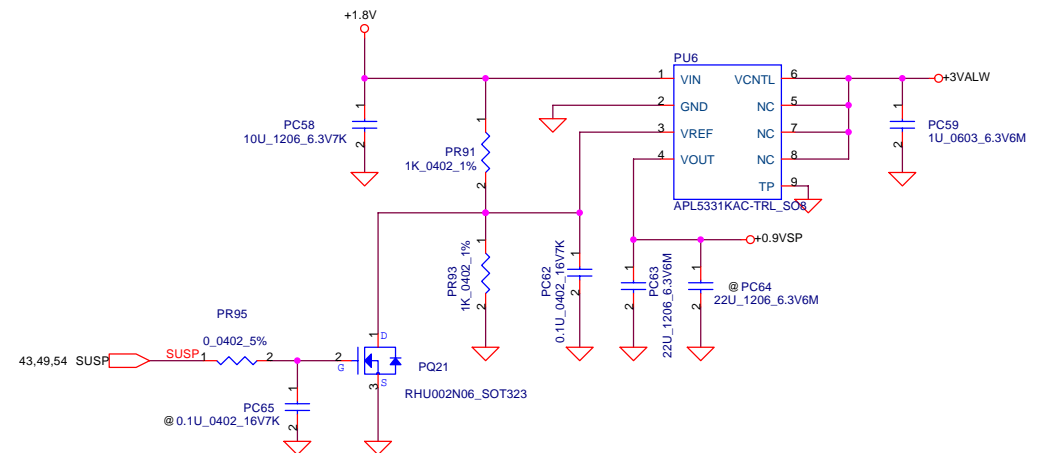
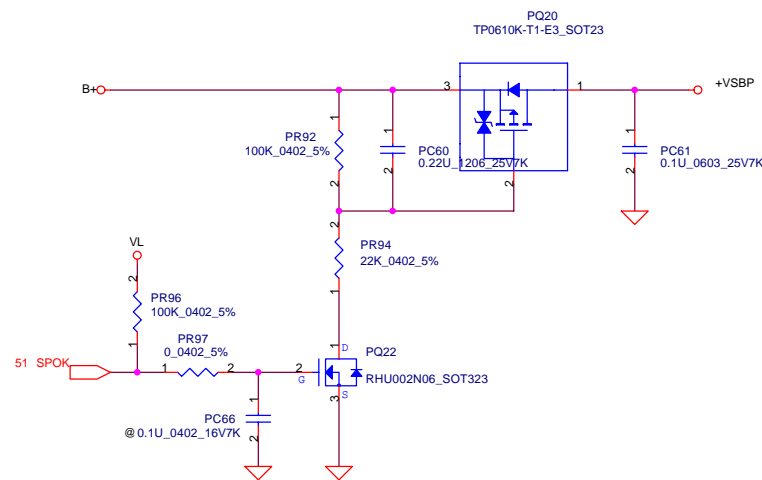
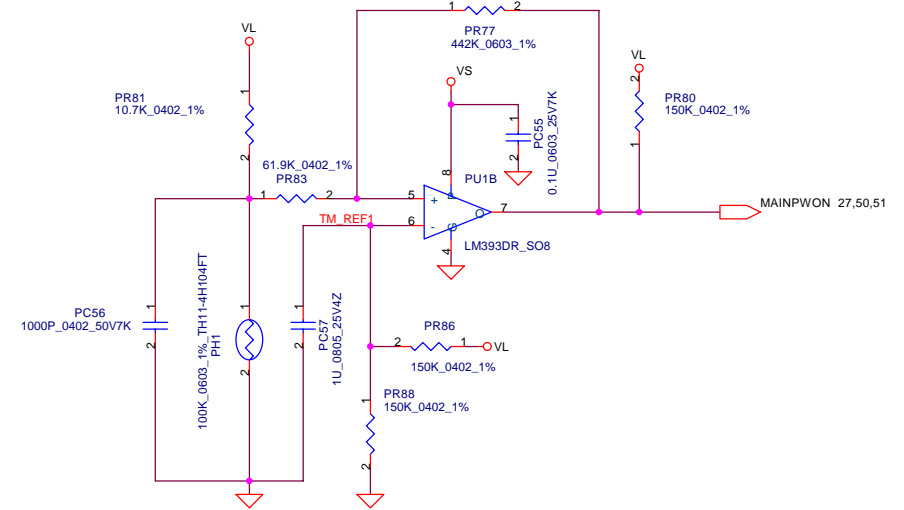
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Compal Electronics, Inc.			Charger
Size B	Document Number	Rev 0.2	
HBL50 LA-2921P		Date: Friday, November 11, 2005 Sheet 52 of 59	

**PJP2 battery connector**

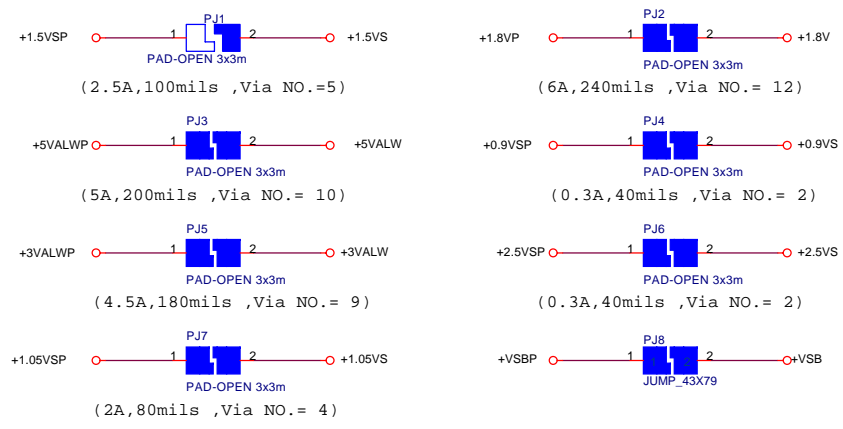
- SMART Battery:**  
 1.GND  
 2.SMC  
 3.SMD  
 4.TS  
 5.B/I  
 6.ID  
 7.BATT+



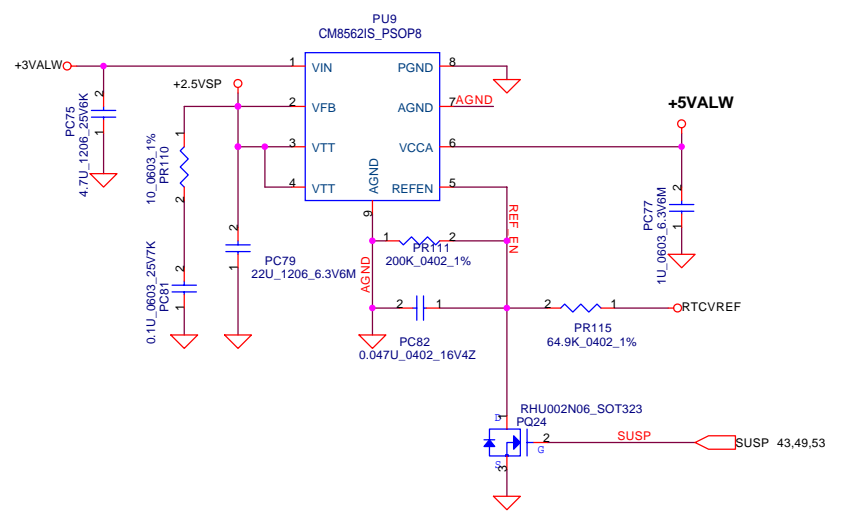
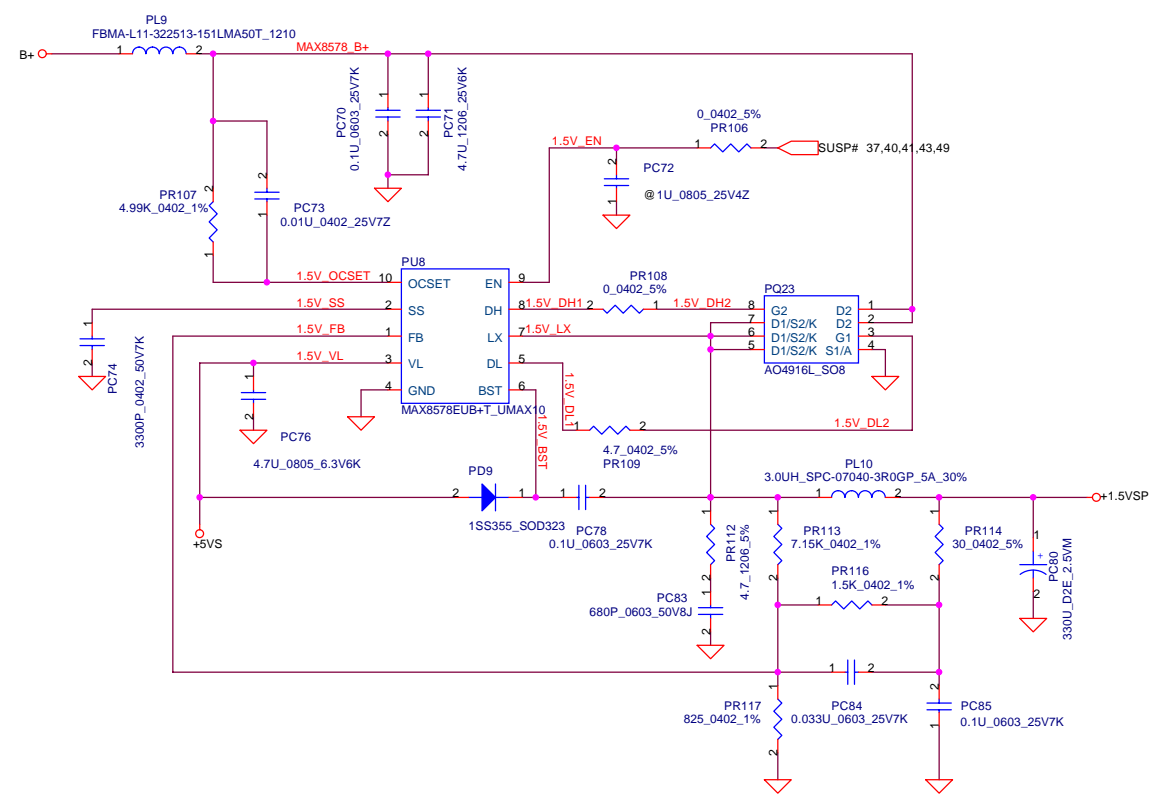
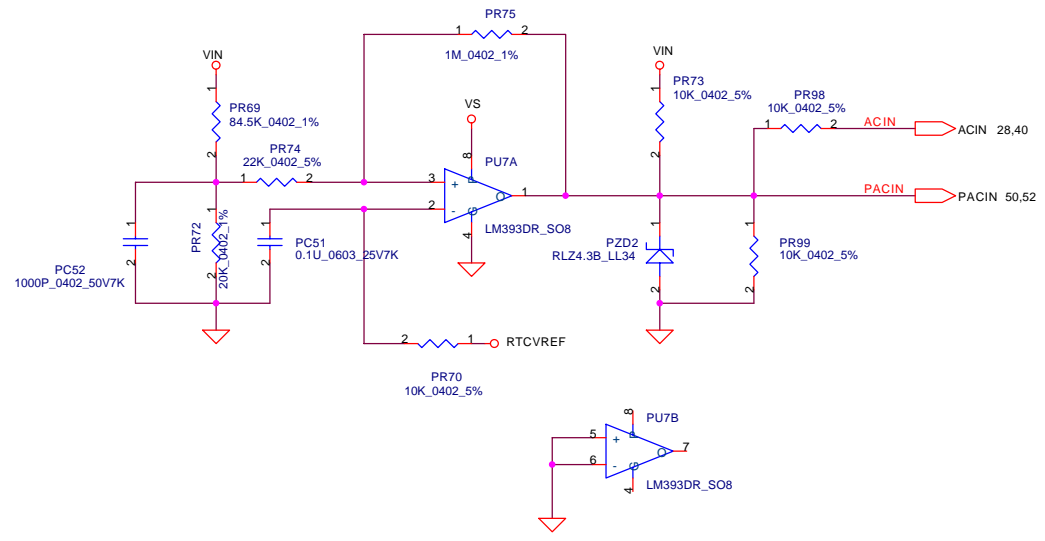
**PH1 under CPU bottom side :**  
 CPU thermal protection at 80 degree C  
 Recovery at 44(45) degree C



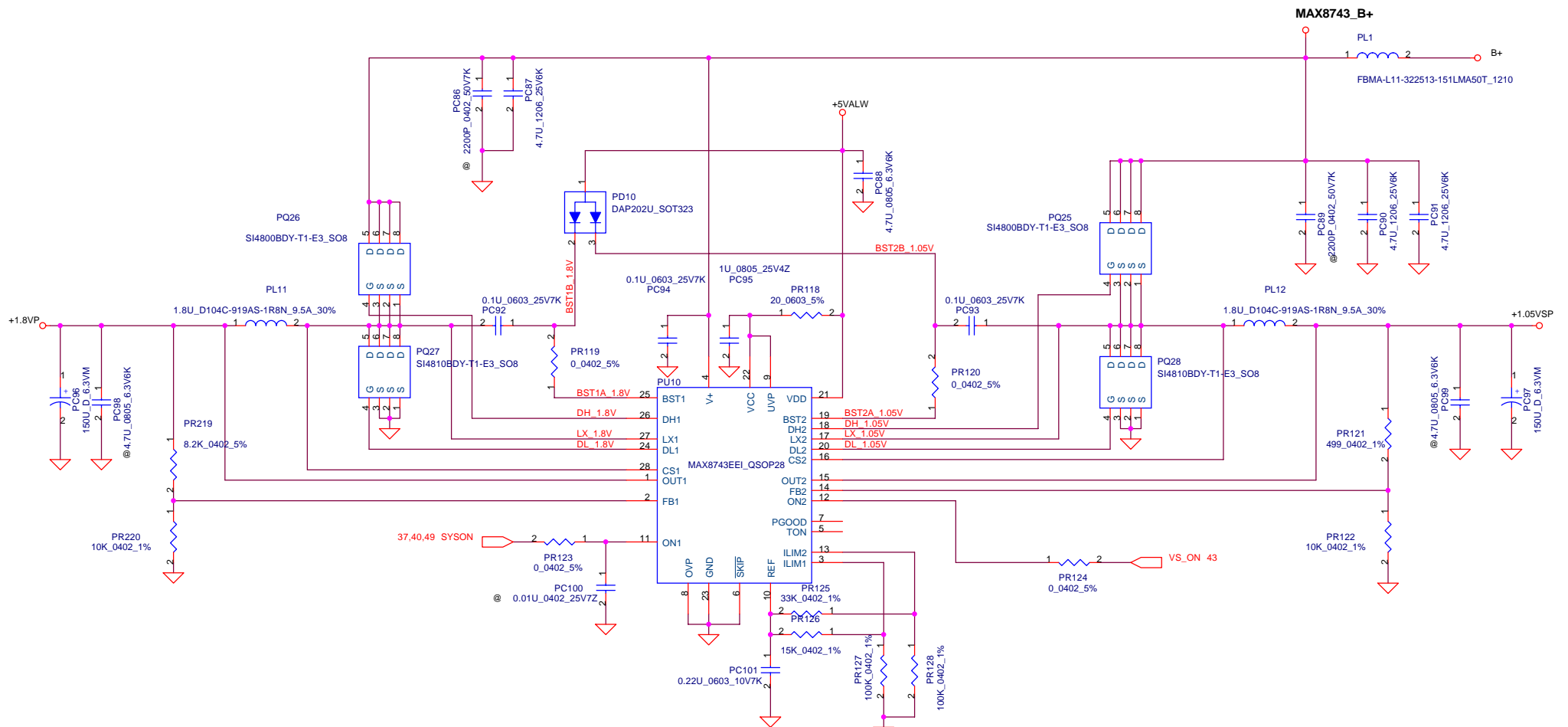
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Size B	Document Number		HBL50 LA-2921P		Rev	0.2
Date:	Friday, November 11, 2005	Sheet	53	of	59	



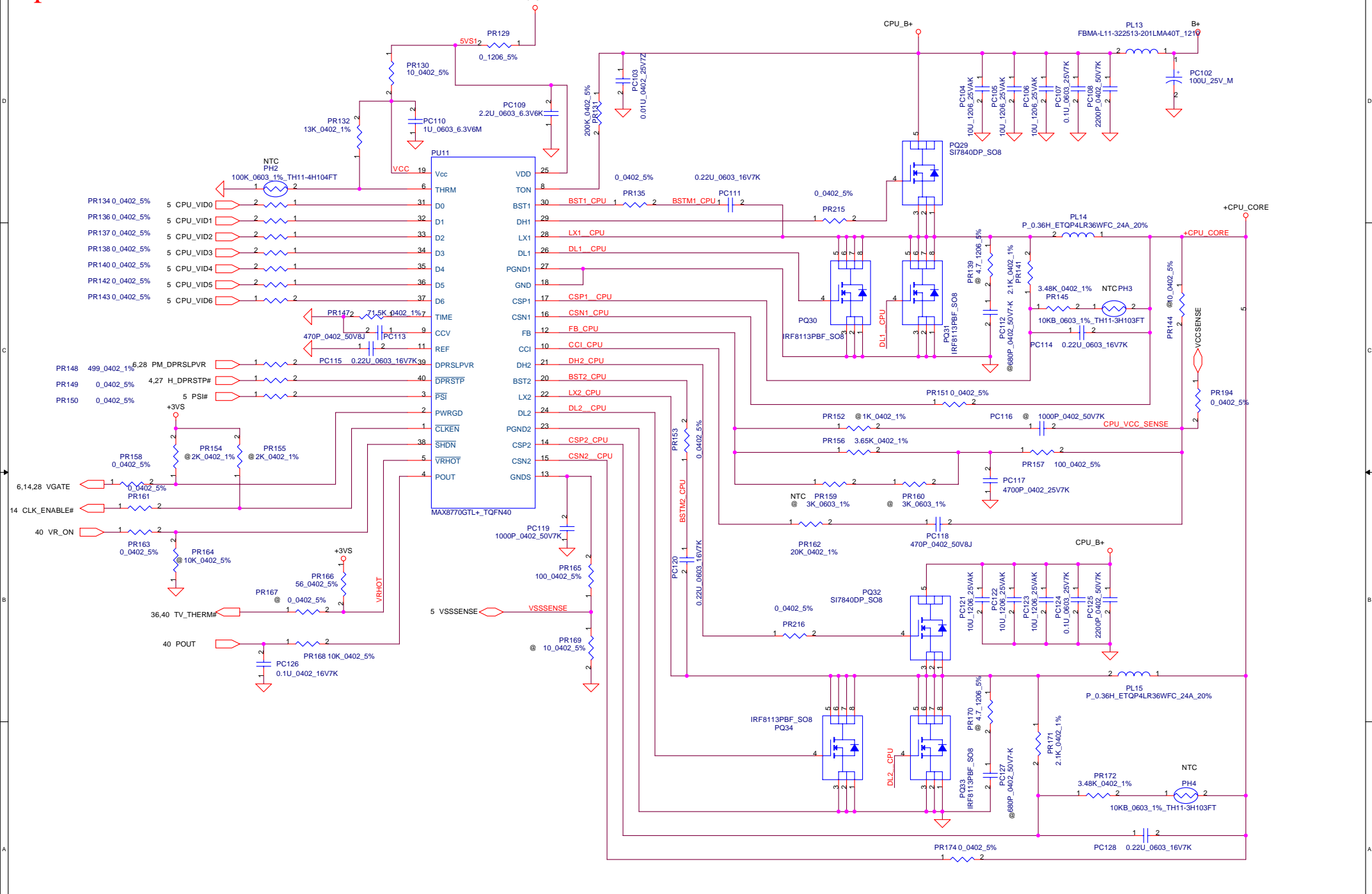
**Vin Detector**  
17.90V/17.24V



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Size	Document Number	HBL50 LA-2921P		Rev	0.2
Date:	Friday, November 11, 2005	Sheet	54	of	59

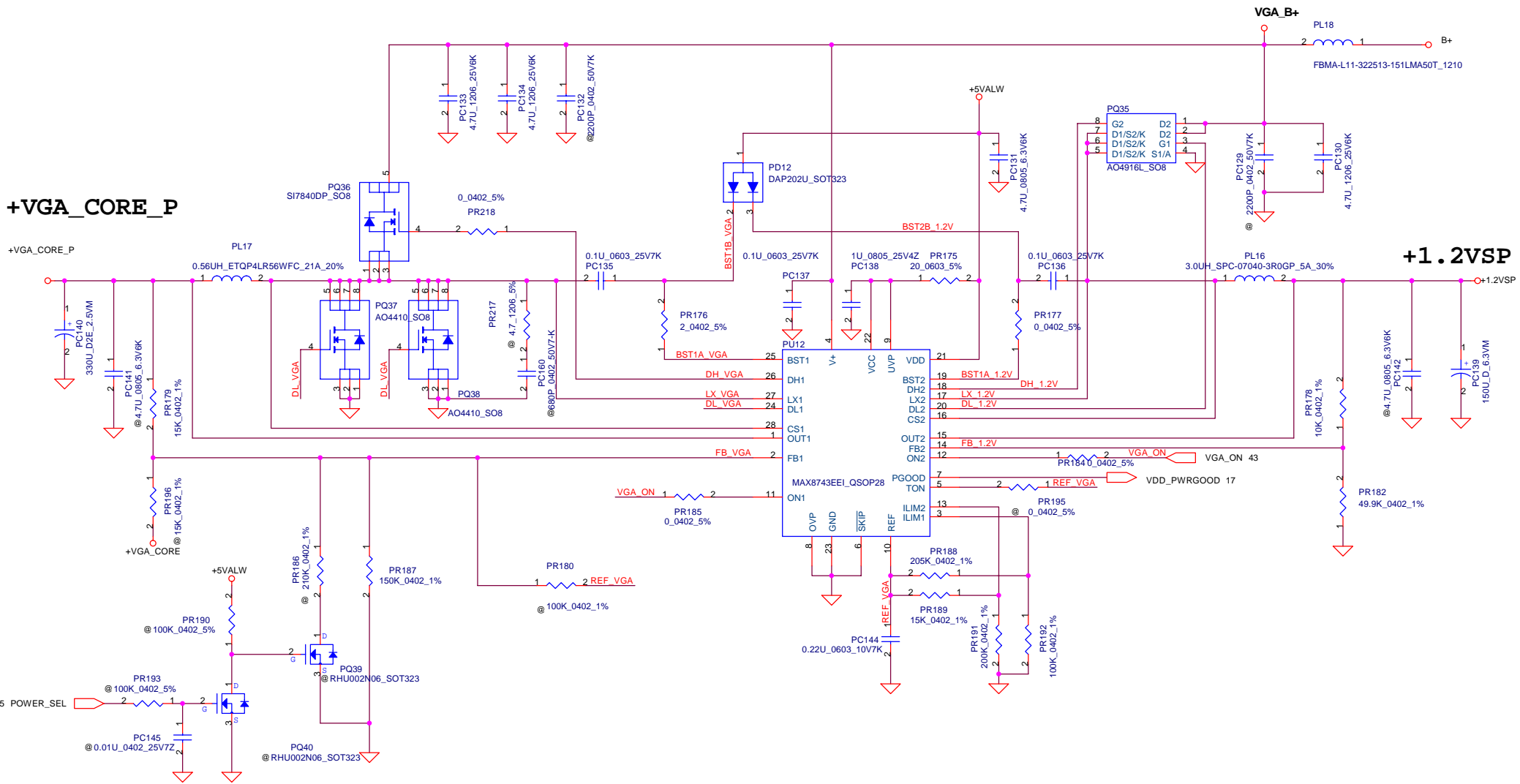


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				HBL50 LA-2921P	
				Date:	Friday, November 11, 2005
				Sheet	55 of 59
				Rev	0.2



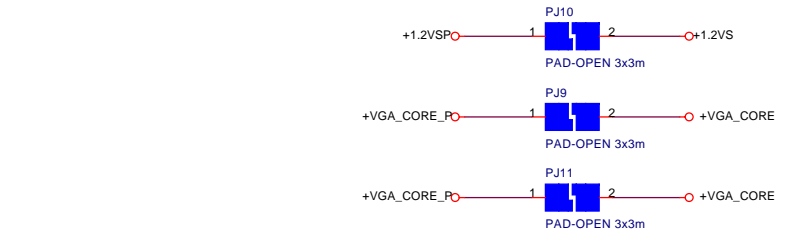
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Title	+CPU_CORE			
Size	Document Number	HBL50 LA-2921P		Rev
Custom			56	0.2
Date:	Friday, November 11, 2005	Sheet	56 of 59	

POWER_SEL	H	L
+VGA_CORE FOR G73.	+0.95V (VGA@+G72@)	+1.025V
+VGA_CORE FOR G72.	+1.1V (VGA@)	



**+VGA\_CORE\_P**

**+1.2VSP**



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Compal Electronics, Inc.			
Title: <b>+VGA_CORE_P/+1.2VSP</b>			
Size B	Document Number	Rev	
	<b>HBL50 LA-2921P</b>	0.2	
Date:	Friday, November 11, 2005	Sheet	57 of 59

**A --> B Change List**

1. Page06 : No stuff R100 10K\_0402\_5%
2. Page09 : Add C49 & C887 220U\_D2\_4VM
3. Page10 : No stuff R57 2.2K\_0402\_5%
4. Page14 : Add R711 10K\_0402\_5% to set 96MHz output  
Change Q14 & Q15 pin1 net name to connect to ICH7M  
Change U19 ICS9LPRS325CKLFT part number to SA00000RE20
5. Page15 : Change C663, C664 from 22P\_0402\_50V8J to 18P\_0402\_50V8J.
6. Page18 : Modify VGA Device ID for G72MV & G73.
7. Page24 : Change VGA\_DDC\_CLK & VGA\_DDC\_DATA to Q26 & Q27 Level shift.  
Add R781 & R782 4.7K\_0402\_5%  
Change C589, C596, C583, C587, C594, C585 to 150P\_0402\_50V8J
8. Page28 : Change SB\_INT\_FLASH\_SEL# from ICH7M GPIO38 to GPIO33.
9. Page29 : Change C437 from 0.1U\_0402\_16V4Z to 1U\_0402\_6.3V4Z
10. Page30 : Change PATA HDD+ODD select resistor form RP to R\_0402 (0\_0402\_5%)
11. Page34 : Stuff R175 & no stuff R182 (0\_0402\_5%) for BCM4401E/BCM5789M/BCM5787M
12. Page35 : Modify LAN\_ACTIVITY# & LAN\_LINK# LED color
13. Page 36 : Add JP38 & C895 for CAMERA.  
Swap JP17 PCIE TX & RX Signal.  
Swap JP30 PCIE TX & RX Signal.
14. Page37 : Connect JP34 SMBus interface to ICH7M  
Change JP4 & JP5 USB connector to BOTTOM.
15. Page38 : Add 1394 @ BOM Structure.
16. Page41 : Delete LCM interface Extension I/O.  
No stuff R390 & Stuff R418 for Flash ROM interface.
17. Page42 : Change JP11 from 34 pin to 24 pin.  
Change SW8 & SW9.  
Add JP37.
18. Page43 : Change U28 Part Number.  
Change SW1 Part Number.  
Change R425 from 10K\_0402\_5% to 62K\_0402\_1%  
Change R422 from 10K\_0402\_5% to 62K\_0402\_1% & add C513 0.1U\_0402\_16V4Z
19. Page44 : Add C554 for MIC\_R  
Add R440, R695 (0\_0603\_5%) & J4, J5 for EMI request.
20. Page45 : Add Echo Cancellation function.
21. Page46 : Correct Headphone L & R signal.  
Reserved C879 for EMI request  
Modify MIC Jack circuit. add R741, R775, R776, L54, C876  
Change JP44 from 14 pin to 16 pin
22. Page48 : H27 connect to GNDA.
23. Page49 : Add R290, R238, R497, Q10, Q7, Q29  
Change R317 to 200K\_0402\_5%  
Change R586 to 510K\_0402\_5%

**B --> C Change List**

1. Page05 : No stuff C608, C614
2. Page12 : Change JP22 Footprint
3. Page14 : Change R620 from 2K\_0402\_5% to 10K\_0402\_5% & add Q38
4. Page15 : Delete DVI pull high resistor
5. Page17 : AddC96 330U for +VGA\_CORE
6. Page18 : Modify PEX\_CFG[0..2] setting from 02 to 01.
7. Page30 : Delete R395 & C486, add R394 for SATA bridge reset timing  
Modify SATA HDD connector library
8. Page31 : Delete IDE\_CD\_L, IDE\_CD\_R & CD\_GNDA
9. Page34 : Add R783, R784, R785 for BCM5787M, stuff R214 when use BCM4401E,  
Del R168, change Q5 P/N
10. Page36 : Add +3VS, GND at JP30 for 3G device
11. Page38 : No stuff U14, R253, R246 & stuff R261
12. Page40 : Reserved R793 for ALC883 pin47 EAPD, & define KB910 Pin174 as EC\_PWROK
13. Page41 : No stuff U21, U30, C490, R391, R390, R388 & stuff R418
14. Page42 : Modify SW9 Pin1, Pin5 as NC, no stuff C7
15. Page43 : Modify Power OK circuit. add R790 for EC\_PWROK, reserved Q41, R420, C512  
add D35, D37, Change BATT1 P/N to SP093PA0200
16. Page44 : Delete ALC883 CD input circuit, add HD\_EAPD# signal
17. Page46 : Add C927, C928, reserved R791, R792
18. Page49 : Stuff Q33

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				B	HBL50 LA-2921P
				Date:	Friday, November 11, 2005
				Sheet	59 of 59
				Rev	0.3