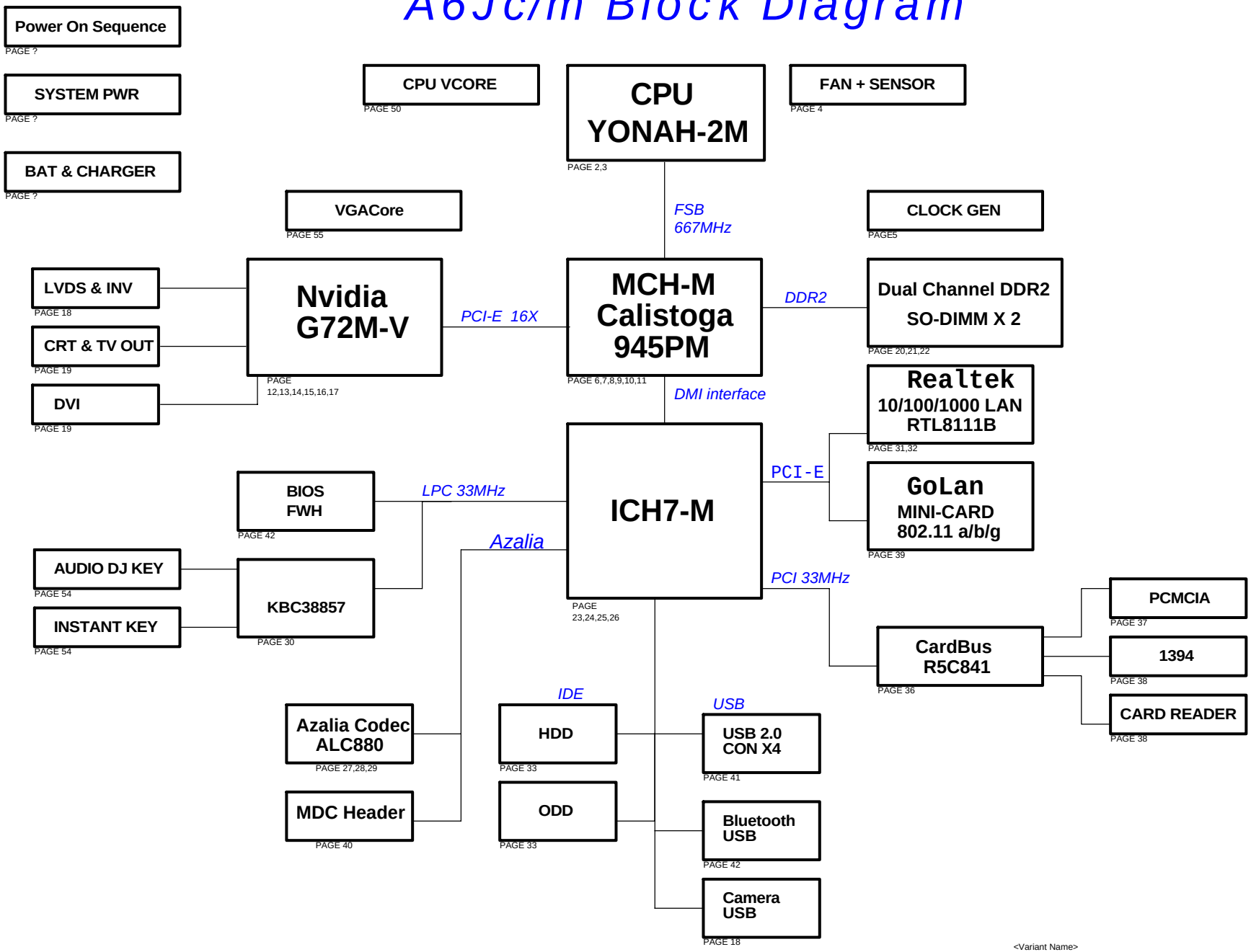
A6Jc/m Block Diagram



http://konweer.kiev.ua

<Variant Name>

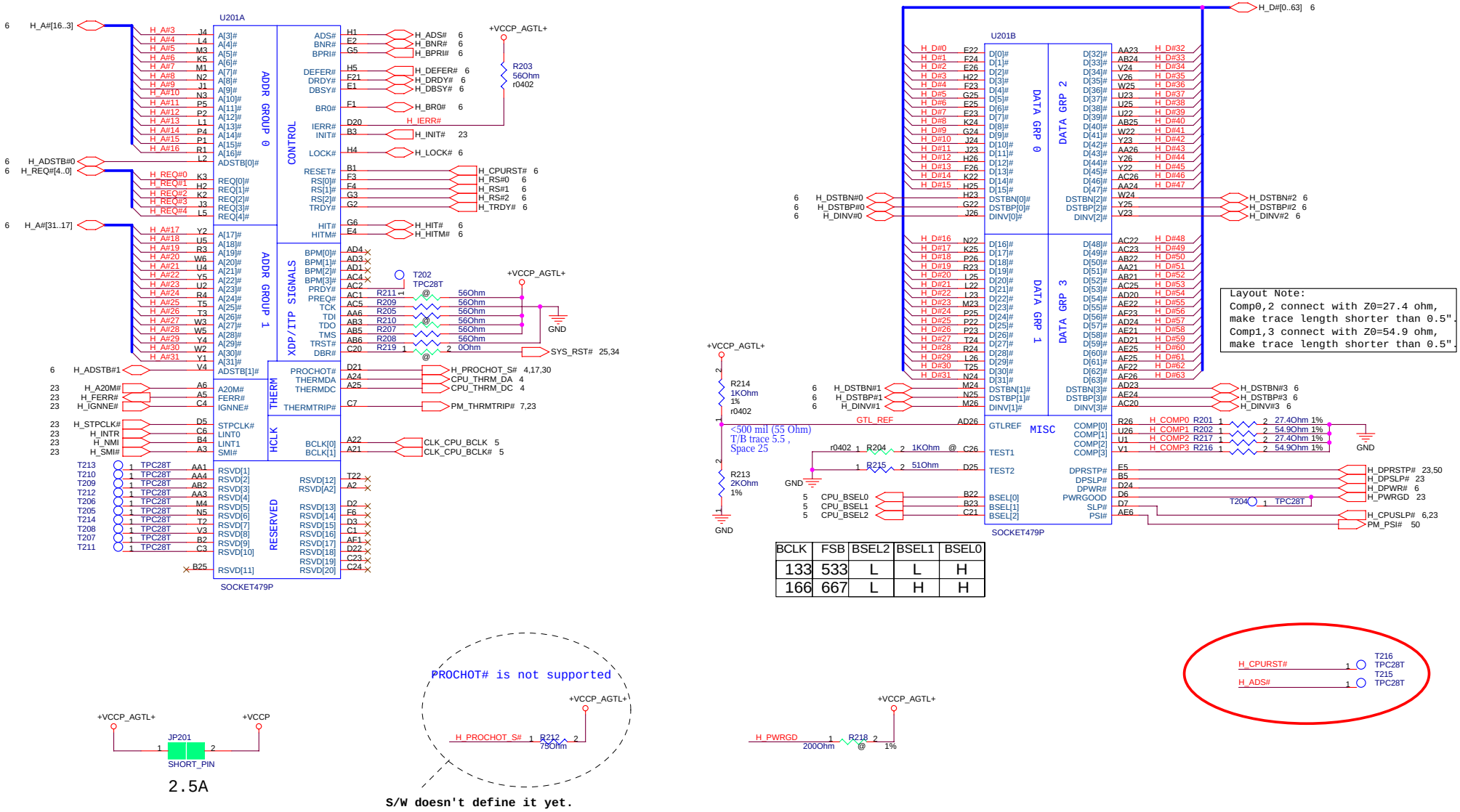
Title : BLOCK DIAGRAM

Engineer: Marco Chen

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 1 of 63



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

http://konweer.kiev.ua

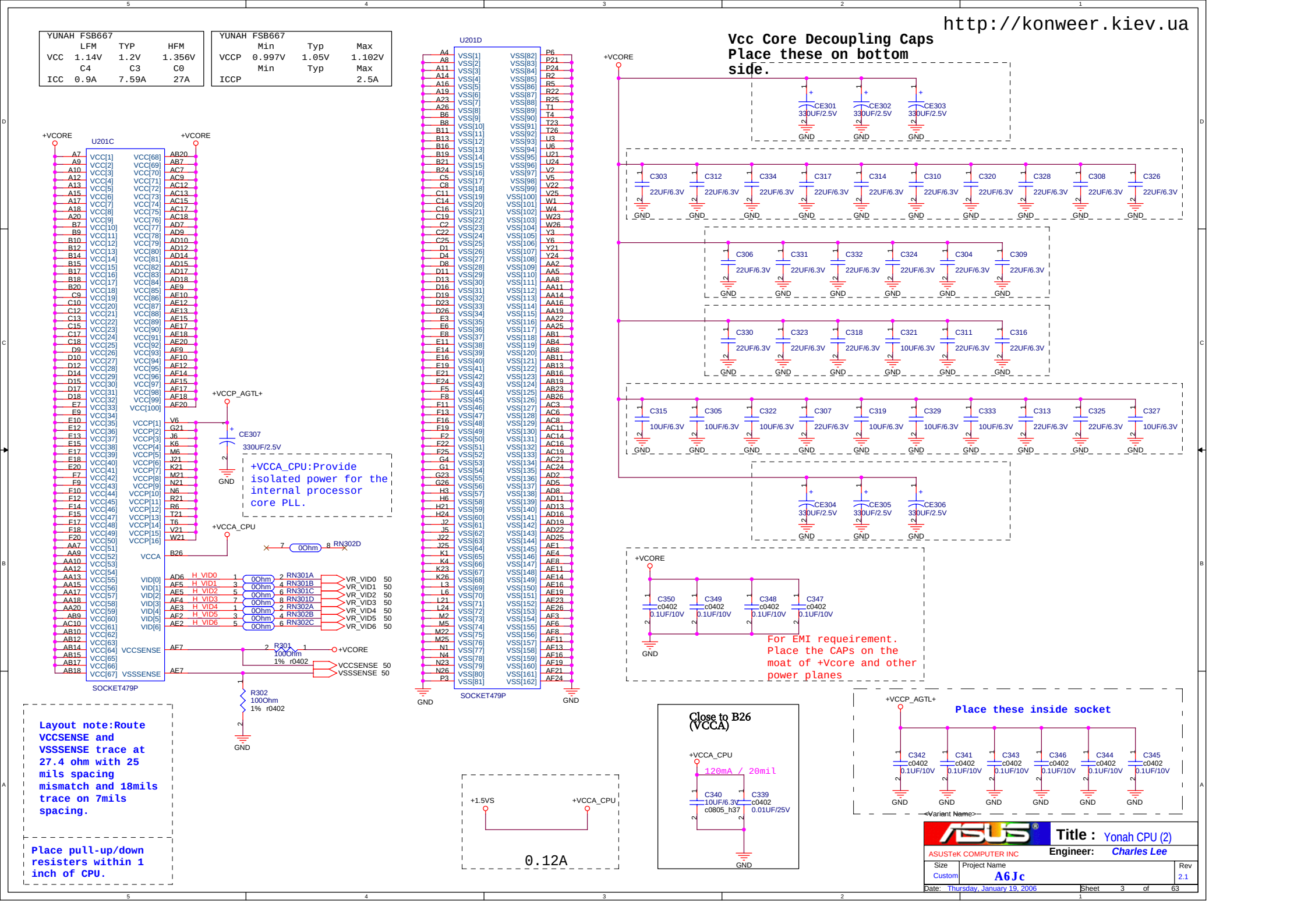
<Variant Name>

Title : YONAH CPU (1)

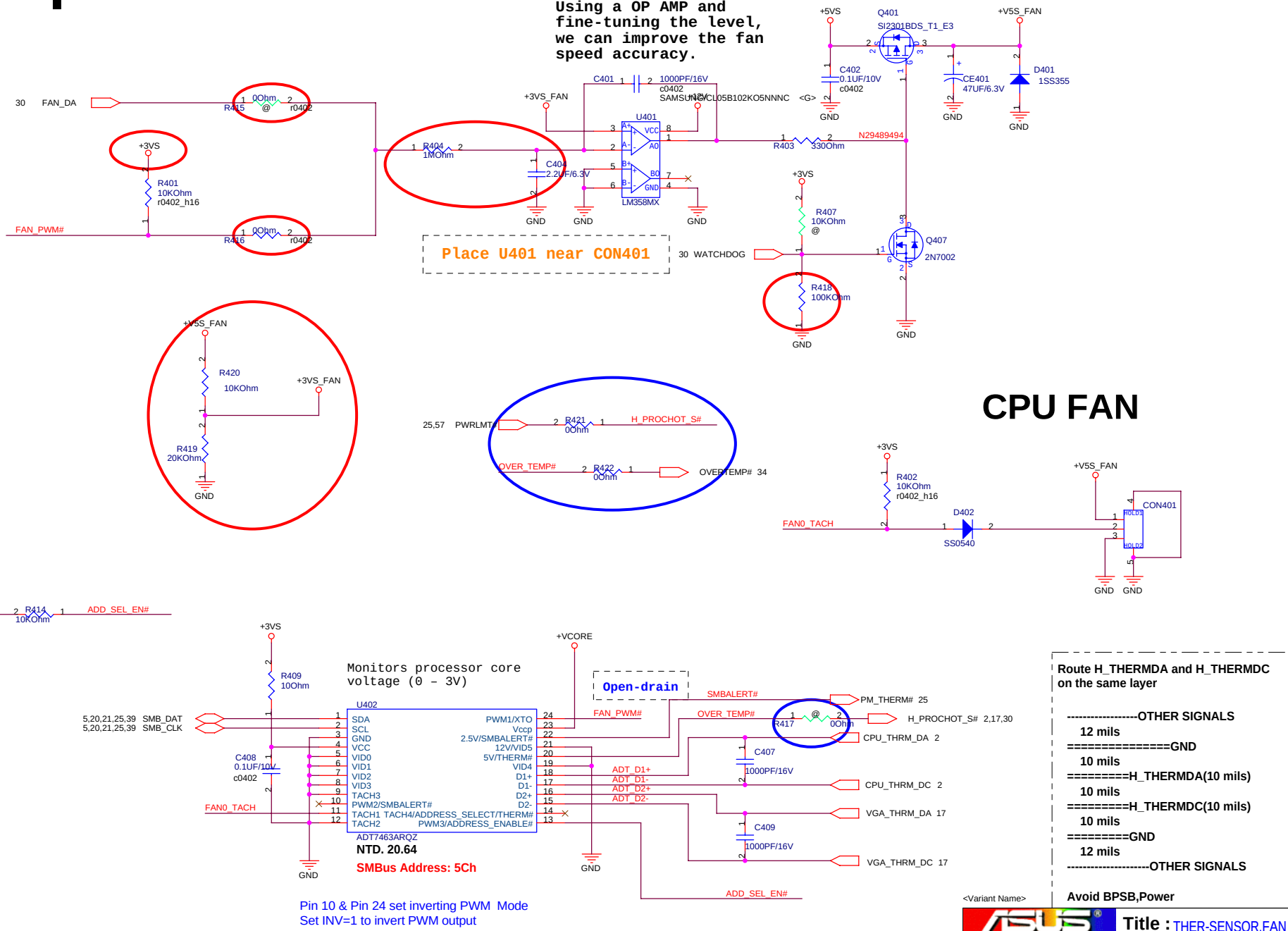
ASUSTeK COMPUTER INC Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 2 of 63

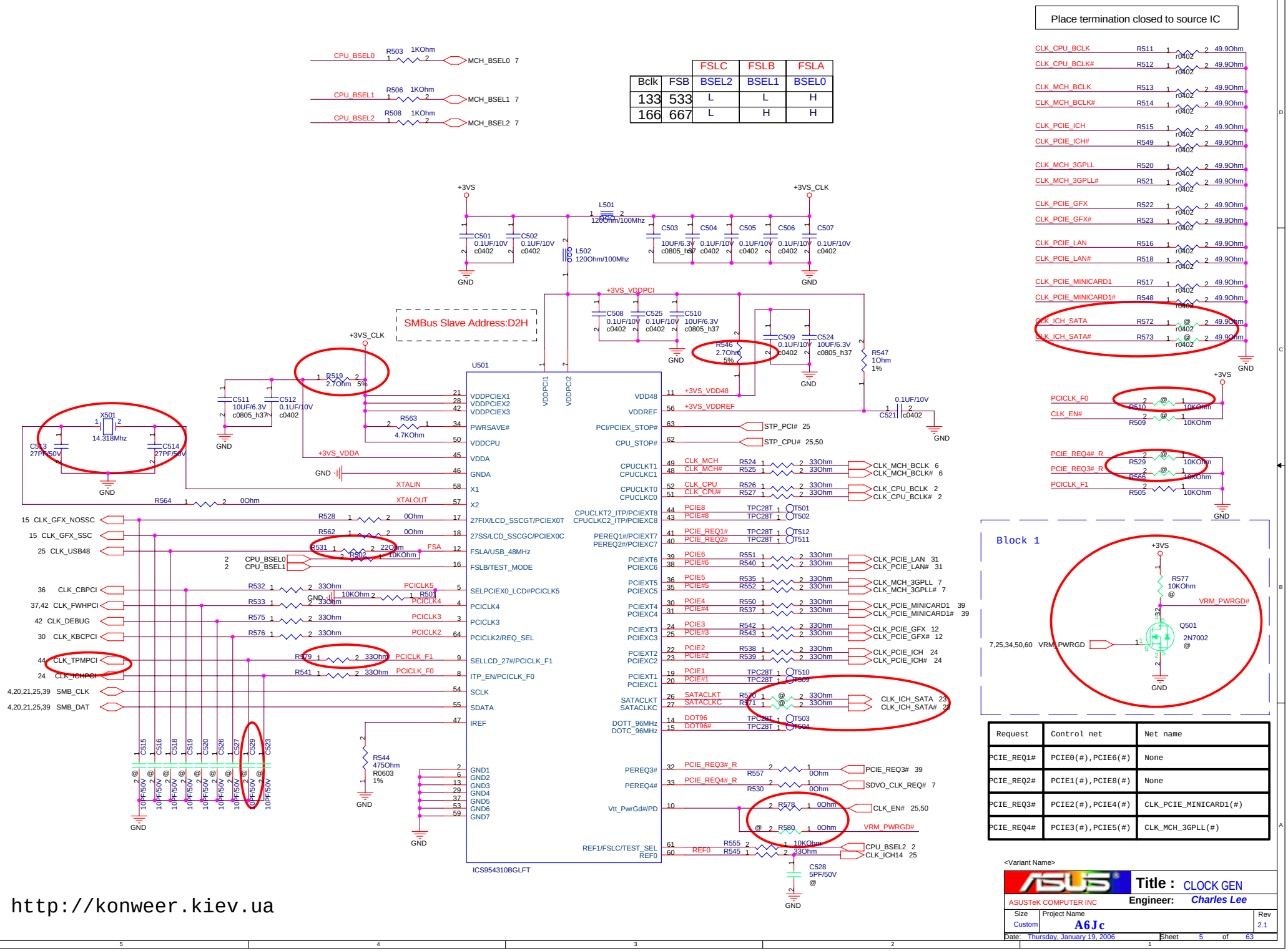

http://konweer.kiev.ua
YUNAH FSB667
LFM TYP HFM
VCC 1.14V 1.2V 1.356V
C4 C3 C0
ICC 0.9A 7.59A 27A
YUNAH FSB667
Min Typ Max
VCCP 0.997V 1.05V 1.102V
Min Typ Max
ICCP 2.5A
Vcc Core Decoupling Caps
Place these on bottom side.
U201C
SOCKET479P
U201D
SOCKET479P
+VCORE
+VCCP_AGTL+
+VCCA_CPU
CE307
330UF/2.5V
+VCCA_CPU:Provide isolated power for the internal processor core PLL.
RN302D
RN301A
RN301B
RN301C
RN301D
RN302A
RN302B
RN302C
VR_VID0 50
VR_VID1 50
VR_VID2 50
VR_VID3 50
VR_VID4 50
VR_VID5 50
VR_VID6 50
R301
100Ohm
1% r0402
VCCSENSE 50
VSSSENSE 50
R302
100Ohm
1% r0402
GND
CE301 330UF/2.5V
CE302 330UF/2.5V
CE303 330UF/2.5V
C303 22UF/6.3V
C312 22UF/6.3V
C334 22UF/6.3V
C317 22UF/6.3V
C314 22UF/6.3V
C310 22UF/6.3V
C320 22UF/6.3V
C328 22UF/6.3V
C308 22UF/6.3V
C326 22UF/6.3V
C306 22UF/6.3V
C331 22UF/6.3V
C332 22UF/6.3V
C324 22UF/6.3V
C304 22UF/6.3V
C309 22UF/6.3V
C330 22UF/6.3V
C323 22UF/6.3V
C318 22UF/6.3V
C321 10UF/6.3V
C311 22UF/6.3V
C316 22UF/6.3V
C315 10UF/6.3V
C305 10UF/6.3V
C322 10UF/6.3V
C307 22UF/6.3V
C319 10UF/6.3V
C329 10UF/6.3V
C333 10UF/6.3V
C313 22UF/6.3V
C325 22UF/6.3V
C327 10UF/6.3V
CE304 330UF/2.5V
CE305 330UF/2.5V
CE306 330UF/2.5V
C350 c0402 0.1UF/10V
C349 c0402 0.1UF/10V
C348 c0402 0.1UF/10V
C347 c0402 0.1UF/10V
For EMI requeirement. Place the CAPs on the moat of +Vcore and other power planes
Layout note:Route VCCSENSE and VSSSENSE trace at 27.4 ohm with 25 mils spacing mismatch and 18mils trace on 7mils spacing.
Place pull-up/down resisters within 1 inch of CPU.
+1.5VS
+VCCA_CPU
0.12A
Close to B26 (VCCA)
+VCCA_CPU
120mA / 20mil
C340 10UF/6.3V c0805_h37
C339 c0402 0.01UF/25V
Place these inside socket
C342 c0402 0.1UF/10V
C341 c0402 0.1UF/10V
C343 c0402 0.1UF/10V
C346 c0402 0.1UF/10V
C344 c0402 0.1UF/10V
C345 c0402 0.1UF/10V
<Variant Name>
Title : Yonah CPU (2)
ASUSTeK COMPUTER INC
Engineer: Charles Lee
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 3 of 63

Fan Speed Control



http://konweer.kiev.ua

<Variant Name>
Title : THER-SENSOR,FAN
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size: Custom
Project Name: A6Jc
Rev: 2.1
Date: Thursday, January 19, 2006
Sheet 4 of 63



Bclk	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
133	533	L	L	H
166	667	L	H	H

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD1(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#)	CLK_MCH_3GPLL(#)

<Variant Name>

ASUSTeK COMPUTER INC

Title : CLOCK GEN

Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 5 of 63

http://konweer.kiev.ua

http://konweer.kiev.ua

H_XRCOMP 10/20mils
R602 24.9Ohm 1%
GND

H_YRCOMP 10/20mils
R608 24.9Ohm 1%
GND

+VTT_AGTL+
R601 54.9Ohm 1%
H_XSCOMP 5.5/20 mils

+VTT_AGTL+
R605 54.9Ohm 1%
H_YSCOMP 5.5/20 mils

+VTT_AGTL+
R604 221Ohm 1% r0402
H_XSWING 12/20 mils
R603 100Ohm 1% r0402
C602 0.1UF/10V c0402
GND

+VTT_AGTL+
R606 221Ohm 1% r0402
H_YSWING 12/20 mils
R607 100Ohm 1% r0402
C605 0.1UF/10V c0402
GND

+VCCP_GMCH
JP602 SHORT_PIN @ 3.2A
+VCCP

+VTT_AGTL+
JP601 SHORT_PIN @ 1.4A
+VCCP

U601A

2 H_D#[0..63]

H_D#0	F1	H_D#_0	
H_D#1	J1	H_D#_1	
H_D#2	H1	H_D#_2	
H_D#3	J6	H_D#_3	
H_D#4	H3	H_D#_4	
H_D#5	K2	H_D#_5	
H_D#6	G1	H_D#_6	
H_D#7	G2	H_D#_7	
H_D#8	K9	H_D#_8	
H_D#9	K1	H_D#_9	
H_D#10	K7	H_D#_10	
H_D#11	J8	H_D#_11	
H_D#12	H4	H_D#_12	
H_D#13	J3	H_D#_13	
H_D#14	K11	H_D#_14	
H_D#15	G4	H_D#_15	
H_D#16	T10	H_D#_16	
H_D#17	W11	H_D#_17	
H_D#18	T3	H_D#_18	
H_D#19	U7	H_D#_19	
H_D#20	U9	H_D#_20	
H_D#21	U11	H_D#_21	
H_D#22	T11	H_D#_22	
H_D#23	W9	H_D#_23	
H_D#24	T1	H_D#_24	
H_D#25	T8	H_D#_25	
H_D#26	T4	H_D#_26	
H_D#27	W7	H_D#_27	
H_D#28	U5	H_D#_28	
H_D#29	T9	H_D#_29	
H_D#30	W6	H_D#_30	
H_D#31	T5	H_D#_31	
H_D#32	AB7	H_D#_32	
H_D#33	AA9	H_D#_33	
H_D#34	W4	H_D#_34	
H_D#35	W3	H_D#_35	
H_D#36	Y3	H_D#_36	
H_D#37	Y7	H_D#_37	
H_D#38	W5	H_D#_38	
H_D#39	Y10	H_D#_39	
H_D#40	AB8	H_D#_40	
H_D#41	W2	H_D#_41	
H_D#42	AA4	H_D#_42	
H_D#43	AA7	H_D#_43	
H_D#44	AA2	H_D#_44	
H_D#45	AA6	H_D#_45	
H_D#46	AA10	H_D#_46	
H_D#47	Y8	H_D#_47	
H_D#48	AA1	H_D#_48	
H_D#49	AB4	H_D#_49	
H_D#50	AC9	H_D#_50	
H_D#51	AB11	H_D#_51	
H_D#52	AC11	H_D#_52	
H_D#53	AB3	H_D#_53	
H_D#54	AC2	H_D#_54	
H_D#55	AD1	H_D#_55	
H_D#56	AD9	H_D#_56	
H_D#57	AC1	H_D#_57	
H_D#58	AD7	H_D#_58	
H_D#59	AC6	H_D#_59	
H_D#60	AB5	H_D#_60	
H_D#61	AD10	H_D#_61	
H_D#62	AD4	H_D#_62	
H_D#63	AC8	H_D#_63	

H_XRCOMP	E1	H_XRCOMP	
H_XSCOMP	E2	H_XSCOMP	
H_XSWING	E4	H_XSWING	
H_YRCOMP	Y1	H_YRCOMP	
H_YSCOMP	U1	H_YSCOMP	
H_YSWING	W1	H_YSWING	
5 CLK_MCH_BCLK	AG2	H_CLKIN	
5 CLK_MCH_BCLK#	AG1	H_CLKIN#	

HOST

CALISTOGA_Q137

H_A#_3	H9	H_A#3	
H_A#_4	C9	H_A#4	
H_A#_5	E11	H_A#5	
H_A#_6	G11	H_A#6	
H_A#_7	F11	H_A#7	
H_A#_8	G12	H_A#8	
H_A#_9	F9	H_A#9	
H_A#_10	H11	H_A#10	
H_A#_11	J12	H_A#11	
H_A#_12	G14	H_A#12	
H_A#_13	D9	H_A#13	
H_A#_14	J14	H_A#14	
H_A#_15	H13	H_A#15	
H_A#_16	J15	H_A#16	
H_A#_17	F14	H_A#17	
H_A#_18	D12	H_A#18	
H_A#_19	A11	H_A#19	
H_A#_20	C11	H_A#20	
H_A#_21	A12	H_A#21	
H_A#_22	A13	H_A#22	
H_A#_23	E13	H_A#23	
H_A#_24	G13	H_A#24	
H_A#_25	F12	H_A#25	
H_A#_26	B12	H_A#26	
H_A#_27	B14	H_A#27	
H_A#_28	C12	H_A#28	
H_A#_29	A14	H_A#29	
H_A#_30	C14	H_A#30	
H_A#_31	D14	H_A#31	

H_A#[31..3] 2

H_ADS#	E8	H_ADS#	2
H_ADSTB#_0	B9	H_ADSTB#0	2
H_ADSTB#_1	C13	H_ADSTB#1	2
H_AVREF	J13		
H_BNR#	C6	H_BNR#	2
H_BPRI#	F6	H_BPRI#	2
H_BREQ#0	C7	H_BR0#	2
H_CPURST#	B7	H_CPURST#	2
H_DBSY#	A7	H_DBSY#	2
H_DEFER#	C3	H_DEFER#	2
H_DPWR#	J9	H_DPWR#	2
H_DRDY#	H8	H_DRDY#	2
H_DVREF	K13		
H_DINV#_0	J7	H_DINV#0	2
H_DINV#_1	W8	H_DINV#1	2
H_DINV#_2	U3	H_DINV#2	2
H_DINV#_3	AB10	H_DINV#3	2
H_DSTBN#_0	K4	H_DSTBN#0	2
H_DSTBN#_1	T7	H_DSTBN#1	2
H_DSTBN#_2	Y5	H_DSTBN#2	2
H_DSTBN#_3	AC4	H_DSTBN#3	2
H_DSTBP#_0	K3	H_DSTBP#0	2
H_DSTBP#_1	T6	H_DSTBP#1	2
H_DSTBP#_2	AA5	H_DSTBP#2	2
H_DSTBP#_3	AC5	H_DSTBP#3	2
H_HIT#	D3	H_HIT#	2
H_HITM#	D4	H_HITM#	2
H_LOCK#	B3	H_LOCK#	2

H_REQ#_0	D8	H_REQ#0	
H_REQ#_1	G8	H_REQ#1	
H_REQ#_2	B8	H_REQ#2	
H_REQ#_3	F8	H_REQ#3	
H_REQ#_4	A8	H_REQ#4	
H_RS#_0	B4	H_RS#0	
H_RS#_1	E6	H_RS#1	
H_RS#_2	D6	H_RS#2	
H_SLPCPU#	E3	H_CPUSLP# NB	2
H_TRDY#	E7	H_TRDY#	

H_REQ#[4..0] 2
H_RS#[0..2] 2

R611 0Ohm
H_CPUSLP# 2,23
H_TRDY# 2

+VTT_AGTL+
R609 100Ohm 1% r0402
H_VREF
R610 200Ohm r0402 1%
C601 0.1UF/10V c0402
GND

<Variant Name>

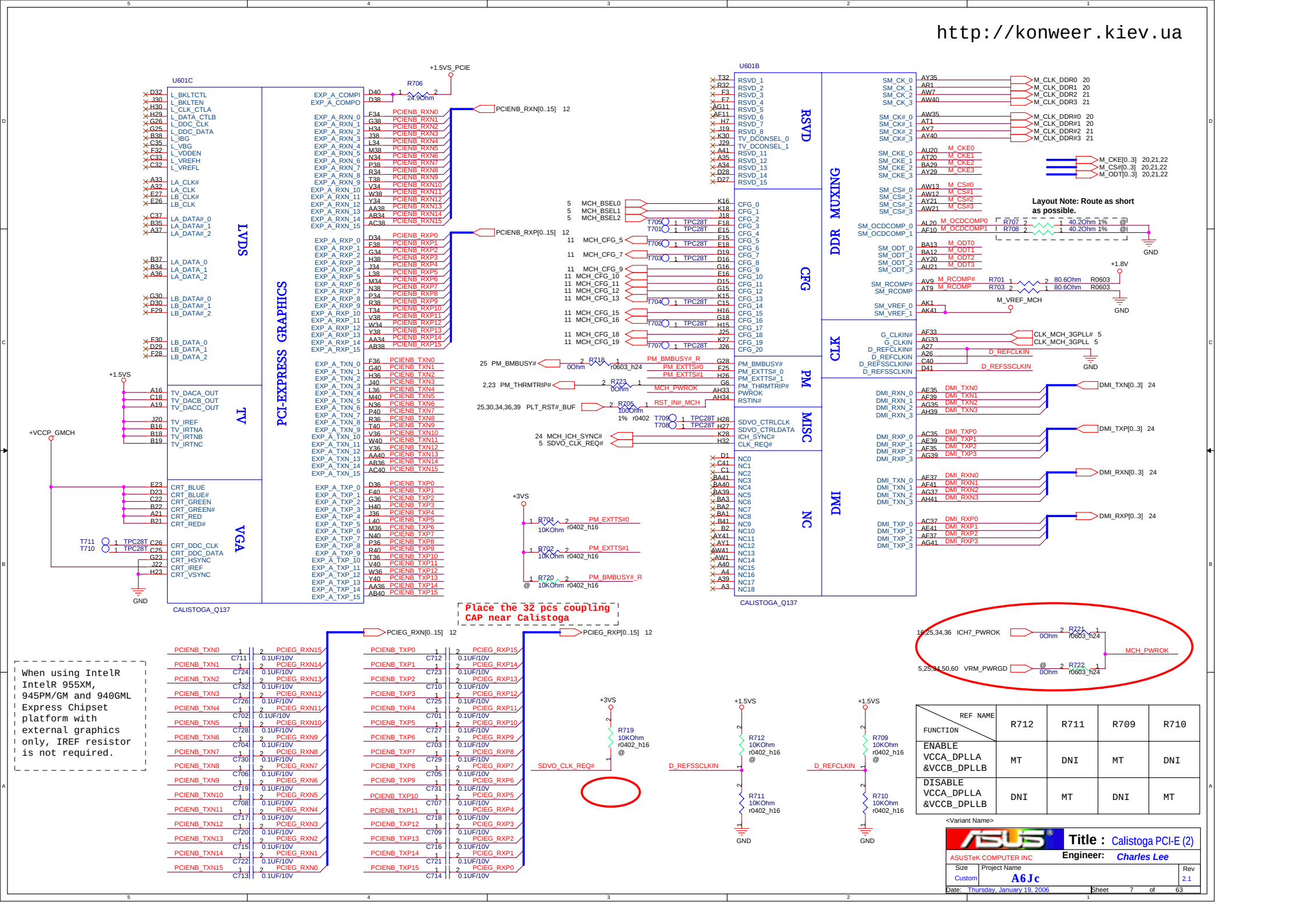
Title : Calistoga MCH (1)

ASUSTeK COMPUTER INC Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 6 of 63

http://konweer.kiev.ua



REF NAME / FUNCTION	R712	R711	R709	R710
ENABLE VCCA_DPLLA &VCCB_DPLLB	MT	DNI	MT	DNI
DISABLE VCCA_DPLLA &VCCB_DPLLB	DNI	MT	DNI	MT

<Variant Name>

ASUSTeK COMPUTER INC

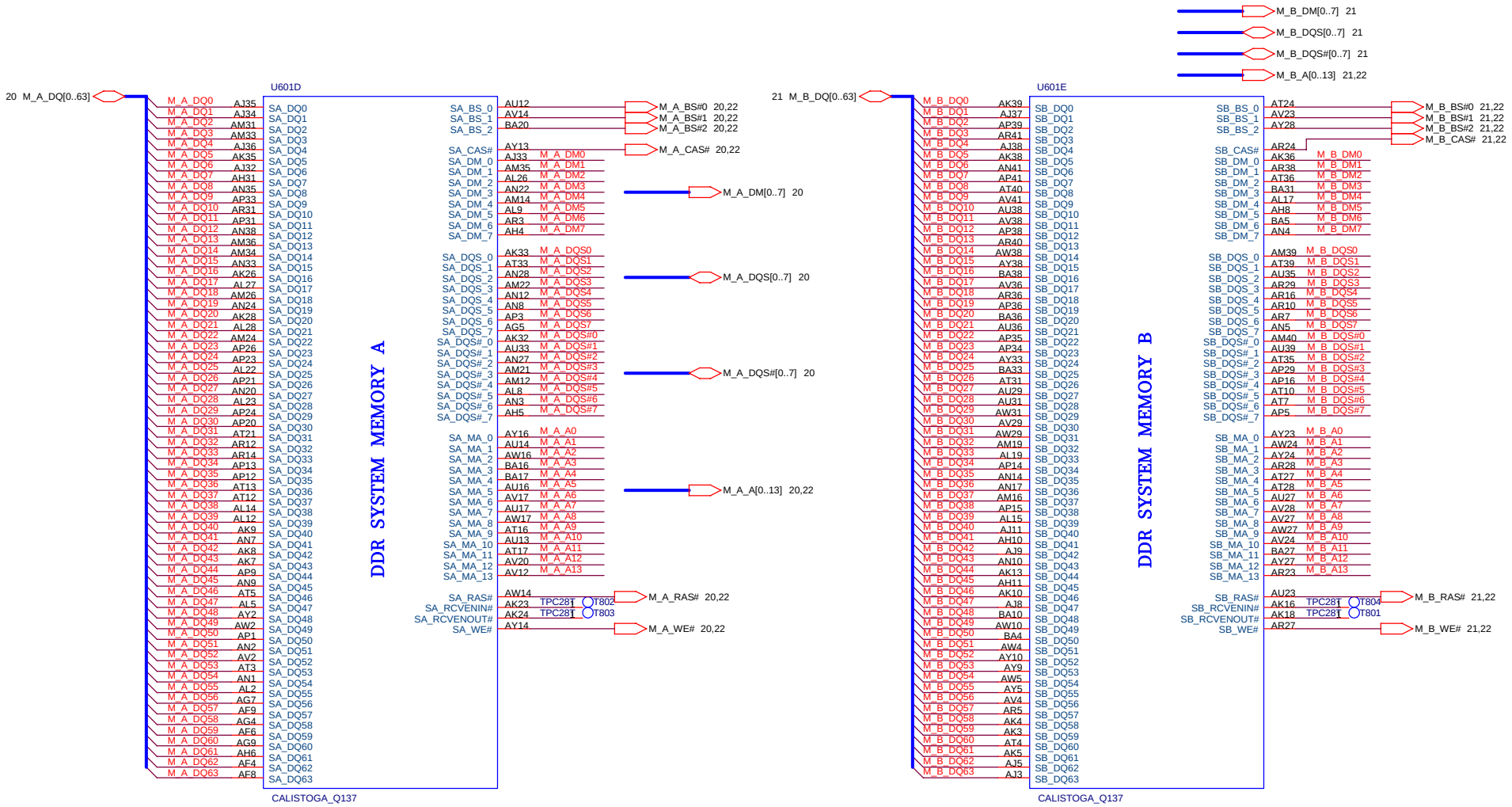
Title : Calistoga PCI-E (2)

Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 7 of 63

http://konweer.kiev.ua



<Variant Name>

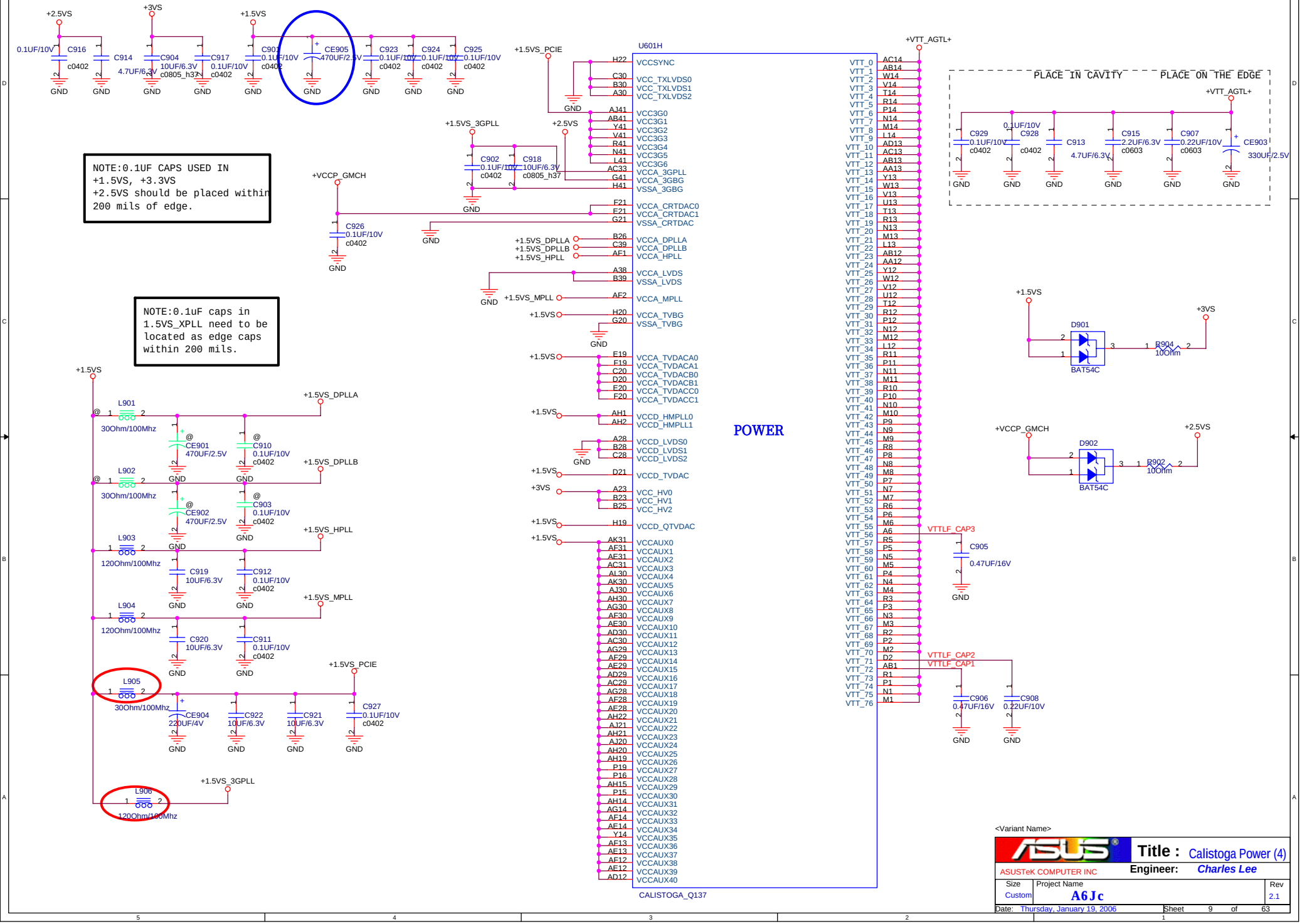
Title : Calistoga DDR2 (3)

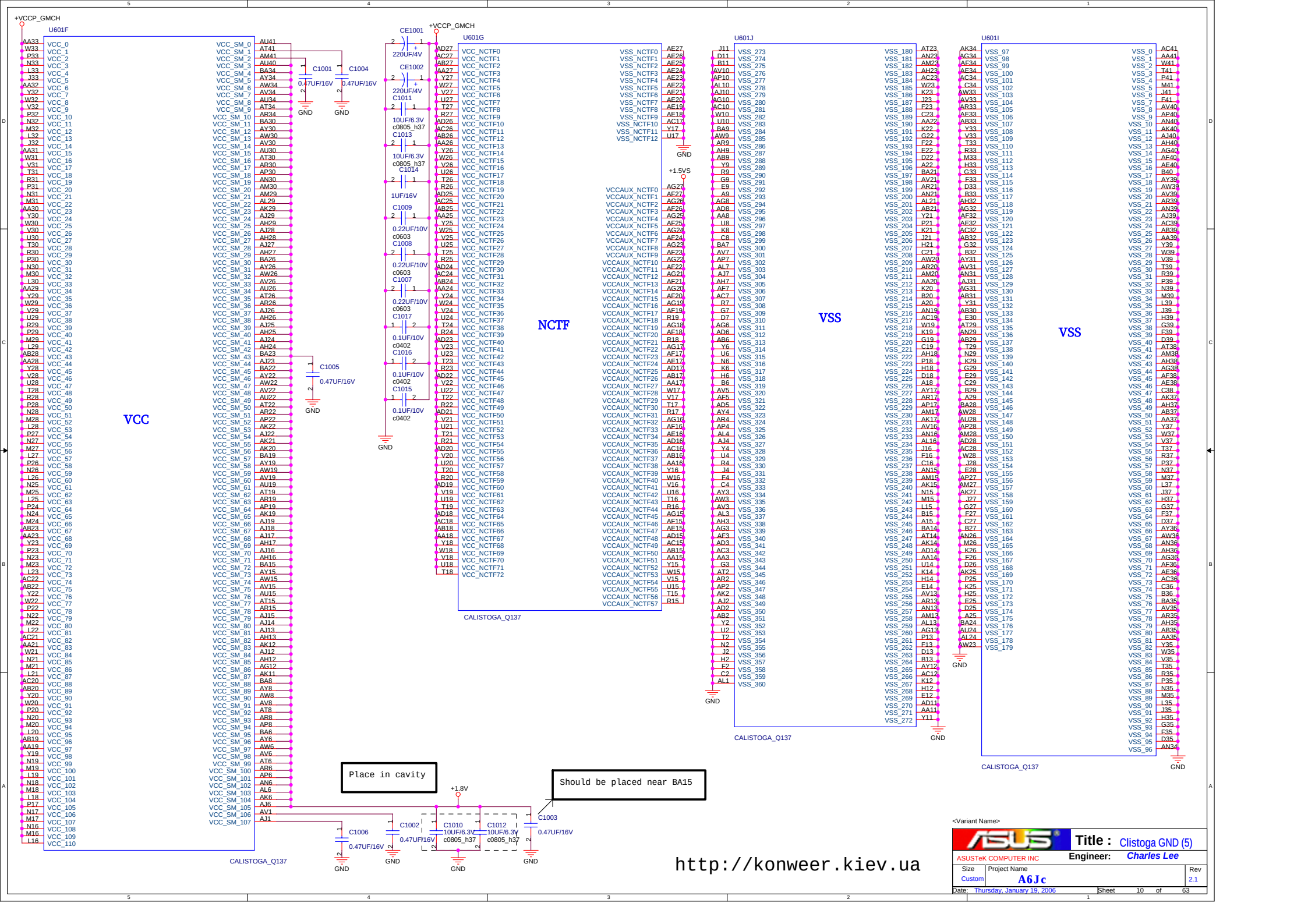
ASUSTeK COMPUTER INC

Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

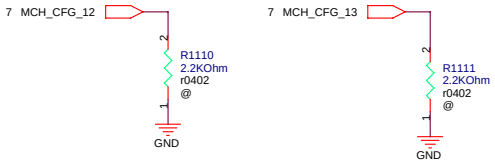
Date: Thursday, January 19, 2006 Sheet 8 of 63


http://konweer.kiev.ua
NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.
NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.
U601H
POWER
CALISTOGA_Q137
PLACE IN CAVITY
PLACE ON THE EDGE
+VTT_AGTL+
+1.5VS_PCIE
+1.5VS_3GPLL
+VCCP_GMCH
+1.5VS_DPLLA
+1.5VS_DPLLB
+1.5VS_HPLL
+1.5VS_MPLL
+1.5VS
+3VS
+2.5VS
GND
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
VTT_0
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
VTT_20
VTT_21
VTT_22
VTT_23
VTT_24
VTT_25
VTT_26
VTT_27
VTT_28
VTT_29
VTT_30
VTT_31
VTT_32
VTT_33
VTT_34
VTT_35
VTT_36
VTT_37
VTT_38
VTT_39
VTT_40
VTT_41
VTT_42
VTT_43
VTT_44
VTT_45
VTT_46
VTT_47
VTT_48
VTT_49
VTT_50
VTT_51
VTT_52
VTT_53
VTT_54
VTT_55
VTT_56
VTT_57
VTT_58
VTT_59
VTT_60
VTT_61
VTT_62
VTT_63
VTT_64
VTT_65
VTT_66
VTT_67
VTT_68
VTT_69
VTT_70
VTT_71
VTT_72
VTT_73
VTT_74
VTT_75
VTT_76
VTTLF_CAP3
VTTLF_CAP2
VTTLF_CAP1
C905 0.47UF/16V
C906 0.47UF/16V
C908 0.22UF/10V
C929 0.1UF/10V c0402
C928 0.1UF/10V c0402
C913 4.7UF/6.3V
C915 2.2UF/6.3V c0603
C907 0.22UF/10V c0603
CE903 330UF/2.5V
D901 BAT54C
D902 BAT54C
R904 10Ohm
R902 10Ohm
C916 0.1UF/10V c0402
C914 4.7UF/6.3V
C904 10UF/6.3V c0805_h37
C917 0.1UF/10V c0402
C901 0.1UF/10V c0402
CE905 470UF/2.5V
C923 0.1UF/10V c0402
C924 0.1UF/10V c0402
C925 0.1UF/10V c0402
C902 0.1UF/10V c0402
C918 10UF/6.3V c0805_h37
C926 0.1UF/10V c0402
L901 30Ohm/100Mhz
L902 30Ohm/100Mhz
L903 120Ohm/100Mhz
L904 120Ohm/100Mhz
L905 30Ohm/100Mhz
L906 120Ohm/100Mhz
CE901 470UF/2.5V
CE902 470UF/2.5V
CE904 220UF/4V
C910 0.1UF/10V c0402
C903 0.1UF/10V c0402
C919 10UF/6.3V
C912 0.1UF/10V c0402
C920 10UF/6.3V
C911 0.1UF/10V c0402
C922 10UF/6.3V
C921 10UF/6.3V
C927 0.1UF/10V c0402
<Variant Name>
Title : Calistoga Power (4)
ASUSTeK COMPUTER INC
Engineer: Charles Lee
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 9 of 63


+VCCP_GMCH
U601F
VCC
U601G
NCTF
CALISTOGA_Q137
U601J
VSS
U601I
VSS
CALISTOGA_Q137
+1.5VS
+1.8V
GND
C1001
C1004
C1005
C1006
C1002
C1010
C1012
C1003
0.47UF/16V
CE1001
CE1002
220UF/4V
C1011
10UF/6.3V
c0805_h37
C1013
C1014
1UF/16V
C1009
0.22UF/10V
c0603
C1008
C1007
C1017
0.1UF/10V
c0402
C1016
C1015
Place in cavity
Should be placed near BA15
http://konweer.kiev.ua
<Variant Name>
Title : Clistoga GND (5)
ASUSTeK COMPUTER INC
Engineer: Charles Lee
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 10 of 63

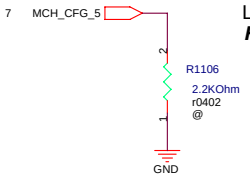
http://konweer.kiev.ua

CFG[17..3] have internal pullup resistors.
CFG[20..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.



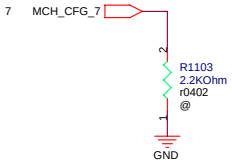
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



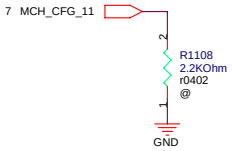
CFG7 : CPU STRAP

LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



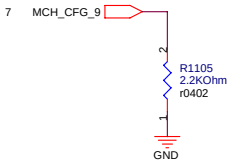
CFG11 : PSB 4X CLK ENABLE

LOW = REVERSAL
HIGH =Calistoga(Default)



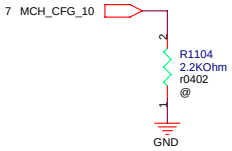
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE (Default)
HIGH = NORMAL OPERATION



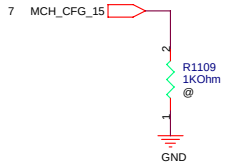
CFG10: HOST PLL VCO SELECT

LOW = RESERVED
HIGH = MOBILITY



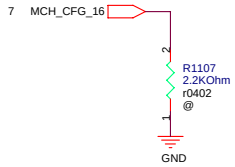
CFG15 :ICH RESET DISABLE

LOW = ICH RESET DISABLE
HIGH = NORMAL OPERATION



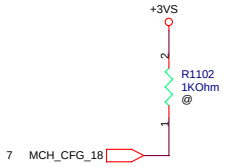
CFG16 : FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



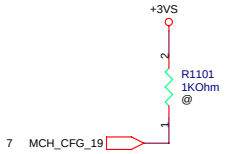
CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V



CFG19 : DMI LANE REVERSAL

LOW = NORMAL
HIGH = LANES REVERSED



<Variant Name>

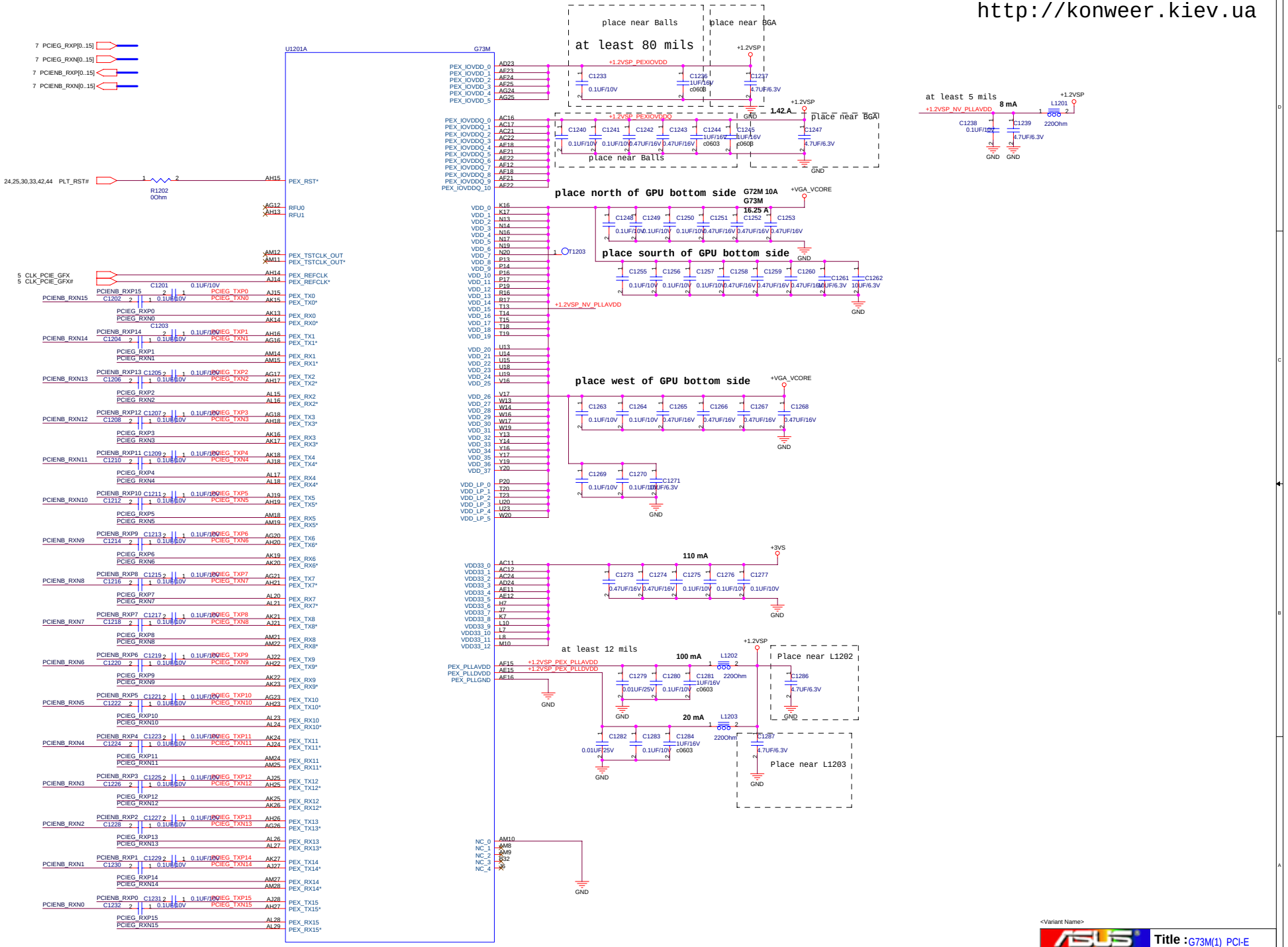
Title : Calistoga Strapping

ASUSTeK COMPUTER INC Engineer: *Charles Lee*

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 11 of 63

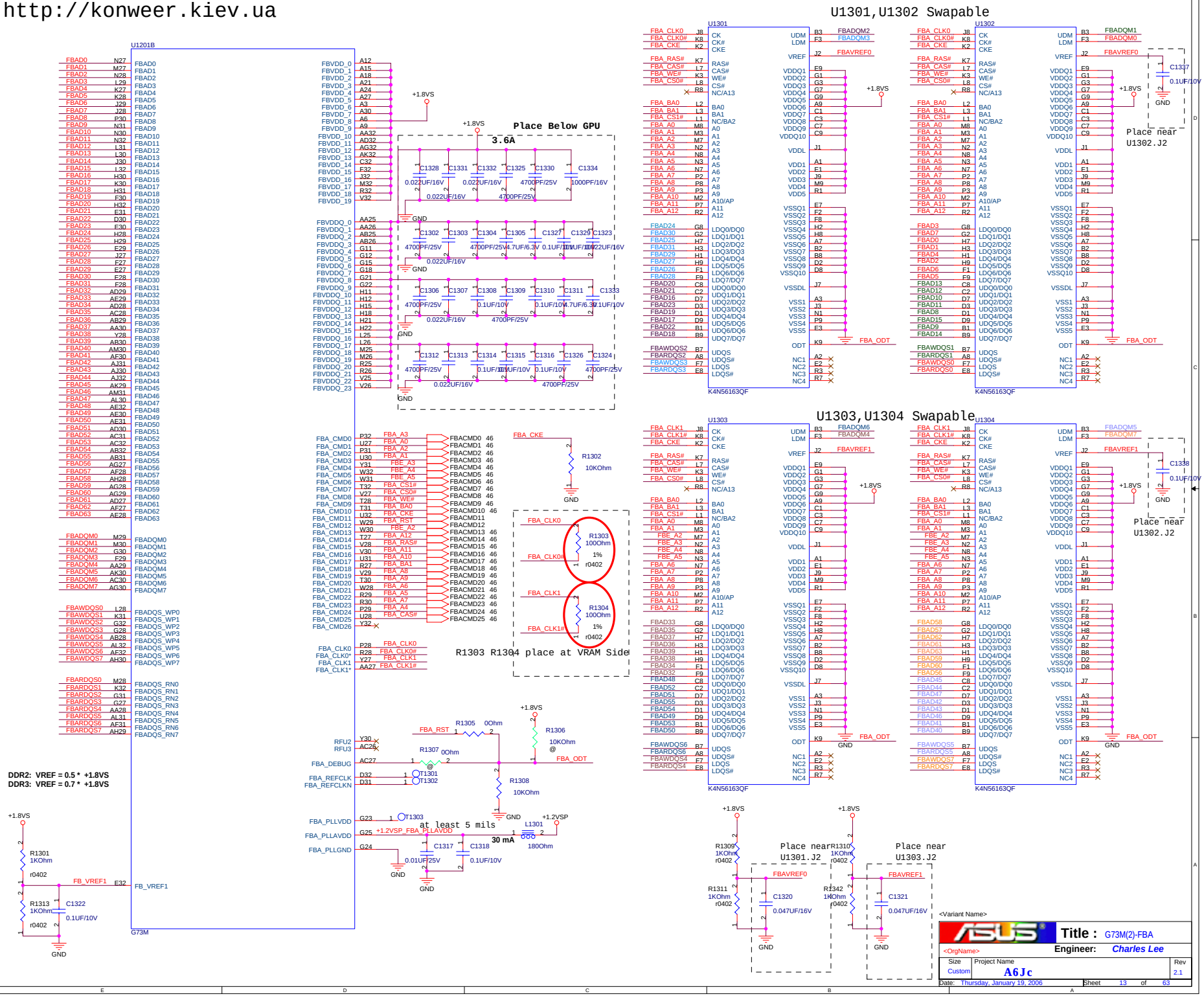
http://konweer.kiev.ua



<Variant Name>

ASUSTek COMPUTER INC	Title : G73M(1)_PCI-E	
	Engineer: Charles Lee	
Size: C	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 12 of 63	

http://konweer.kiev.ua



<Variant Name>

Title : G73M(2)-FBA

<OrgName>

Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 13 of 63

DDR2 Terminated FBVTT=0.5* +1.8VS
Unterminated FBVTT=+1.8VS

U1401,U1402 Swapable

U1403,U1404 Swapable

R1402 R1403 place at VRAM Side

http://konweer.kiev.ua

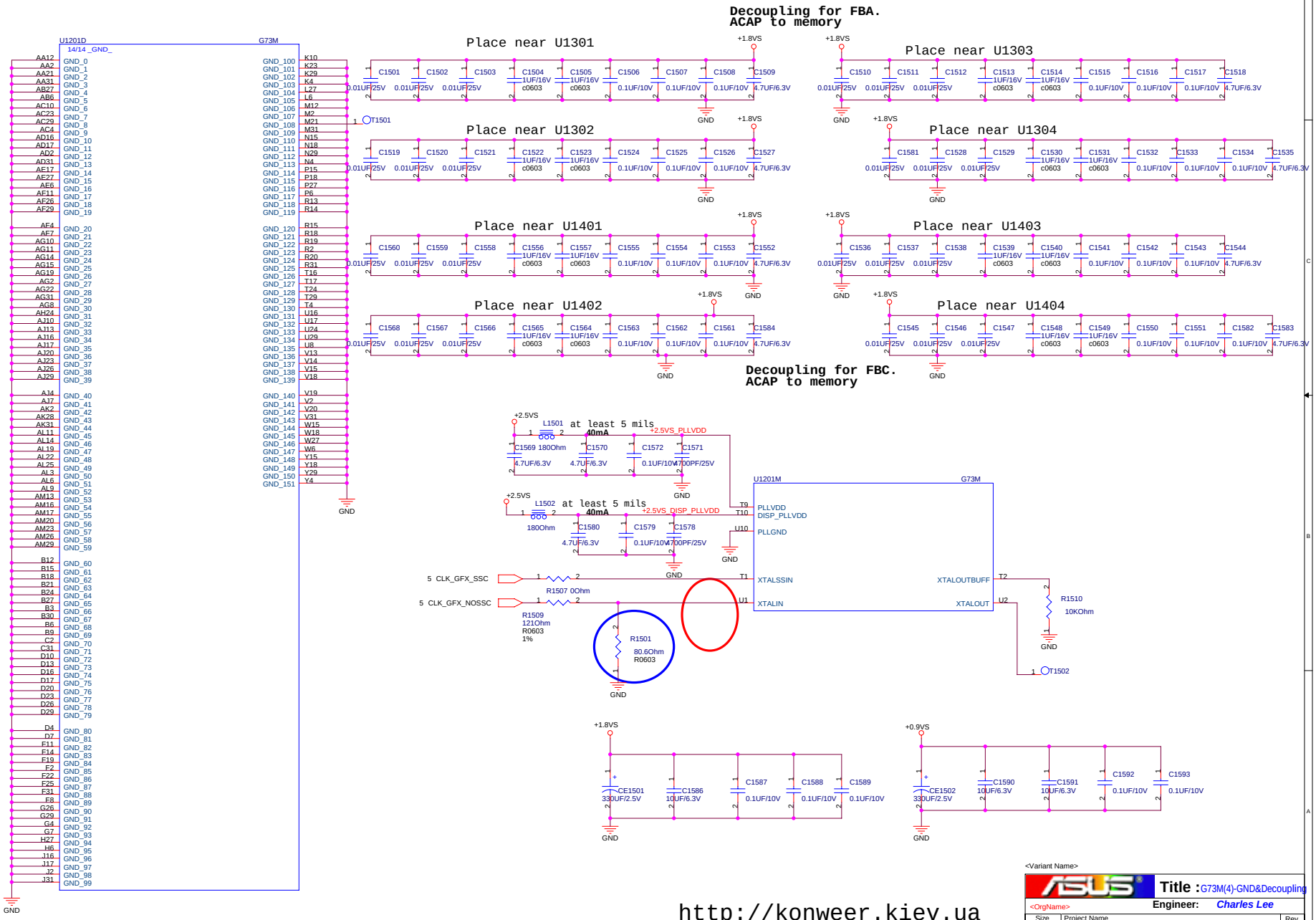
<Variant Name>

Title : G73M(3)-FBC

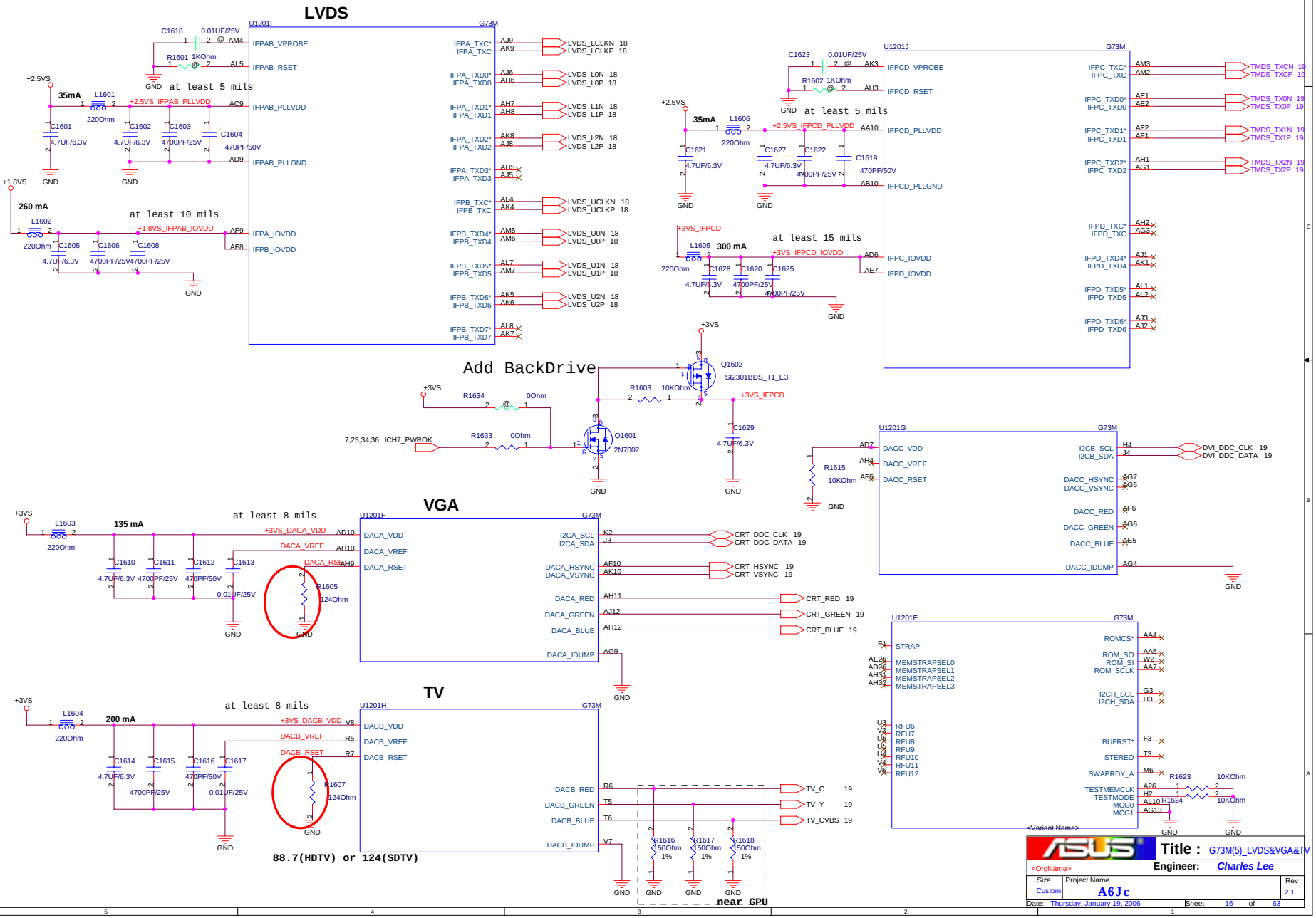
<OrgName> Engineer: Charles Lee

Size: Custom | Project Name: A6Jc | Rev: 2.1

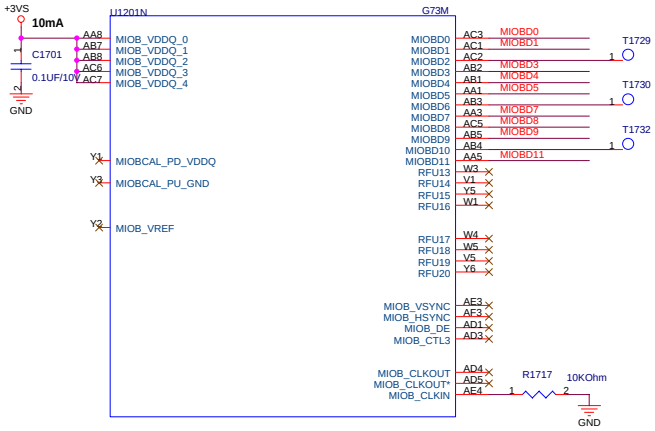
Date: Thursday, January 19, 2006 | Sheet 14 of 63

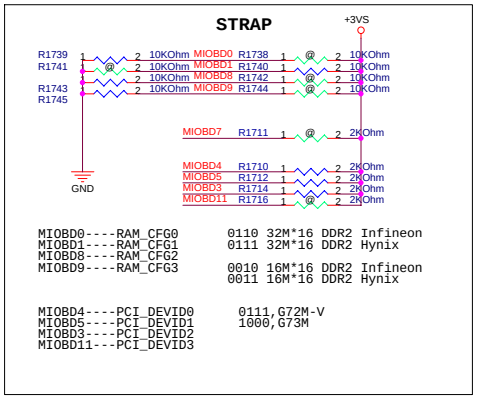

Decoupling for FBA.
ACAP to memory
Place near U1301
Place near U1303
Place near U1302
Place near U1304
Place near U1401
Place near U1403
Place near U1402
Place near U1404
Decoupling for FBC.
ACAP to memory
U1201D
G73M
14/14 _GND_
U1201M
+1.8VS
+0.9VS
+2.5VS
GND
L1501 at least 5 mils
40mA
+2.5VS_PLLVDD
L1502 at least 5 mils
+2.5VS_DISP_PLLVDD
PLLVDD
DISP_PLLVDD
PLLGND
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
5 CLK_GFX_SSC
5 CLK_GFX_NOSSC
R1507 0Ohm
R1509
121Ohm
R0603
1%
R1501
80.6Ohm
R0603
R1510
10KOhm
T1501
T1502
http://konweer.kiev.ua

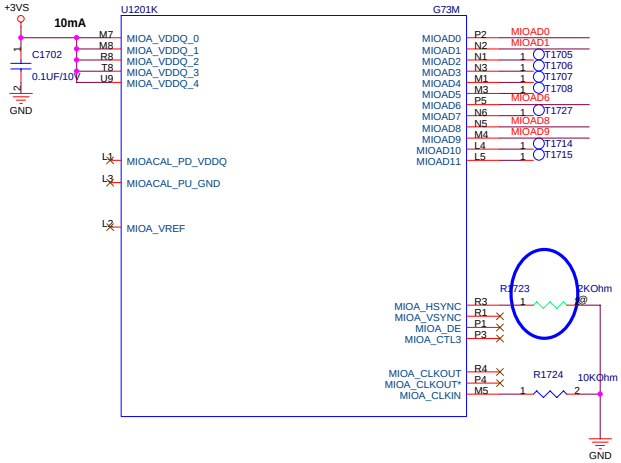
http://konweer.kiev.ua

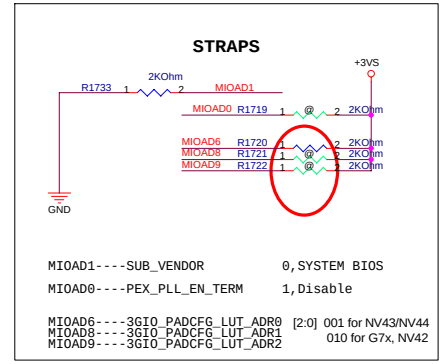


http://konweer.kiev.ua

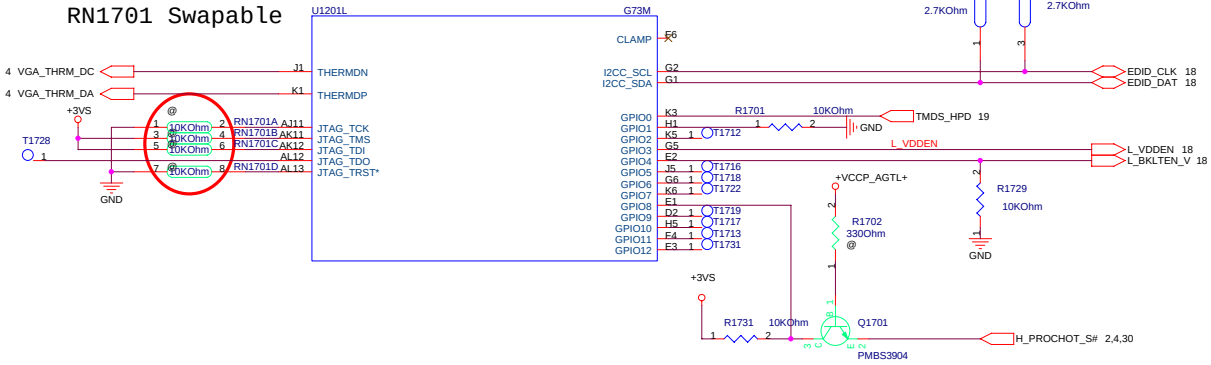








RN1701 Swapable



RN1702 Swapable

GPIO0, 1 -- Hot Plug Detect (For DVI)
GPIO2 -- Panel backlight brightness (PWM),
GPIO3 -- Panel power enable
GPIO4 -- Panel backlight ON/OFF
GPIO5 -- GPU VID0
GPIO6 -- GPU VID1
GPIO7 -- GPU VID2 or MEM VID
GPIO8 -- Thermal diode ALERT
GPIO9 -- Fan control
GPIO11 -- HDTV enable

Internal Pull-down
GPIO0, 1, 2, 4, 5, 6, 7

<Variant Name>

Title : G73M(6)_MIOBD&GPIO

<OrgName>

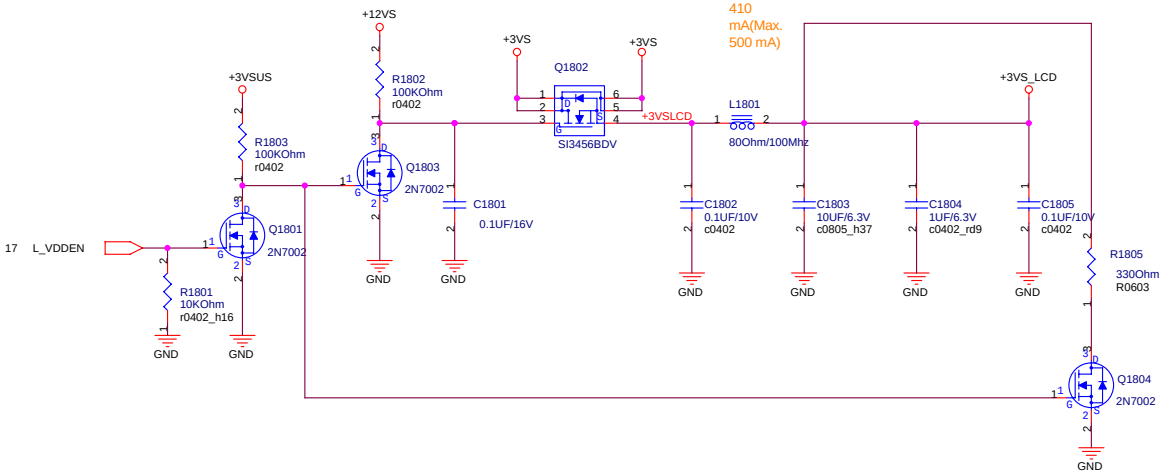
Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

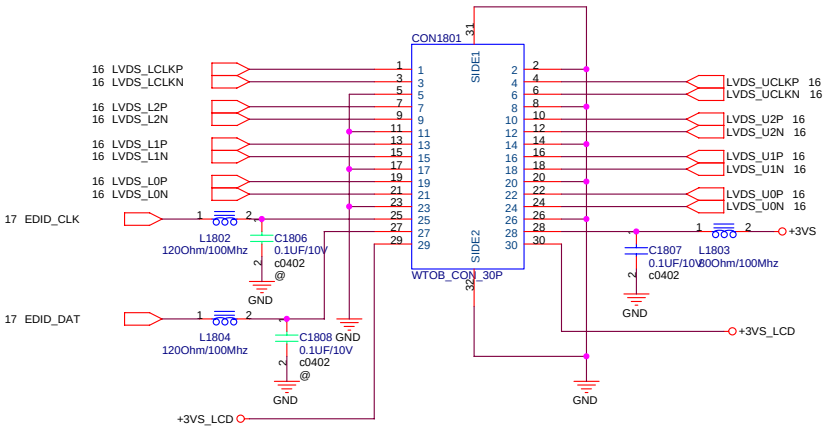
Date: Thursday, January 19, 2006 Sheet 17 of 63

LCD Power

3V-3.6V
Full
Active:
410
mA(Max.
500 mA)



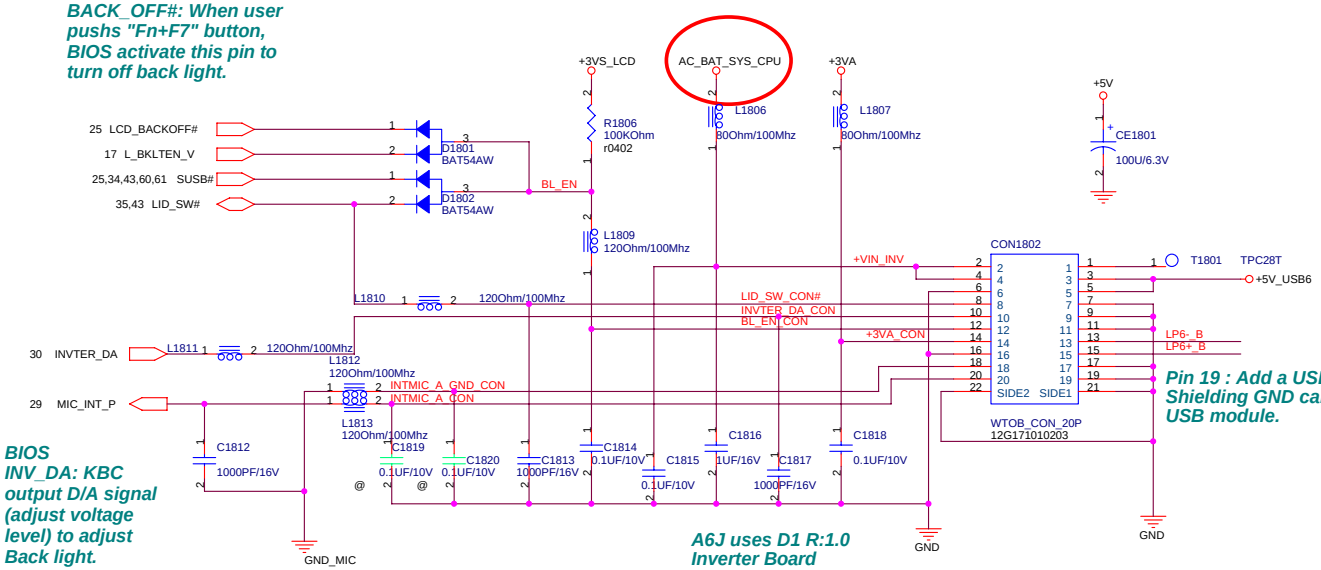
LCD LVDS Interface



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

INVERTER Interface

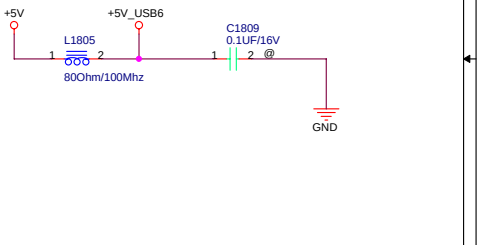
BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.



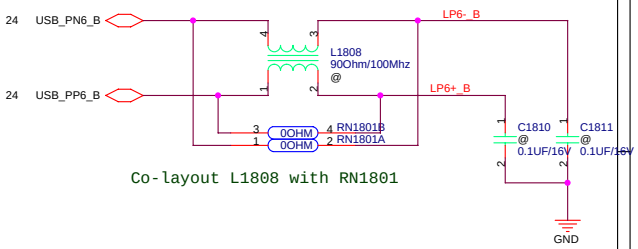
BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

A6J uses D1 R:1.0 Inverter Board

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

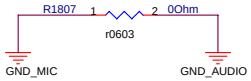


USB PORT 6 for USB CAMERA



Co-layout L1808 with RN1801

For EMI

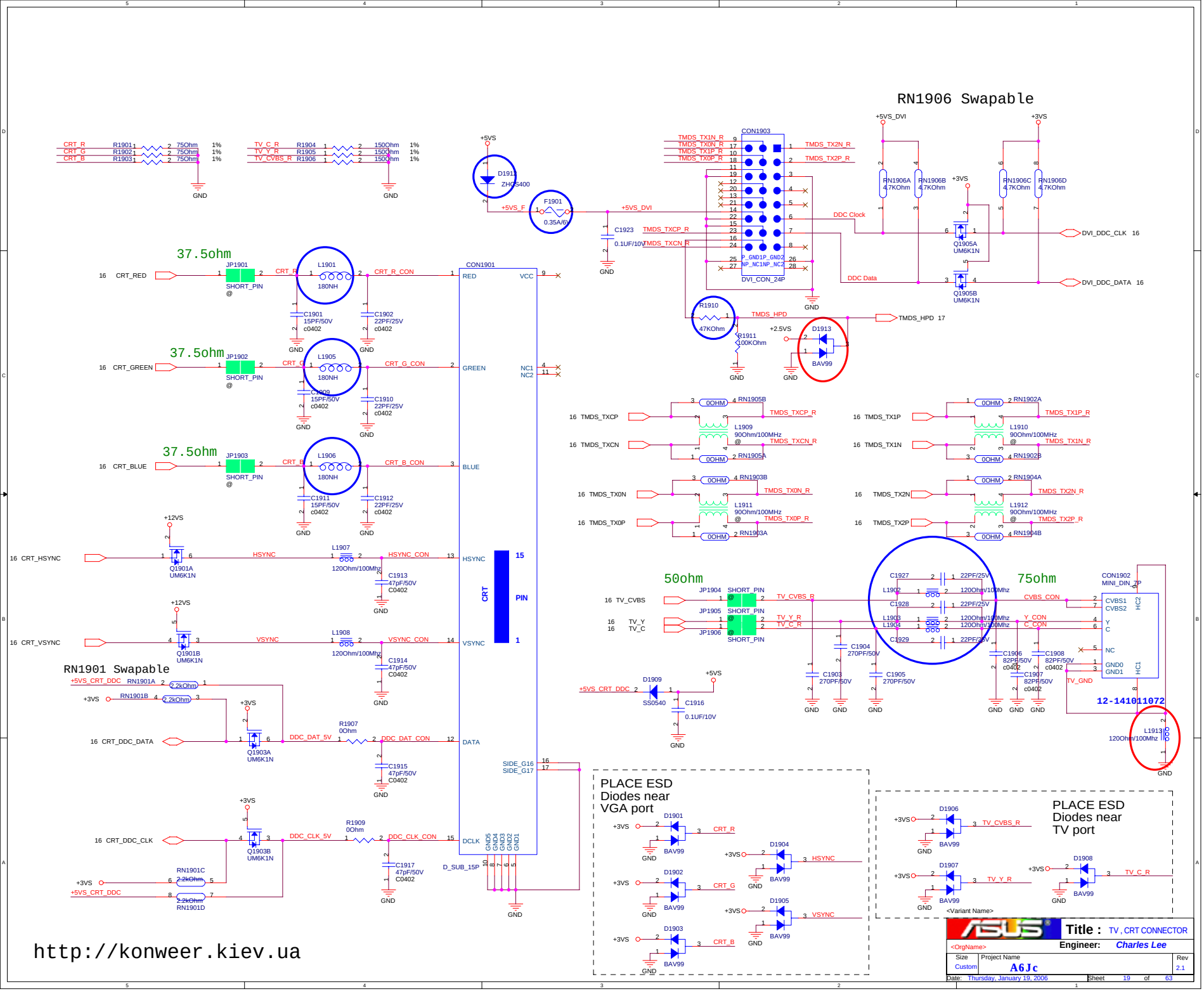


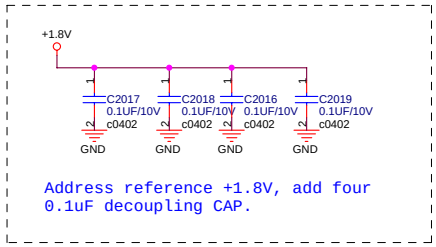
A6J doesn't support USB WLAN function!

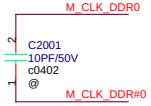
http://konweer.kiev.ua

<Variant Name>

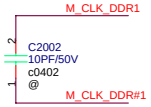
ASUS	Title : LVDS & INVERTER	
<OrgName>	Engineer: Charles Lee	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 18 of 63	

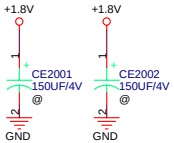

RN1906 Swapable
RN1901 Swapable
37.5ohm
37.5ohm
37.5ohm
50ohm
75ohm
CON1901
CON1903
DVI_CON_24P
CON1902
MINI_DIN_7P
12-141011072
PLACE ESD
Diodes near
VGA port
PLACE ESD
Diodes near
TV port
<Variant Name>
Title : TV , CRT CONNECTOR
<OrgName>
Engineer: Charles Lee
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 19 of 63
http://konweer.kiev.ua

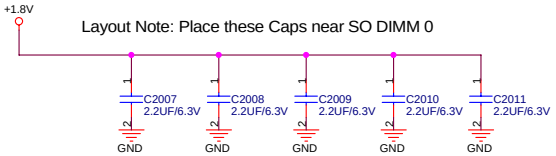




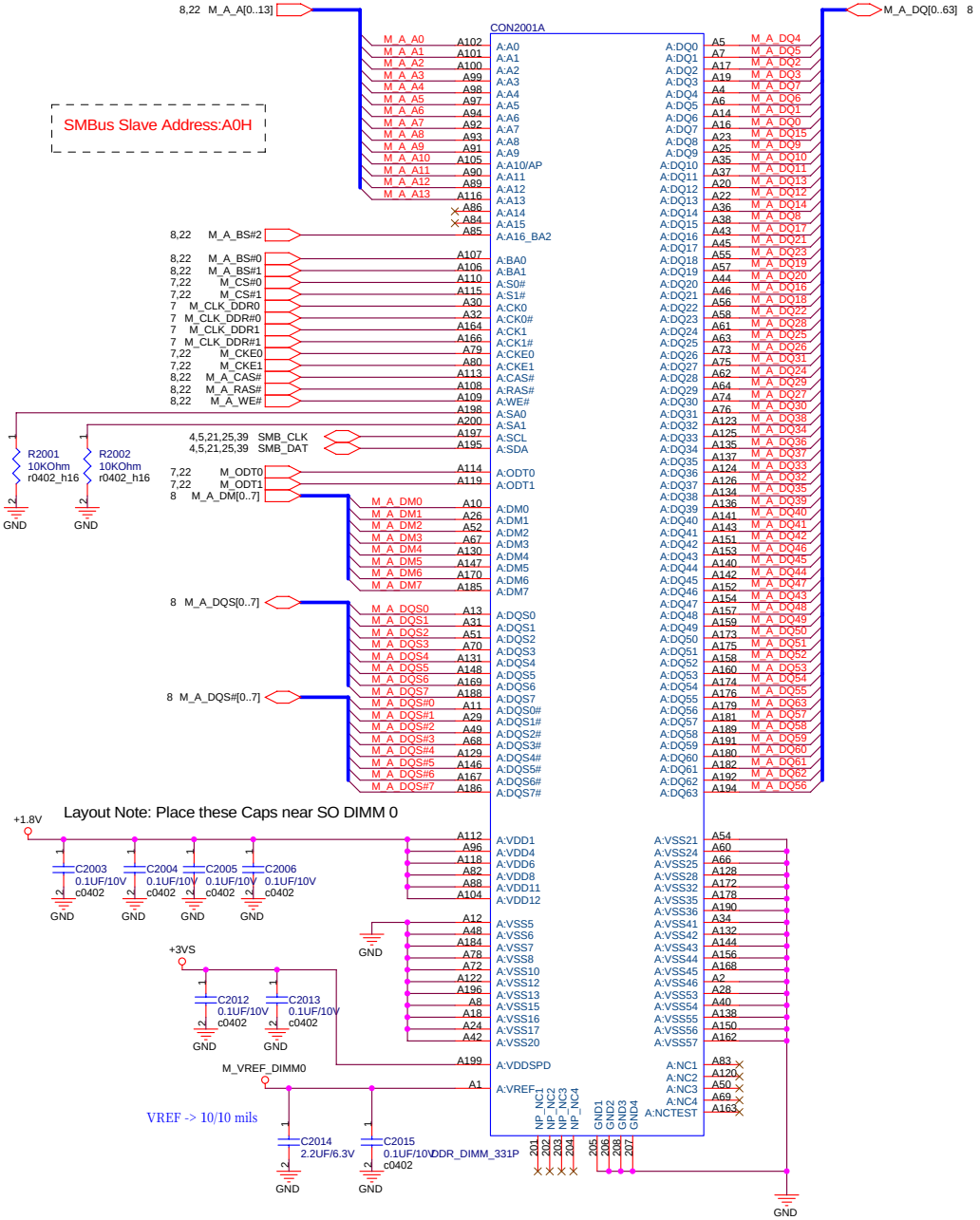
PLACE NEAR SO-DIMM_0



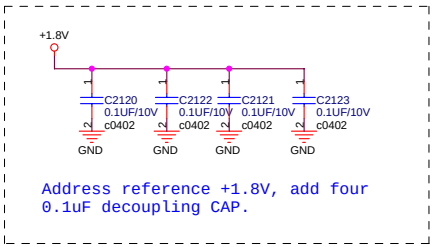




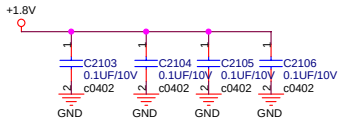
SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1



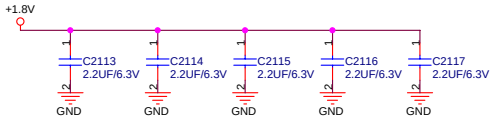
http://konweer.kiev.ua

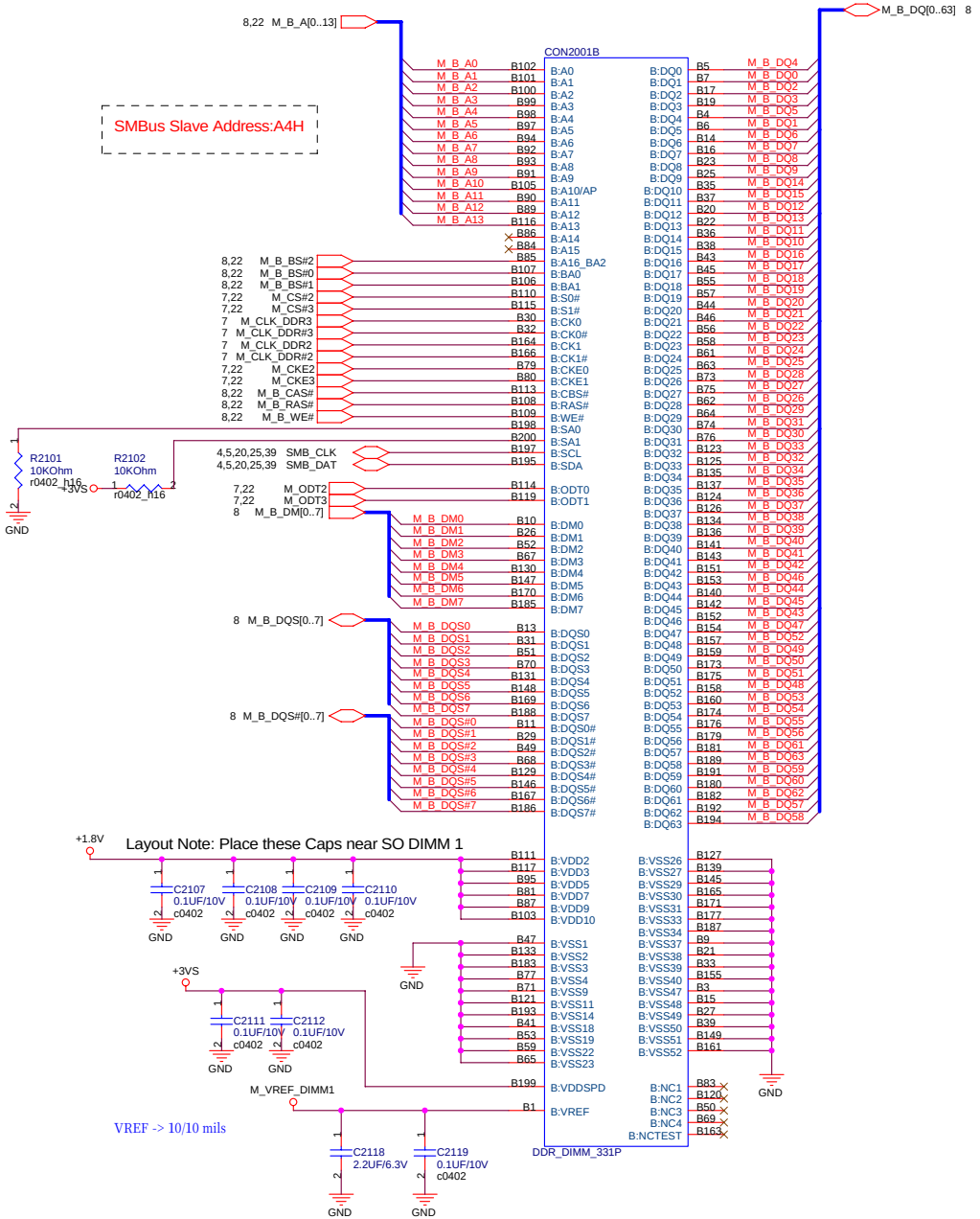


Layout Note: Place these High-Freq decoupling Caps near the GMCH



Layout Note: Place these CAPs near the GMCH





Layout Note: Place these Caps near SO DIMM 0

http://konweer.kiev.ua

<Variant Name>

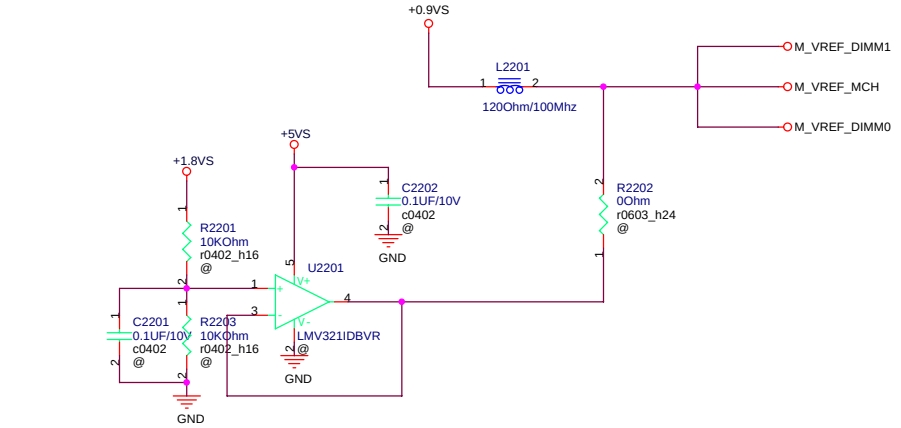
Title : DDR2 SO-DIMM_1

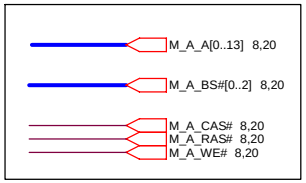
<OrgName>

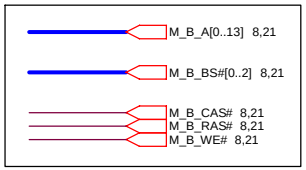
Engineer: Charles Lee

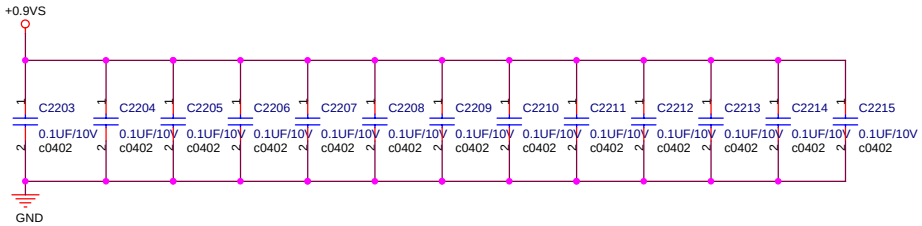
Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 21 of 63

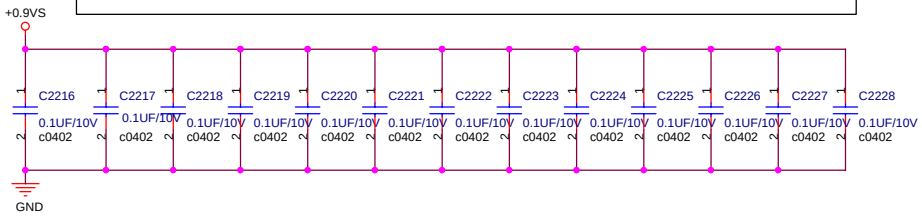


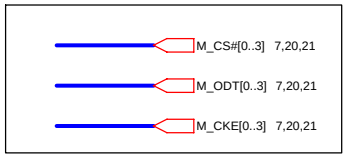


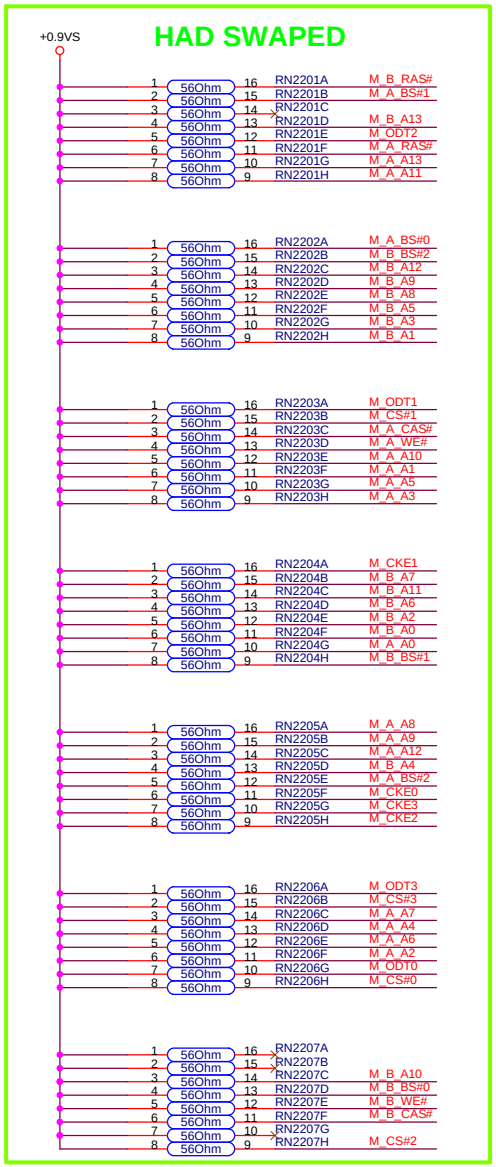




Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS







<variant_name><Variant Name></variant_name>

Title : DDR2 TERM

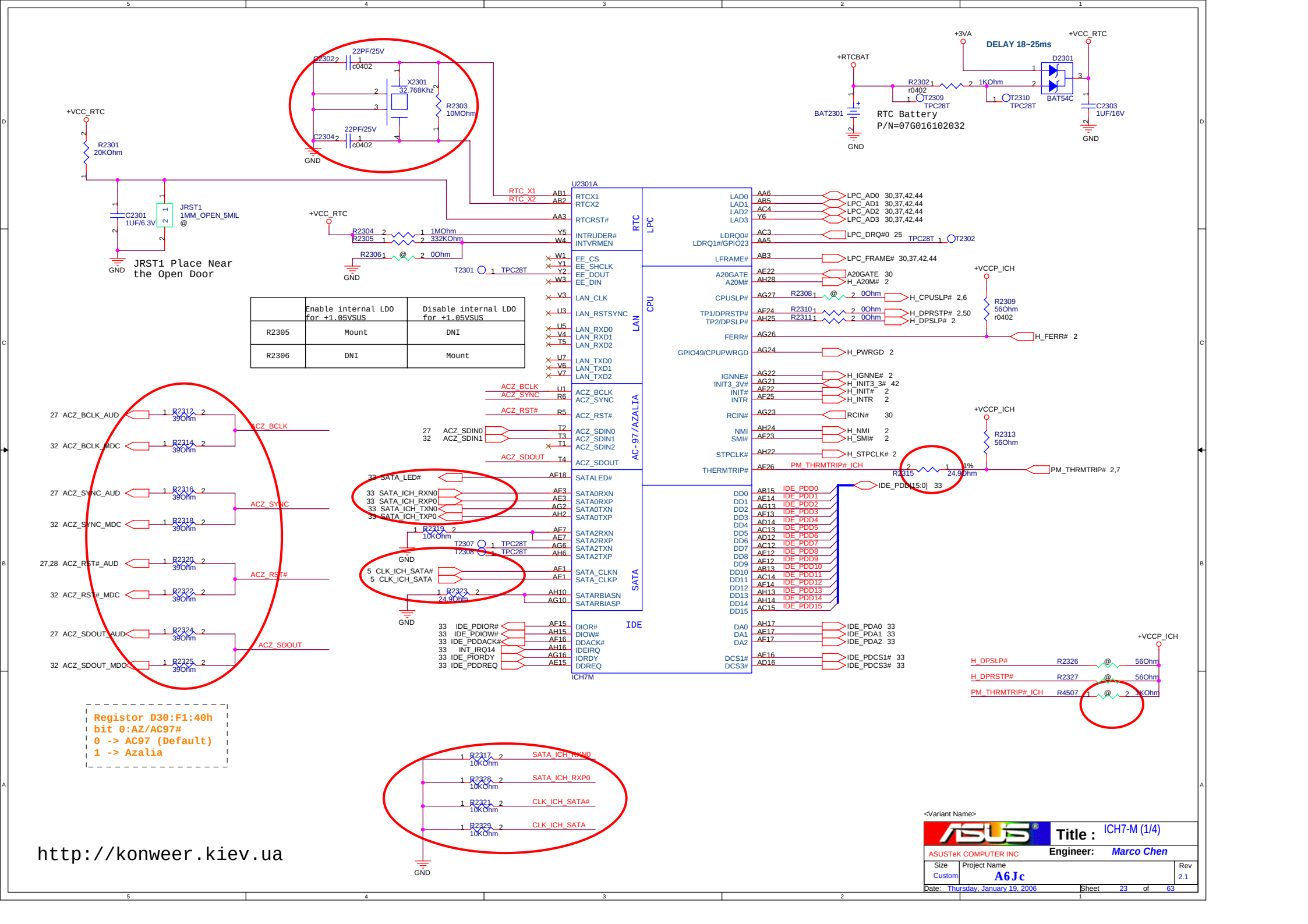
ASUSTeK COMPUTER INC

Engineer: Charles Lee

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 22 of 63

http://konweer.kiev.ua



	Enable internal LDO for +1.05VSUS	Disable internal LDO for +1.05VSUS
R2305	Mount	DNI
R2306	DNI	Mount

Registor D30:F1:40h
bit 0:AZ/AC97#
0 -> AC97 (Default)
1 -> Azalia

http://konweer.kiev.ua

<Variant Name>

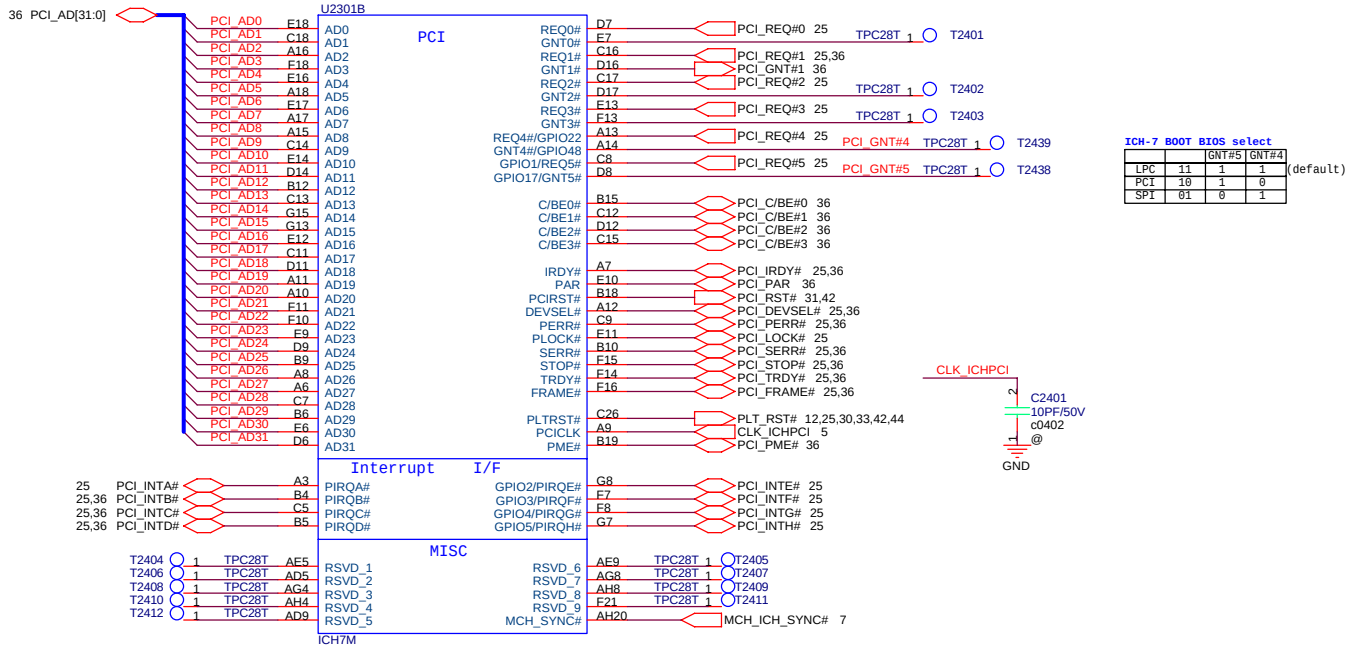
ASUSTeK COMPUTER INC

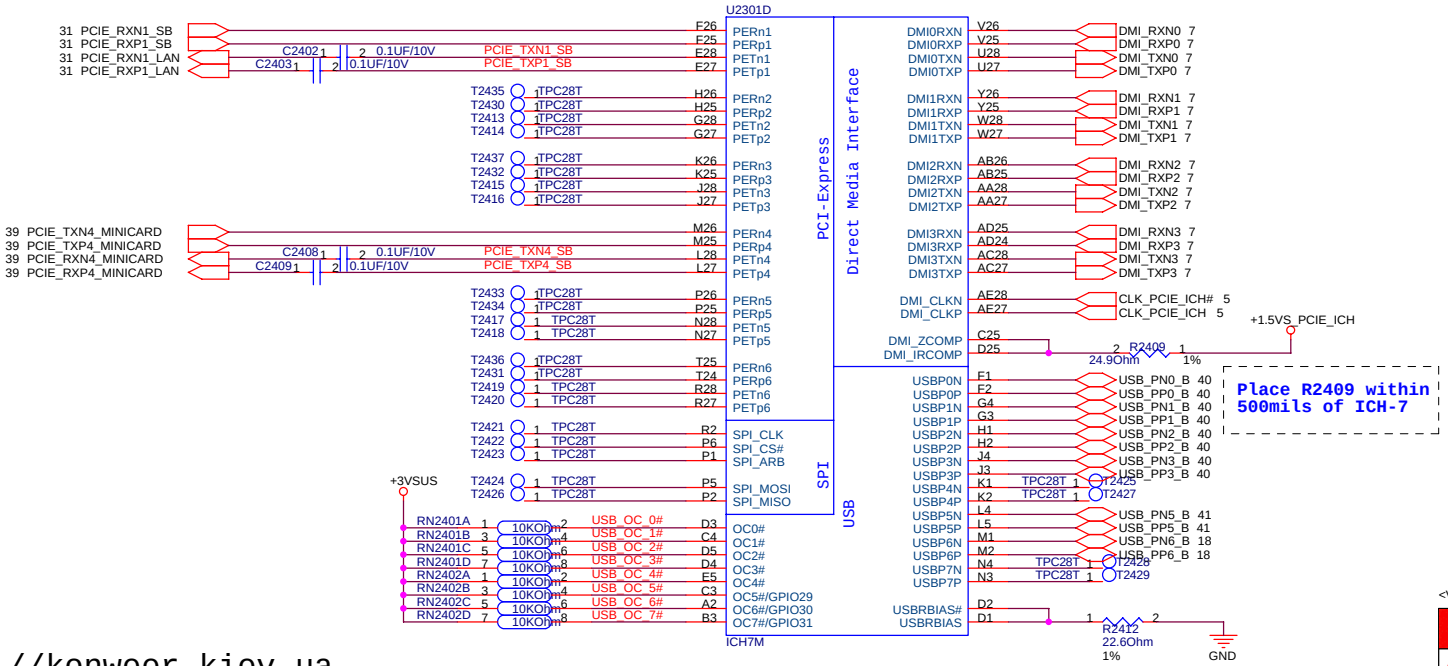
Title : ICH7-M (1/4)

Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 23 of 63





http://konweer.kiev.ua

<Variant Name>

ASUSTeK COMPUTER INC

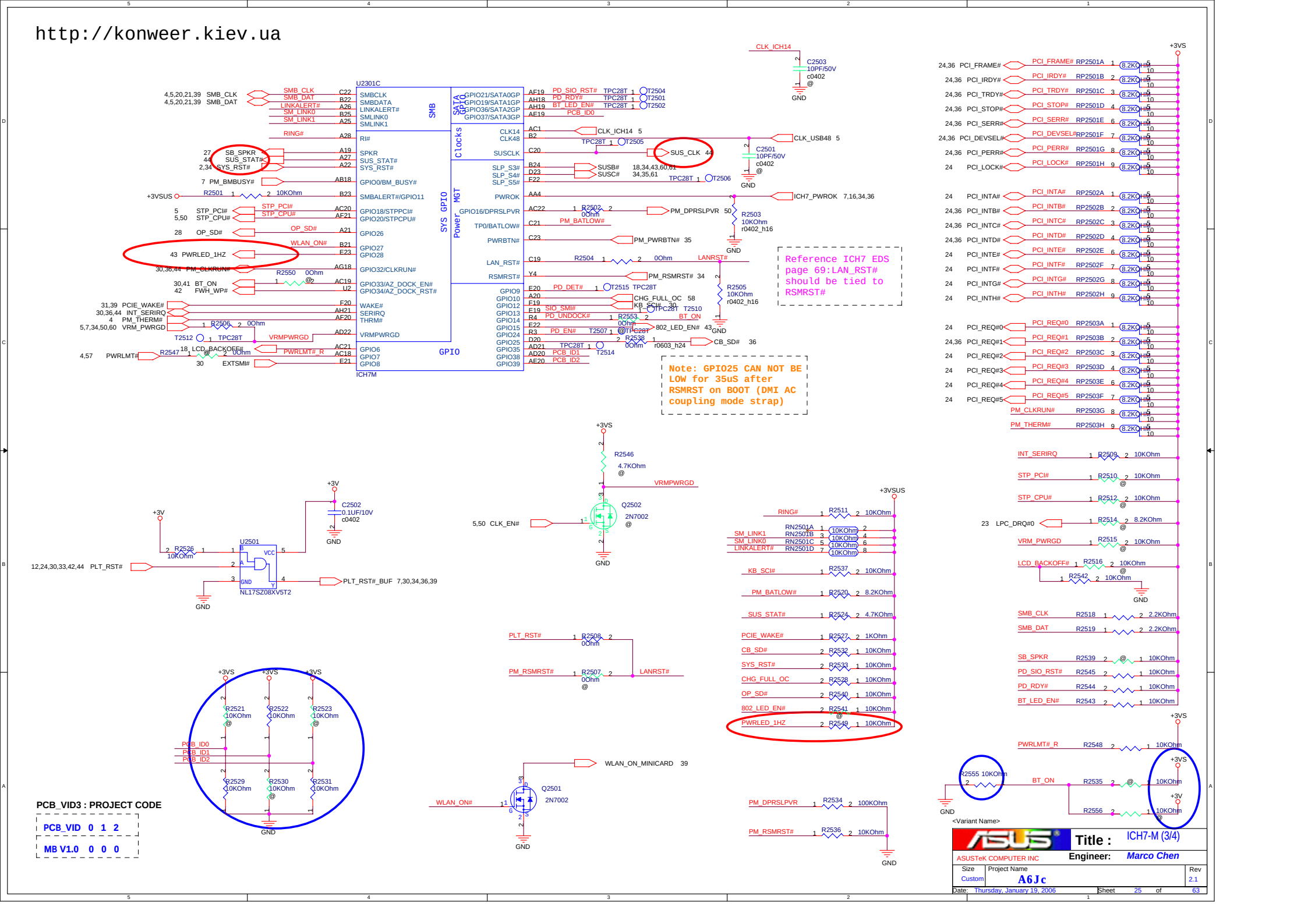
Title : ICH7-M (2/4)

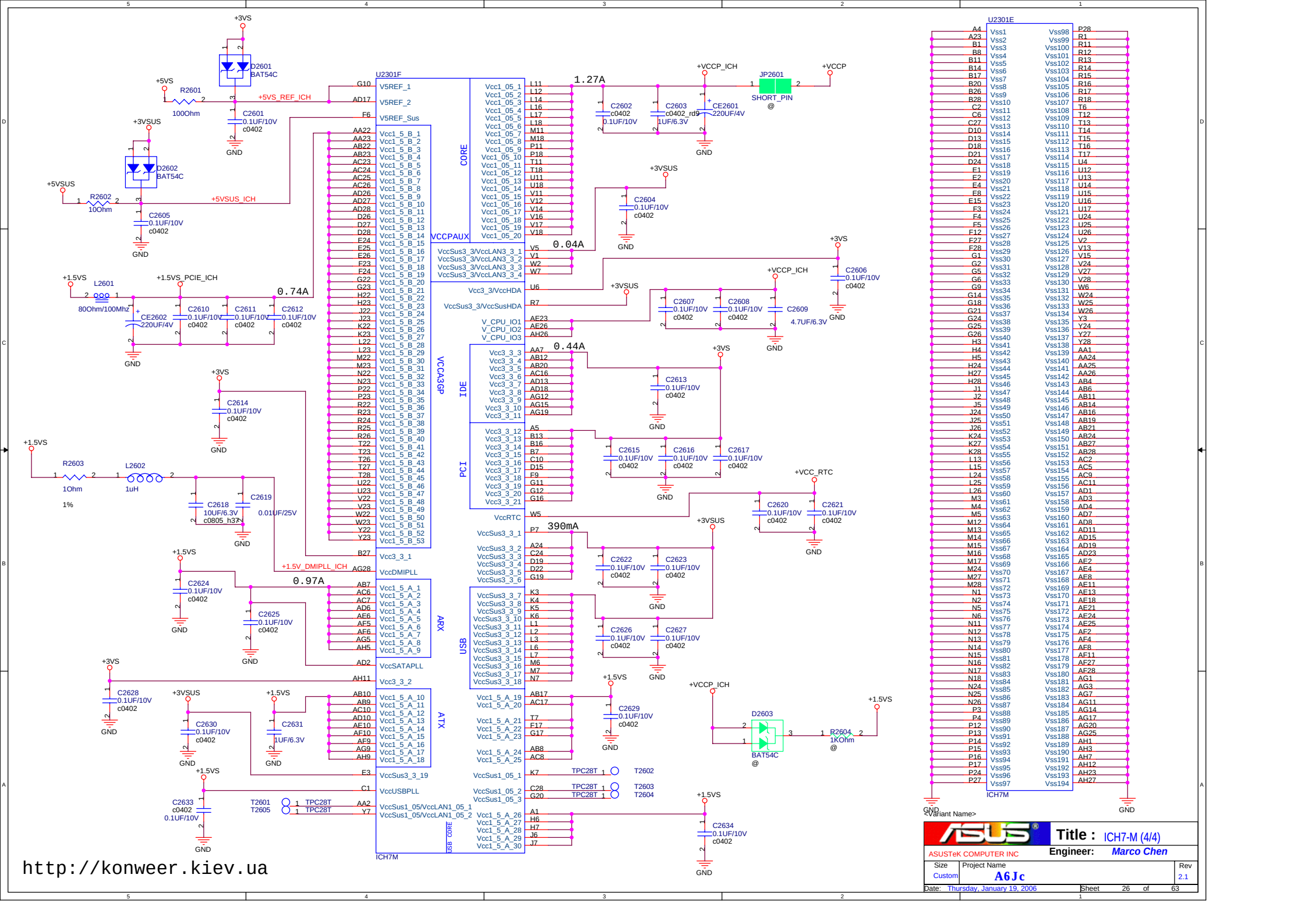
Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6Jc	2.1

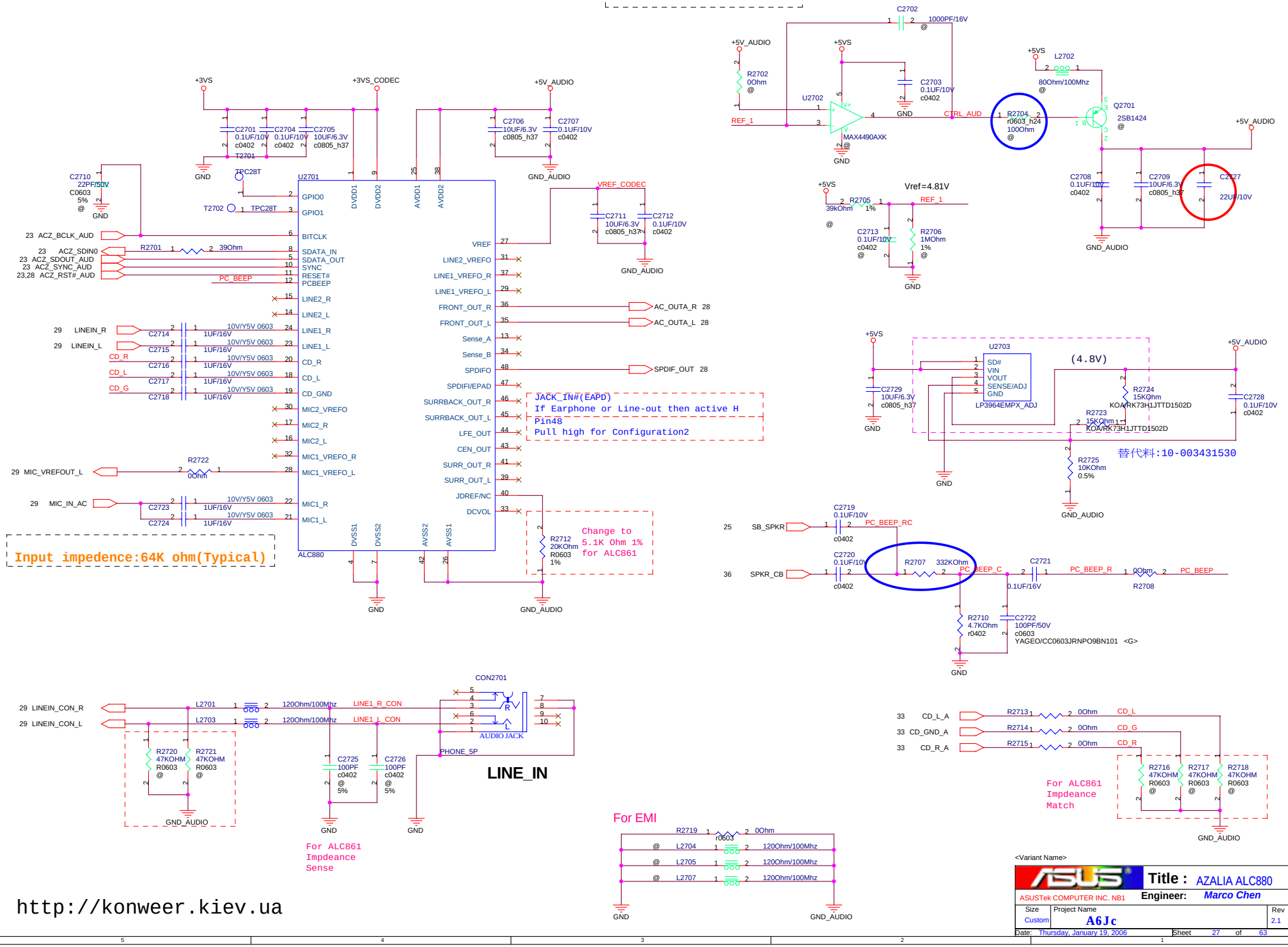
Date: Thursday, January 19, 2006 Sheet 24 of 63

http://konweer.kiev.ua




U2301F
U2301E
ICH7M
+3VS
+5VS
+5VSUS
+1.5VS
+3VSUS
+VCCP_ICH
+VCCP
+VCC_RTC
+1.5VS_PCIE_ICH
+5VS_REF_ICH
+5VSUS_ICH
+1.5V_DMIPLL_ICH
1.27A
0.74A
0.04A
0.44A
390mA
0.97A
CORE
VCCPAUX
VCCA3GP
IDE
PCI
ARX
USB
ATX
USB CORE
D2601 BAT54C
D2602 BAT54C
D2603 BAT54C
R2601 100Ohm
R2602 10Ohm
R2603 1Ohm 1%
R2604 1KOhm @
JP2601 SHORT_PIN @
L2601 80Ohm/100Mhz
L2602 1uH
C2601 0.1UF/10V c0402
C2602 c0402 0.1UF/10V
C2603 c0402_rd9 1UF/6.3V
CE2601 220UF/4V
C2604 0.1UF/10V c0402
C2605 0.1UF/10V c0402
C2606 0.1UF/10V c0402
C2607 0.1UF/10V c0402
C2608 0.1UF/10V c0402
C2609 4.7UF/6.3V
CE2602 220UF/4V
C2610 0.1UF/10V c0402
C2611 0.1UF/10V c0402
C2612 0.1UF/10V c0402
C2613 0.1UF/10V c0402
C2614 0.1UF/10V c0402
C2615 0.1UF/10V c0402
C2616 0.1UF/10V c0402
C2617 0.1UF/10V c0402
C2618 10UF/6.3V c0805_h32
C2619 0.01UF/25V
C2620 0.1UF/10V c0402
C2621 0.1UF/10V c0402
C2622 0.1UF/10V c0402
C2623 0.1UF/10V c0402
C2624 0.1UF/10V c0402
C2625 0.1UF/10V c0402
C2626 0.1UF/10V c0402
C2627 0.1UF/10V c0402
C2628 0.1UF/10V c0402
C2629 0.1UF/10V c0402
C2630 0.1UF/10V c0402
C2631 1UF/6.3V
C2633 0.1UF/10V c0402
C2634 0.1UF/10V c0402
T2601 TPC28T
T2602 TPC28T
T2603 TPC28T
T2604 TPC28T
T2605 TPC28T
GND
ICH7M
<Variant Name>
ASUSTeK COMPUTER INC
Title : ICH7-M (4/4)
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 26 of 63
http://konweer.kiev.ua

Place U2802near U2801



http://konweer.kiev.ua

<Variant Name>

ASUSTek COMPUTER INC. NB1

Title : AZALIA ALC880

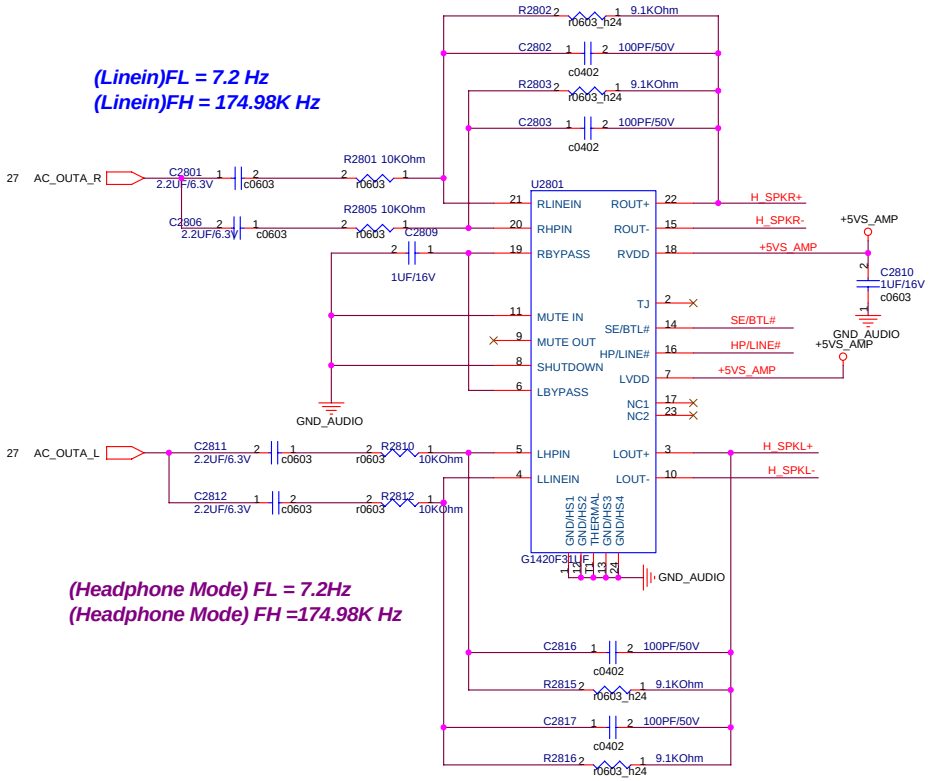
Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6Jc	2.1

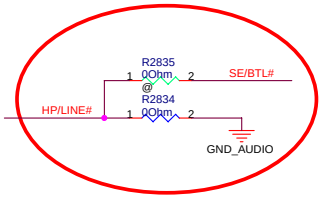
Date: Thursday, January 19, 2006 Sheet 27 of 63

http://konweer.kiev.ua

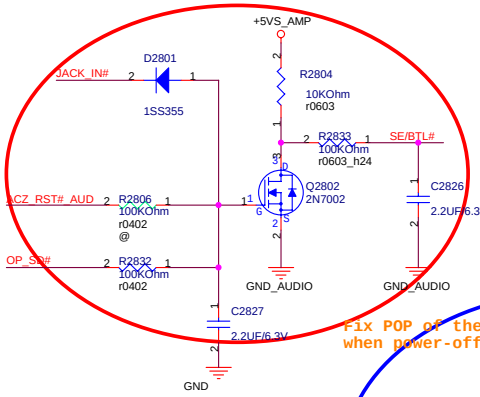
(Linein)FL = 7.2 Hz
(Linein)FH = 174.98K Hz

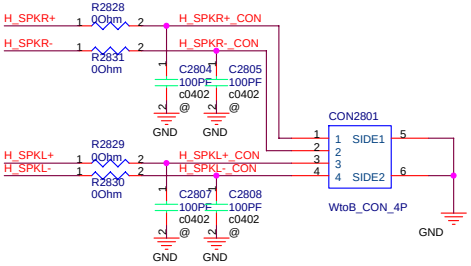


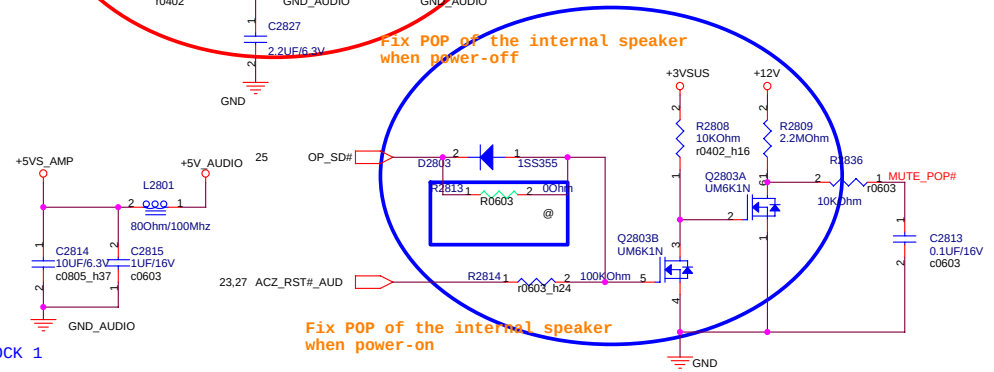
(Headphone Mode) FL = 7.2Hz
(Headphone Mode) FH =174.98K Hz



	SE/BTL#	SPDIF_IN
SPDIF Mode	H	Hi-Z
HP Mode	H	L
SPK Mode	L	X

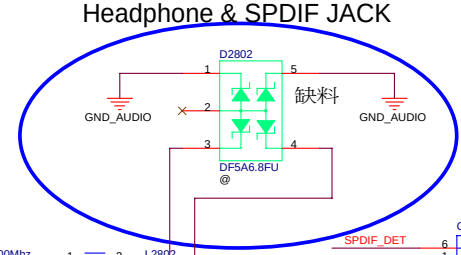


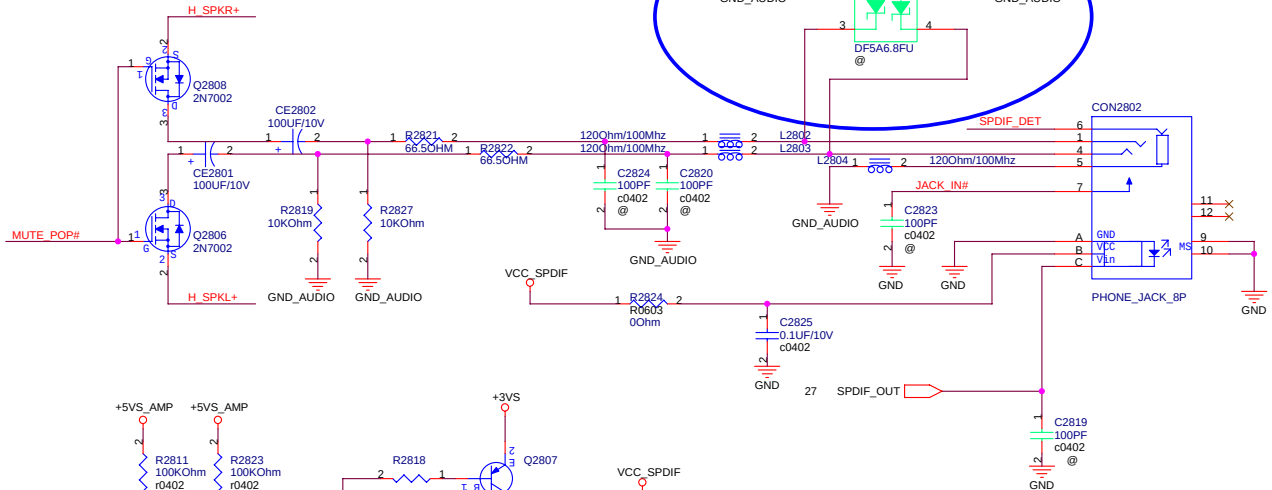


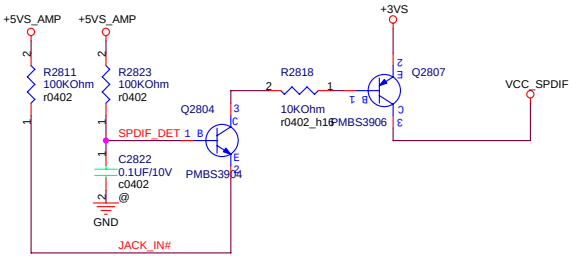


PR BlOCK 1

Headphone & SPDIF JACK

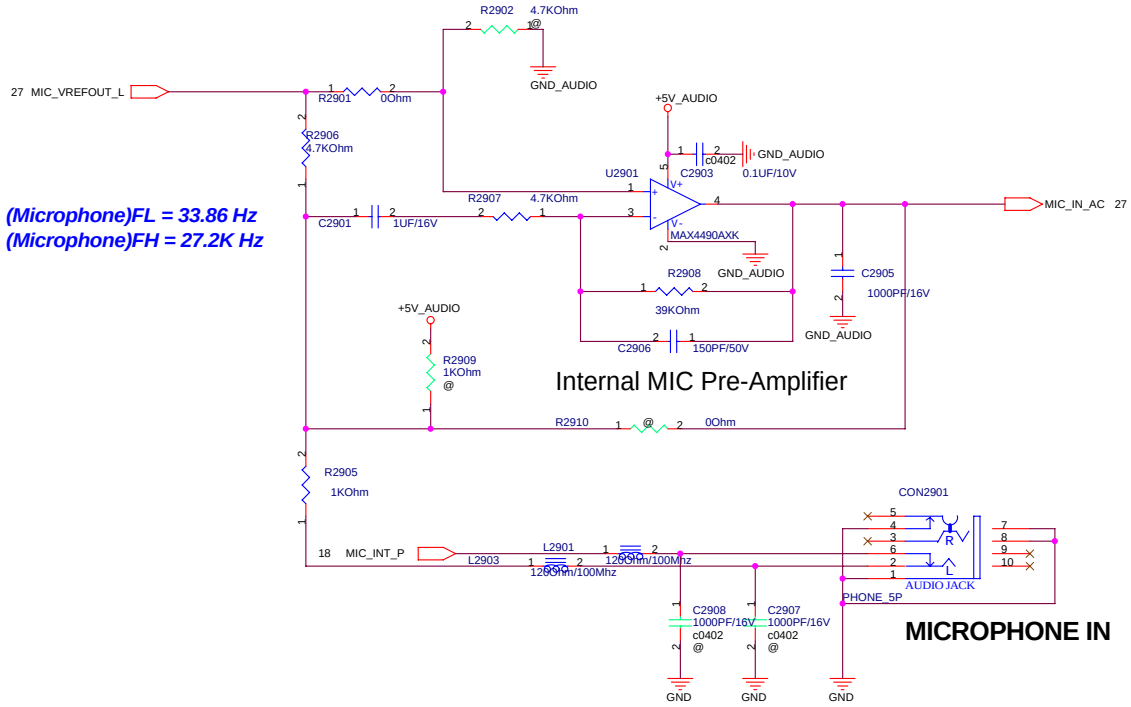


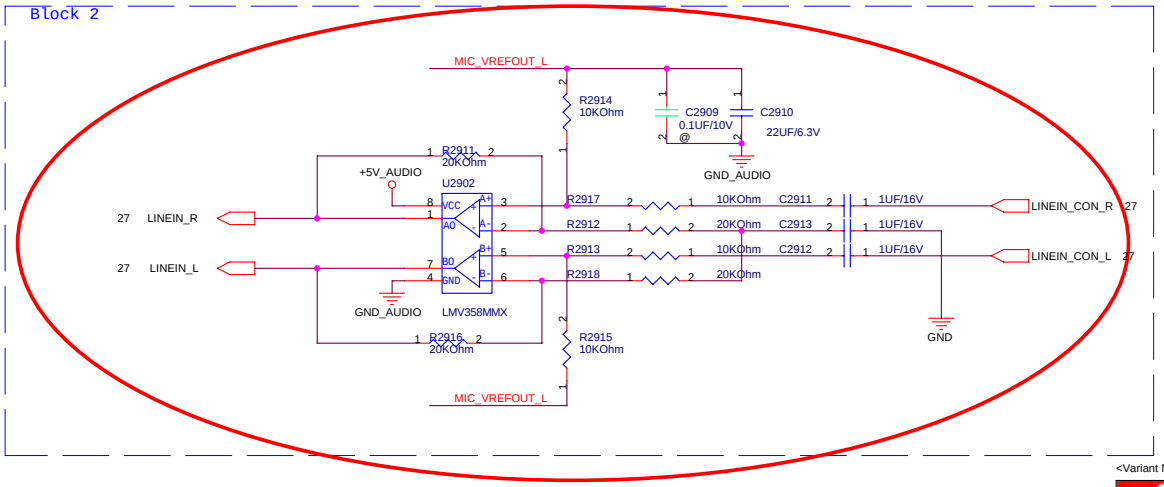




<Variant Name>

ASUSTeK COMPUTER INC	Title : Audio AMP	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 28 of 63	

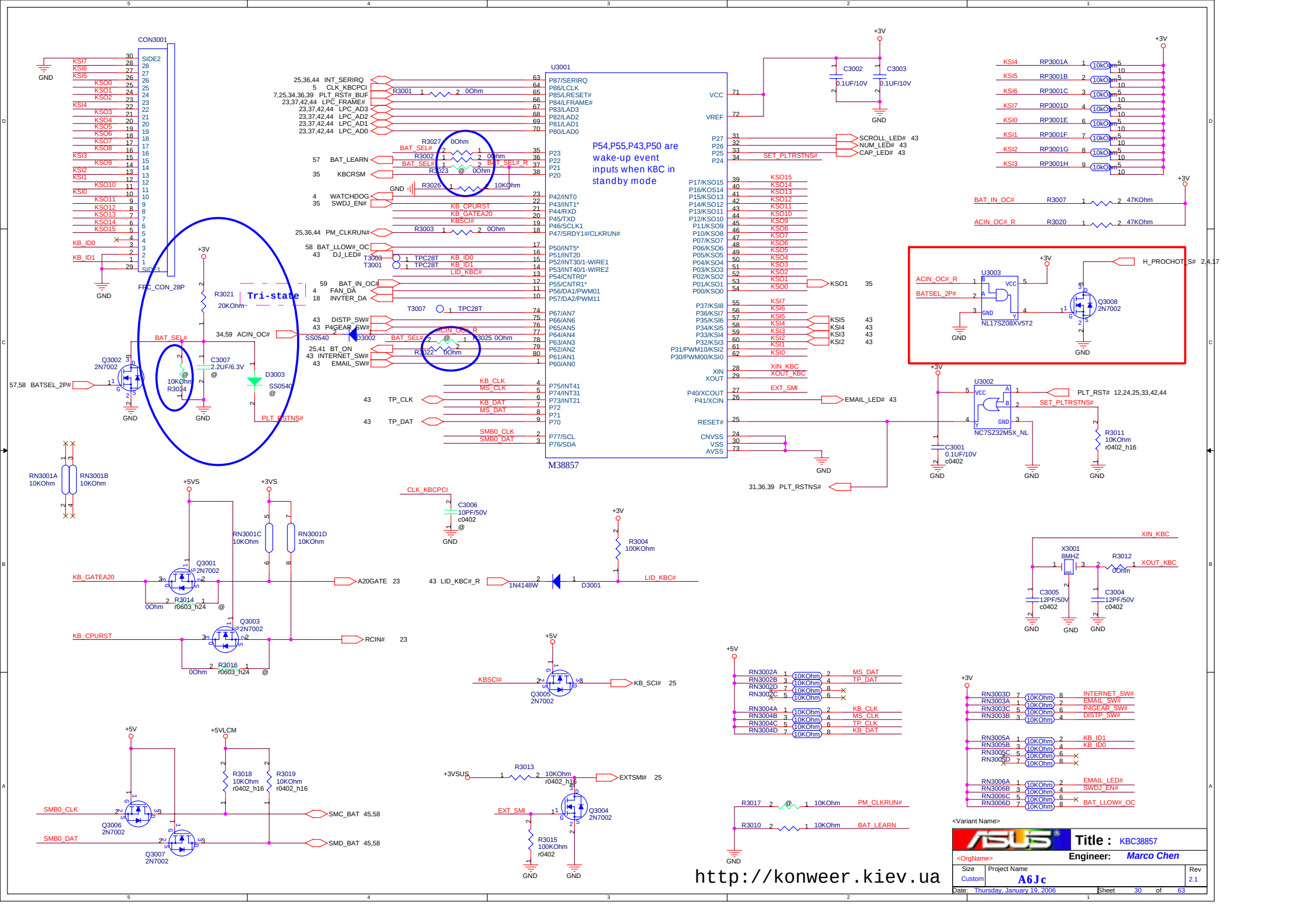




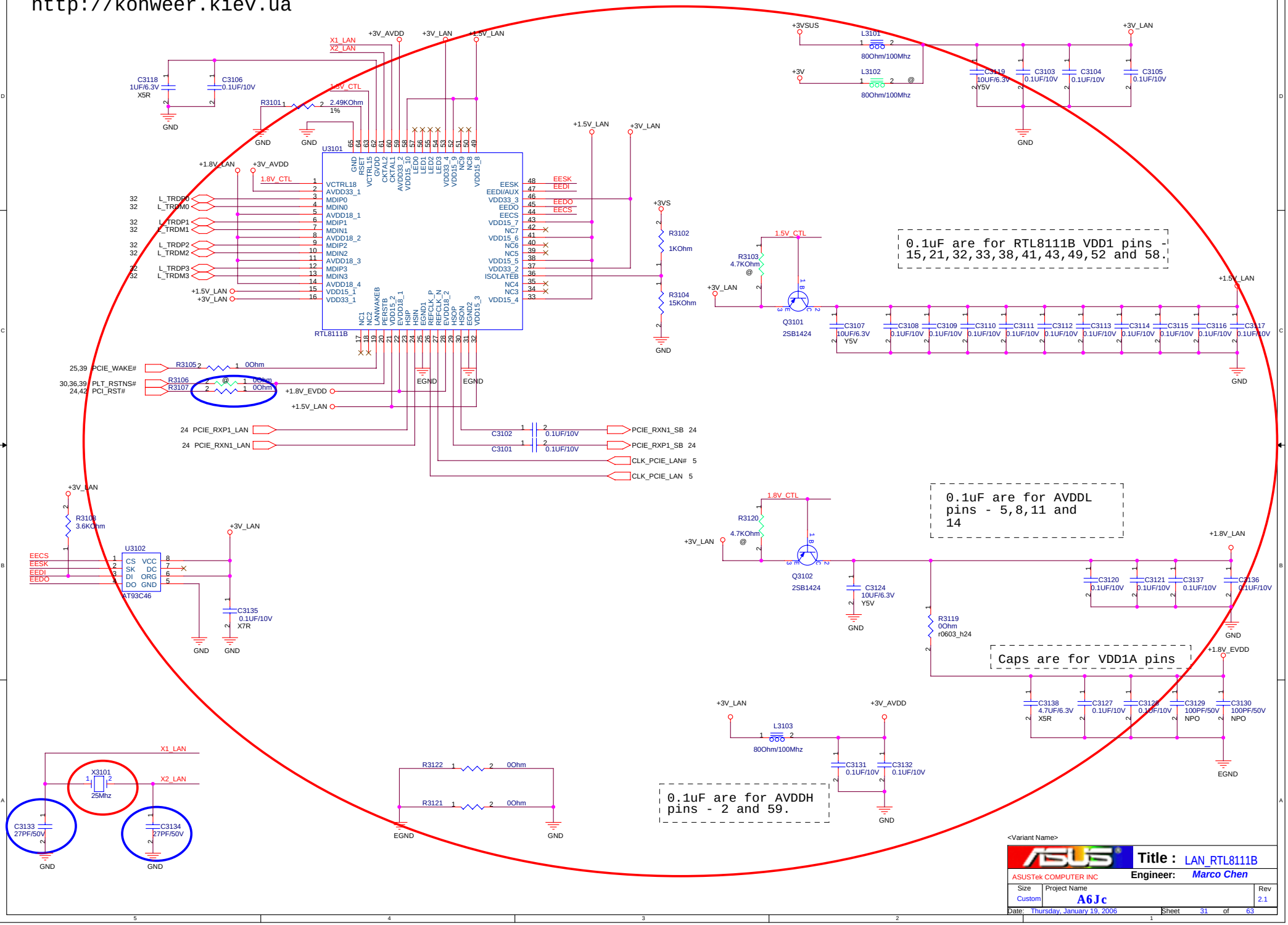
http://konweer.kiev.ua

<Variant Name>

ASUSTeK COMPUTER INC	Title : MICROPHONE	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 29 of 63	


CON3001
FRC_CON_28P
U3001
M38857
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
Tri-state
R3021 20KOhm
BAT_SEL#
ACIN_OC#
Q3002 2N7002
C3007 2.2UF/6.3V
D3003 SS0540
PLT_RSTNS#
D3002 SS0540
R3025 0Ohm
R3022 0Ohm
R3024 10KOhm
57,58 BATSEL_2P#
34,59 ACIN_OC#
RN3001A 10KOhm
RN3001B 10KOhm
RN3001C 10KOhm
RN3001D 10KOhm
Q3001 2N7002
Q3003 2N7002
KB_GATEA20
KB_CPURST
A20GATE 23
RCIN# 23
R3014 0Ohm r0603_h24
R3016 0Ohm r0603_h24
CLK_KBCPCI
C3006 10PF/50V c0402
R3004 100KOhm
43 LID_KBC#_R
1N4148W
D3001
LID_KBC#
KBSCI#
Q3005 2N7002
KB_SCI# 25
R3027 0Ohm
R3002 0Ohm
R3023 0Ohm
R3026 10KOhm
R3003 0Ohm
T3003 TPC28T
T3001 TPC28T
T3007 TPC28T
KB_ID0
KB_ID1
LID_KBC#
KB_CLK
MS_CLK
KB_DAT
MS_DAT
SMB0_CLK
SMB0_DAT
43 TP_CLK
43 TP_DAT
25,36,44 INT_SERIRQ
5 CLK_KBCPCI
7,25,34,36,39 PLT_RST#_BUF
23,37,42,44 LPC_FRAME#
23,37,42,44 LPC_AD3
23,37,42,44 LPC_AD2
23,37,42,44 LPC_AD1
23,37,42,44 LPC_AD0
57 BAT_LEARN
35 KBCRSM
4 WATCHDOG
35 SWDJ_EN#
25,36,44 PM_CLKRUN#
58 BAT_LLOW#_OC
43 DJ_LED#
59 BAT_IN_OC#
4 FAN_DA
18 INVTER_DA
43 DISTP_SW#
43 P4GEAR_SW#
25,41 BT_ON
43 INTERNET_SW#
43 EMAIL_SW#
SCROLL_LED# 43
NUM_LED# 43
CAP_LED# 43
SET_PLTRSTNS#
KSO15
KSO14
KSO13
KSO12
KSO11
KSO10
KSO9
KSO8
KSO7
KSO6
KSO5
KSO4
KSO3
KSO2
KSO1
KSO0
KSO1 35
KSI7
KSI6
KSI5
KSI4
KSI3
KSI2
KSI1
KSI0
KSI5 43
KSI4 43
KSI3 43
KSI2 43
XIN_KBC
XOUT_KBC
EXT_SMI
EMAIL_LED# 43
RESET#
31,36,39 PLT_RSTNS#
C3002 0.1UF/10V
C3003 0.1UF/10V
C3001 0.1UF/10V c0402
U3002 NC7SZ32M5X_NL
PLT_RST# 12,24,25,33,42,44
SET_PLTRSTNS#
R3011 10KOhm r0402_h16
RP3001A 10KOhm
RP3001B 10KOhm
RP3001C 10KOhm
RP3001D 10KOhm
RP3001E 10KOhm
RP3001F 10KOhm
RP3001G 10KOhm
RP3001H 10KOhm
BAT_IN_OC# R3007 47KOhm
ACIN_OC#_R R3020 47KOhm
ACIN_OC#_R
BATSEL_2P#
U3003 NL17SZ08XV5T2
Q3008 2N7002
H_PROCHOT_S# 2,4,17
X3001 8MHZ
R3012 0Ohm
C3005 12PF/50V c0402
C3004 12PF/50V c0402
XIN_KBC
XOUT_KBC
RN3002A MS_DAT
RN3002B TP_DAT
RN3002C
RN3002D
RN3004A KB_CLK
RN3004B MS_CLK
RN3004C TP_CLK
RN3004D KB_DAT
RN3003D INTERNET_SW#
RN3003A EMAIL_SW#
RN3003C P4GEAR_SW#
RN3003B DISTP_SW#
RN3005A KB_ID1
RN3005B KB_ID0
RN3005C
RN3005D
RN3006A EMAIL_LED#
RN3006B SWDJ_EN#
RN3006C
RN3006D BAT_LLOW#_OC
R3017 10KOhm PM_CLKRUN#
R3010 10KOhm BAT_LEARN
R3013 10KOhm r0402_h16
EXTSMI# 25
R3015 100KOhm r0402
Q3004 2N7002
Q3006 2N7002
Q3007 2N7002
R3018 10KOhm r0402_h16
R3019 10KOhm r0402_h16
SMC_BAT 45,58
SMD_BAT 45,58
+3V
+5V
+5VS
+3VS
+5VLCM
+3VSUS
GND
http://konweer.kiev.ua
Title : KBC38857
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 30 of 63

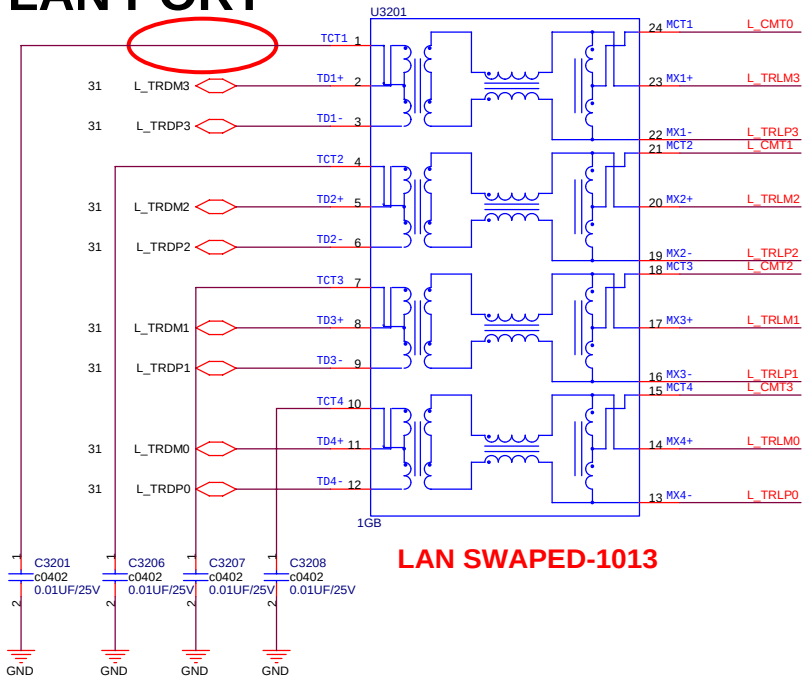
http://konweer.kiev.ua



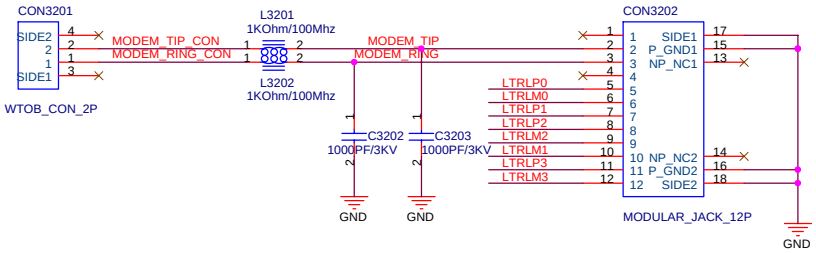
<Variant Name>

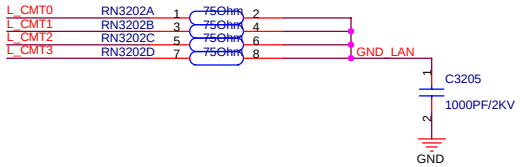
ASUSTek COMPUTER INC	Title : LAN_RTL8111B	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 31 of 63	

LAN PORT

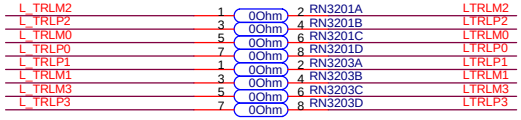


LAN SWAPED-1013

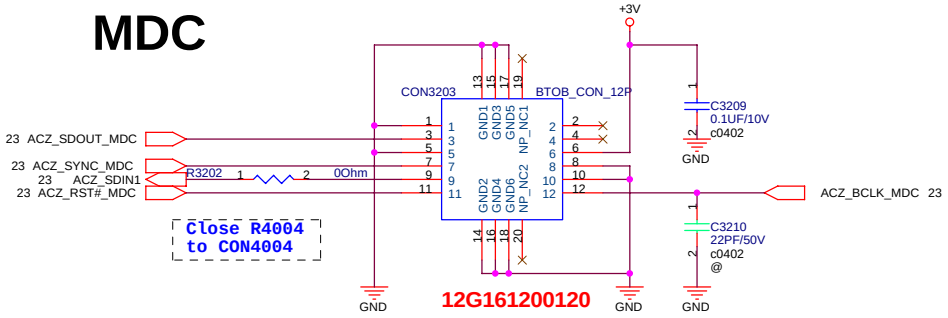


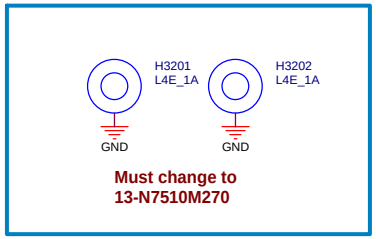


FOR EMI



MDC

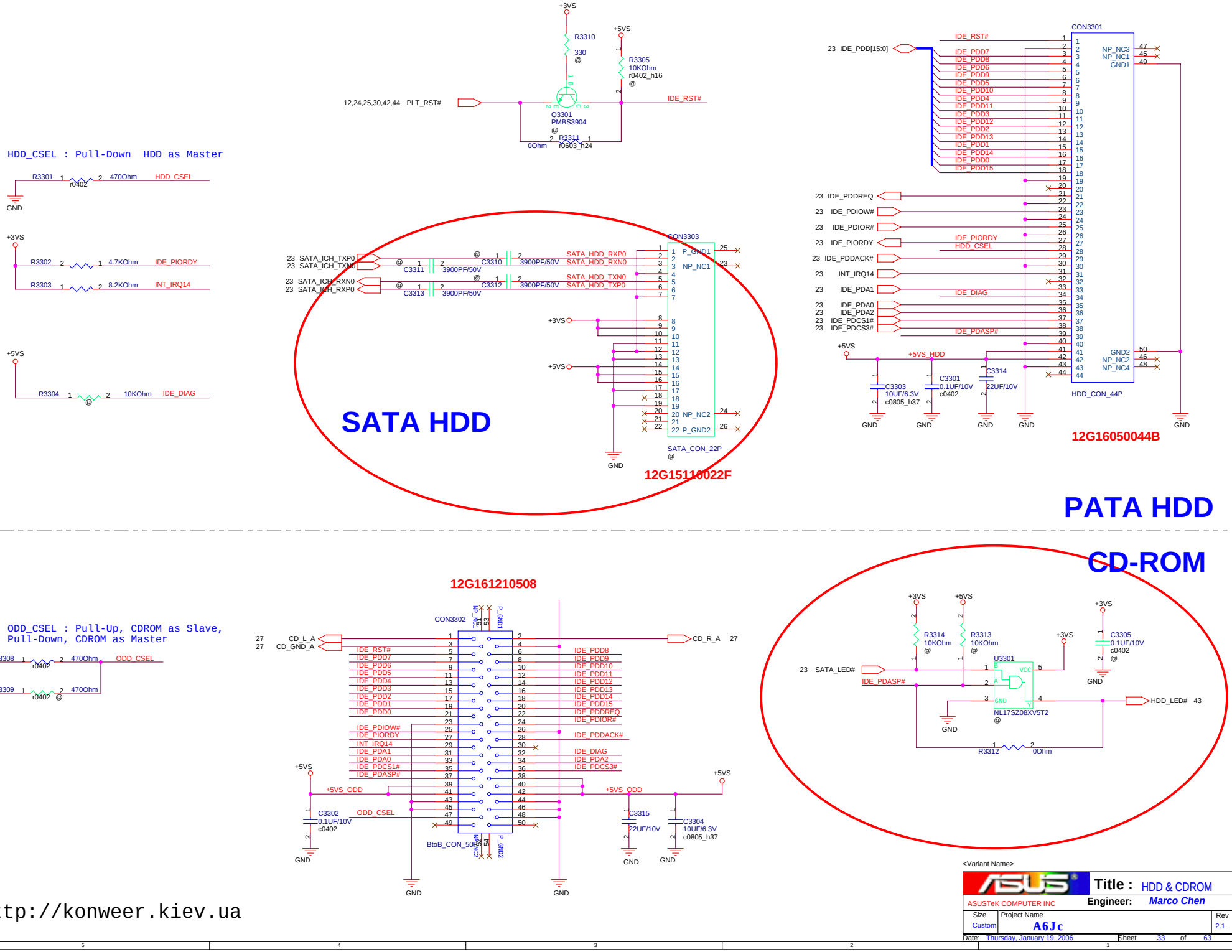




http://konweer.kiev.ua

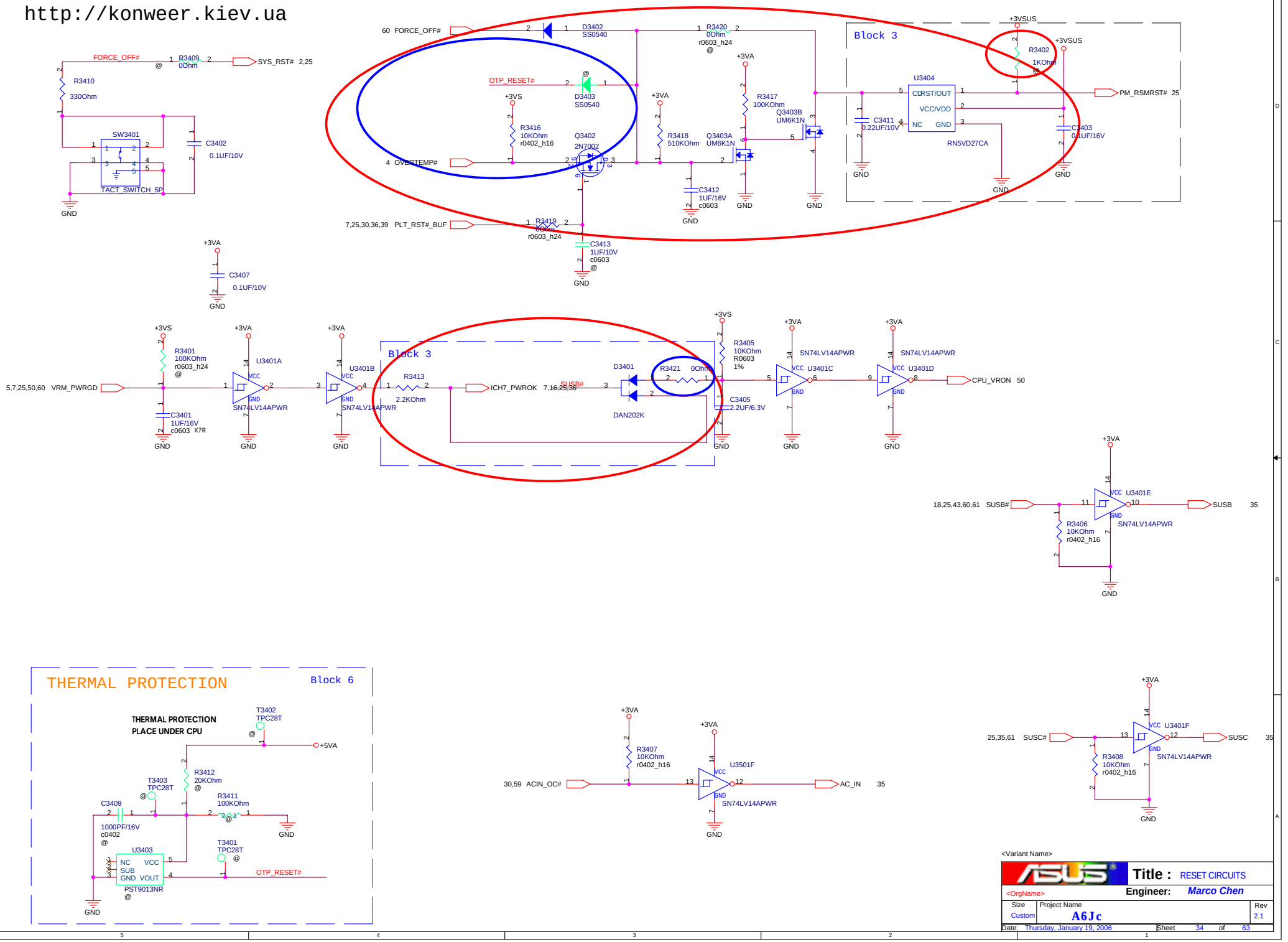
<Variant Name>

ASUSTeK COMPUTER INC	Title : RJ11+45,MDC	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 32 of 63	



http://konweer.kiev.ua

http://konweer.kiev.ua



<Variant Name>

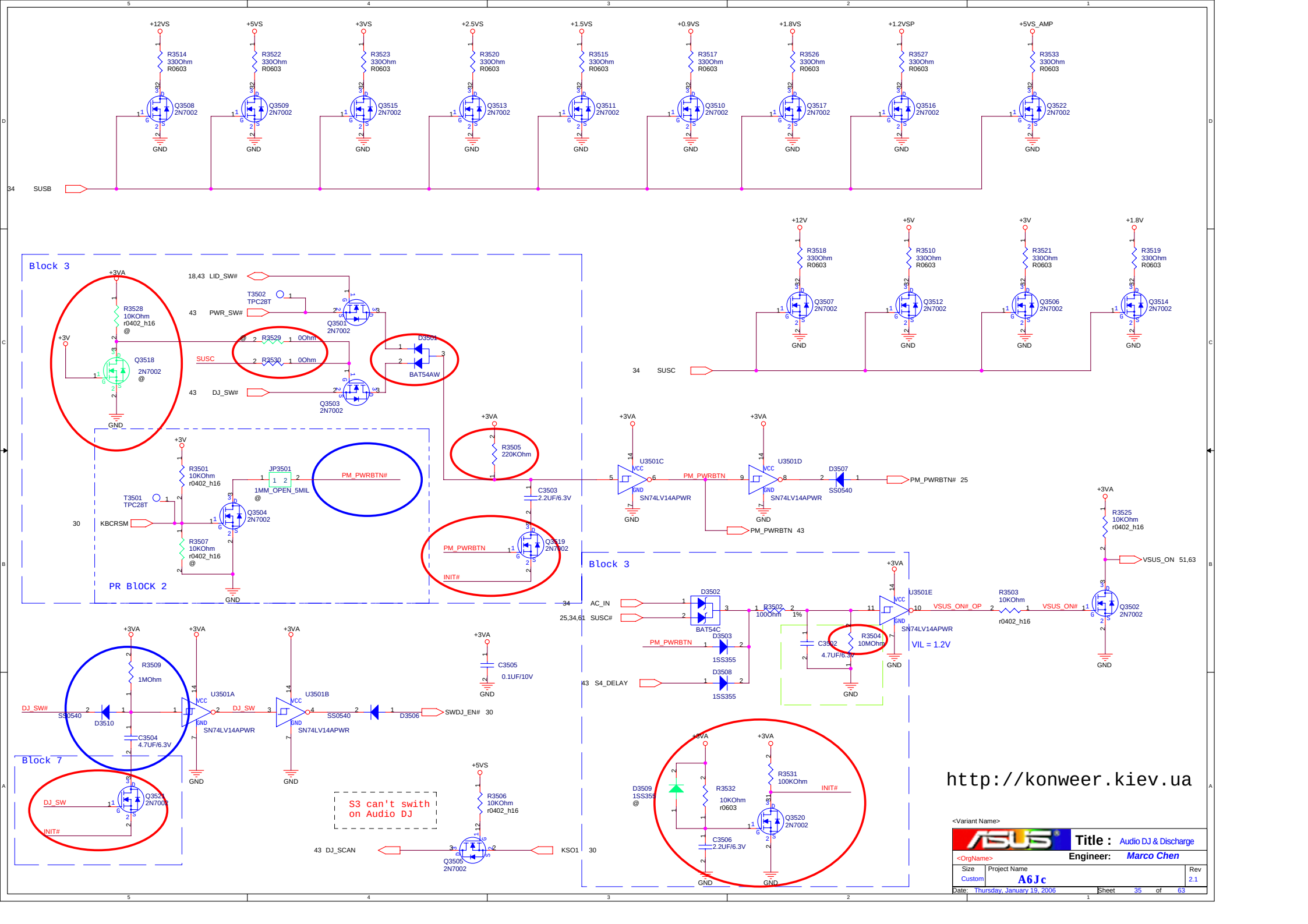
Title : RESET CIRCUITS

<OrgName>

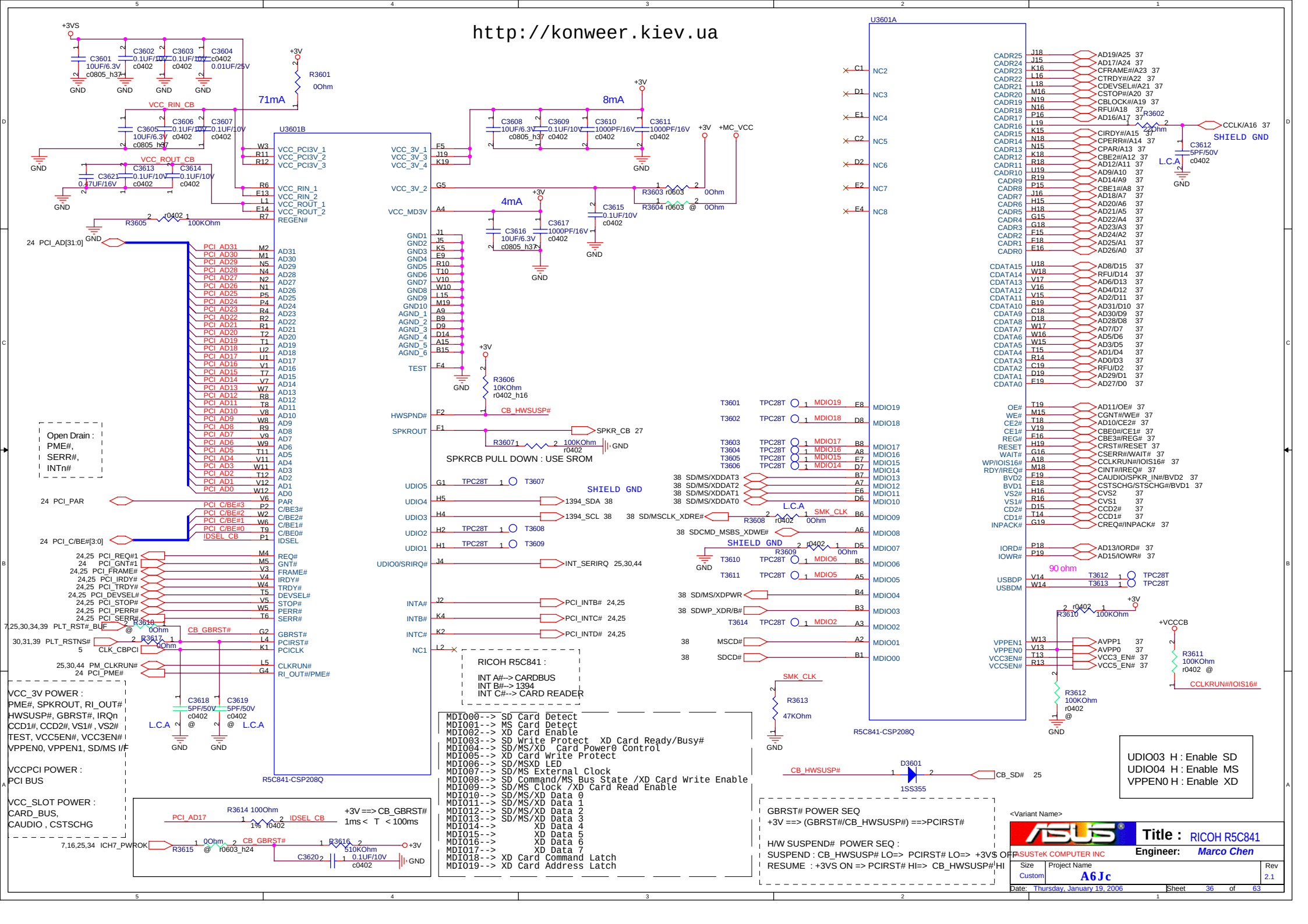
Engineer: Marco Chen

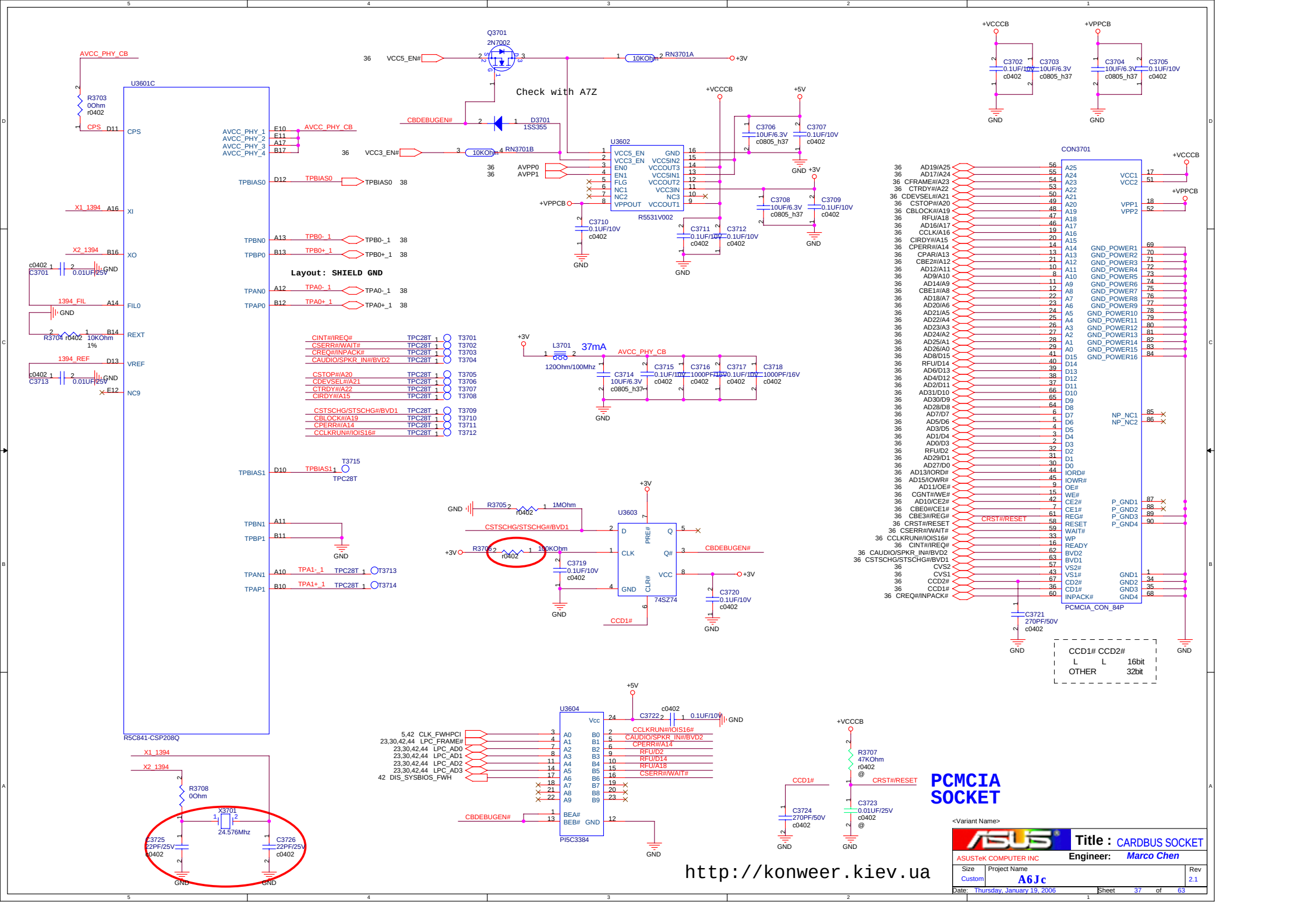
Size	Project Name	Rev
Custom	A6Jc	2.1

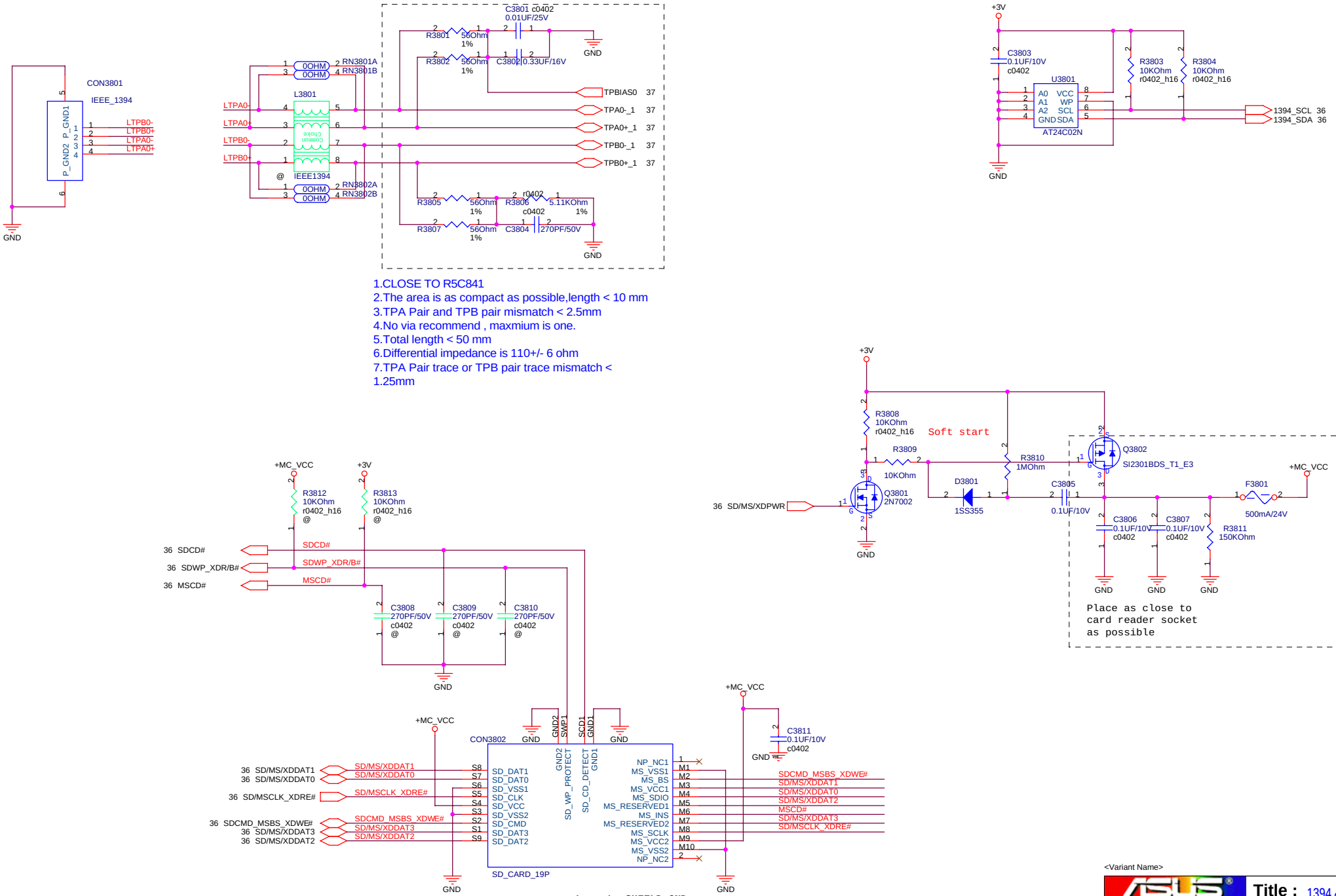
Date: Thursday, January 19, 2006 Sheet 34 of 63

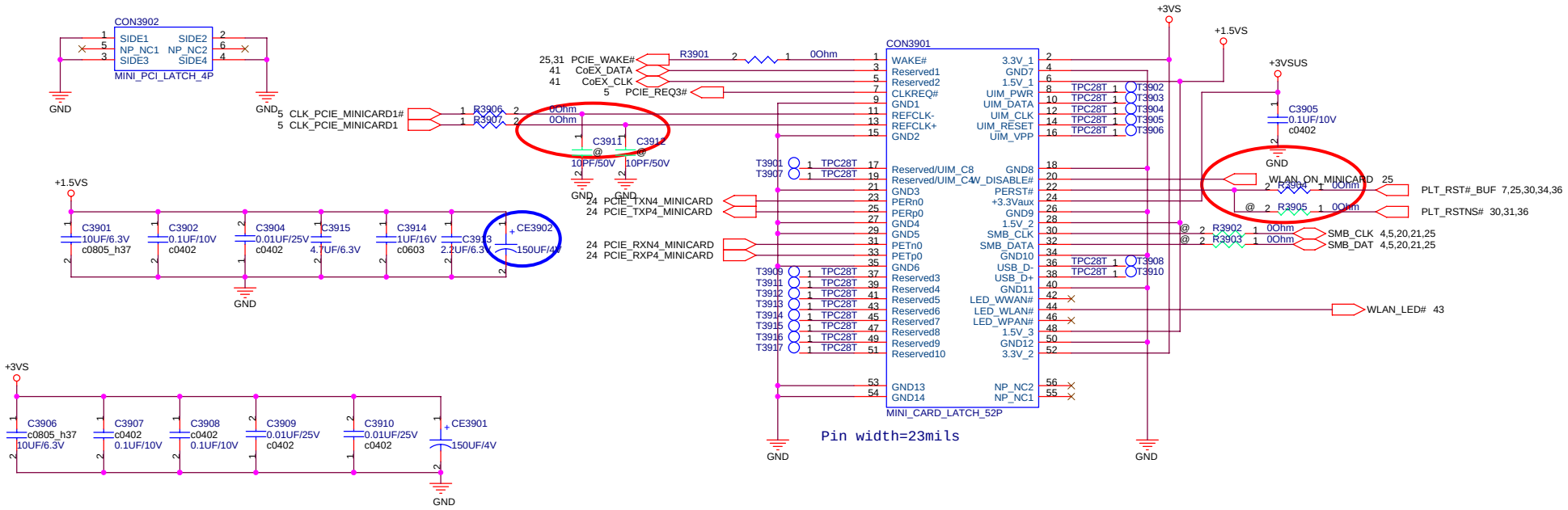

+12VS
+5VS
+3VS
+2.5VS
+1.5VS
+0.9VS
+1.8VS
+1.2VSP
+5VS_AMP
R3514 330Ohm R0603
R3522 330Ohm R0603
R3523 330Ohm R0603
R3520 330Ohm R0603
R3515 330Ohm R0603
R3517 330Ohm R0603
R3526 330Ohm R0603
R3527 330Ohm R0603
R3533 330Ohm R0603
Q3508 2N7002
Q3509 2N7002
Q3515 2N7002
Q3513 2N7002
Q3511 2N7002
Q3510 2N7002
Q3517 2N7002
Q3516 2N7002
Q3522 2N7002
GND
34 SUSB
+12V
+5V
+3V
+1.8V
R3518 330Ohm R0603
R3510 330Ohm R0603
R3521 330Ohm R0603
R3519 330Ohm R0603
Q3507 2N7002
Q3512 2N7002
Q3506 2N7002
Q3514 2N7002
34 SUSC
Block 3
+3VA
18,43 LID_SW#
T3502 TPC28T
43 PWR_SW#
R3528 10KOhm r0402_h16 @
+3V
Q3518 2N7002 @
SUSC
R3529 0Ohm
R3530 0Ohm
43 DJ_SW#
Q3501 2N7002
Q3503 2N7002
D3501
BAT54AW
R3505 220KOhm
C3503 2.2UF/6.3V
PR BLOCK 2
R3501 10KOhm r0402_h16
JP3501 1MM_OPEN_5MIL @
PM_PWRBTN#
T3501 TPC28T
30 KBCRSM
Q3504 2N7002
R3507 10KOhm r0402_h16 @
PM_PWRBTN
INIT#
Q3519 2N7002
U3501C
U3501D
SN74LV14APWR
D3507 SS0540
PM_PWRBTN# 25
PM_PWRBTN 43
Block 3
AC_IN
25,34,61 SUSC#
D3502 BAT54C
D3503 1SS355
43 S4_DELAY
D3508 1SS355
R3502 100Ohm 1%
U3501E
VSUS_ON#_OP
R3504 10MOhm
C3502 4.7UF/6.3V
VIL = 1.2V
R3503 10KOhm r0402_h16
VSUS_ON#
R3525 10KOhm r0402_h16
VSUS_ON 51,63
Q3502 2N7002
R3509 1MOhm
U3501A
U3501B
DJ_SW#
SS0540
D3510
C3504 4.7UF/6.3V
DJ_SW
D3506
SWDJ_EN# 30
C3505 0.1UF/10V
Block 7
Q3521 2N7002
INIT#
S3 can't swith on Audio DJ
+5VS
R3506 10KOhm r0402_h16
43 DJ_SCAN
Q3505 2N7002
KSO1 30
D3509 1SS355 @
R3532 10KOhm r0603
R3531 100KOhm
C3506 2.2UF/6.3V
Q3520 2N7002
http://konweer.kiev.ua
<Variant Name>
Title : Audio DJ & Discharge
<OrgName>
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 35 of 63

http://konweer.kiev.ua




U3601C
R5C841-CSP208Q
Q3701
2N7002
Check with A7Z
U3602
R5531V002
CON3701
PCMCIA_CON_84P
U3603
74SZ74
U3604
PI5C3384
Layout: SHIELD GND
CCD1# CCD2#
L L 16bit
OTHER 32bit
PCMCIA SOCKET
Title : CARDBUS SOCKET
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Project Name A6Jc
Date: Thursday, January 19, 2006
http://konweer.kiev.ua


CON3801
IEEE_1394
P_GND1
P_GND2
LTPB0-
LTPB0+
LTPA0-
LTPA0+
GND
C3801 c0402
0.01UF/25V
R3801 56Ohm 1%
R3802 56Ohm 1%
C3802 0.33UF/16V
TPBIAS0 37
TPA0-_1 37
TPA0+_1 37
TPB0-_1 37
TPB0+_1 37
RN3801A
RN3801B
RN3802A
RN3802B
0OHM
L3801
Common Choke
IEEE1394
R3805 56Ohm 1%
R3806 r0402 c0402 5.11KOhm 1%
R3807 56Ohm 1%
C3804 270PF/50V
+3V
C3803 0.1UF/10V c0402
U3801
A0 A1 A2 GND VCC WP SCL SDA
AT24C02N
R3803 10KOhm r0402_h16
R3804 10KOhm r0402_h16
1394_SCL 36
1394_SDA 36
1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm
R3808 10KOhm r0402_h16
Soft start
R3809 10KOhm
Q3801 2N7002
D3801 1SS355
R3810 1MOhm
C3805 0.1UF/10V
Q3802 SI2301BDS_T1_E3
F3801 500mA/24V
C3806 0.1UF/10V c0402
C3807 0.1UF/10V c0402
R3811 150KOhm
36 SD/MS/XDPWR
Place as close to card reader socket as possible
+MC_VCC
R3812 10KOhm r0402_h16 @
R3813 10KOhm r0402_h16 @
36 SDCD#
36 SDWP_XDR/B#
36 MSCD#
C3808 270PF/50V c0402 @
C3809 270PF/50V c0402 @
C3810 270PF/50V c0402 @
CON3802
SD_CARD_19P
SD_DAT1
SD_DAT0
SD_VSS1
SD_CLK
SD_VCC
SD_VSS2
SD_CMD
SD_DAT3
SD_DAT2
SD_WP_PROTECT
SD_CD_DETECT
NP_NC1
MS_VSS1
MS_BS
MS_VCC1
MS_SDIO
MS_RESERVED1
MS_INS
MS_RESERVED2
MS_SCLK
MS_VCC2
MS_VSS2
NP_NC2
36 SD/MS/XDDAT1
36 SD/MS/XDDAT0
36 SD/MSCLK_XDRE#
36 SDCMD_MSBS_XDWE#
36 SD/MS/XDDAT3
36 SD/MS/XDDAT2
SDCMD_MSBS_XDWE#
MSCD#
C3811 0.1UF/10V c0402
Layout: SHIELD GND
http://konweer.kiev.ua
<Variant Name>
Title : 1394 & 3 IN 1 CON
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 38 of 63

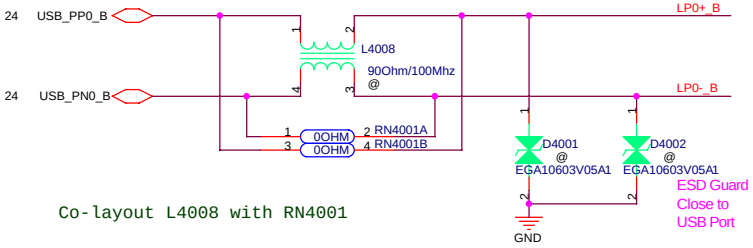


http://konweer.kiev.ua

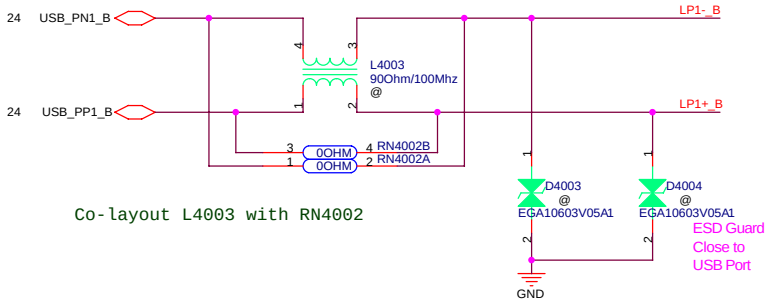
<Variant Name>

ASUSTeK COMPUTER INC	Title : MINICARD (Golan)	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 39 of 63	

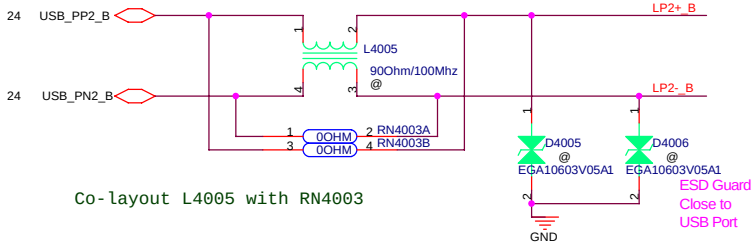
http://konweer.kiev.ua



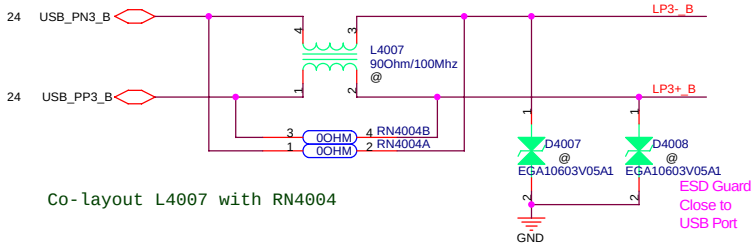
Co-layout L4008 with RN4001



Co-layout L4003 with RN4002

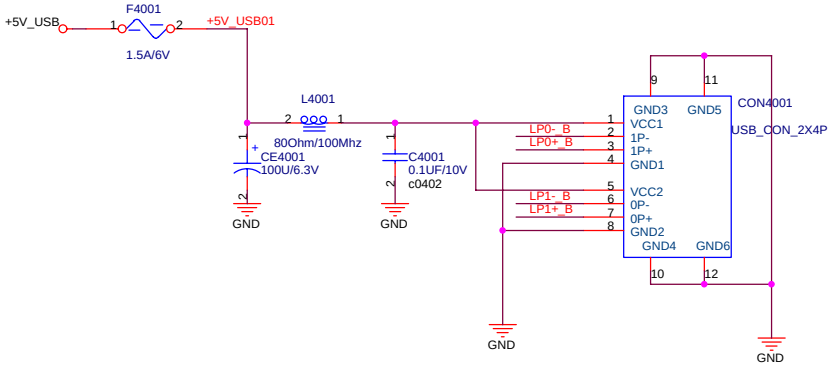


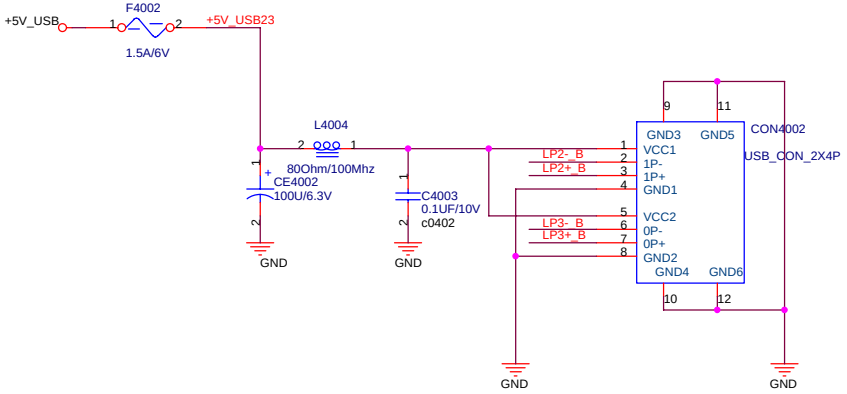
Co-layout L4005 with RN4003

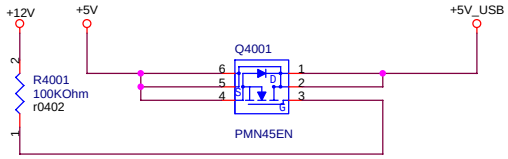


Co-layout L4007 with RN4004

4P2R array resister
co-layout with comman choke







<Variant Name>

ASUSTeK COMPUTER INC

Title : USB CONN X 4

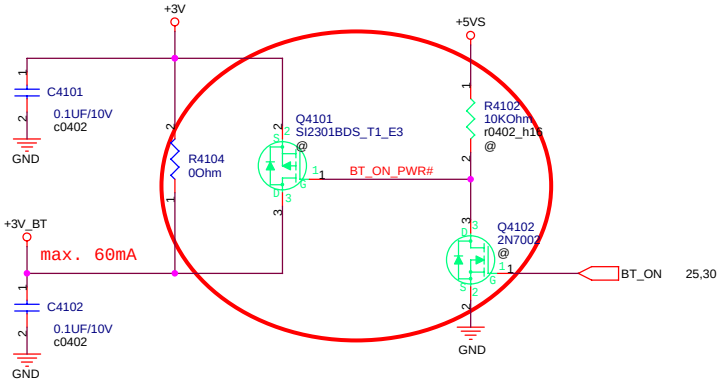
Engineer: Marco Chen

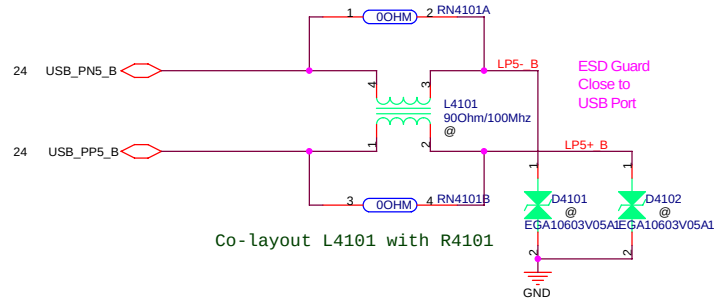
Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 40 of 63

http://konweer.kiev.ua

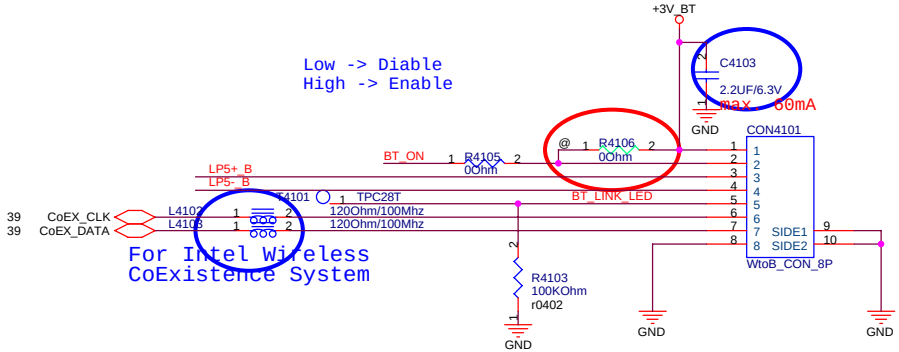
BT ON/OFF Control





Co-layout L4101 with R4101

Bluetooth Module

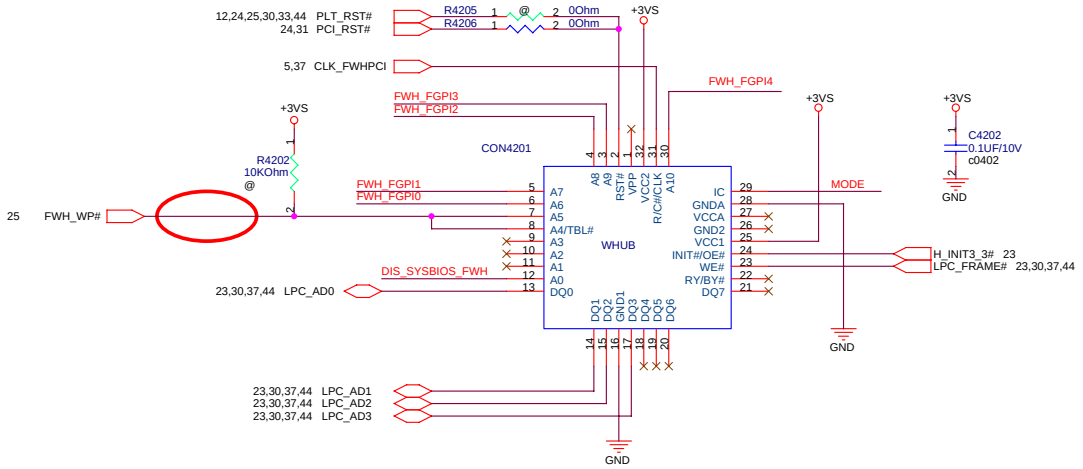


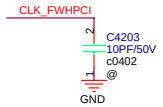
For Intel Wireless CoExistence System

<Variant Name>

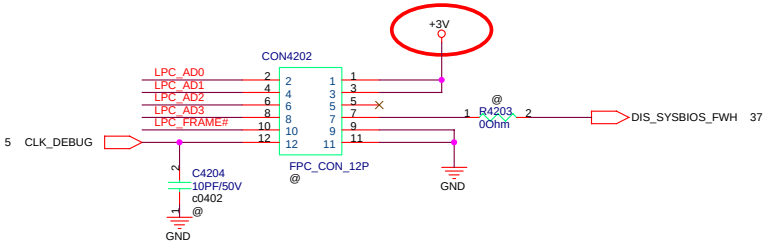
ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 41 of 63	

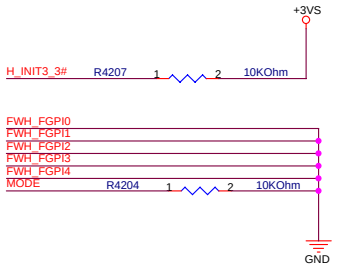
http://konweer.kiev.ua





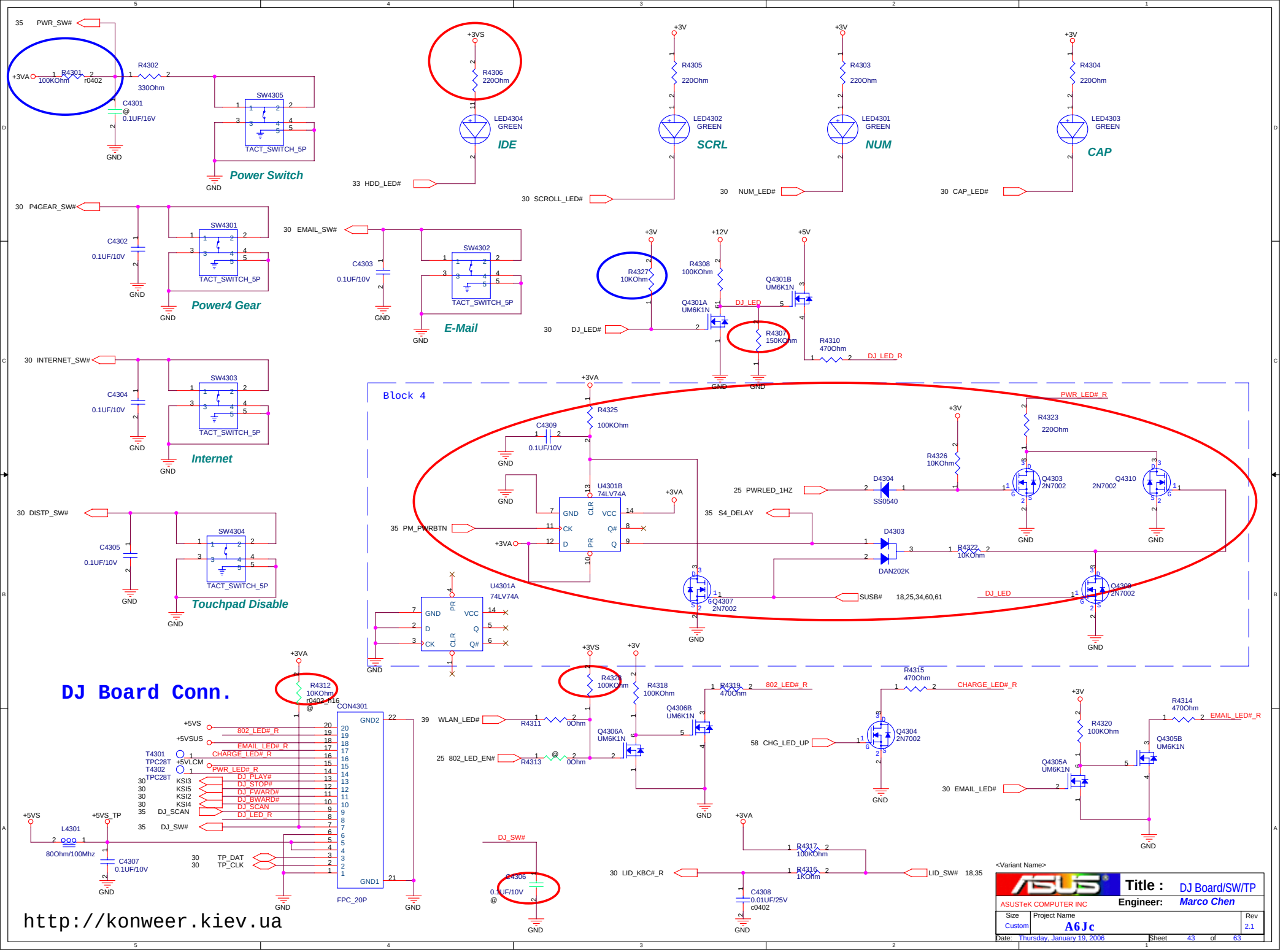
PLCC32 Socket Part Number : 12-043000323
SST FWH/LPC Part Number : 05G00101712L(燒)



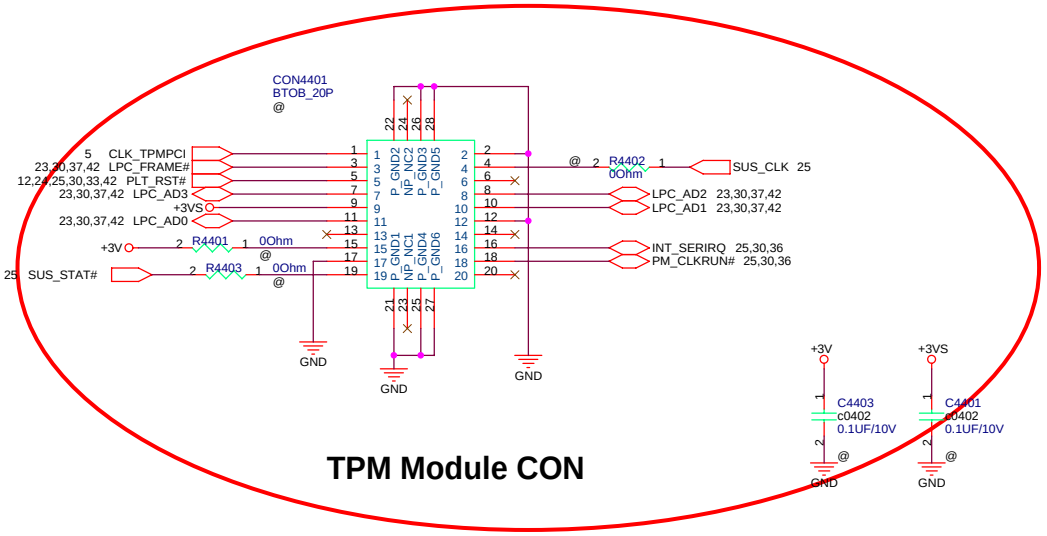


<Variant Name>

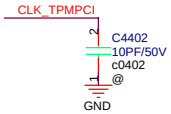
ASUSTeK COMPUTER INC	Title : Startup Circuit	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 42 of 63	

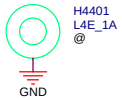

35 PWR_SW#
+3VA
R4301 100KOhm r0402
R4302 330Ohm
C4301 @ 0.1UF/16V
SW4305
TACT_SWITCH_5P
GND
Power Switch
+3VS
R4306 220Ohm
LED4304 GREEN
IDE
33 HDD_LED#
+3V
R4305 220Ohm
LED4302 GREEN
SCRL
30 SCROLL_LED#
R4303 220Ohm
LED4301 GREEN
NUM
30 NUM_LED#
R4304 220Ohm
LED4303 GREEN
CAP
30 CAP_LED#
30 P4GEAR_SW#
C4302 0.1UF/10V
SW4301
TACT_SWITCH_5P
Power4 Gear
30 EMAIL_SW#
C4303 0.1UF/10V
SW4302
TACT_SWITCH_5P
E-Mail
R4327 10KOhm
R4308 100KOhm
Q4301A UM6K1N
Q4301B UM6K1N
DJ_LED
R4307 150KOhm
R4310 470Ohm
DJ_LED_R
30 DJ_LED#
+12V
+5V
30 INTERNET_SW#
C4304 0.1UF/10V
SW4303
TACT_SWITCH_5P
Internet
30 DISTP_SW#
C4305 0.1UF/10V
SW4304
TACT_SWITCH_5P
Touchpad Disable
Block 4
R4325 100KOhm
C4309 0.1UF/10V
U4301B 74LV74A
U4301A 74LV74A
35 PM_PWRBTN
35 S4_DELAY
25 PWRLED_1HZ
D4304 SS0540
D4303 DAN202K
R4326 10KOhm
R4322 10KOhm
R4323 220Ohm
PWR_LED#_R
Q4303 2N7002
Q4310 2N7002
Q4307 2N7002
Q4308 2N7002
SUSB# 18,25,34,60,61
DJ_LED
DJ Board Conn.
R4312 10KOhm r0402_h16
CON4301
FPC_20P
+5VS
+5VSUS
+5VLCM
802_LED#_R
EMAIL_LED#_R
CHARGE_LED#_R
PWR_LED#_R
DJ_PLAY#
DJ_STOP#
DJ_FWARD#
DJ_BWARD#
DJ_SCAN
DJ_LED_R
DJ_SW#
TP_DAT
TP_CLK
L4301 80Ohm/100Mhz
+5VS_TP
C4307 0.1UF/10V
R4321 100KOhm
R4318 100KOhm
R4319 470Ohm
802_LED#_R
39 WLAN_LED#
R4311 0Ohm
25 802_LED_EN#
R4313 @ 0Ohm
Q4306A UM6K1N
Q4306B UM6K1N
R4315 470Ohm
CHARGE_LED#_R
58 CHG_LED_UP
Q4304 2N7002
R4320 100KOhm
R4314 470Ohm
EMAIL_LED#_R
Q4305A UM6K1N
Q4305B UM6K1N
30 EMAIL_LED#
C4306 0.1UF/10V @
R4317 100KOhm
R4316 1KOhm
30 LID_KBC#_R
LID_SW# 18,35
C4308 0.01UF/25V c0402
<Variant Name>
Title : DJ Board/SW/TP
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name A6Jc
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 43 of 63
http://konweer.kiev.ua

http://konweer.kiev.ua



TPM Module CON

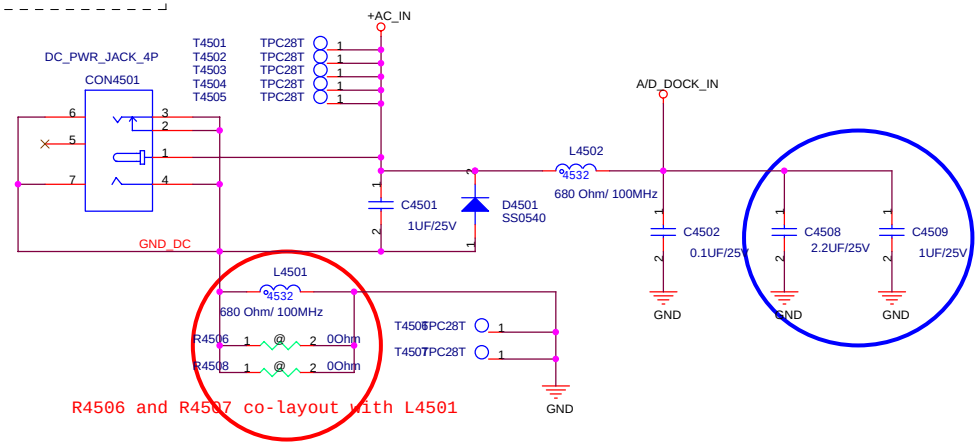


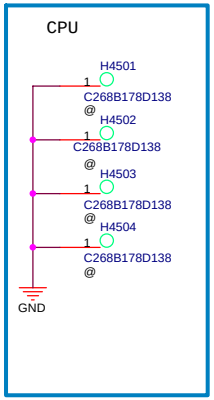


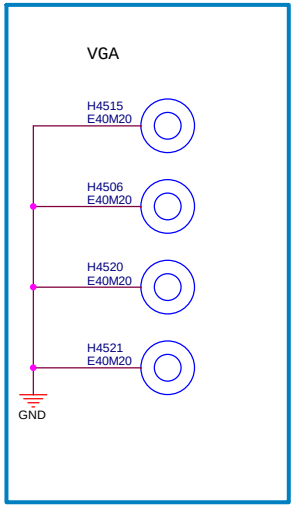
<Variant Name>

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: *Marco Chen*	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 44 of 63	

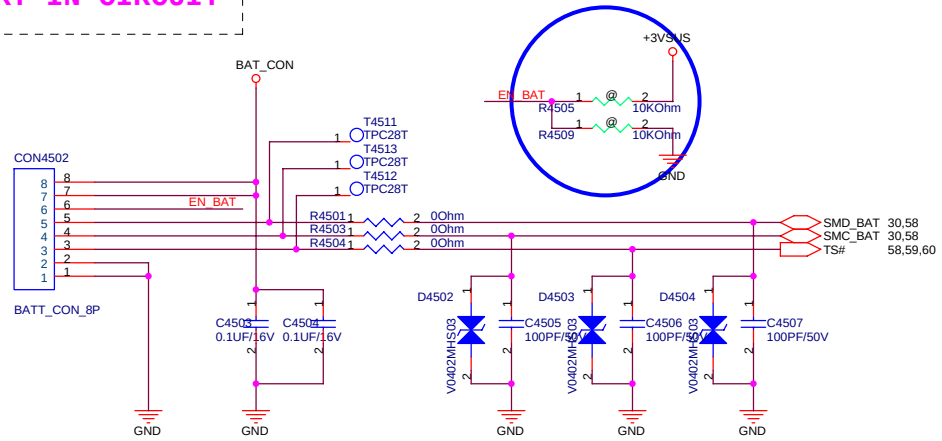
Adaptor IN Circuit

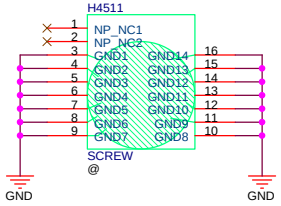


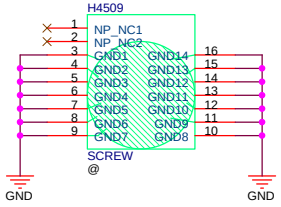


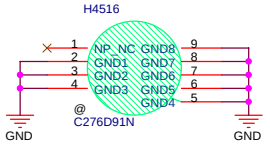


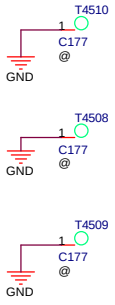
BATTERY IN CIRCUIT

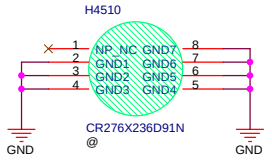


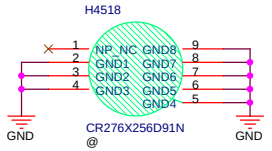


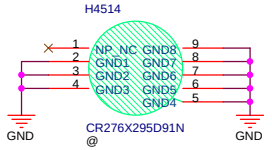


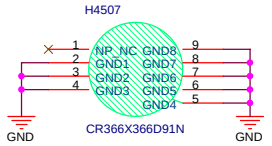


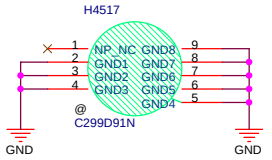


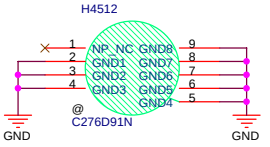


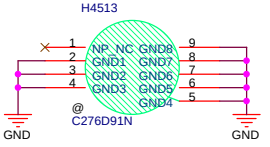


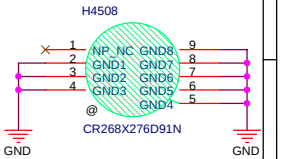












http://konweer.kiev.ua

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power Connector

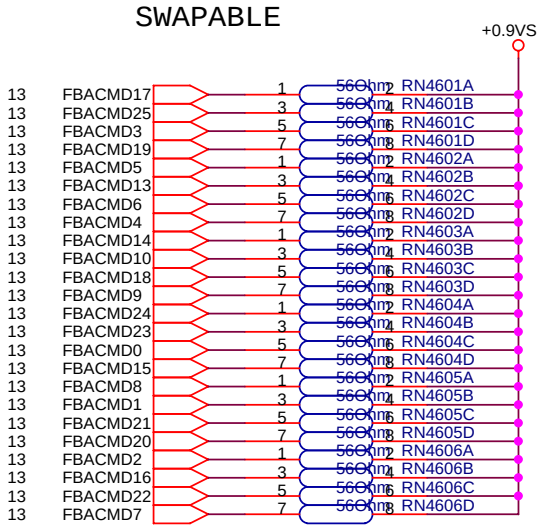
Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6Jc	2.1

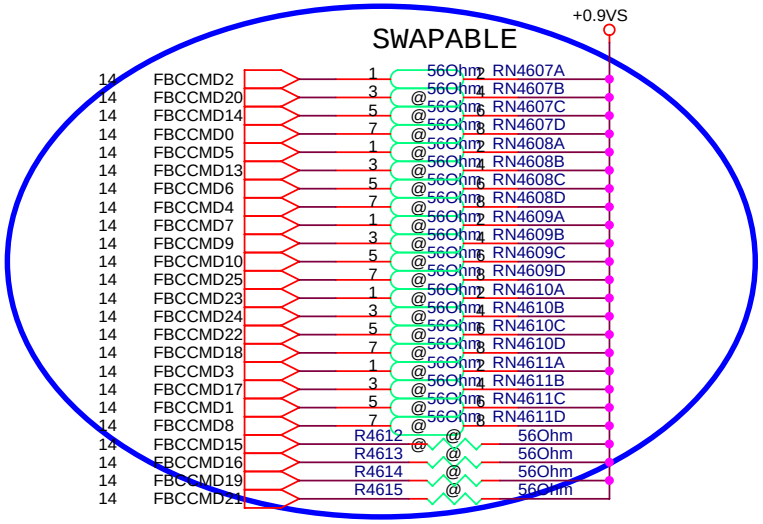
Date: Thursday, January 19, 2006 Sheet 45 of 63

http://konweer.kiev.ua

FBA CMD/ADDR Termination



FBC CMD/ADDR Termination



<Variant Name>

ASUS	Title : G73M-Termination	
<OrgName>	Engineer: Charles Lee	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 46 of 63	

http://konweer.kiev.ua

Host	SM-Bus Device	SM-Bus Address	Device
ICH7-M	Clock Generator	1101001x (D2)	ICS954310
ICH7-M	SO-DIMM 0	1010000x (A0)	DDR SOCKET1
ICH7-M	SO-DIMM 1	1010001x (A4)	DDR SOCKET2
ICH7-M	Thermal Sensor	0101110x (5C)	ADT7463 (Optinal)

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D

<Variant Name>

Title : SYSTEM

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	A6Jc	2.1

Date: Thursday, January 19, 2006 Sheet 47 of 63

R1.0 -> R1.1

1. Page2: Add test points T215 and T216 for H_ADS# and H_CPURST#

2. Page4: Modify FAN solution from DA to PWM and change R-C delay timing.

   A. Mount R416 and DNI R415

   B. Change C404 to 1uF

3. Page4: Connect +3VS_FAN(R419*3.3K ohm and R420*2.2K ohm 分壓 from +V5S_FAN) to U401.3 because FAN_DA level is 3V and FAN_PWM# is open-drain, change pull-up to +3VS and U401.3 level shift from 5V to 3V

4. Page4: Add pull-down resister R418*10M ohm to protect noise when power-on

5. Page5: Add (R579*33 ohm and C529*10pF) for TPM PCI 33MHz clock

6. Page5: Change R531 from 10 ohm to 22ohm to eliminate swing.

7. Page5: DNI R510 to disable ITP enable.

8. Page7: Delete R715 because it duplicate with R529.

9. Page9: Change L905 to P/N:09G012030000 and L905 to P/N:09G013120409 because +1.5VS_PCIE consume about 1.3A and +1.5VS_3GPLL consume 200mA only.

10. Page13: VGA_GPIO5 add pull-up 10K ohm to +3VS for ATI recommendation.

11. Page13: DNI R1320 and mount R1321 to change back light enable from DC level to PWM and meet VBIOS support.

12. Page13: Add R1343*0 ohm for reserving bead to ground.

13. Page15: Change L1504.2 to connect from +VGA_VCORE to +1.2VSP for ATI recommendation.

14. Page15: Change bead L1506 from 120Ohm/100Mhz to 30Ohm/100Mhz type.

15. Page19: Add bead L1913 between TV_GND and GND.

16. Page23: Change High Definition damping resisters*R2312, R2314, R2316, R2318, R2320, R2322, R2324, R2325 from 22 ohm to 39 ohm for reducing reflection.

17. Page29: Add Line-in solution, please commt Black 2.

18. Page31, 32: Change LAN chip from Marvell 88E8053 to Realtek RTL8111B.

19. Page34: Add Q3401 and R3414 to replace U3402B.

20. Page34,35: Modify reset circuits to meet Intel specification, please commt Black 3.

21. Page35,43 : DNI R4312 and change R3509 from 4.7M ohm to 2.2 M ohm to short SWDJ_EN# detected to 2secends for BIOS requirement and add INIT# solution(please comment Block 7).

22. Page37: Change R3706 from 10K ohm to 100K ohm to enlarge R-C delay time.

23. Page39: Reserve R3905 to PLT_RSTNS# Wire-Or with PLT_RST#_BUF.

24. Page41: Short CON4101.1 and CON4101.2 and delete R4105, R4104, and C4103 because no timing issue between power and enable signal.

25. Page42: Delete D4201 and DNI R4202 because no power loss issue exist.

26. Page43: Modify S4 strech circuits, please comment Block 4.

27. Page44: Add TPM connecter.

28. Page45: Add C4508, C4509, R4506 and R4507 for EMI requirment.

29. Page42: Change CON4202.1 and CON4202.3 power from +3VSUS to +3V.

30. Page18: Change L1806.2 power from AC_BAT_SYS to AC_BAT_SYS_CPU for EMI requirement.

31. Page7: Change from VRM_PWRGD to ICH7_PWROK to enable MCH_PWROK for Intel requirement(Mount R721 and DNI R722).

32. Page23,34: Change thermal-trip solution.

   A. Mount R2315 and DNI R4507

   B. Remove the circuits.(please comment Block 5)

   C. Mount thermal protection circuits.(please comment Block 6)

33. Page5, 23, 37: Change capacitor values for TXC recommendations(C513,C514 from 33pF to 27pF, C2302, C2304 from 12pF to 22pF ,Change X3701 to 07G010S22450*30 ppm and C3725 and C3726 to 22pf).

34. Page15, 47: Add Back Bias circuits for ATI recommendations.

35. Page5, 23, 33: Add SATA circuits for OEM requirement.

36. Page12: Remove R1205 for ATI recommendations.

37. Page39: Reserve R-C to tune waveform quanlity.(R3906,R3907,C3911,C3912)

38. Page41: Reserve R4104, R4105, R4106 to modify enable blue tooth solution.

R1.1 -> R2.0

1. Page4, 34: Add power limit solution and change thermal protection solution.

   A. Add R421*0 ohm and connect to H_PROCHOT_S#

   B. DNI R417*0 ohm

   C. Add R422*0 ohm and connect to OVERTEMP# that is wire-or with FORCE_OFF#.

   D. DNI OTP solution.

2. Page15: Add BBIAS_CNTL pull-down resister R1508*10K ohm to GND.

3. Page19: Modify parts (D1912 and F1901).

4. Page24: Add 3 pcs decoupling CAPs(C2410, C2411, C2412) to short return path because PCI Bus(IN1) reference +1.8VS(Vcc).

5. Page25, 44: Add BT_LED solution to co-layout with Scroll Lock for Epson requirement.

6. Page27: Change R2704 from 0 ohm to 150 ohm.

7. Page27: Change R2707 from 47K ohm to 332K ohm.

8. Page27, 28: Add MUTE_POP# solution for Epson requirements. Please comment PR BlOCK 1.

9. Page30: Add LID switch solution.

   A. Change BAT_SEL# push-pull resister from +3V to GND.

   B. DNI Q3002*2N7002.

10. Page31: Change LAN chip reset signal from PLT_RSTNS# to PCI_RST#. (Mount R3107 and DNI R3106).

11. Page35: Change KBCRSM solution to connect to PM_PWRBTN# directly, please comment PR BLOCK 2.

12. Page36: Change CARDBUS chip reset signal from PLT_RST#_BUF to PLT_RST#. (Mount R3618 and DNI R3617).

13. Page39: Add WLAN_LED# pull-high resister R3908*100K ohm to solve LED was lighted when miniCARD was un-plug in.

http://konweer.kiev.ua

<Variant Name>

ASUSTeK COMPUTER INC	Title : History (1)	
	Engineer: Marco Chen	
Size: Custom	Project Name: A6Jc	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 48 of 63	

14. Page40: Remove L4003, L4005, L4007, L4008 for EMI requirement.

15. Page43: Mount R4301*100K ohm to avoid PWR_SW# is floating.

16. Page43: Mount R4327*10K ohm to fix DJ_LED light soon issue when power on.

VGA NV G72M-V R1.0 -> R1.1

1. Page15: Change R1507 from 121 ohm to 0 ohm and Remove R1511 for SSC 3.3V requirment.
2. Page13: Change VRAM CLK Terminators R1303, R1304 from 120 ohm to 100 ohm for NV recommendation.
3. Page14: Change VRAM CLK Terminators R1402, R1403 from 120 ohm to 100 ohm for NV recommendation.
4. Page16: Change DACX_RSET R1605, R1607 to 124 ohm and remove R1604, R1606 for NV recommendation.
5. Page17: Mount 3GIO_PADCFG R1720 and DNI R1721 for NV recommendation.
6. Page17: Change RN1701 from 4R8P 0603 to 4R8P 0402 for BOM issue
7. Page19: Change D1913 from LM385M3 to BAV99.
8. Page19: Change L1901, L1905, L1906 to 180NH.
9. Page43: DJ_LED# Pull high to +3V via R4327 10Kohm.
10. Page35: Add D3509 (DNI) in parallel to R3532 for C3506 discharge path.
11. Page34: Change U3404 RN5VD to CMOS Topology and R3402(DNI).
12. Page04: Change R420 from 22K ohm to 10K ohm and change R419 from 33K ohm to 20K ohm for Volt divide.
13. Page43 :DNI C4306.
14. Page05: Change R519,R546 from 1 ohm to 2.7 ohm.
15. Page27: Change CE2701 from 47uF to 22uF and rename to C2727.
16. Page32: Change CE3301, CE3302 from 47uF to 22uF and rename to C3314, C3315.
17. Page17: Add U3003, Q3008(DNI) for 4S1P Battery detected.
18. Page23: Change X2301 to PN:07G010303270.
19. Page31: Change X3101 to PN:07G010S22500 for cost issue.
20. Page37: Change con3701 footprint to "nb_pcmcia_84p_6hold_a3n_lf2" for factory issue.
21. Page45: Change H4506, H4515, H4520, H4521 footprint to "nb_smt_nut_e40m20_lf2" for factory issue.
22. Page43: WLAN_LED# Pull-high to +3VS via R4328.
23. Page29: Change U2902 to PN 06G010147010.
24. Page14: Add R1415 and DNI L1403 for NV recommendation.
25. Page28: Change R2832 from 10K to 100K and R2806(DNI).
26. Page27: Change R2704 from 0 ohm to 100ohm.
27. Page35: Change R3509 from 2.2M ohm to 1Mohm and C3504 change from 1uF to 4.7uF.
28. Page31: Change R3106 DNI and R3107 stuff .
29. Page27: Change R2707 from 47k ohm to 332K ohm.
30. Page43:Mount R4301
31. Page35: Modify KBCRSM Circuit.
32. Page30:Add D3003 and C3007.

VGA NV G72M-V R1.1 -> R2.0

1. Page19: Change L1901, L1905, L1906 to 09G013120409 120ohm/100MHz.
2. Page31: Change C3133,C3134 from 22PF to 27PF.
3. Page46: Change ChipResistor RN4607~RN4612 to Single Resistor R4607 ~ R4630.
4. Page45: Change C4509 from 10uF to 2.2uf.
5. Page19: Change R1910 from 33Kohm to 47Kohm for BOM reduction.
6. Page15: Change R1501 from 71.5ohm to 81.6ohm for BOM reduction.
7. Page25: Add R2550 ,R 2553, R2555 for BT_ON.
8. Page14: Mount R1414 for NV recommendation.

C2827	MLCC 2.2UF/10V(0603)Y5V+80-20%	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3007	CAP 2.2UF/6.3V(0603) Y5V (225)	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3503	MLCC 2.2UF/6.3V(0603)Y5V+80-20	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3506	MLCC 2.2UF/6.3V(0603)Y5V+80-20	-->	MLCC 2.2UF/6.3V(0603)X5R 10%
C3502	MLCC 4.7UF/6.3V(0805) X5R 20%	-->	MLCC 4.7U/6.3V(0805) X7R 10%
C3405	MLCC 2.2UF/6.3V(0603)X5R 10%	不變	
C3411	MLCC 0.22UF/10V(0603)X7R 10%	不變	
C3504	MLCC 4.7UF/6.3V(0603)X5R 10%	不變	

http://konweer.kiev.ua

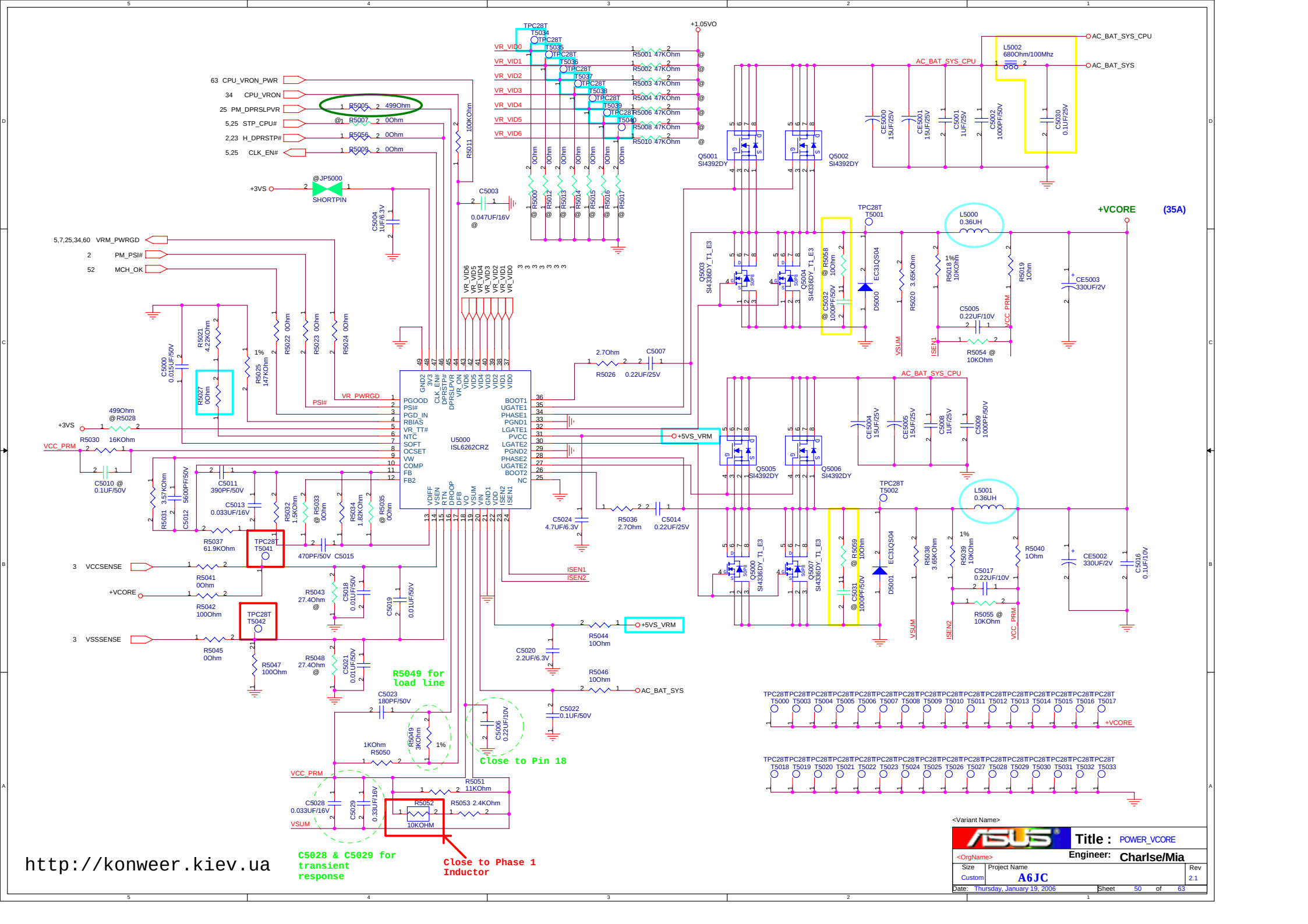
<Variant Name>

Title : History(2)

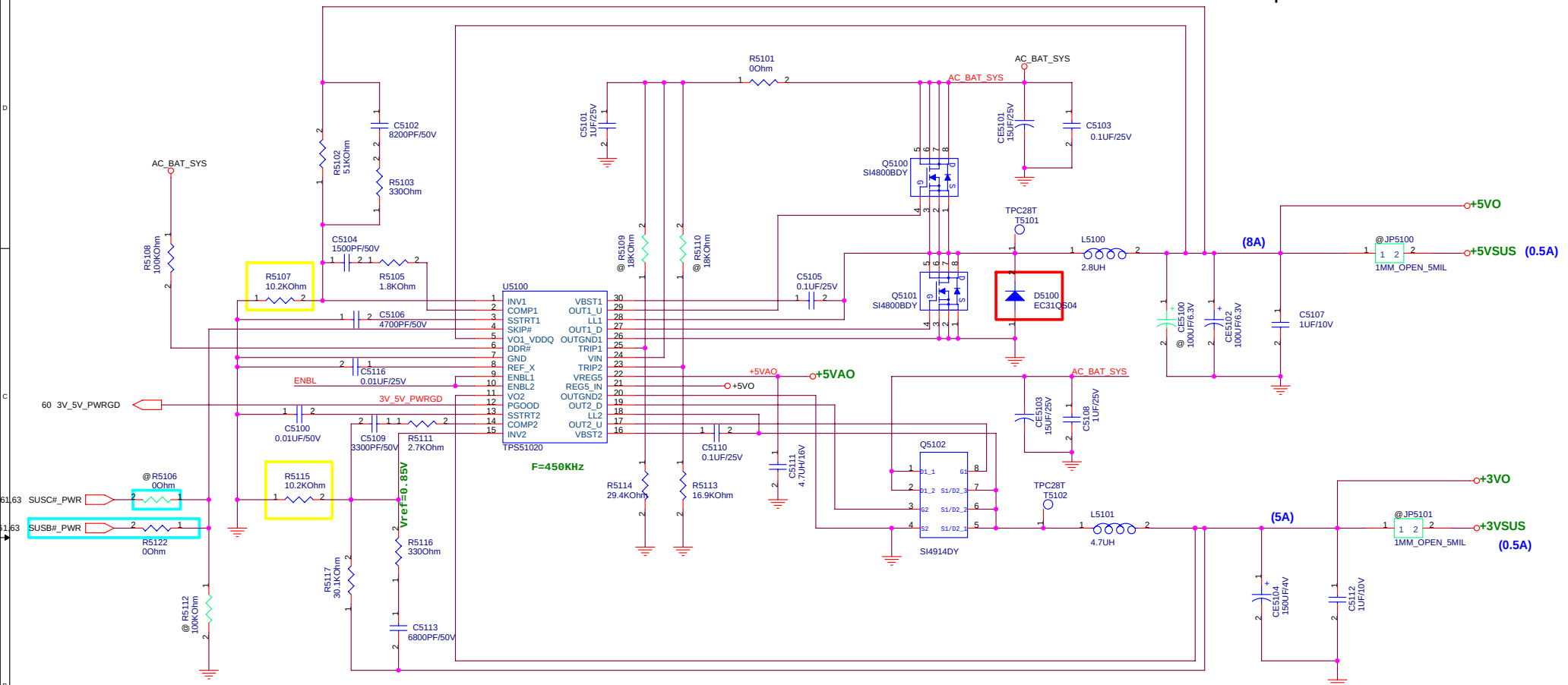
<OrgName> Engineer: Marco Chen

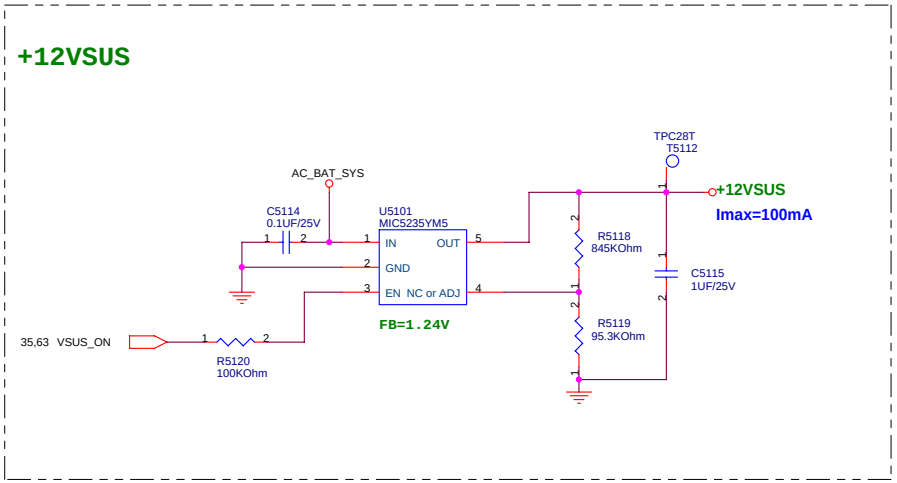
Size	Project Name	Rev
Custom	A6Jc	2.1

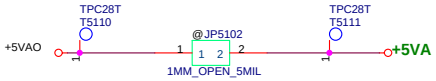
Date: Thursday, January 19, 2006 Sheet 49 of 63

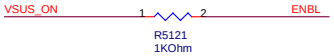

+VCORE (35A)
U5000 ISL6262CRZ
Q5001 SI4392DY
Q5002 SI4392DY
Q5005 SI4392DY
Q5006 SI4392DY
Q5003 SI4336DY_T1_E3
Q5004 SI4336DY_T1_E3
Q5000 SI4336DY_T1_E3
Q5007 SI4336DY_T1_E3
L5000 0.36UH
L5001 0.36UH
L5002 680Ohm/100Mhz
AC_BAT_SYS_CPU
AC_BAT_SYS
+5VS_VRM
+3VS
VCC_PRM
VSUM
ISEN1
ISEN2
R5049 for load line
Close to Pin 18
C5028 & C5029 for transient response
Close to Phase 1 Inductor
http://konweer.kiev.ua
Title : POWER_VCORE
Engineer: Charlse/Mia
A6JC
Thursday, January 19, 2006

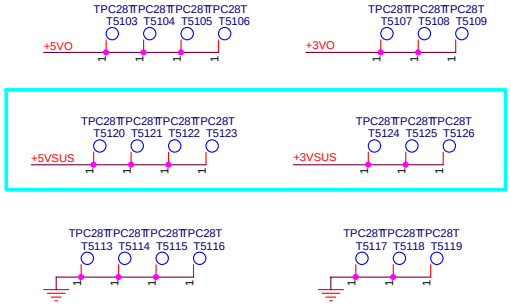
http://konweer.kiev.ua







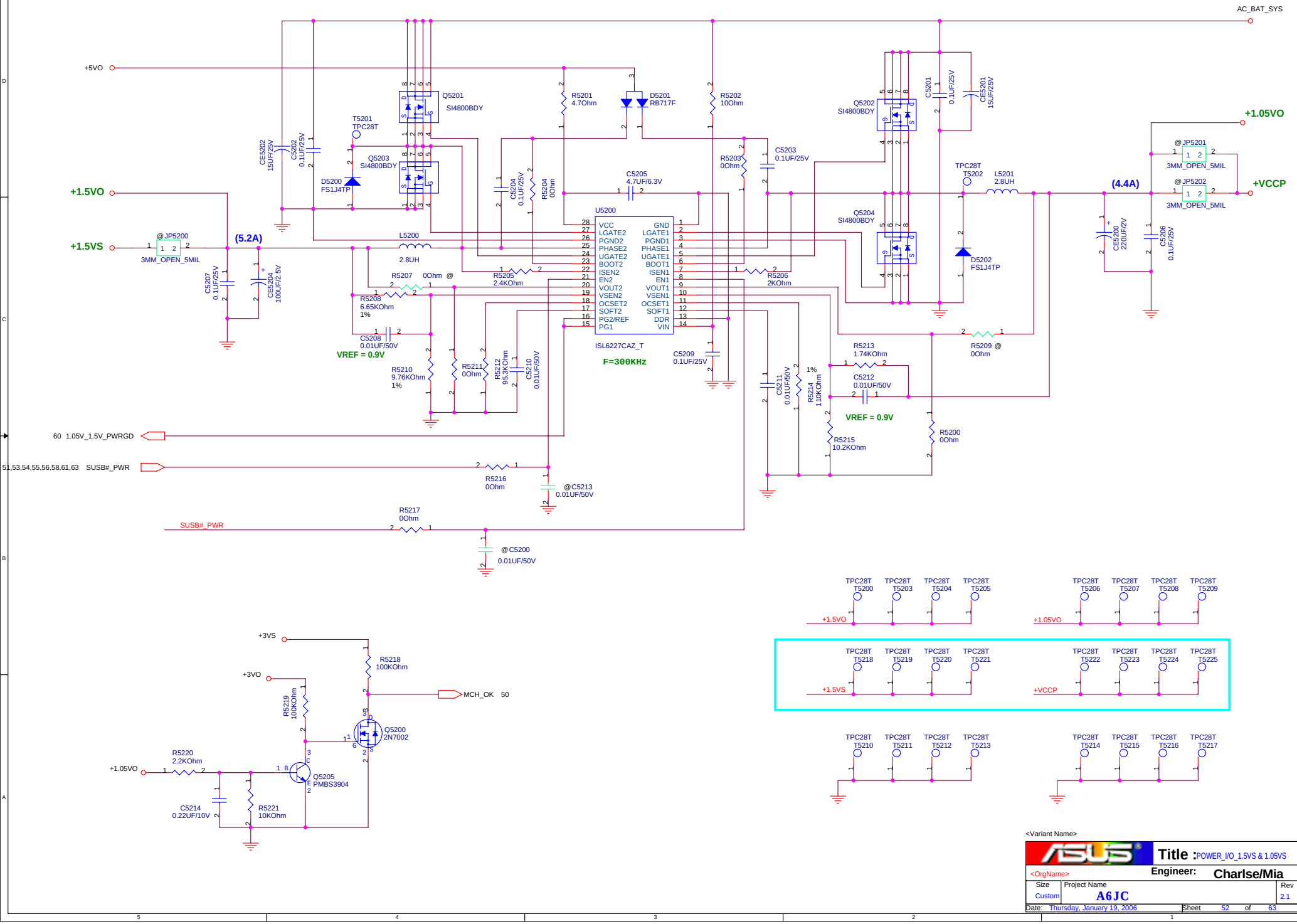




<Variant Name>

Title : POWER_SYSTEM		
<OrgName>	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6JC	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 51 of 63	

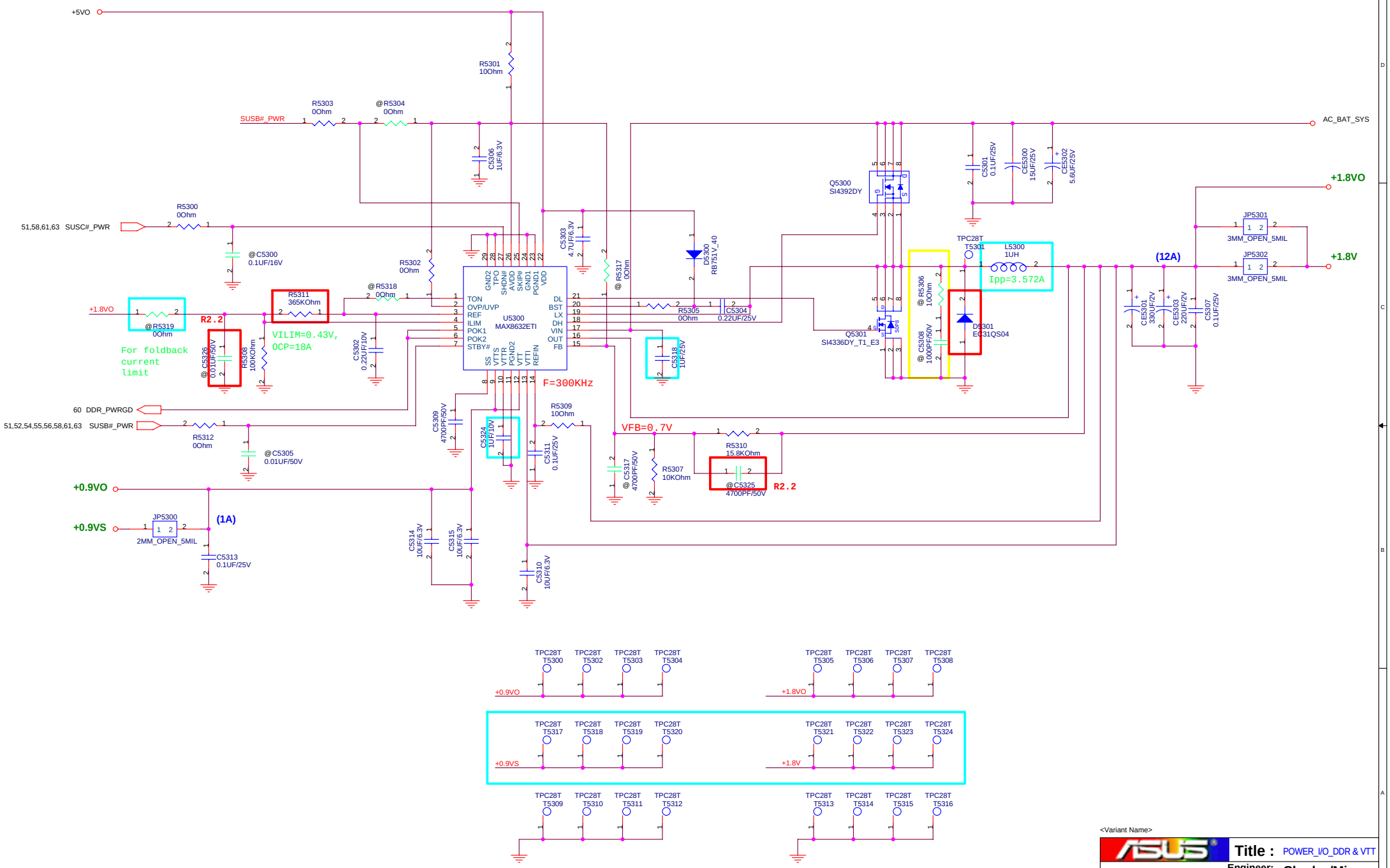
http://konweer.kiev.ua



<Variant Name>

<OrgName>	Title : POWER_I/O_1.5VS & 1.05VS	
	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6JC	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 52 of 63	

http://konweer.kiev.ua



<Variant Name>

Title : POWER_I/O_DDR & VTT

<OrgName>

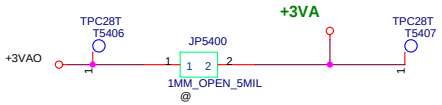
Engineer: Charlse/Mia

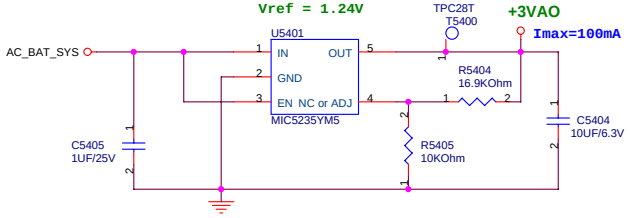
Size	Project Name	Rev
Custom	A6JC	2.1

Date: Thursday, January 19, 2006 Sheet 53 of 63

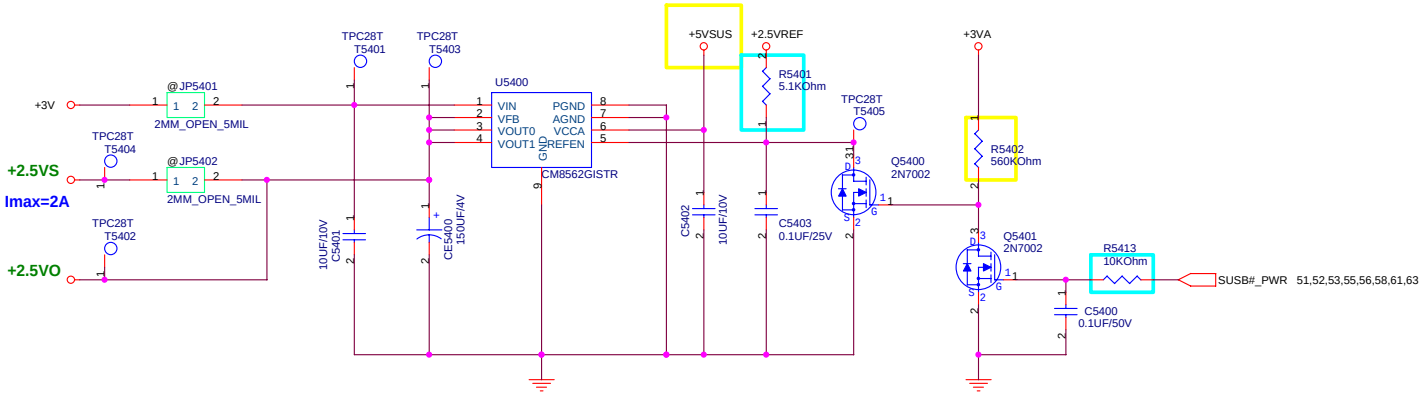
http://konweer.kiev.ua

+3VA0





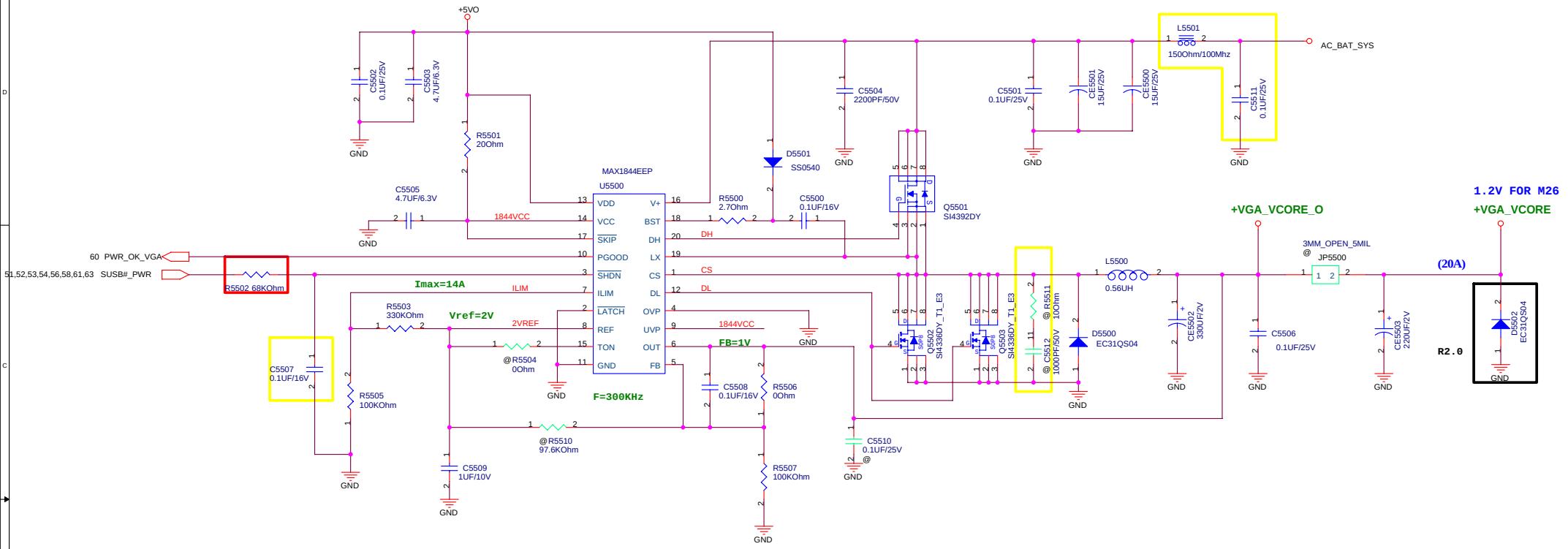
+2.5VS



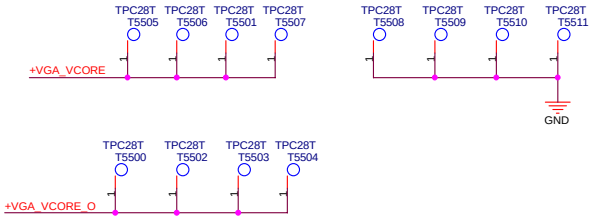
<Variant Name>

Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6JC	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 54 of 63	

http://konweer.kiev.ua



Model	VGA	+VGA_CORE	R5506	R5507	R5510
A6JC	G72M-V	1.0V	0	100K	@
A6JM	G73M	1.1V	10K	100K	@



<Variant Name>

Title : +VGA_CORE

<OrgName>

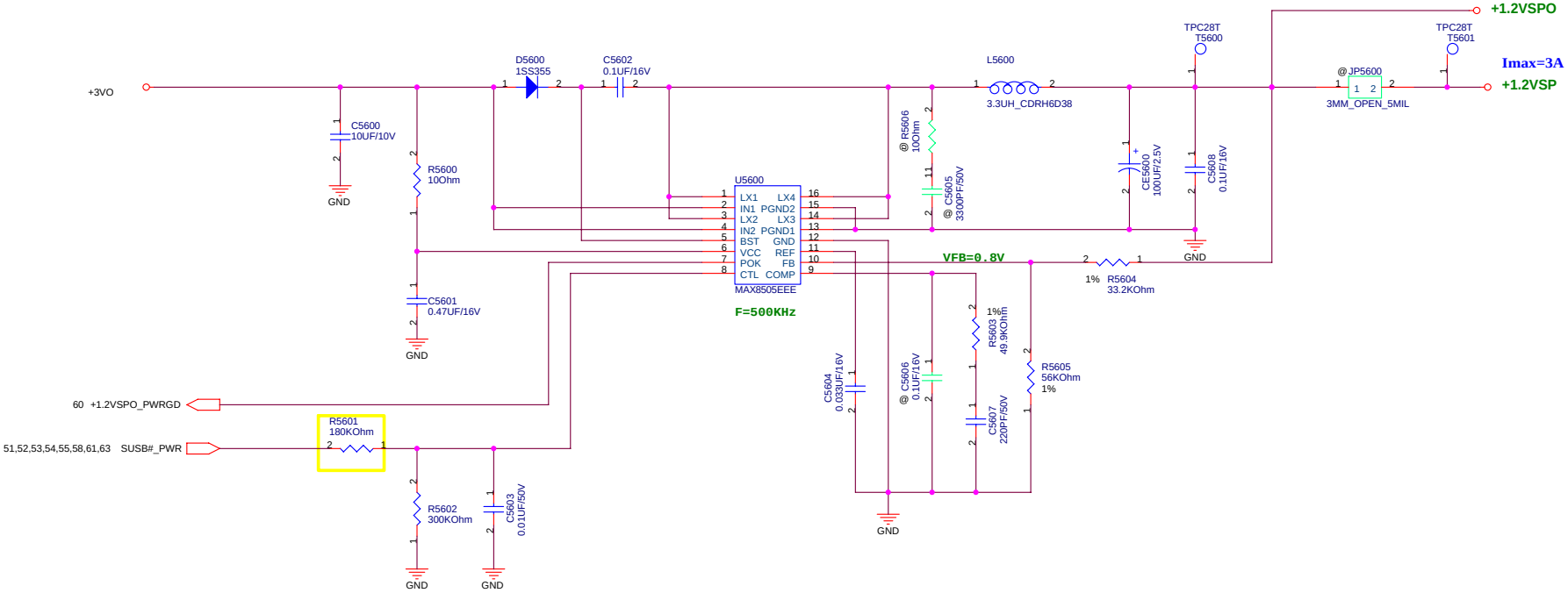
Engineer: Charlse/Mia

Size	Project Name	Rev
Custom	A6JC	2.1

Date: Thursday, January 19, 2006 Sheet 55 of 63

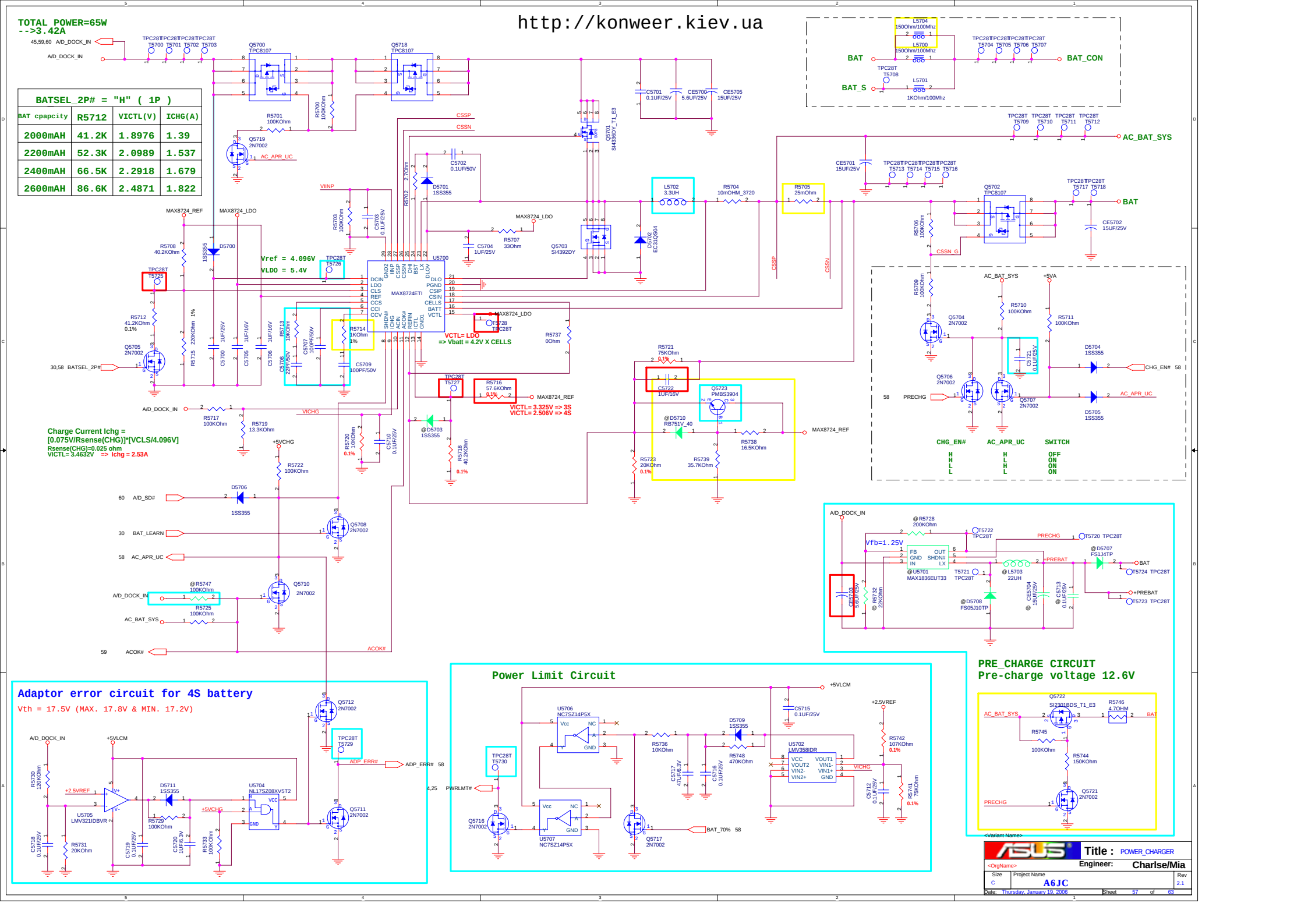
http://konweer.kiev.ua

+1.2VSP



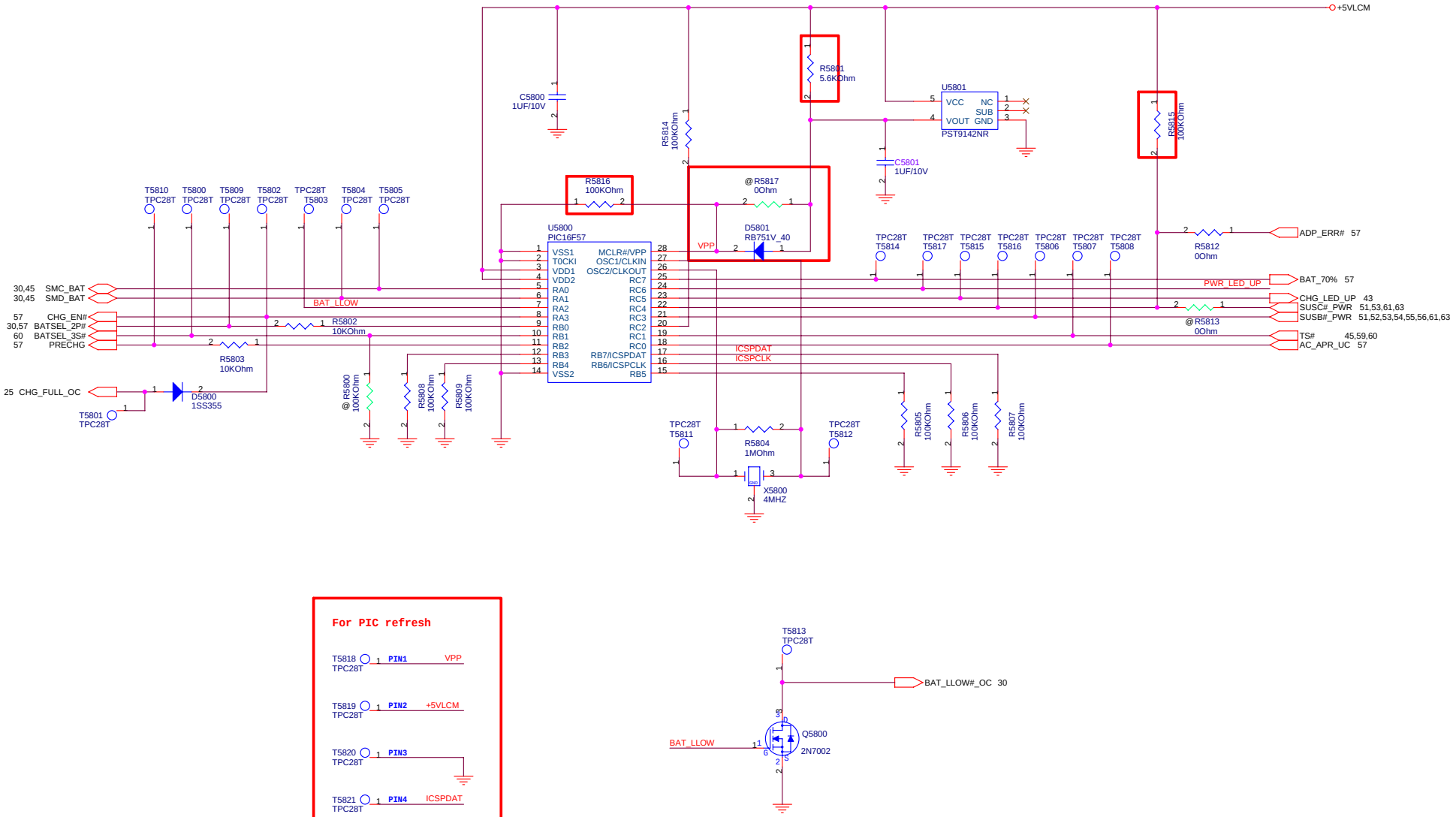
<Variant Name>

ASUS	Title :	POWER_VGA_+1.2VSP
<OrgName>	Engineer:	Charlse/Mia
Size: Custom	Project Name: A6JC	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 56 of 63	



http://konweer.kiev.ua
TOTAL POWER=65W
-->3.42A
BATSEL_2P# = "H" (1P)
BAT cpapcity | R5712 | VICTL(V) | ICHG(A)
2000mAH | 41.2K | 1.8976 | 1.39
2200mAH | 52.3K | 2.0989 | 1.537
2400mAH | 66.5K | 2.2918 | 1.679
2600mAH | 86.6K | 2.4871 | 1.822
Vref = 4.096V
VLDO = 5.4V
VCTL= LDO
=> Vbatt = 4.2V X CELLS
VICTL= 3.325V => 3S
VICTL= 2.506V => 4S
Charge Current Ichg =
[0.075V/Rsense(CHG)]*[VCLS/4.096V]
Rsense(CHG)=0.025 ohm
VICTL= 3.4632V => Ichg = 2.53A
CHG_EN# AC_APR_UC SWITCH
H H OFF
H L ON
L H ON
L L ON
Vfb=1.25V
PRE_CHARGE CIRCUIT
Pre-charge voltage 12.6V
Adaptor error circuit for 4S battery
Vth = 17.5V (MAX. 17.8V & MIN. 17.2V)
Power Limit Circuit
Title : POWER_CHARGER
Engineer: Charlse/Mia
A6JC
Date: Thursday, January 19, 2006
Sheet 57 of 63

PIC16F57



For PIC refresh

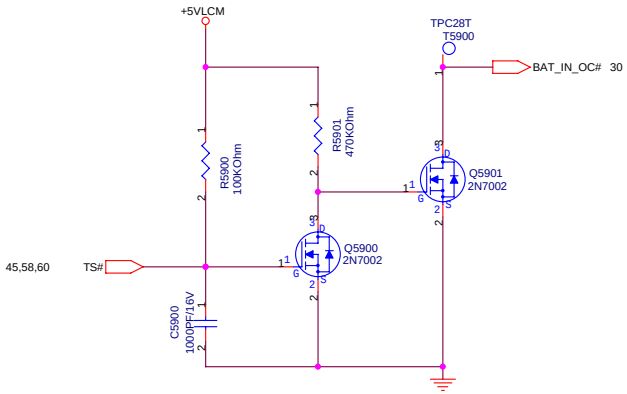
T5818 TPC28T	PIN1	VPP
T5819 TPC28T	PIN2	+5VLCM
T5820 TPC28T	PIN3	
T5821 TPC28T	PIN4	ICSPDAT
T5822 TPC28T	PIN5	ICSPCLK

http://konweer.kiev.ua

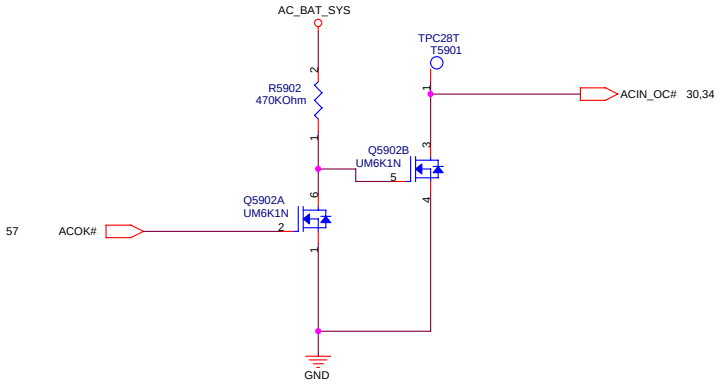
<Variant Name>

Title : POWER_PIC		
<OrgName>	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6JC	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 58 of 63	

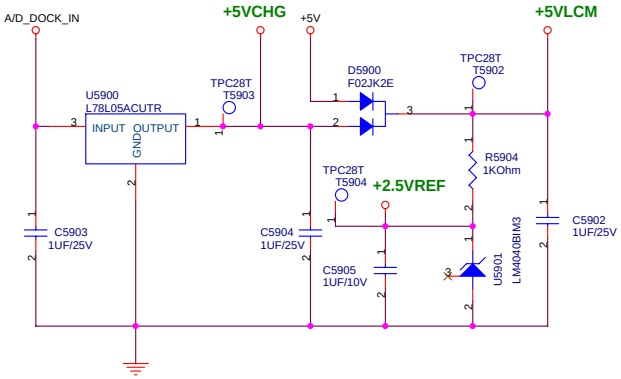
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF

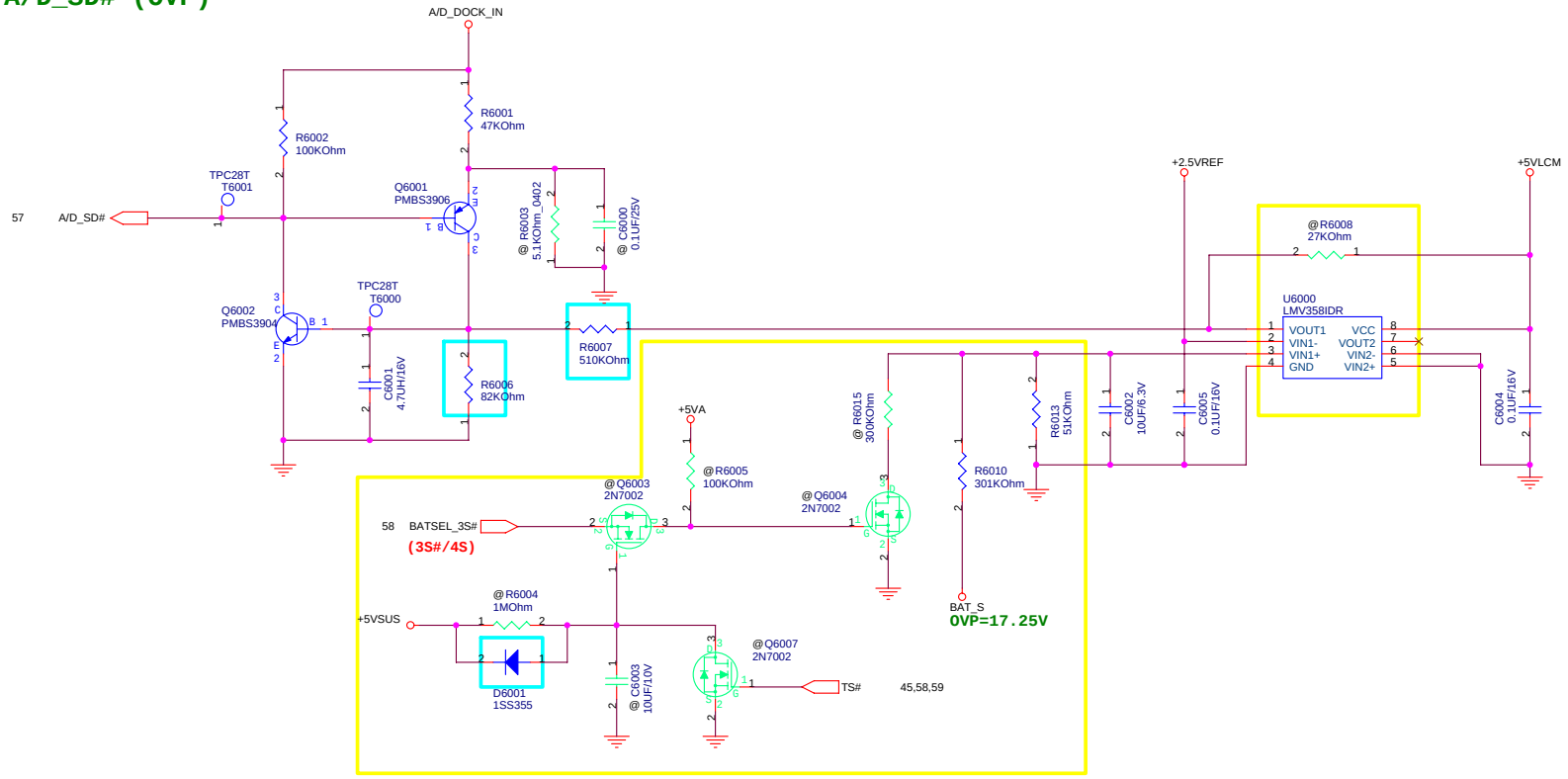


http://konweer.kiev.ua

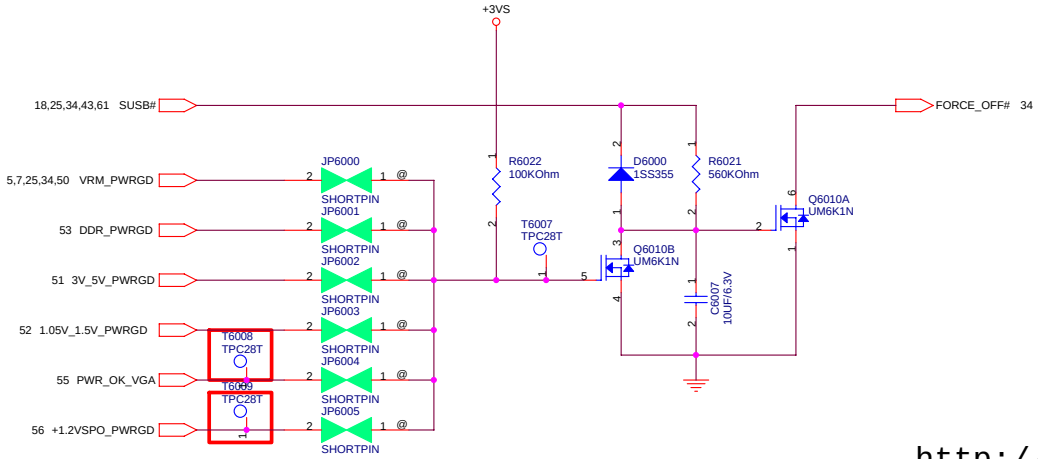
<Variant Name>

Title : POWER_DETECT		
<OrgName>	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6JC	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 59 of 63	

BATTERY A/D_SD# (OVP)



POWER GOOD DETECTER



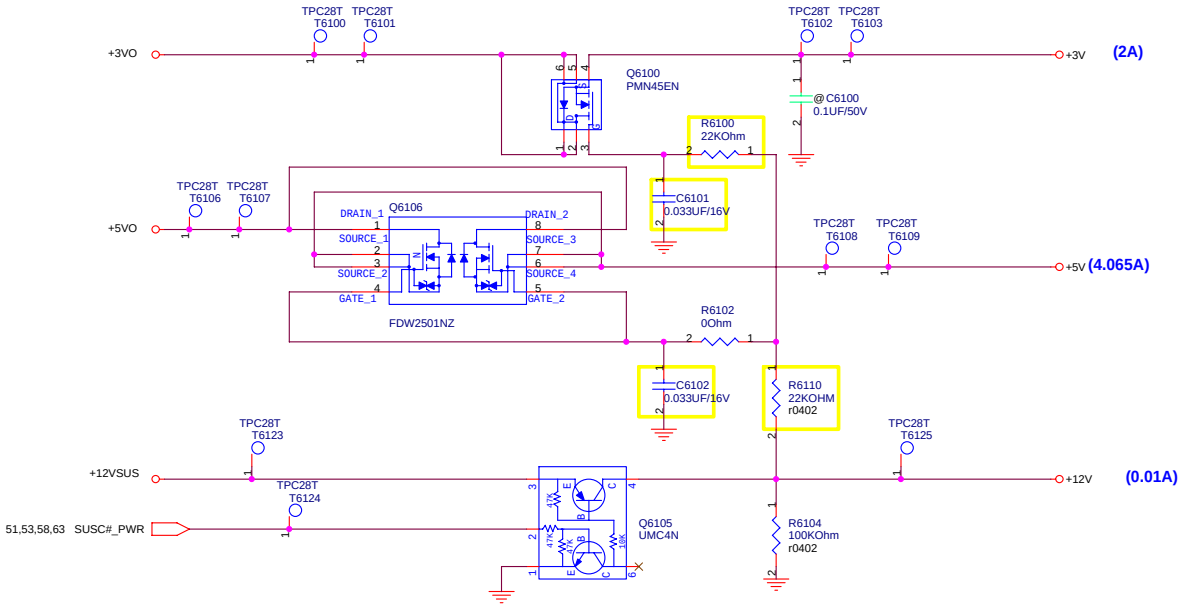
TPC28T T6002 1 VRM_PWRGD
TPC28T T6003 1 DDR_PWRGD
TPC28T T6004 1 3V_5V_PWRGD
TPC28T T6005 1 1.05V_1.5V_PWRGD

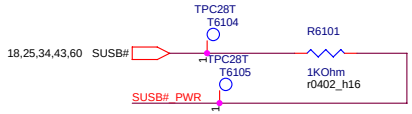
http://konweer.kiev.ua

<Variant Name>

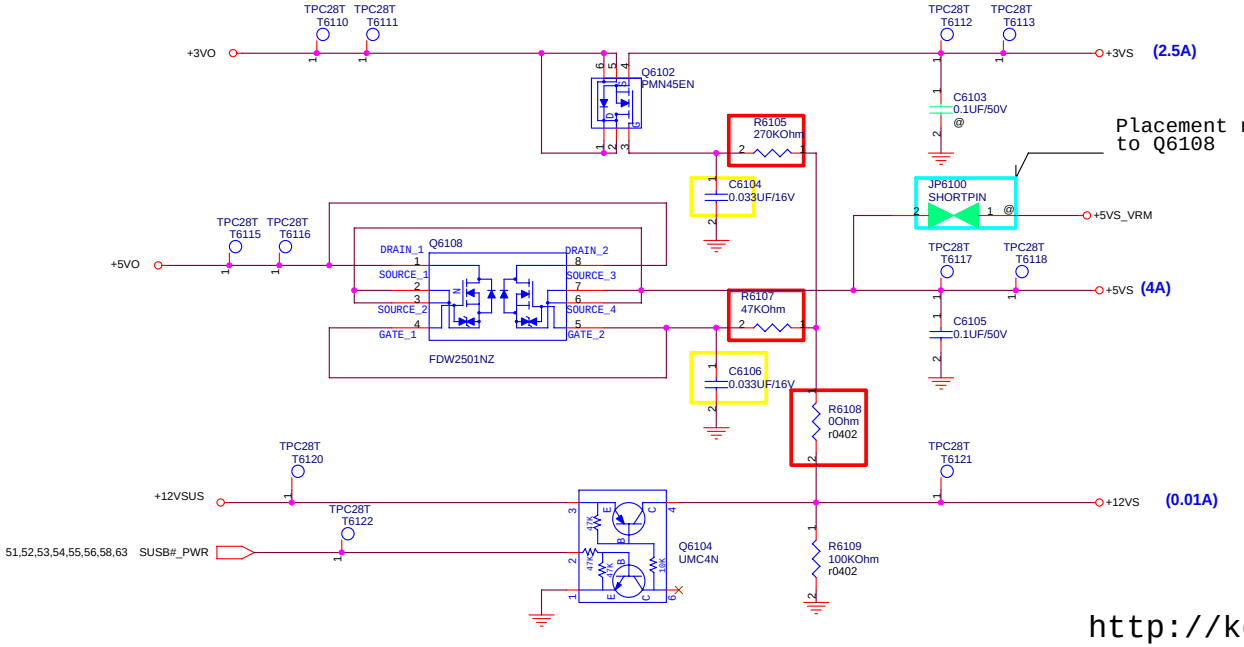
Title : POWER_PROTECT
<OrgName> Engineer: Charlse/Mia
Size: Custom | Project Name: A6JC | Rev: 2.1
Date: Thursday, January 19, 2006 | Sheet 60 of 63

SUSC#_PWR POWER

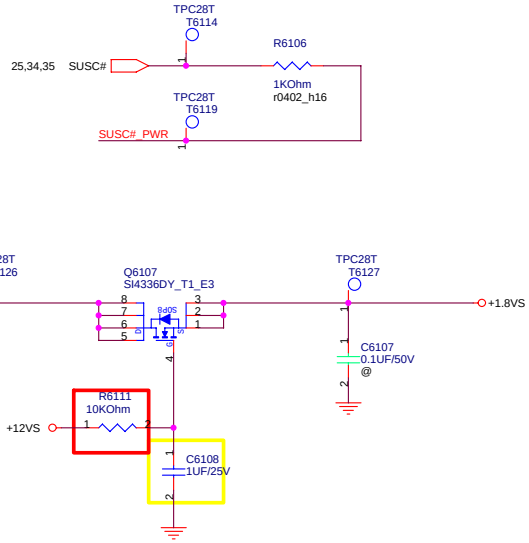




SUSB#_PWR POWER



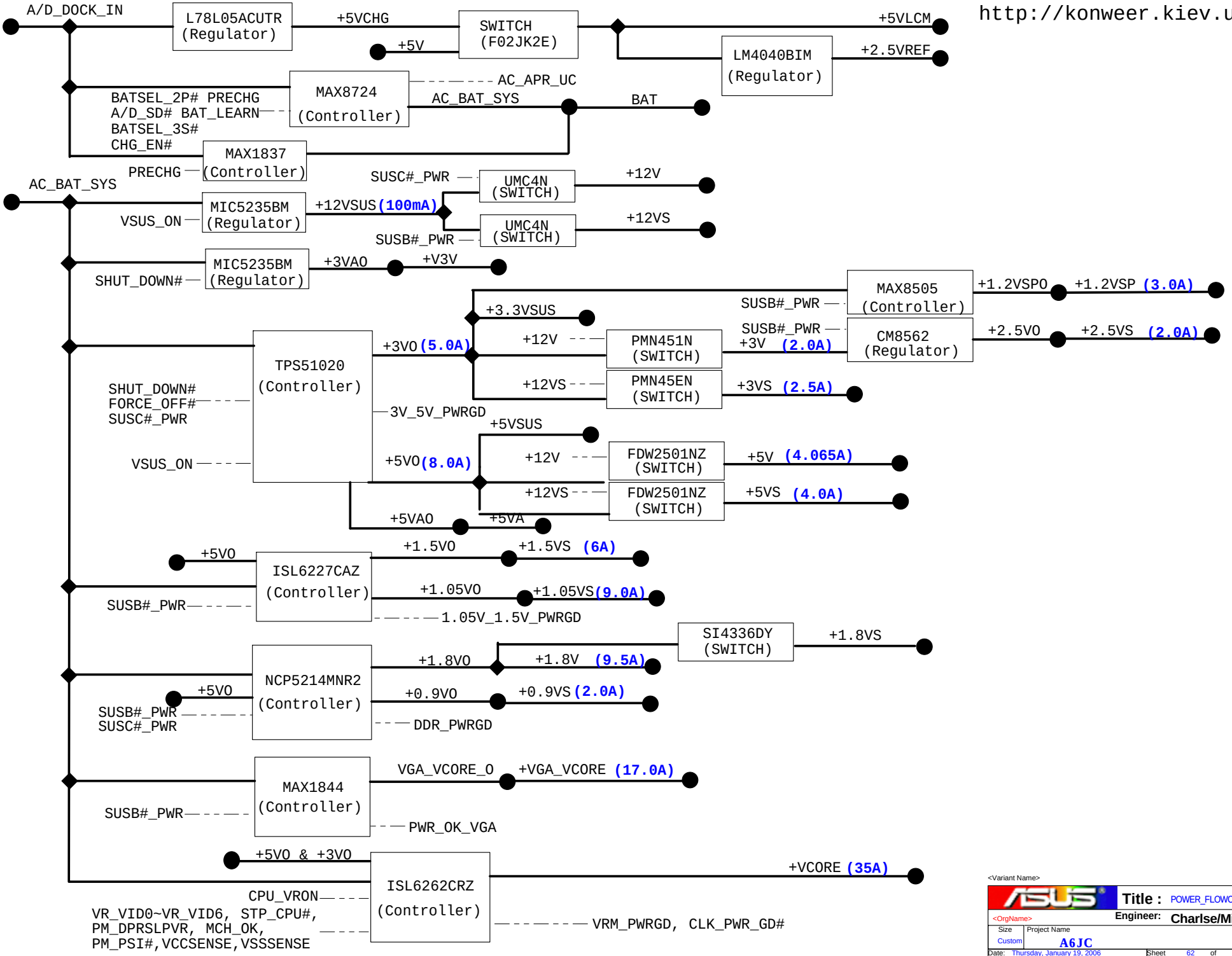
Placement near to Q6108



http://konweer.kiev.ua

<Variant Name>

Title : POWER_LOAD SWITCH		
<OrgName>	Engineer: Charlse/Mia	
Size: Custom	Project Name: A6JC	Rev: 2.1
Date: Thursday, January 19, 2006	Sheet 61 of 63	


http://konweer.kiev.ua
A/D_DOCK_IN
L78L05ACUTR (Regulator)
+5VCHG
SWITCH (F02JK2E)
+5V
+5VLCM
LM4040BIM (Regulator)
+2.5VREF
MAX8724 (Controller)
AC_APR_UC
BATSEL_2P# PRECHG
A/D_SD# BAT_LEARN
BATSEL_3S#
CHG_EN#
AC_BAT_SYS
BAT
MAX1837 (Controller)
PRECHG
AC_BAT_SYS
SUSC#_PWR
UMC4N (SWITCH)
+12V
MIC5235BM (Regulator)
VSUS_ON
+12VSUS (100mA)
UMC4N (SWITCH)
+12VS
SUSB#_PWR
MIC5235BM (Regulator)
SHUT_DOWN#
+3VAO
+V3V
MAX8505 (Controller)
SUSB#_PWR
+1.2VSPO
+1.2VSP (3.0A)
+3.3VSUS
TPS51020 (Controller)
+3VO (5.0A)
+12V
PMN451N (SWITCH)
+3V (2.0A)
SUSB#_PWR
CM8562 (Regulator)
+2.5VO
+2.5VS (2.0A)
SHUT_DOWN#
FORCE_OFF#
SUSC#_PWR
+12VS
PMN45EN (SWITCH)
+3VS (2.5A)
3V_5V_PWRGD
+5VSUS
VSUS_ON
+5VO (8.0A)
+12V
FDW2501NZ (SWITCH)
+5V (4.065A)
+12VS
FDW2501NZ (SWITCH)
+5VS (4.0A)
+5VAO
+5VA
+5VO
ISL6227CAZ (Controller)
+1.5VO
+1.5VS (6A)
SUSB#_PWR
+1.05VO
+1.05VS (9.0A)
1.05V_1.5V_PWRGD
SI4336DY (SWITCH)
+1.8VS
NCP5214MNR2 (Controller)
+1.8VO
+1.8V (9.5A)
+5VO
+0.9VO
+0.9VS (2.0A)
SUSB#_PWR
SUSC#_PWR
DDR_PWRGD
MAX1844 (Controller)
VGA_VCORE_O
+VGA_VCORE (17.0A)
SUSB#_PWR
PWR_OK_VGA
+5VO & +3VO
ISL6262CRZ (Controller)
+VCORE (35A)
CPU_VRON
VR_VID0~VR_VID6, STP_CPU#,
PM_DPRSLPVR, MCH_OK,
PM_PSI#,VCCSENSE,VSSSENSE
VRM_PWRGD, CLK_PWR_GD#
<Variant Name>
Title : POWER_FLOWCHART
<OrgName>
Engineer: Charlse/Mia
Size Custom
Project Name A6JC
Rev 2.1
Date: Thursday, January 19, 2006
Sheet 62 of 63

http://konweer.kiev.ua

AC_BAT_SYS → AC_BAT_SYS 50,51,52,53,54,55,57,59

+3VA → +3VA 18,23,34,35,43,54

+5VA → +5VA 34,51,57,60

+5VO → +5VO 51,52,53,55,61

+3VO → +3VO 51,52,56,61

+3V → +3V 25,30,31,32,35,36,37,38,41,42,43,44,54,61

+3VS → +3VS 4,5,7,9,11,12,16,17,18,19,20,21,25,26,27,28,30,31,33,34,35,36,39,42,43,44,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 4,28,35,40,43,61

+12VS → +12VS 18,19,35,61

+5V → +5V 18,30,35,37,40,43,59,61

+5VS → +5VS 4,19,22,26,27,30,33,35,41,43,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 9,15,16,19,35,54

+1.8VO → +1.8VO 53,61

+1.8V → +1.8V 7,10,20,21,35,53

+1.8VS → +1.8VS 13,14,15,16,22,35,61

+0.9VS → +0.9VS 14,15,22,35,46,53

BAT → BAT 57

+5VCHG → +5VCHG 57,59

+5VLCM → +5VLCM 30,43,57,58,59,60

+2.5VREF → +2.5VREF 54,57,59,60

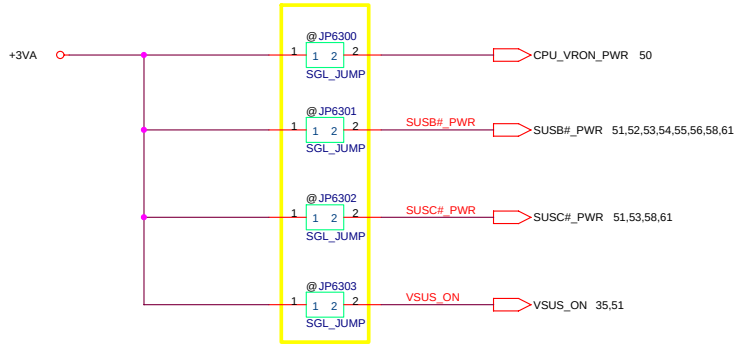
+VCORE → +VCORE 3,4,50

+VGA_VCORE → +VGA_VCORE 12,55

+1.2VSP → +1.2VSP 12,13,14,35,56

BAT_CON → BAT_CON 45,57

FOR POWER TEST



<Variant Name>

Title : POWER_SIGNAL

<OrgName>

Engineer: Charlse/Mia

Size	Project Name	Rev
Custom	A6JC	2.1

Date: Thursday, January 19, 2006 Sheet 63 of 63