

# Compal confidential

## Schematics Document

### Mobile Merom uFCPGA with Satna Rosa Platform

2007-07-30

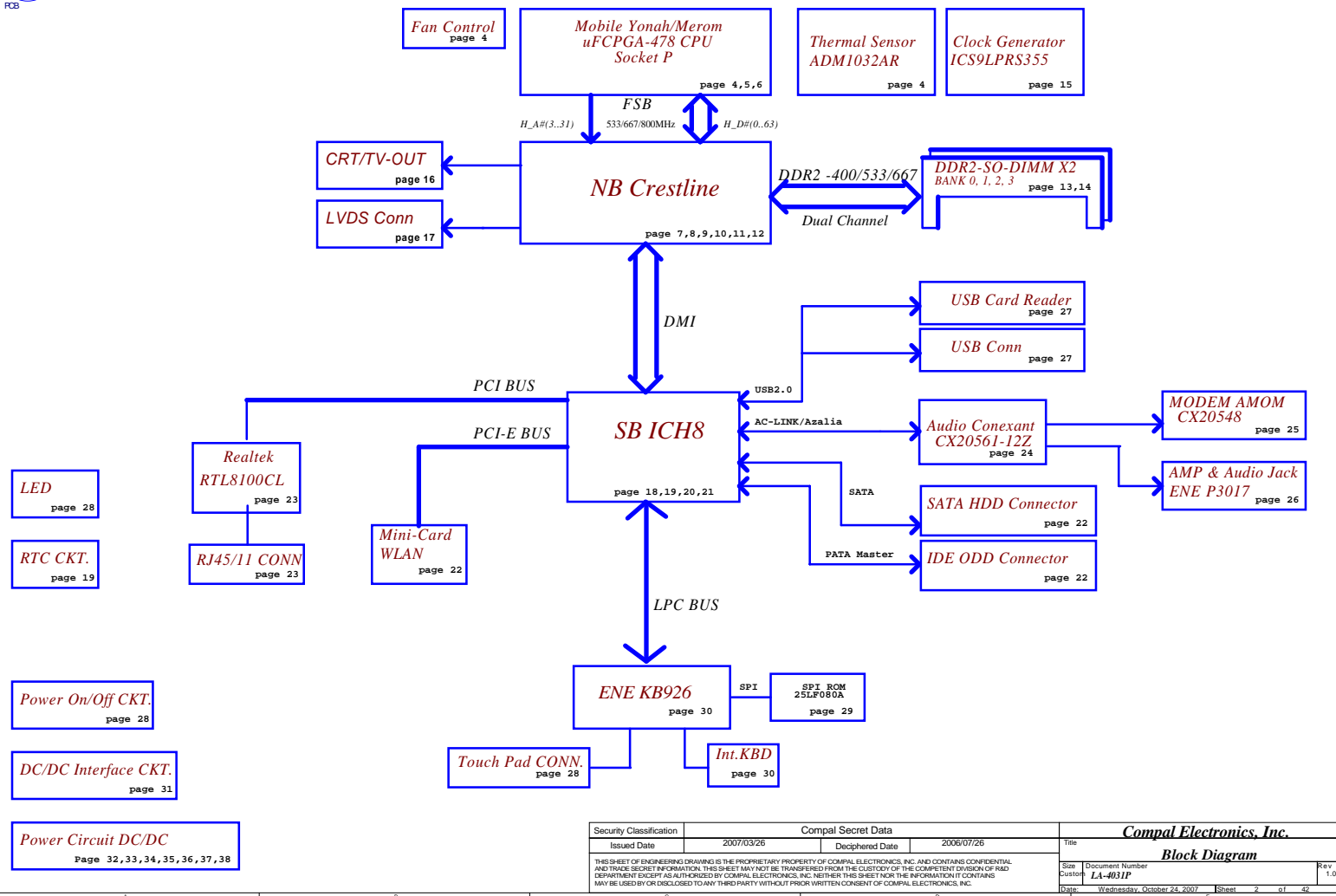
REV: 0.2

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# Spartan 1.1 (Merom +Crestline+ICH8)

File Name : LA-4031P

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<p style="text-align: right;"><b>Compal Electronics, Inc.</b> <b>Block Diagram</b></p>				<p>Document Number <b>LA-4031P</b> Rev 1.0</p>

Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

-  : means Digital Ground
-  : means Analog Ground
- @ : means just reserve , no build
- DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD17	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

SMBUS Control Table

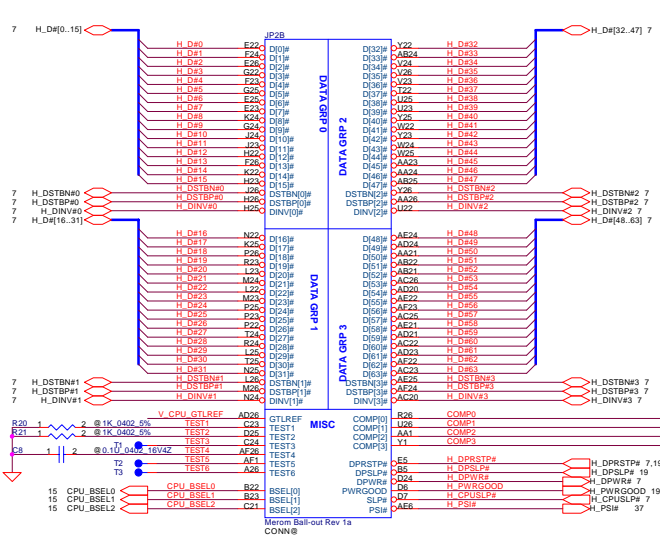
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1022	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CR_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43152432L03(965GM) & 43152432L04(960GML) with card reader  
 BOM: 43152432L01(965GM) & 43152432L02(960GML) without card reader

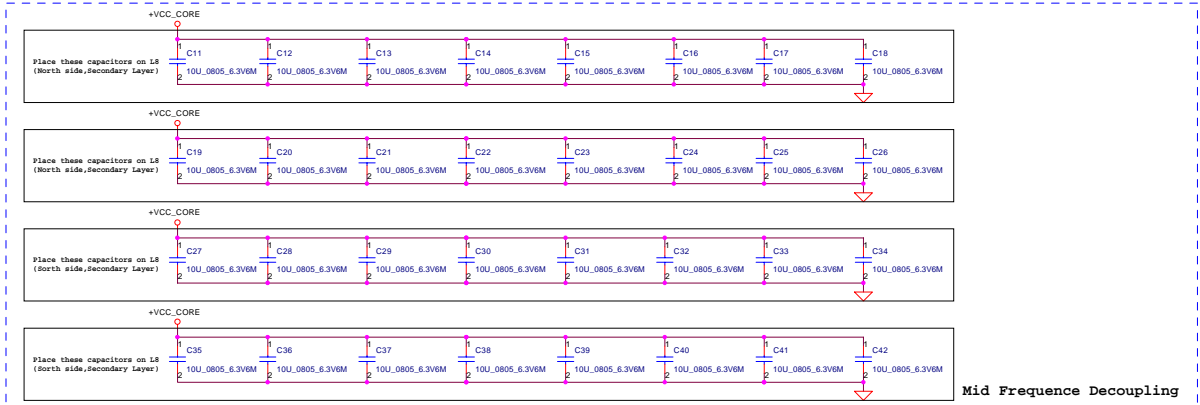
Jump-Short: PJP?

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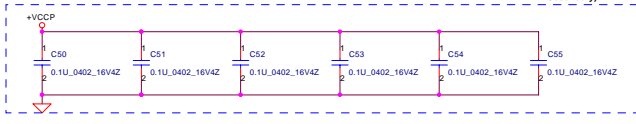
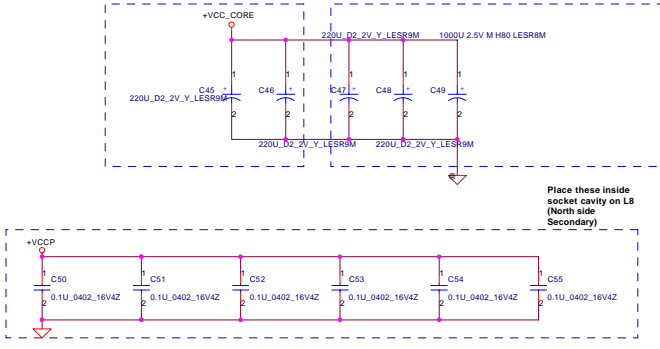




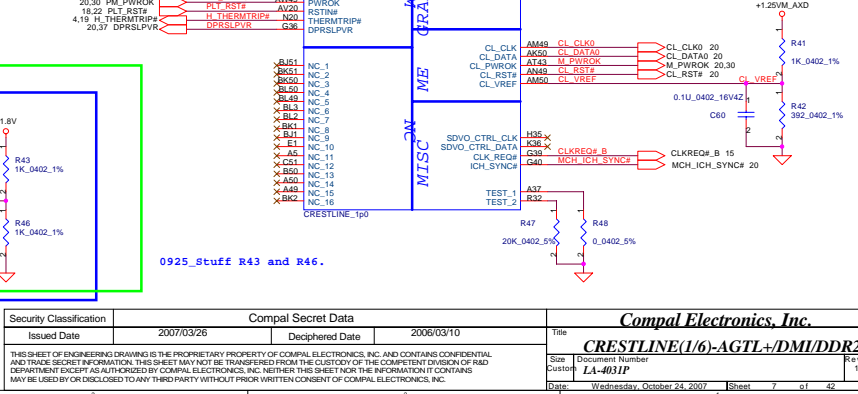
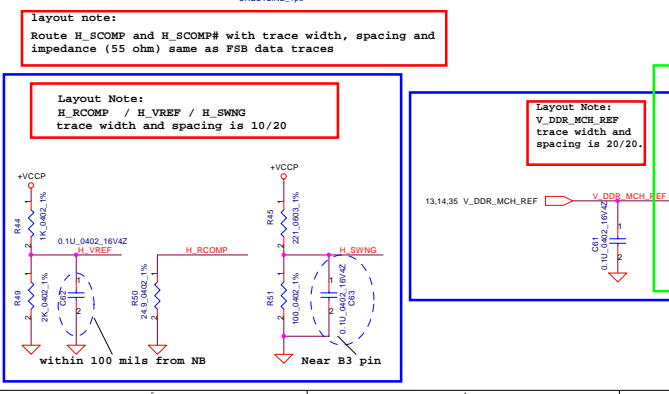
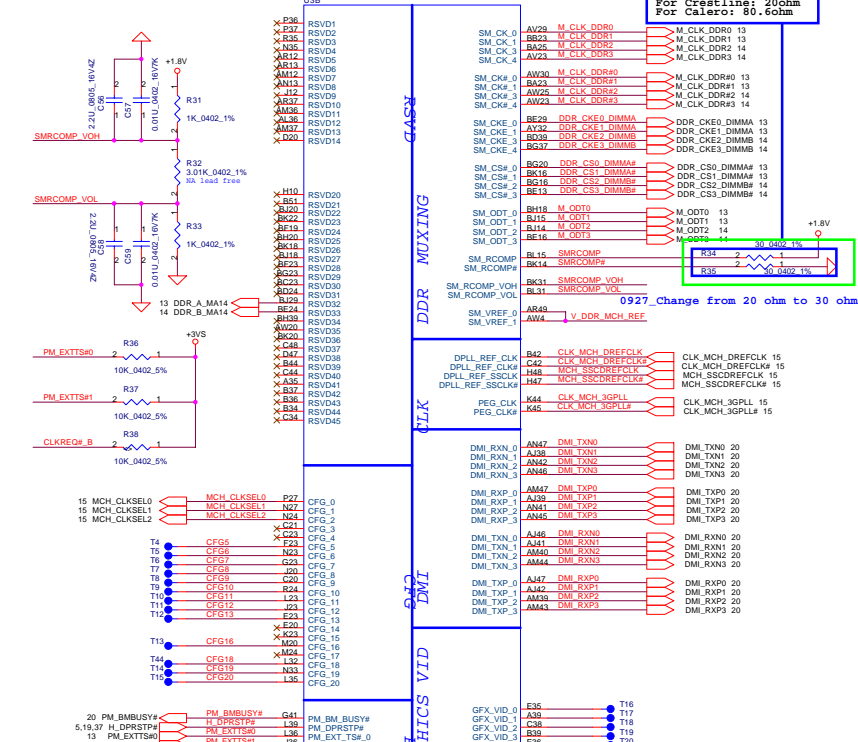
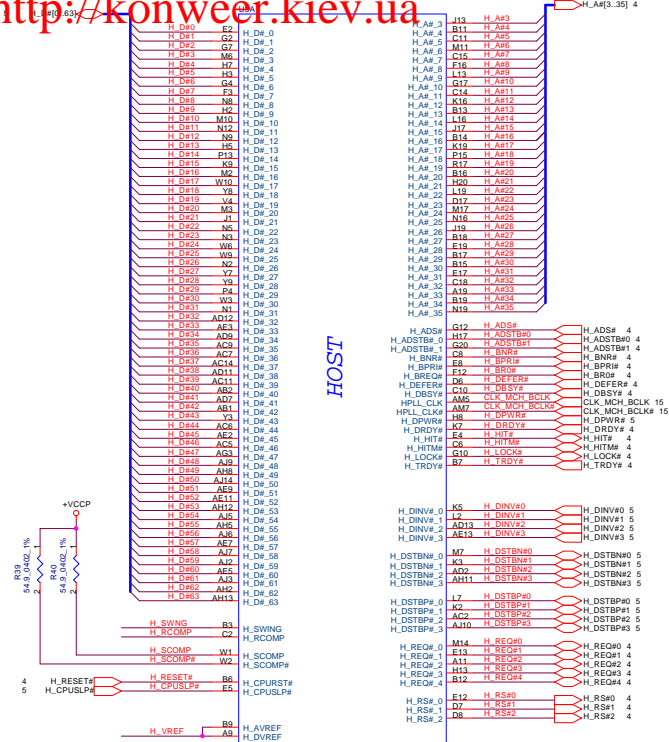
JP2D			
A4	VSS001	VSS080	P8
A5	VSS002	VSS083	P21
A11	VSS003	VSS084	P22
A14	VSS004	VSS085	P22
A16	VSS005	VSS086	P22
A19	VSS006	VSS087	P22
A22	VSS007	VSS088	T1
AF2	VSS008	VSS089	T1
B6	VSS009	VSS090	T4
B8	VSS010	VSS091	T7
B11	VSS011	VSS092	T26
B13	VSS012	VSS093	T17
B18	VSS013	VSS094	U6
B19	VSS014	VSS095	U2
B21	VSS015	VSS096	U24
C2	VSS016	VSS097	U5
C4	VSS017	VSS098	U22
C8	VSS018	VSS099	U25
C11	VSS019	VSS100	W1
C14	VSS020	VSS101	W1
C19	VSS021	VSS102	W2
C2	VSS022	VSS103	W2
C22	VSS023	VSS104	V3
C25	VSS024	VSS105	V3
D1	VSS025	VSS106	V1
D11	VSS026	VSS107	V24
D4	VSS027	VSS108	V24
D8	VSS028	VSS109	V22
D11	VSS029	VSS110	V22
D13	VSS030	VSS111	AA2
D18	VSS031	VSS112	AA4
D19	VSS032	VSS113	AA4
D21	VSS033	VSS114	AA16
D23	VSS034	VSS115	AA19
D28	VSS035	VSS116	AA22
E3	VSS036	VSS117	AA25
E8	VSS037	VSS118	AB1
E11	VSS038	VSS119	AB4
E14	VSS039	VSS120	AB5
E16	VSS040	VSS121	AB11
E19	VSS041	VSS122	AB13
E21	VSS042	VSS123	AB16
E24	VSS043	VSS124	AB19
F4	VSS044	VSS125	AB23
F8	VSS045	VSS126	AB26
F11	VSS046	VSS127	AC2
F13	VSS047	VSS128	AC2
F16	VSS048	VSS129	AC11
F19	VSS049	VSS130	AC14
F21	VSS050	VSS131	AC16
F22	VSS051	VSS132	AC19
F25	VSS052	VSS133	AC21
G4	VSS053	VSS134	AC24
G8	VSS054	VSS135	AD2
G28	VSS055	VSS136	AD5
H4	VSS056	VSS137	AD8
H8	VSS057	VSS138	AD11
H9	VSS058	VSS139	AD13
H21	VSS059	VSS140	AD16
H24	VSS060	VSS141	AD19
J2	VSS061	VSS142	AD22
J22	VSS062	VSS143	AD25
K5	VSS063	VSS144	AE1
K1	VSS064	VSS145	AE4
K4	VSS065	VSS146	AE5
K29	VSS066	VSS147	AE8
K38	VSS067	VSS148	AE11
L3	VSS068	VSS149	AE14
L6	VSS069	VSS150	AE16
L1	VSS070	VSS151	AE19
L21	VSS071	VSS152	AE23
L24	VSS072	VSS153	AE26
M2	VSS073	VSS154	AF1
M5	VSS074	VSS155	AF2
M22	VSS075	VSS156	AF3
M28	VSS076	VSS157	AF6
N1	VSS077	VSS158	AF13
N4	VSS078	VSS159	AF16
N23	VSS079	VSS160	AF19
N28	VSS080	VSS161	AF21
P1	VSS081	VSS162	AZ2
		VSS163	AZ5



Near CPU CORE regulator ESR <= 1.5m ohm Capacitor > 1980uF



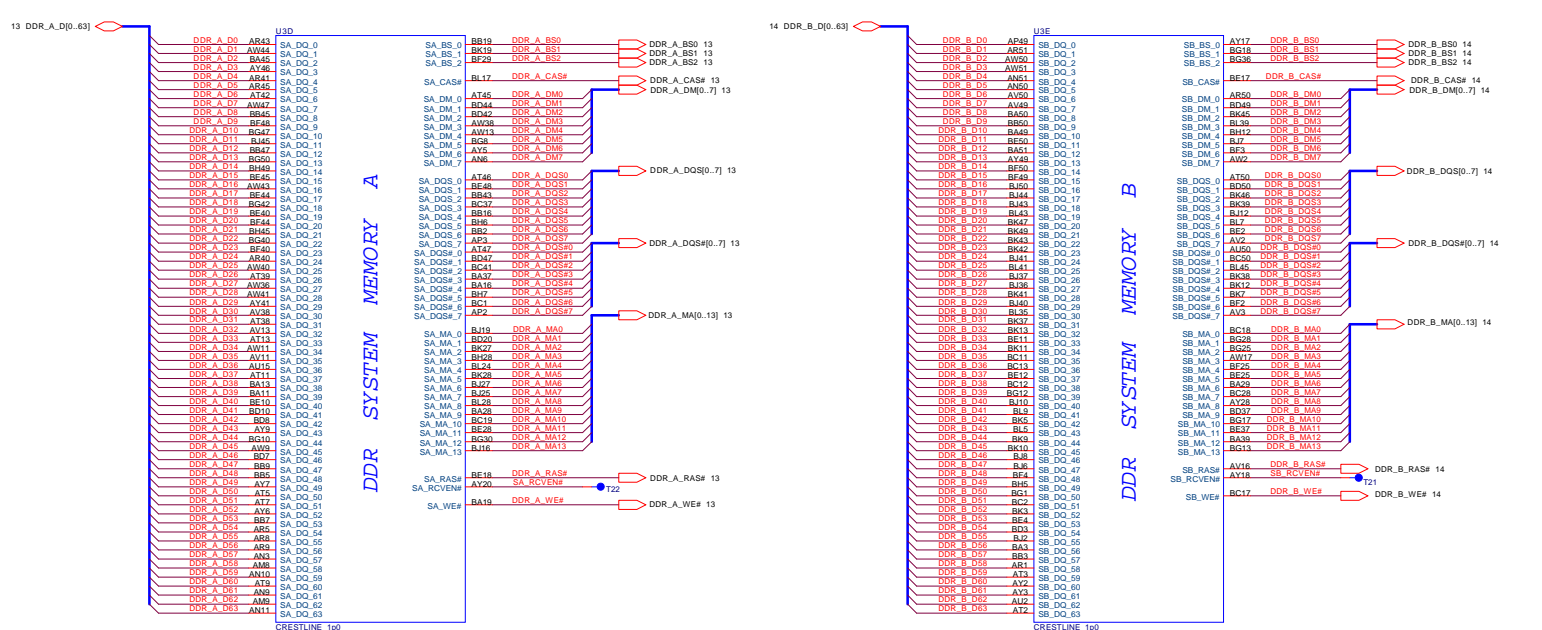
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Security Classification	Compal Secret Data	Deciphered Date	2006/03/10	Title
Issued Date	2007/03/26	Deciphered Date	2006/03/10	CRESTLINE(1/6)-AGTL+DMI/DDR2

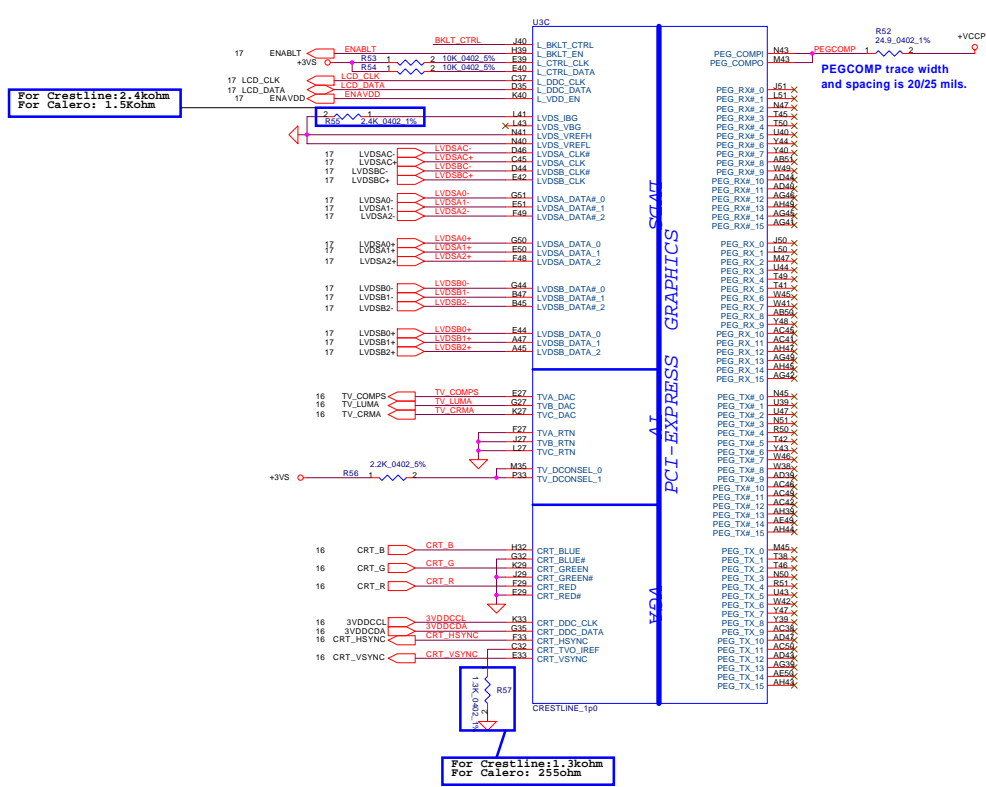
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Strap Pin Table

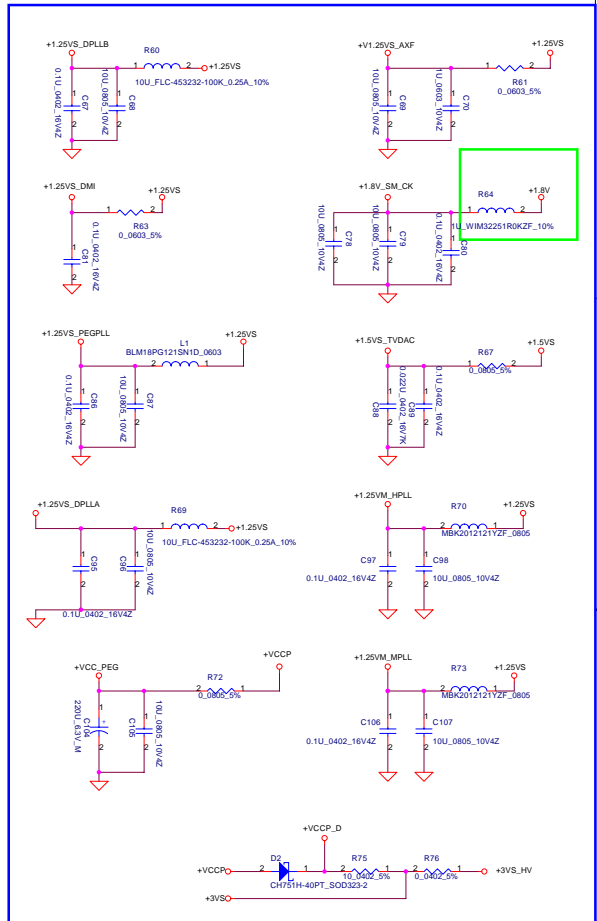
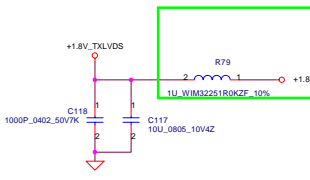
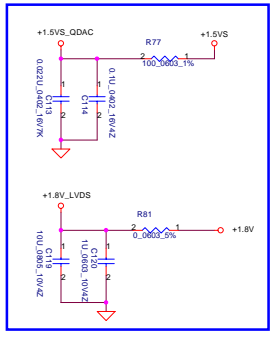
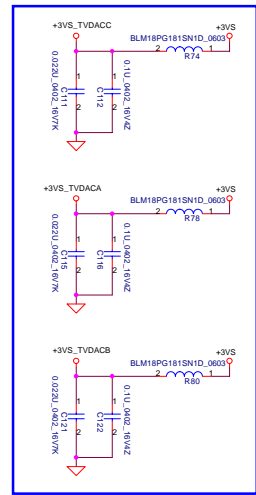
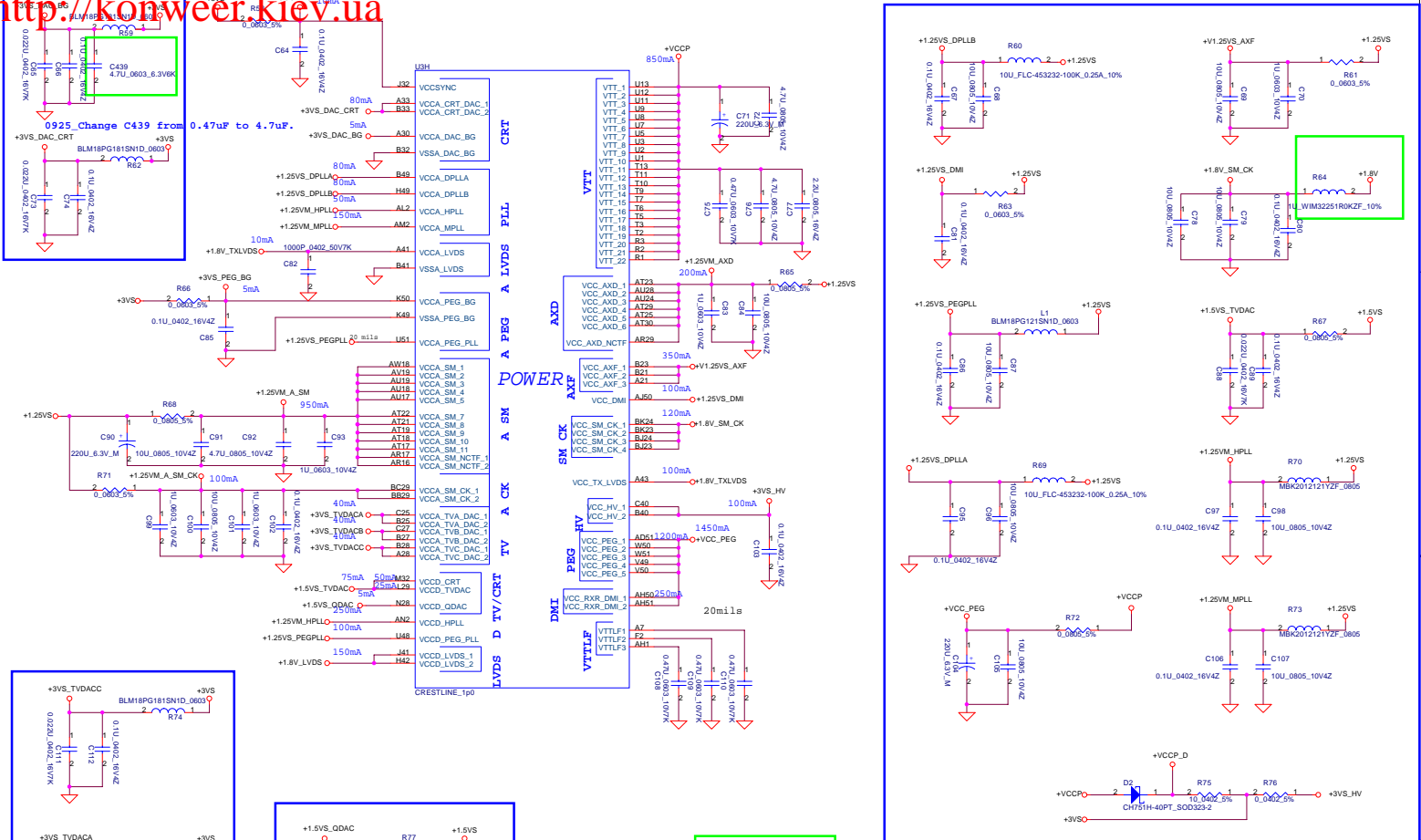


CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

CFG[17:3] have internal pull up  
CFG[19:18] have internal pull down

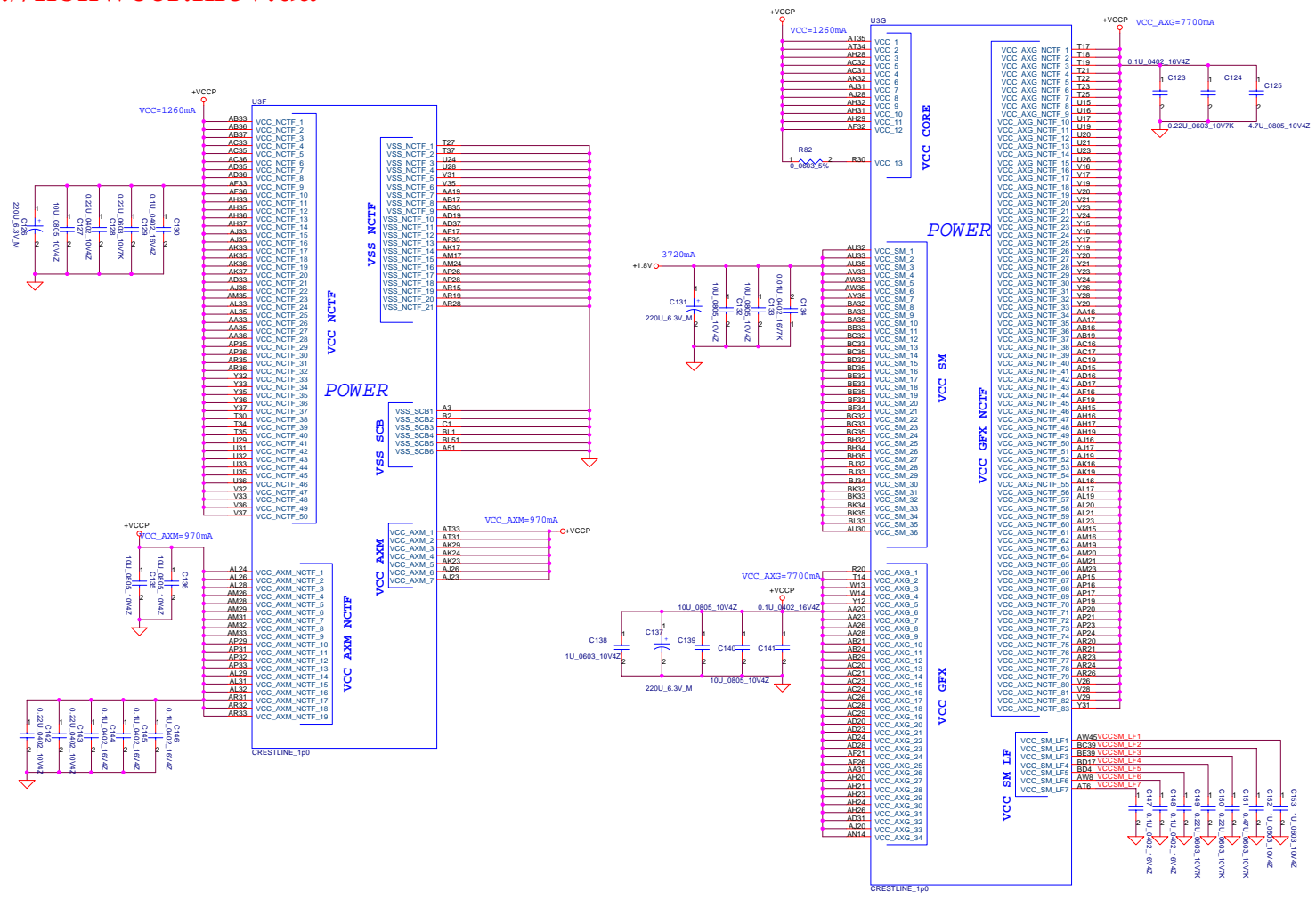
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Compal Electronics, Inc.  
CRESTLINE(3/6)-VGA/LVDS/TV

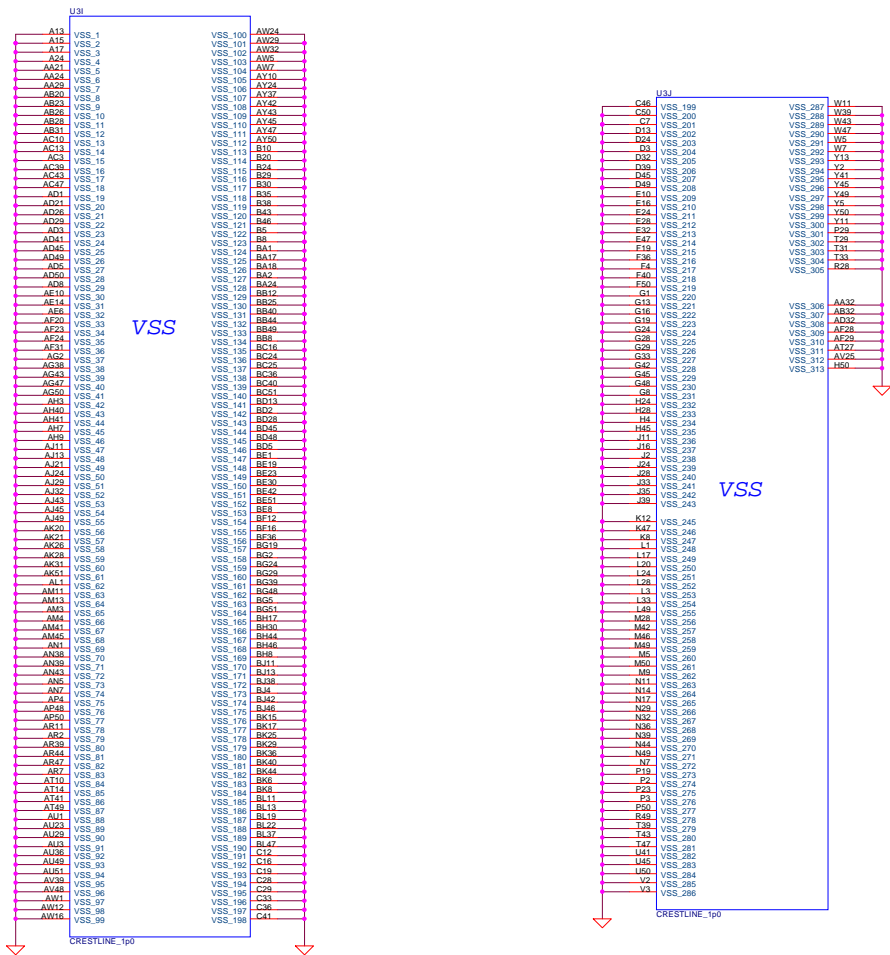


1022\_Change R64, R79 from 0 ohm to 1uH/400mA inductor.

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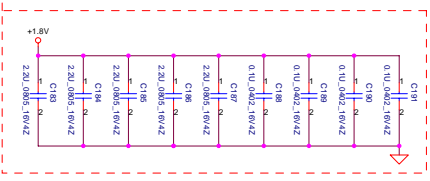
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**CRESTLINE(6/6)-PWR/GND**

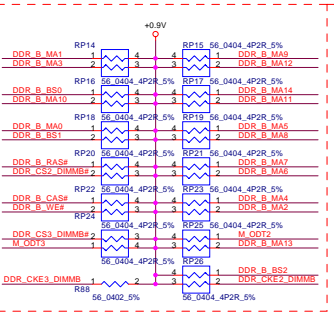
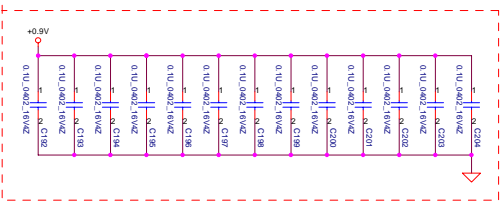


- 8 DDR\_B\_CS0[0..63]
- 8 DDR\_B\_D0[0..63]
- 8 DDR\_B\_DM[0..7]
- 8 DDR\_B\_DS0[0..7]
- 7.8 DDR\_B\_MA[0..14]

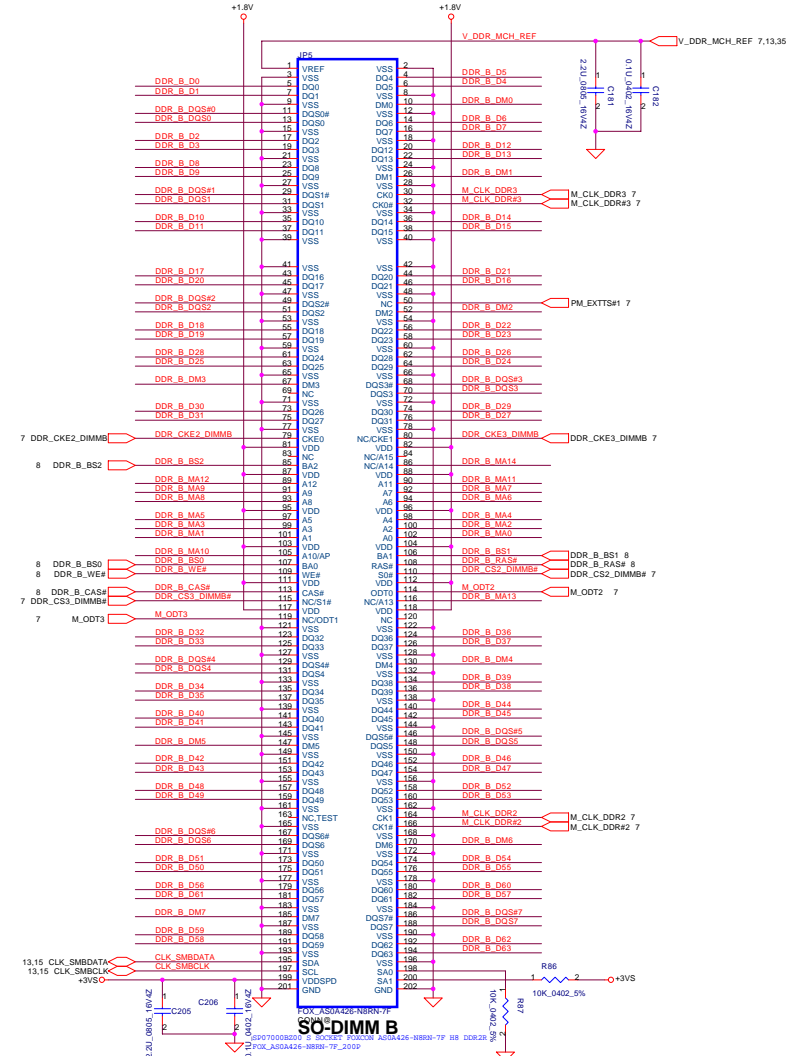
**Layout Note:**  
Place near JP10



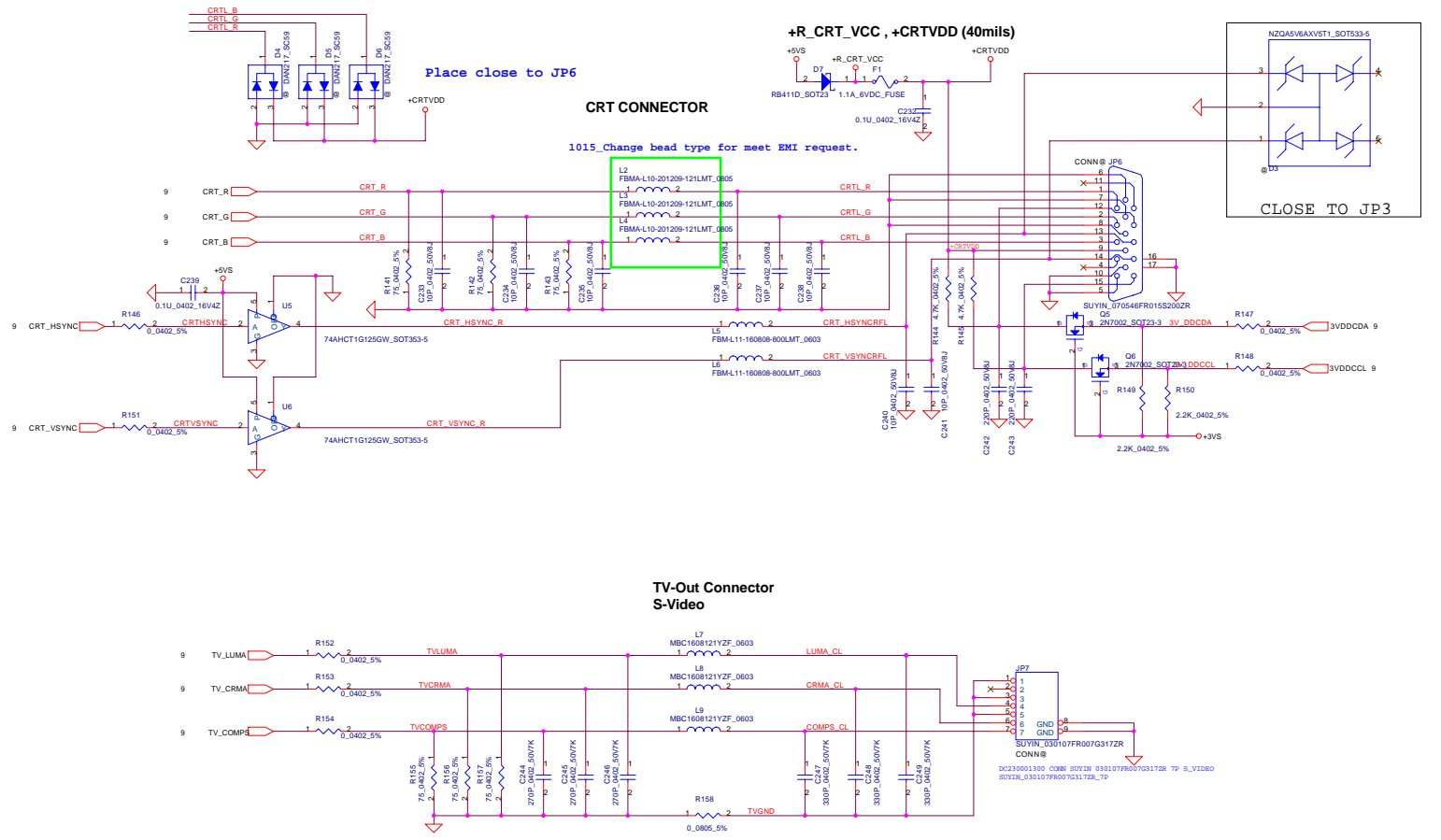
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



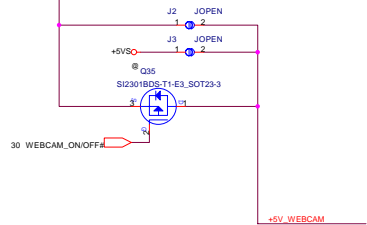
**Layout Note:**  
Place these resistor closely JP10, all trace length Max=1.5"



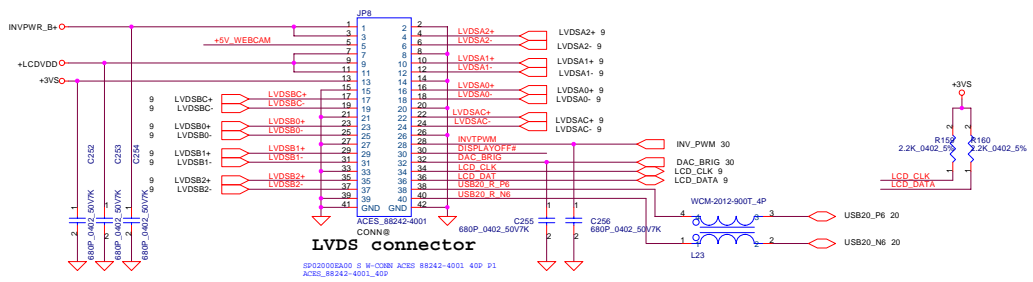
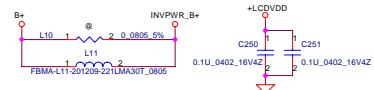




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<b>Compal Electronics, Inc.</b> <b>CRT &amp; TVout Connector</b>			Title <b>CRT &amp; TVout Connector</b>
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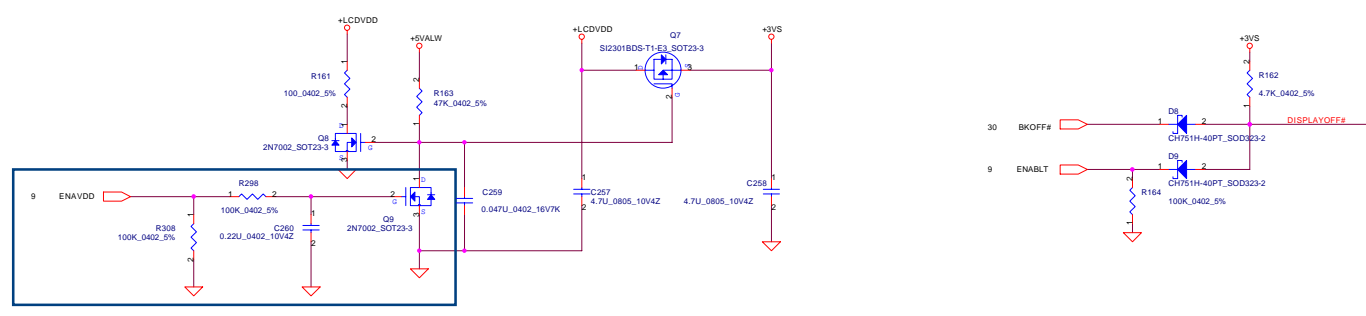


**LVDS CONN**



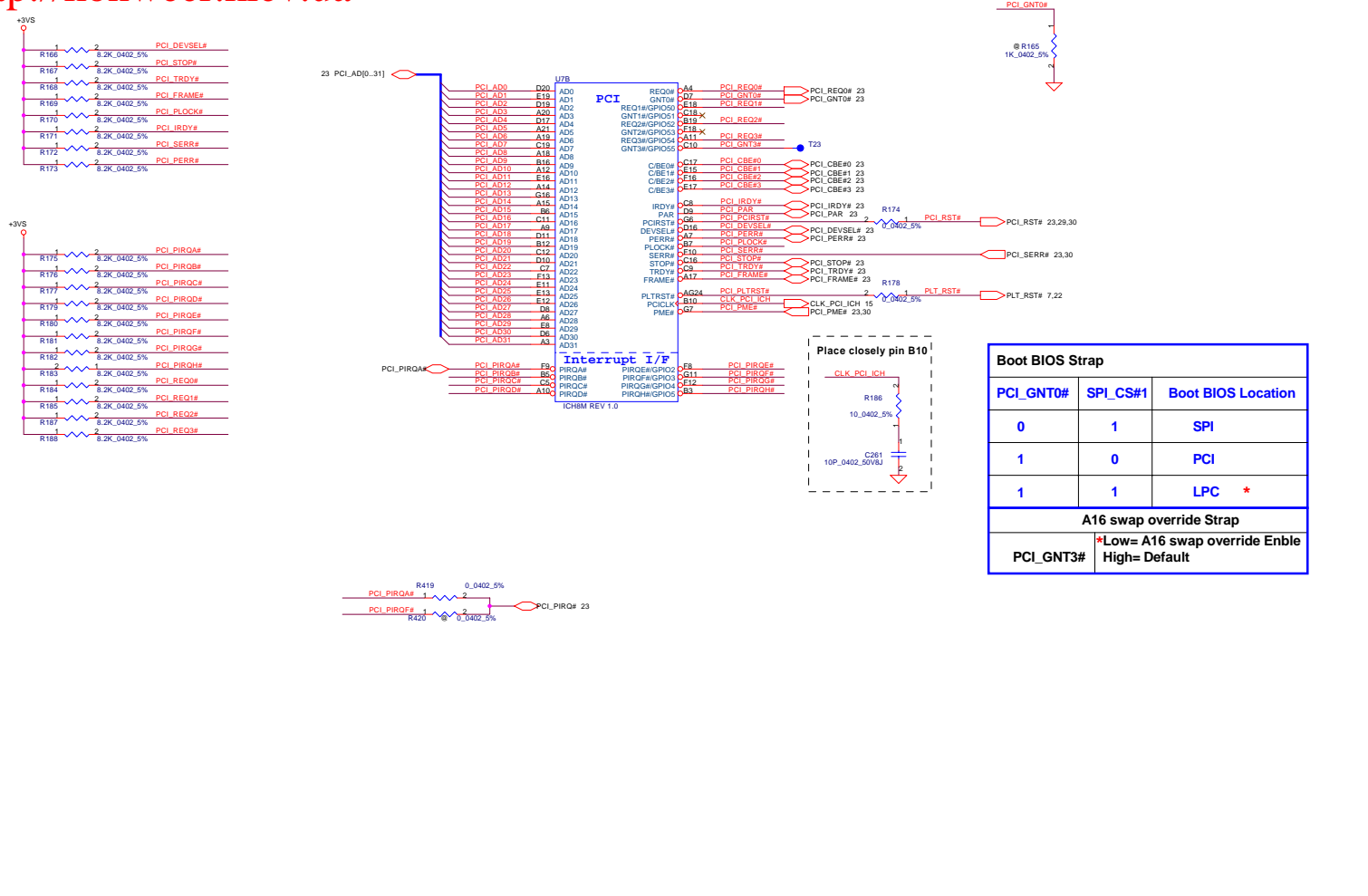
**LVDS connector**

SP920089A00 0 W-CONN ACES 88242-4001 40P P1  
ACES\_88242-4001\_40P



Avoid Panel display garbage after power on.

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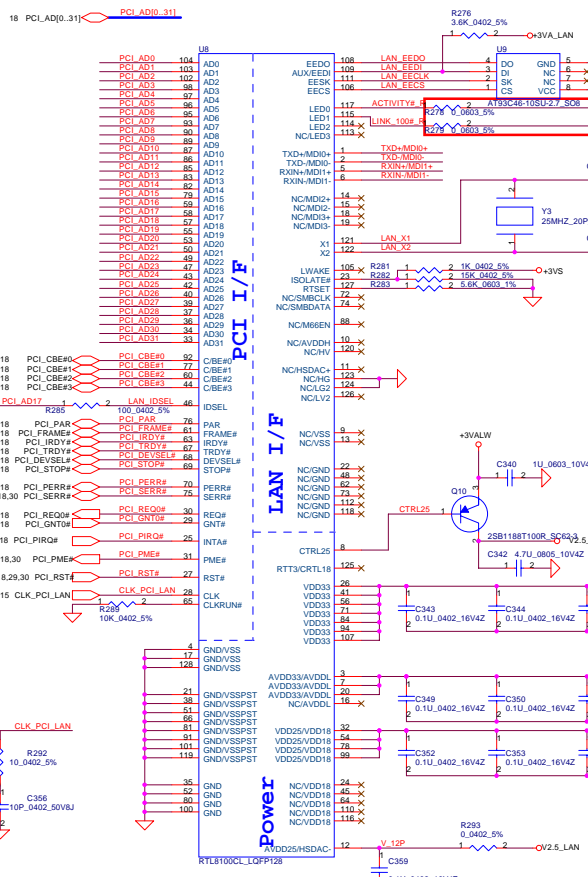
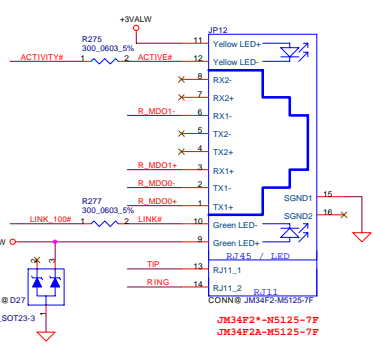
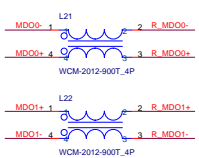








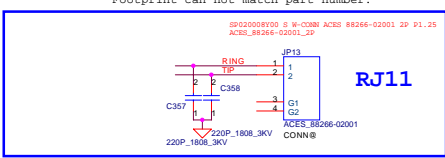
Close to JP12



For RMI, locate close to LAN chip

close to chip

close to magnetic



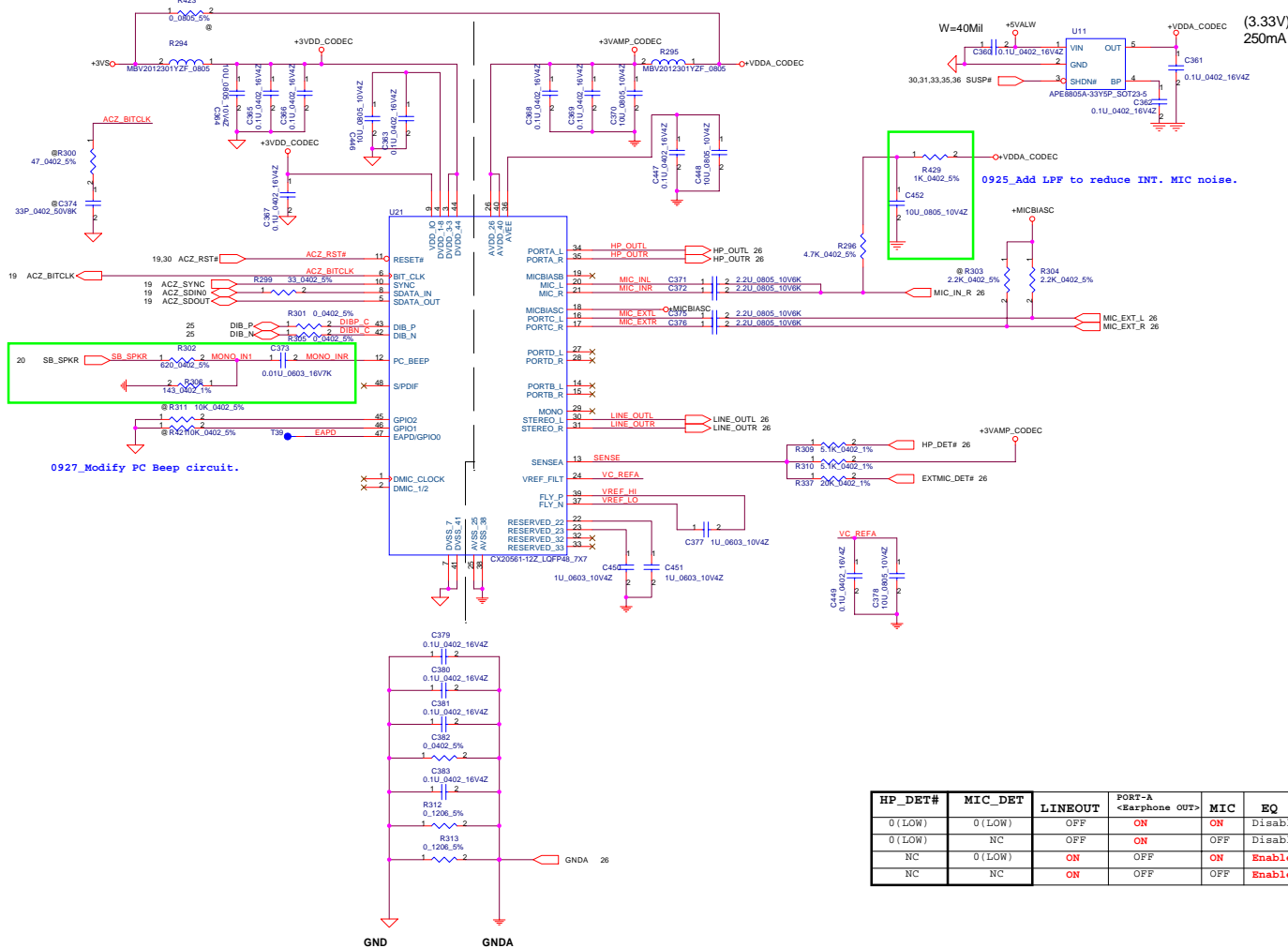
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2007/08/29	LAN-8100CL	
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	LA-4031P	1.0			

**AUDIO CODEC**

For Layout:  
Place decoupling caps near the power pins of SmartAMC device.

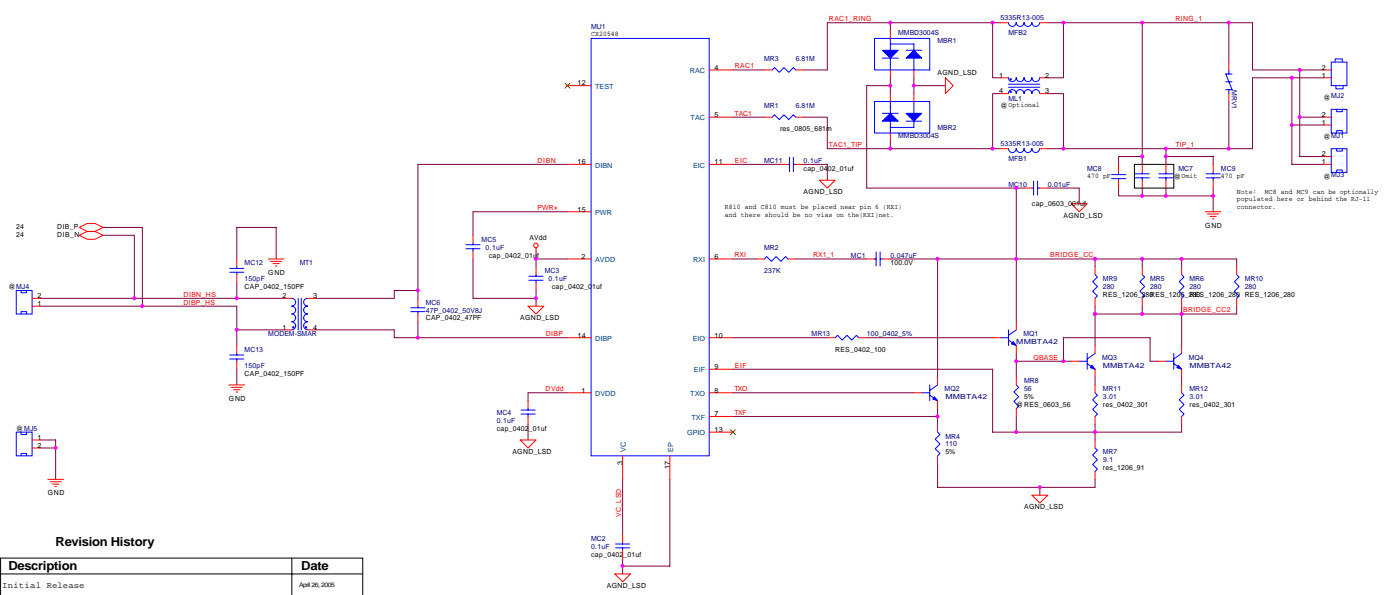
**CODEC POWER**

(3.33V)  
250mA



HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

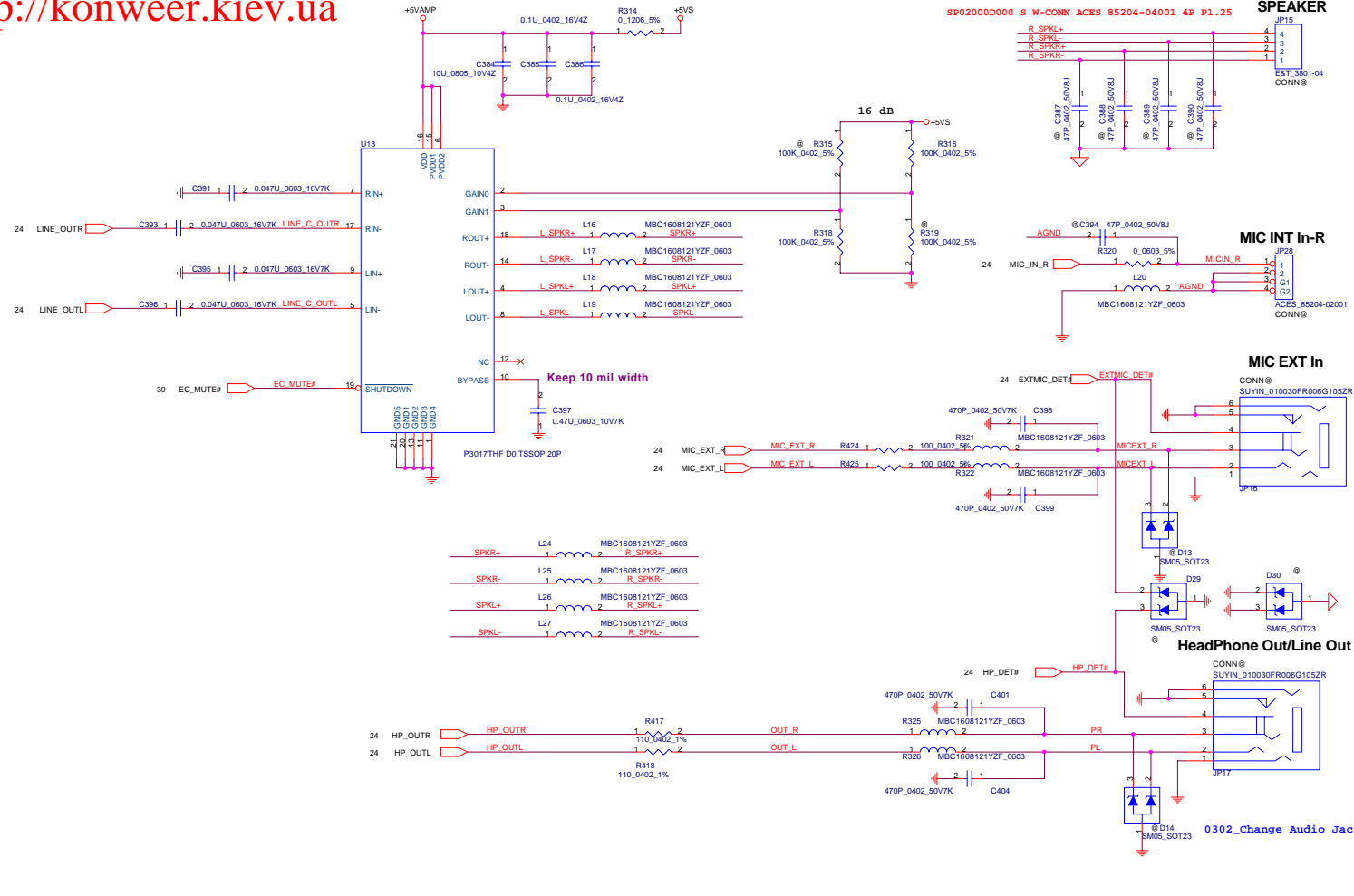
Security Classification		Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Size	Document Number		Rev
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				Date	Wednesday, October 24, 2007	Sheet	24 of 42



Revision History

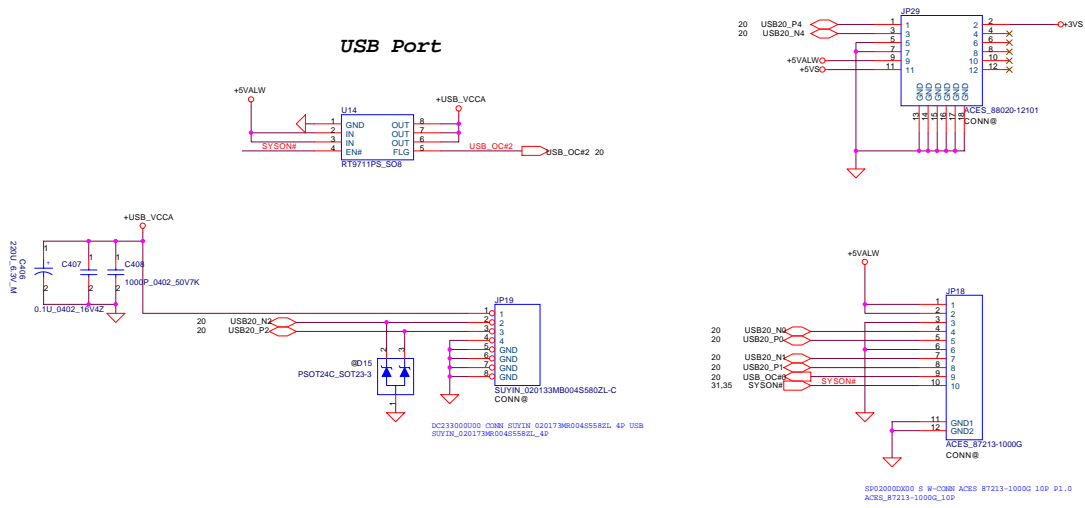
REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	April 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

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Doc No.	LA-401P	Rev	1.0	
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				LA-403IP	Rev 1.0
				Date: Wednesday, October 24, 2007	Sheet 26 of 42

**USB Port**

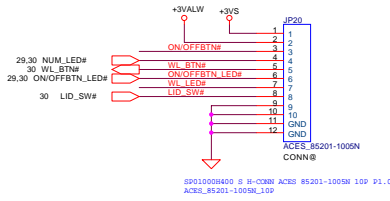


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Issued Date	2007/03/26	Deciphered Date	2006/07/26	<b>USB CONN.</b>
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Size	Document Number	Rev	Date	
	LA-403P	1.0	Wednesday, October 24, 2007	
			Sheet	27 of 42

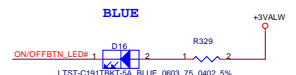
1015\_Remove U22 and U23.



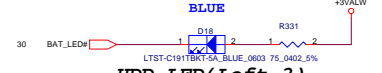
M/BtoS/B



POWER LED(Left 1)



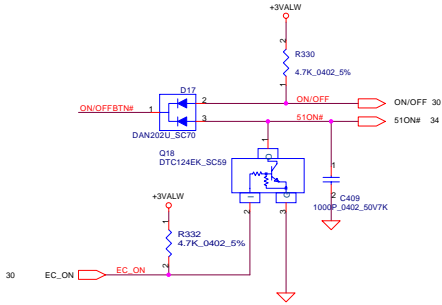
Battery Charge LED(Left 2)



HDD LED(Left 3)

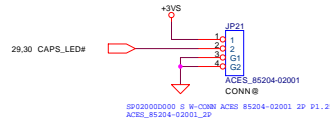


Power ON/OFF

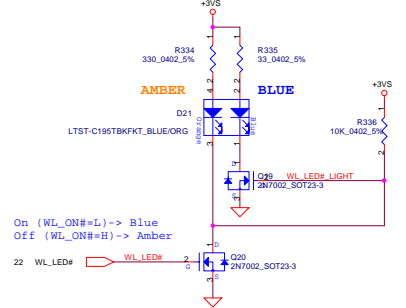


0426\_Change all LED power source from 5V to 3V.

M/B to SB(Caps Lock LED)



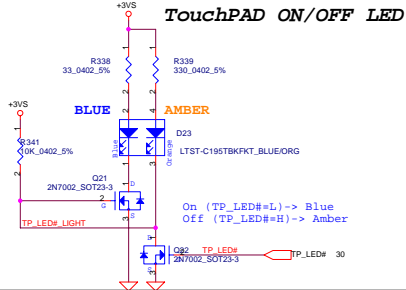
Wireless ON/OFF LED(Left 4)



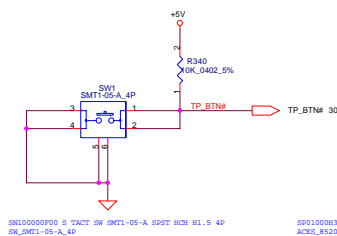
On (WL\_ON#=L) -> Blue  
Off (WL\_ON#=H) -> Amber

D21, D25, D23 Footprint can not match part number.

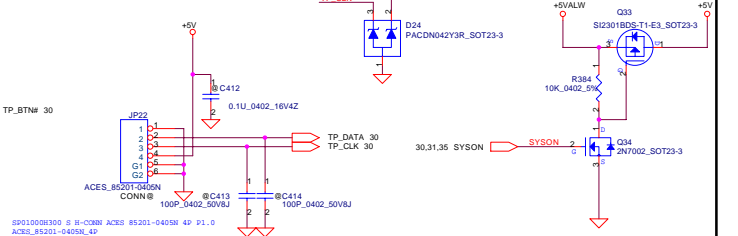
TouchPAD ON/OFF LED



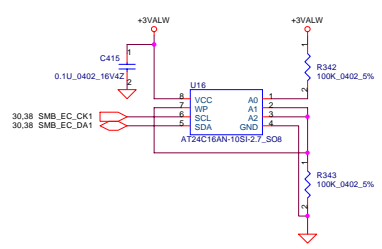
TP ON/OFF



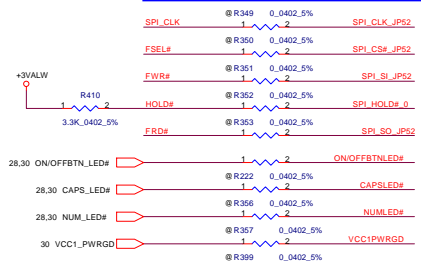
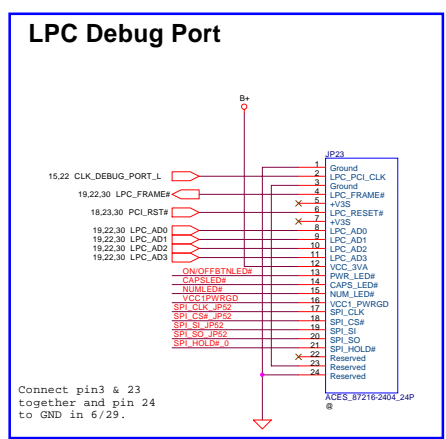
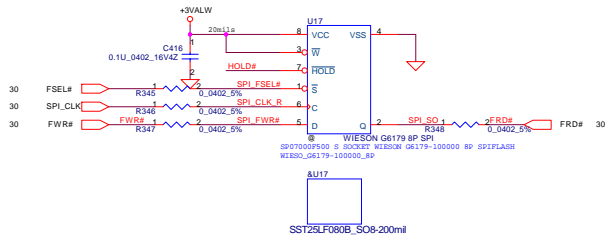
T/P Board



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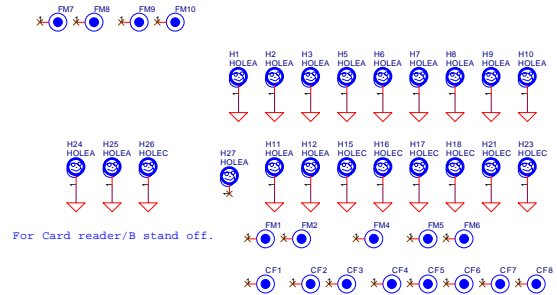
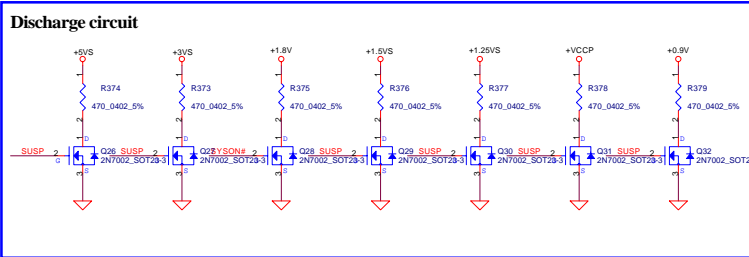
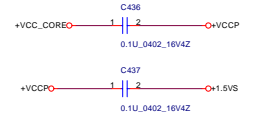
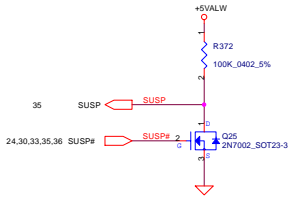
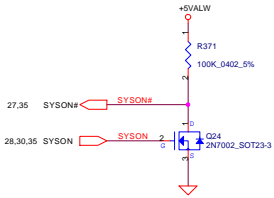
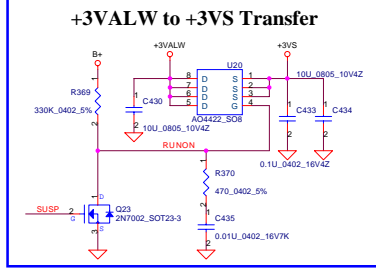
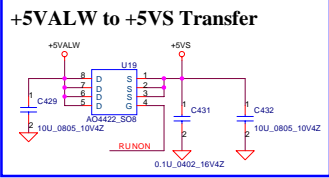


**SPI ROM**

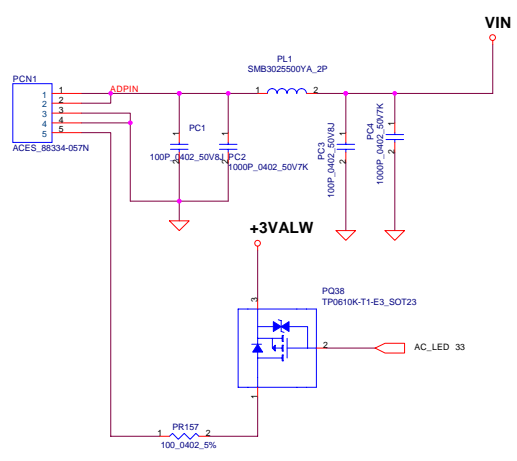


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Date	Wednesday, October 24, 2007	Sheet	29	of 42

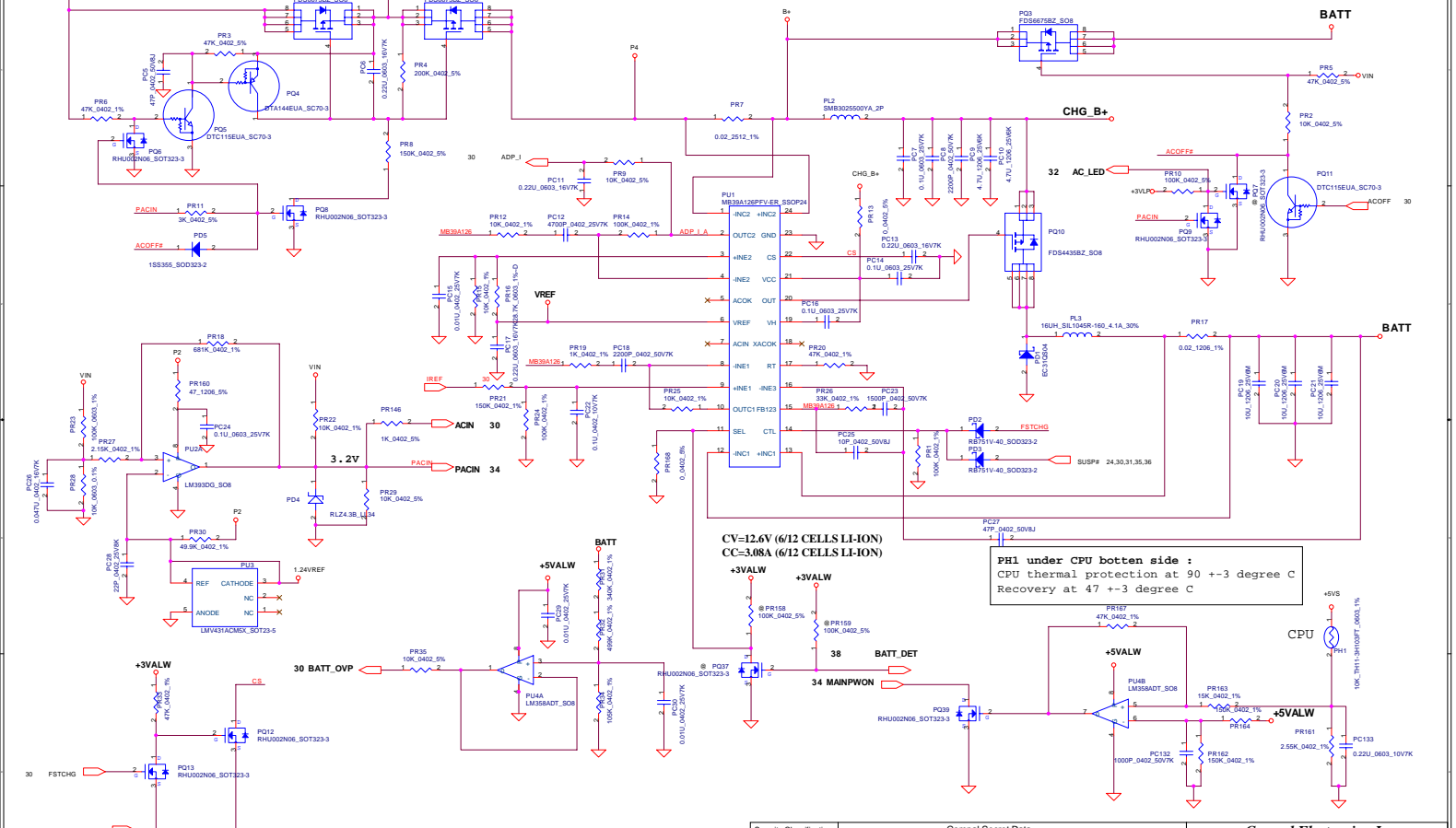




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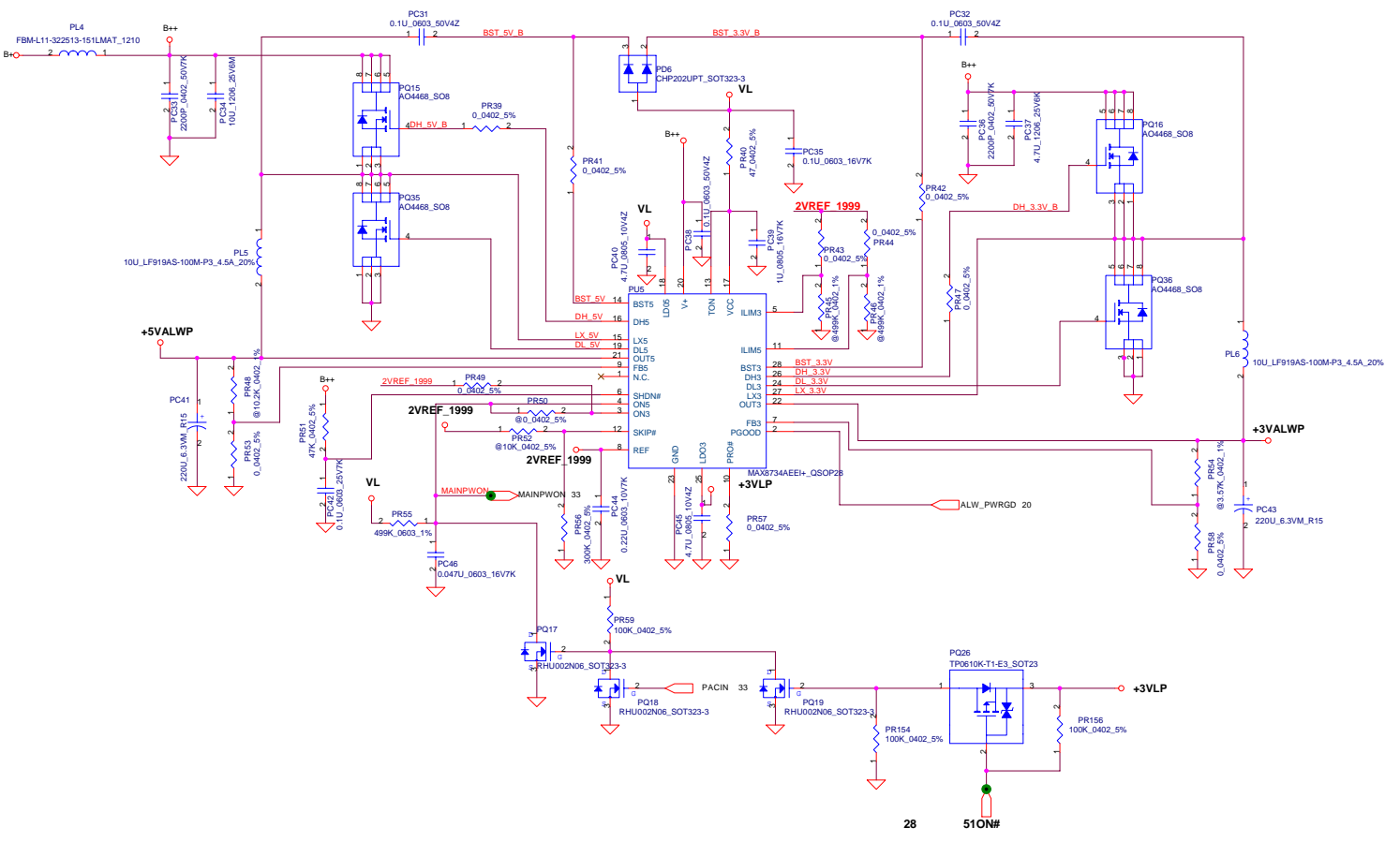


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Issued Date	<issued_Date>	Deciphered Date	<Deciphered_Date>	<b>DC CONN</b>
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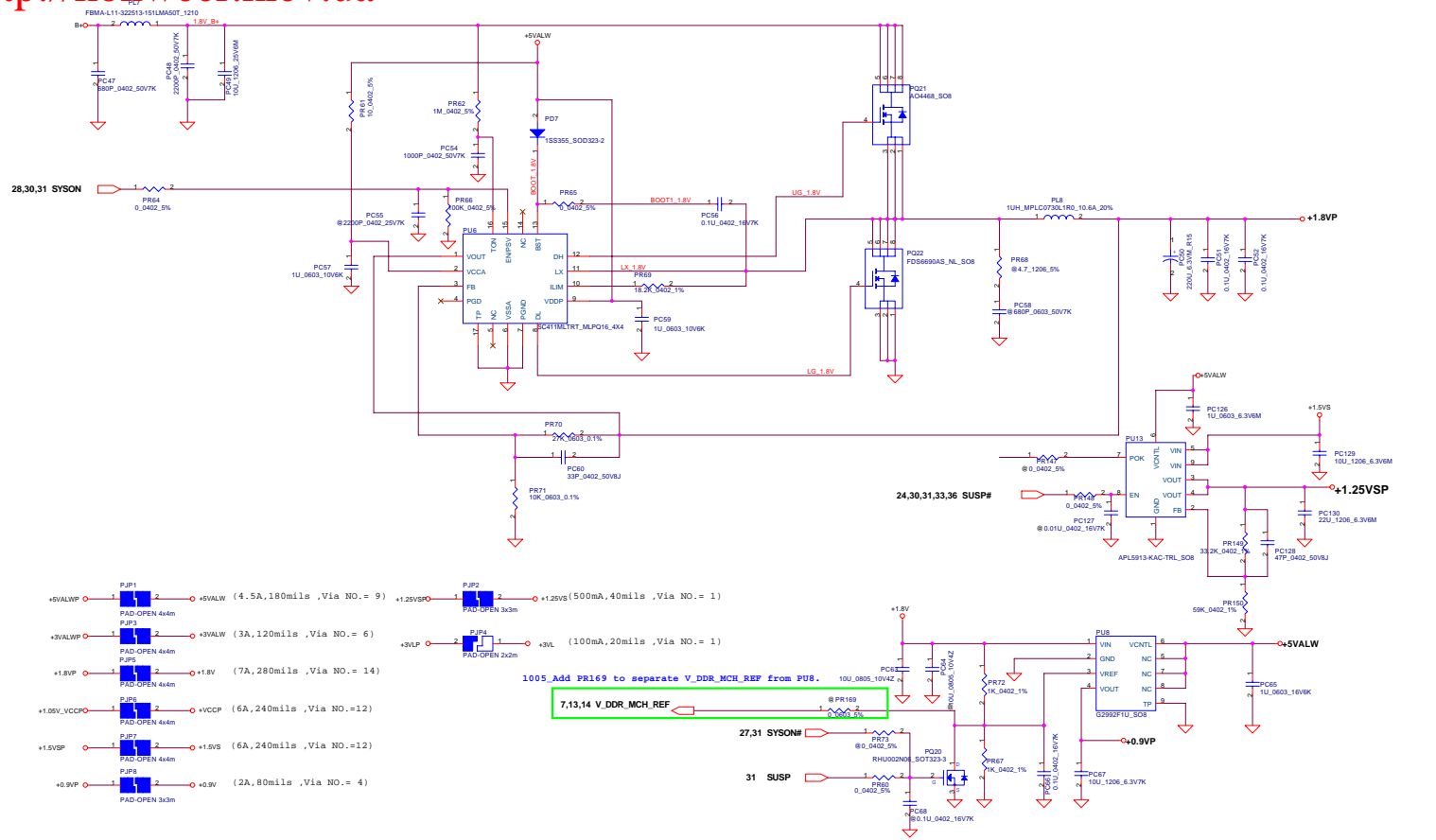
PH1 under CPU bottom side :  
 CPU thermal protection at 90 +3 degree C  
 Recovery at 47 +3 degree C

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100K	WSP02550Y	00000000	00000000



28 510N#

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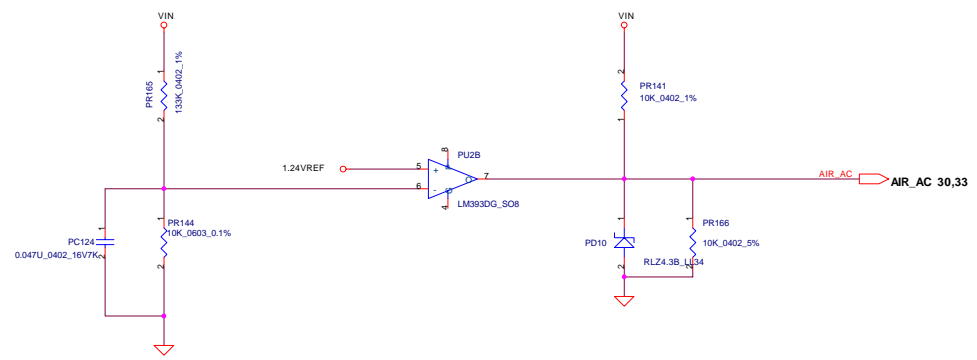
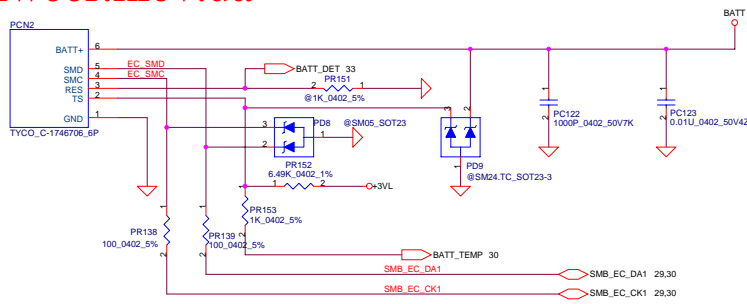


- +SVALW → PJP1 → +SVALW (4.5A, 180mils, Via NO.= 9)
- +SVALW → PJP2 → +1.25VSP (500mA, 40mils, Via NO.= 1)
- +SVALW → PJP3 → +SVALW (3A, 120mils, Via NO.= 6)
- +1.8VP → PJP4 → +1.8V (7A, 280mils, Via NO.= 14)
- +1.05V\_VCCP → PJP6 → +VCCP (6A, 240mils, Via NO.= 12)
- +1.5VSP → PJP7 → +1.5VS (6A, 240mils, Via NO.= 12)
- +0.9VP → PJP8 → +0.9V (2A, 80mils, Via NO.= 4)

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				1.8VP/0.9VSP/2.5VSP	LA-403P		1.0	
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<small>Date: Wednesday, October 28, 2009 8:58:36 AM Page 35 of 42</small>								







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				Size	Document Number	Rev
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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

Security Classification	Compal Secret Data		Title		
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Item	Change item	Page	Date	Phase
1	Change R296 2.2K to 4.7K and Reserved R303	24	8/6	SI-->PV
2	Add R424 R425 100ohm on MIC_EXT_R and MIC_EXT_L	26	8/6	SI-->PV
3	Fine tune R298 C260 value	17	8/6	SI-->PV
4	Change PIRQ from F to A	18	8/14	SI-->PV
5	Connect PCI_SERR# to EC GPIO pin.	18	8/31	SI-->PV
6	Modify PC BEEP circuit.	20	8/31	SI-->PV
7	For support Intel Penryn CPU.	04	9/3	SI-->PV
8	For ESD request.	28	9/3	SI-->PV
9	For EMI request.	26	9/5	SI-->PV
10	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	9/7	SI-->PV
11	Add R417 and R418 to fine-tune Vp-p.	26	9/7	SI-->PV
12	For ESD request.	20	9/7	SI-->PV
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Item	Change item	Page	Date	Phase
1	Solve Vref miss when entry S3 mode.	7	9/25	PV-->MV
2	Solve wave ripple on CRT and TV.	10	9/25	PV-->MV
3	Solve RTC timing too exceed.	18	9/25	PV-->MV
4	Reduce INT_MIC noise.	24	9/25	PV-->MV
5	Solve S3 resume fail when use Micron DDR module.	35	10/05	PV-->MV
6	Solve pop noise when entry or resume from S3.	24	9/27	PV-->MV
7	Solve EMI fail for Memory module.	7	9/27	PV-->MV
8	ICH 1.5V power rail 700mA current requirement.	21	10/04	PV-->MV
9	Remove U22 and U23.	28	10/15	PV-->MV
10	For EMI request.	16	10/15	PV-->MV
11	To avoid too easy to open solder for CLRP2.	15	10/15	PV-->MV
12	Solve acoustic noise issue.	10	10/22	PV-->MV
13				
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