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PV

2007/03/30

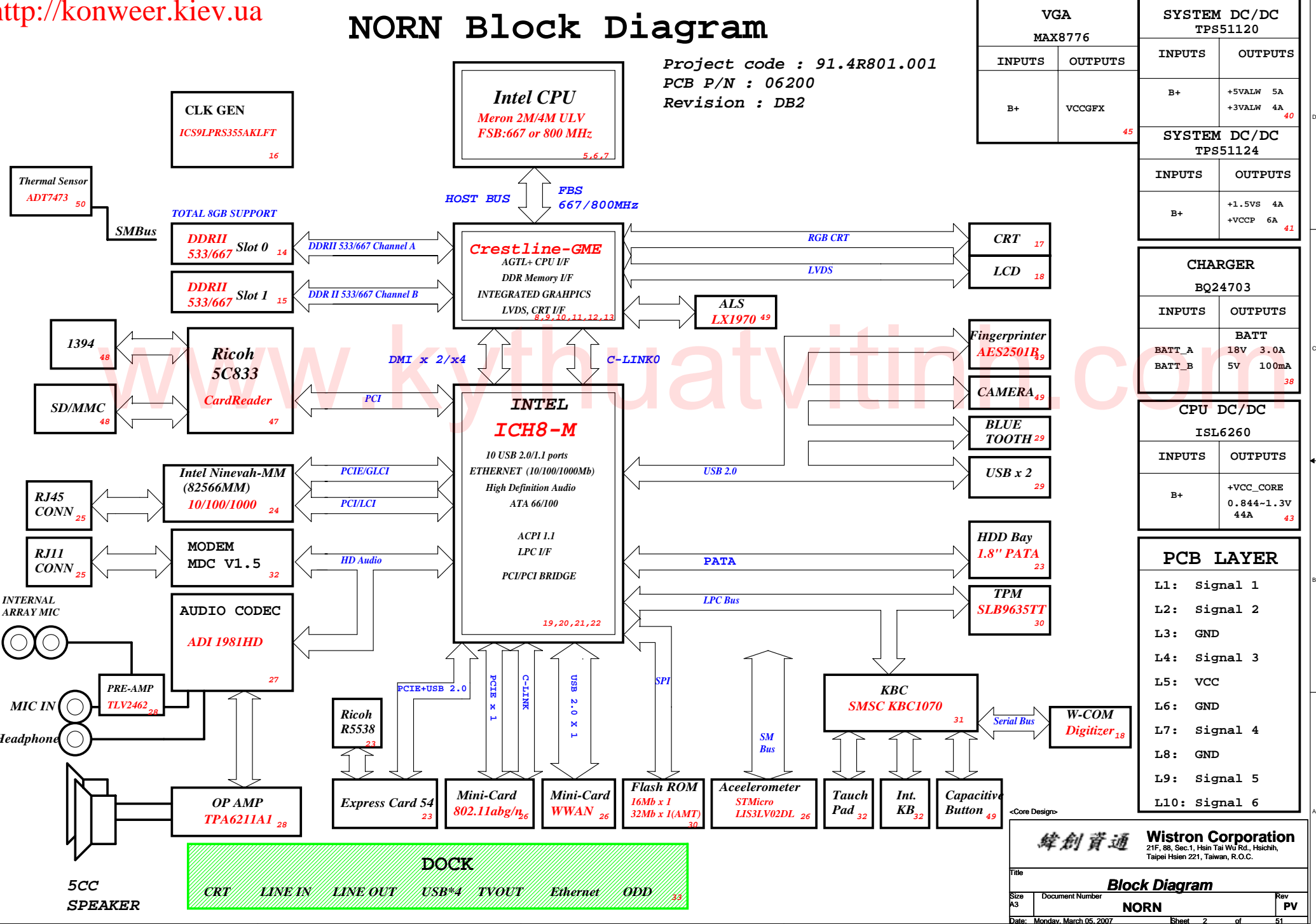
REV : PV-04

<Variant Name>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NORN			
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NORN Block Diagram

Project code : 91.4R801.001
 PCB P/N : 06200
 Revision : DB2



VGA MAX8776		SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
B+	VCCGFX	B+	+5VALW 5A +3VALW 4A

SYSTEM DC/DC TPS51124	
INPUTS	OUTPUTS
B+	+1.5VS 4A +VCCP 6A

CHARGER BQ24703	
INPUTS	OUTPUTS
BATT_A	BATT
BATT_B	1.8V 3.0A 5V 100mA

CPU DC/DC ISL6260	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844-1.3V 44A

PCB LAYER	
L1:	Signal 1
L2:	Signal 2
L3:	GND
L4:	Signal 3
L5:	VCC
L6:	GND
L7:	Signal 4
L8:	GND
L9:	Signal 5
L10:	Signal 6

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: A3 Document Number: **NORN** Rev: **PV**

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Change Notes List			
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power plane \ State	+BB LDO3 LDO5	+5VALW +5VALW	+1.8V +0.9V	+5VS +3VS +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM +1.25VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader & 1394	AD22	2	G, E

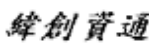
DMA Channel	Device
DMA0	Modem/LAN
DMA1	ECP
DMA2	Floppy Disk
DMA3	Audio
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	FREE
1	Fingerprint
2	EXPRESS SLOT
3	Camera
4	Walk-up1 (Right Side)
5	Walk-up2 (Left Side)
6	Bluetooth
7	Dock 1
8	WWAN
9	Dock 2

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	Floppy
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family) USB Universal Host Control
18	Intel 82801H (ICH8 Family) USB Universal Host Control Richo R5C853 Integrates FlashMedia Control Richo R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family) PCI Express Root Port -27D6 Intel 82801H (ICH8 Family) USB Universal Host Control
20	Intel 82801H (ICH8 Family) USB Universal Host Control Intel 82801H (ICH8 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH8 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

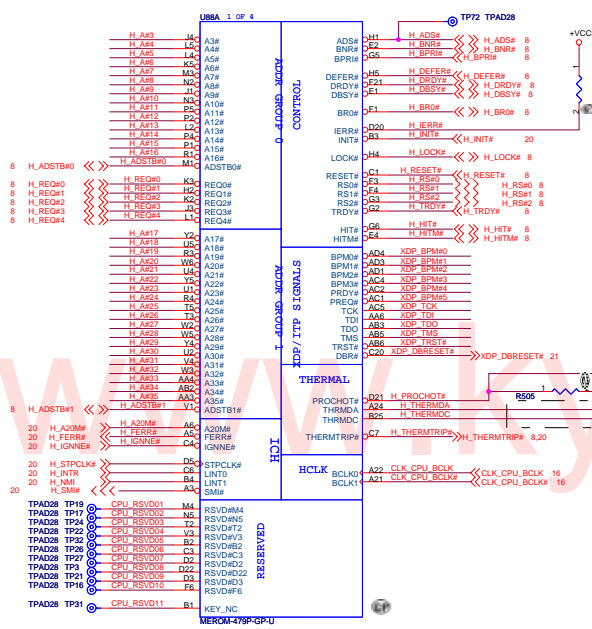
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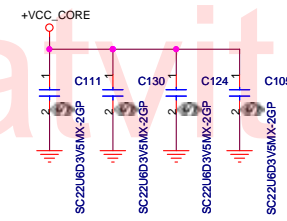
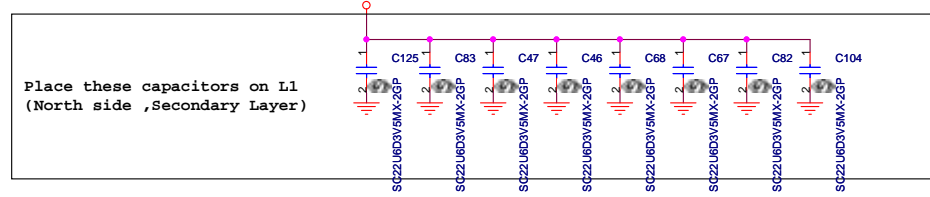
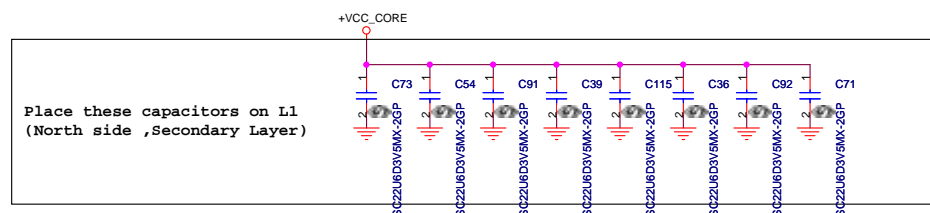
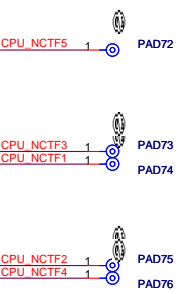
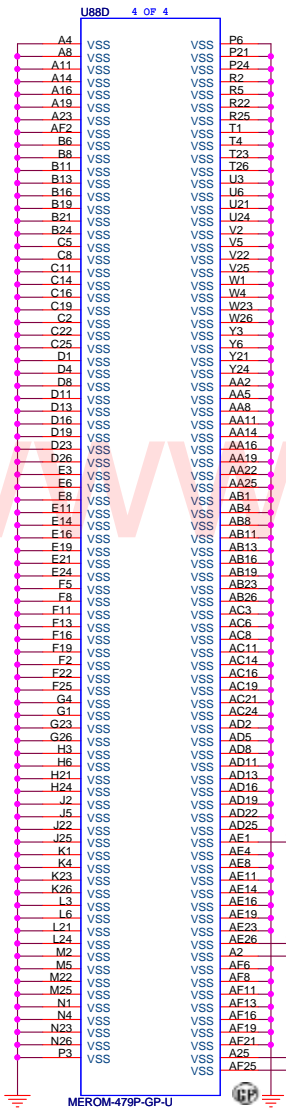
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D
C
B
A

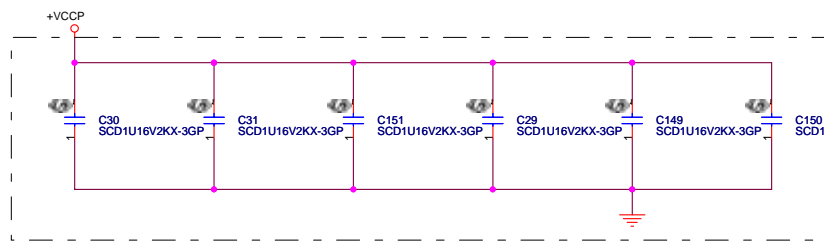
8 H_AD3[35] <<<

layout note : Change R305 to 649 ohm if using XTP to ITP adapter





Mid Frequenced Decoupling



Place these inside socket cavity on L1 (North side Secondary)

<Core Design>

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Title			
Meron(3/3)-GND&Bypass			
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<< >> DDR_A_D[0..63] 14
 << >> DDR_A_BS[0..2] 14
 << >> DDR_A_DM[0..7] 14
 << >> DDR_A_DQS[0..7] 14
 << >> DDR_A_DQS# [0..7] 14
 << >> DDR_A_MA[0..13] 14

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DDR A D0	AR43	SA_DQ0	SA_BS0	BB19	DDR A BS0
DDR A D1	AW44	SA_DQ1	SA_BS1	BK19	DDR A BS1
DDR A D2	BA45	SA_DQ2	SA_BS2	BF29	DDR A BS2
DDR A D3	AY46	SA_DQ3			
DDR A D4	AR46	SA_DQ3			
DDR A D5	AR45	SA_DQ4	SA_CAS#	BL17	DDR A CAS# >>> DDR_A_CAS# 14
DDR A D6	AT42	SA_DQ5	SA_DM0	AT45	DDR A DM0
DDR A D7	AW47	SA_DQ6	SA_DM1	BD44	DDR A DM1
DDR A D8	BF48	SA_DQ7	SA_DM2	BD42	DDR A DM2
DDR A D9	BF48	SA_DQ8	SA_DM3	AW38	DDR A DM3
DDR A D10	BG47	SA_DQ9	SA_DM4	AW13	DDR A DM4
DDR A D11	BJ45	SA_DQ10	SA_DM5	BG8	DDR A DM5
DDR A D12	BB47	SA_DQ11	SA_DM6	AY5	DDR A DM6
DDR A D13	BG50	SA_DQ12	SA_DM7	AN6	DDR A DM7
DDR A D14	BH49	SA_DQ13			
DDR A D15	BE45	SA_DQ14			
DDR A D16	AW43	SA_DQ15	SA_DQS0	AT46	DDR A DQS0
DDR A D17	BE44	SA_DQ16	SA_DQS1	BE48	DDR A DQS1
DDR A D18	BG42	SA_DQ17	SA_DQS2	BB43	DDR A DQS2
DDR A D19	BE40	SA_DQ18	SA_DQS3	BC37	DDR A DQS3
DDR A D20	BF44	SA_DQ19	SA_DQS4	BB16	DDR A DQS4
DDR A D21	BH45	SA_DQ20	SA_DQS5	BH6	DDR A DQS5
DDR A D22	BG40	SA_DQ21	SA_DQS6	BB2	DDR A DQS6
DDR A D23	BE40	SA_DQ22	SA_DQS7	AP3	DDR A DQS7
DDR A D24	AR40	SA_DQ23	SA_DQS#0	CA17	DDR A DQS#0
DDR A D25	AW40	SA_DQ24	SA_DQS#1	CD47	DDR A DQS#1
DDR A D26	AT39	SA_DQ25	SA_DQS#2	CB41	DDR A DQS#2
DDR A D27	AW36	SA_DQ26	SA_DQS#3	CA37	DDR A DQS#3
DDR A D28	AW41	SA_DQ27	SA_DQS#4	CB16	DDR A DQS#4
DDR A D29	AY41	SA_DQ28	SA_DQS#5	CBZ	DDR A DQS#5
DDR A D30	AV38	SA_DQ29	SA_DQS#6	BC1	DDR A DQS#6
DDR A D31	AT38	SA_DQ30	SA_DQS#7	AP2	DDR A DQS#7
DDR A D32	AV13	SA_DQ31			
DDR A D33	AT13	SA_DQ32	SA_MA0	BJ19	DDR A MA0
DDR A D34	AW11	SA_DQ33	SA_MA1	BD20	DDR A MA1
DDR A D35	AV11	SA_DQ34	SA_MA2	BK27	DDR A MA2
DDR A D36	AU15	SA_DQ35	SA_MA3	BH28	DDR A MA3
DDR A D37	AT11	SA_DQ36	SA_MA4	BL24	DDR A MA4
DDR A D38	BA13	SA_DQ37	SA_MA5	BK28	DDR A MA5
DDR A D39	BA11	SA_DQ38	SA_MA6	BJ27	DDR A MA6
DDR A D40	BE10	SA_DQ39	SA_MA7	BJ25	DDR A MA7
DDR A D41	BD10	SA_DQ40	SA_MA8	BL28	DDR A MA8
DDR A D42	BD8	SA_DQ41	SA_MA9	BA28	DDR A MA9
DDR A D43	AY9	SA_DQ42	SA_MA10	BC19	DDR A MA10
DDR A D44	BG10	SA_DQ43	SA_MA11	BE28	DDR A MA11
DDR A D45	AV9	SA_DQ44	SA_MA12	BG30	DDR A MA12
DDR A D46	BD7	SA_DQ45	SA_MA13	BJ16	DDR A MA13
DDR A D47	BB9	SA_DQ46	SA_MA14	BJ29	DDR A MA14 <<< >>> DDR_A_MA14 14
DDR A D48	BB5	SA_DQ47			
DDR A D49	AY7	SA_DQ48	SA_RAS#	BE18	DDR A RAS# >>> DDR_A_RAS# 14
DDR A D50	AT5	SA_DQ49	SA_RCVEN#	AY20	SA_RCVEN# < TP6
DDR A D51	AY5	SA_DQ50			
DDR A D52	AY5	SA_DQ51	SA_WE#	BA19	DDR A WE# >>> DDR_A_WE# 14
DDR A D53	BB7	SA_DQ52			
DDR A D54	AR5	SA_DQ53			
DDR A D55	AR8	SA_DQ54			
DDR A D56	AR3	SA_DQ55			
DDR A D57	AN3	SA_DQ56			
DDR A D58	AM8	SA_DQ57			
DDR A D59	AN10	SA_DQ58			
DDR A D60	AT3	SA_DQ59			
DDR A D61	AN9	SA_DQ60			
DDR A D62	AM8	SA_DQ61			
DDR A D63	AN11	SA_DQ62			
		SA_DQ63			

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<< >> DDR_B_D[0..63] 15
 << >> DDR_B_BS[0..2] 15
 << >> DDR_B_DM[0..7] 15
 << >> DDR_B_DQS[0..7] 15
 << >> DDR_B_DQS# [0..7] 15
 << >> DDR_B_MA[0..13] 15

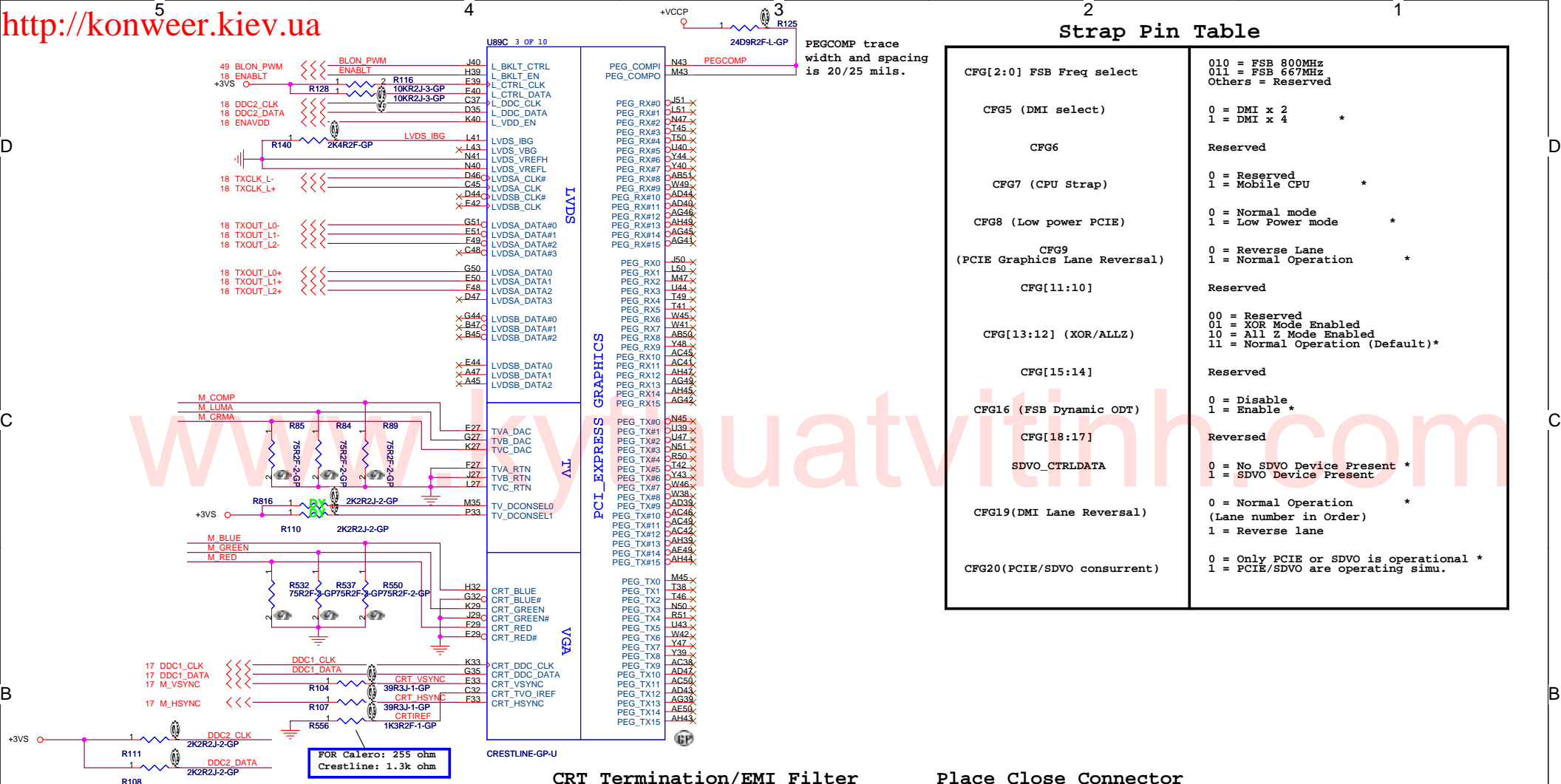
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DDR B D0	AP49	SB_DQ0	SB_BS0	AY17	DDR B BS0
DDR B D1	AR51	SB_DQ1	SB_BS1	BG18	DDR B BS1
DDR B D2	AW50	SB_DQ2	SB_BS2	BG36	DDR B BS2
DDR B D3	AW51	SB_DQ3			
DDR B D4	AN51	SB_DQ4	SB_CAS#	BE17	DDR B CAS# >>> DDR_B_CAS# 15
DDR B D5	AN50	SB_DQ5			
DDR B D6	AV50	SB_DQ6	SB_DM0	AR50	DDR B DM0
DDR B D7	AV49	SB_DQ7	SB_DM1	BD49	DDR B DM1
DDR B D8	BF50	SB_DQ8	SB_DM2	BK45	DDR B DM2
DDR B D9	B850	SB_DQ9	SB_DM3	BL39	DDR B DM3
DDR B D10	BA49	SB_DQ10	SB_DM4	BH12	DDR B DM4
DDR B D11	BE50	SB_DQ11	SB_DM5	BJ7	DDR B DM5
DDR B D12	BA51	SB_DQ12	SB_DM6	BF3	DDR B DM6
DDR B D13	AY49	SB_DQ13	SB_DM7	AW2	DDR B DM7
DDR B D14	BF50	SB_DQ14			
DDR B D15	BF49	SB_DQ15	SB_DQS0	AT50	DDR B DQS0
DDR B D16	BJ50	SB_DQ16	SB_DQS1	BD50	DDR B DQS1
DDR B D17	BJ44	SB_DQ17	SB_DQS2	BK46	DDR B DQS2
DDR B D18	BL43	SB_DQ18	SB_DQS3	BK39	DDR B DQS3
DDR B D19	BL43	SB_DQ19	SB_DQS4	BJ12	DDR B DQS4
DDR B D20	BK47	SB_DQ20	SB_DQS5	BL7	DDR B DQS5
DDR B D21	BK49	SB_DQ21	SB_DQS6	BE2	DDR B DQS6
DDR B D22	BK43	SB_DQ22	SB_DQS7	AV2	DDR B DQS7
DDR B D23	BK42	SB_DQ23	SB_DQS#0	AU50	DDR B DQS#0
DDR B D24	BJ41	SB_DQ24	SB_DQS#1	BC50	DDR B DQS#1
DDR B D25	BL41	SB_DQ25	SB_DQS#2	BL45	DDR B DQS#2
DDR B D26	BJ37	SB_DQ26	SB_DQS#3	BK38	DDR B DQS#3
DDR B D27	BJ36	SB_DQ27	SB_DQS#4	BK12	DDR B DQS#4
DDR B D28	BK41	SB_DQ28	SB_DQS#5	BK7	DDR B DQS#5
DDR B D29	BJ40	SB_DQ29	SB_DQS#6	BE2	DDR B DQS#6
DDR B D30	BL35	SB_DQ30	SB_DQS#7	AV3	DDR B DQS#7
DDR B D31	BK37	SB_DQ31			
DDR B D32	BK13	SB_DQ32	SB_MA0	BC18	DDR B MA0
DDR B D33	BE11	SB_DQ33	SB_MA1	BG28	DDR B MA1
DDR B D34	BK11	SB_DQ34	SB_MA2	BG25	DDR B MA2
DDR B D35	BC11	SB_DQ35	SB_MA3	AW17	DDR B MA3
DDR B D36	BC13	SB_DQ36	SB_MA4	BF25	DDR B MA4
DDR B D37	BE12	SB_DQ37	SB_MA5	BE25	DDR B MA5
DDR B D38	BC12	SB_DQ38	SB_MA6	BA29	DDR B MA6
DDR B D39	BG12	SB_DQ39	SB_MA7	BC28	DDR B MA7
DDR B D40	BJ10	SB_DQ40	SB_MA8	AY28	DDR B MA8
DDR B D41	BL9	SB_DQ41	SB_MA9	BD37	DDR B MA9
DDR B D42	BK5	SB_DQ42	SB_MA10	BC17	DDR B MA10
DDR B D43	BL5	SB_DQ43	SB_MA11	BE37	DDR B MA11
DDR B D44	BK9	SB_DQ44	SB_MA12	BA39	DDR B MA12
DDR B D45	BK10	SB_DQ45	SB_MA13	BG13	DDR B MA13
DDR B D46	BJ8	SB_DQ46	SB_MA14	BE24	DDR B MA14 <<< >>> DDR_B_MA14 15
DDR B D47	BJ6	SB_DQ47			
DDR B D48	BF4	SB_DQ48	SB_RAS#	AV16	DDR B RAS# >>> DDR_B_RAS# 15
DDR B D49	BH5	SB_DQ49	SB_RCVEN#	AY18	SB_RCVEN# < TP11
DDR B D50	BG1	SB_DQ50			
DDR B D51	BC2	SB_DQ51	SB_WE#	BC17	DDR B WE# >>> DDR_B_WE# 15
DDR B D52	BK3	SB_DQ52			
DDR B D53	BE4	SB_DQ53			
DDR B D54	BD3	SB_DQ54			
DDR B D55	BJ2	SB_DQ55			
DDR B D56	BA3	SB_DQ56			
DDR B D57	BB3	SB_DQ57			
DDR B D58	AR1	SB_DQ58			
DDR B D59	AT3	SB_DQ59			
DDR B D60	AY2	SB_DQ60			
DDR B D61	AY3	SB_DQ61			
DDR B D62	AU2	SB_DQ62			
DDR B D63	AT2	SB_DQ63			

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<Core Design>

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Title			
CRESTLINE(2/6)-DDR2 A/B CH			
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Strap Pin Table

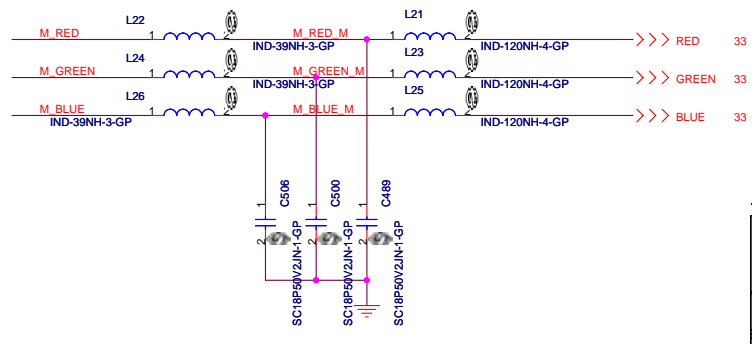
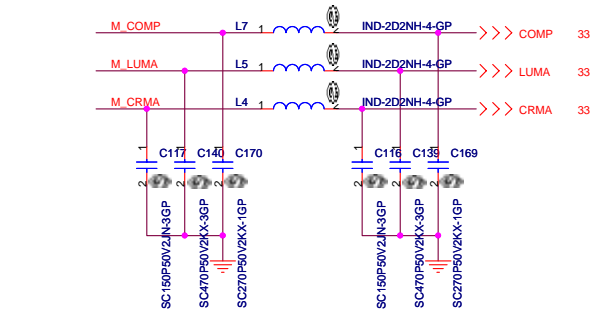
CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation 1 = Reverse lane *
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

PEGCOMP trace width and spacing is 20/25 mils.

CRT Termination/EMI Filter

Place Close Connector

TV-Out Termination/EMI Filter Place Close N/B



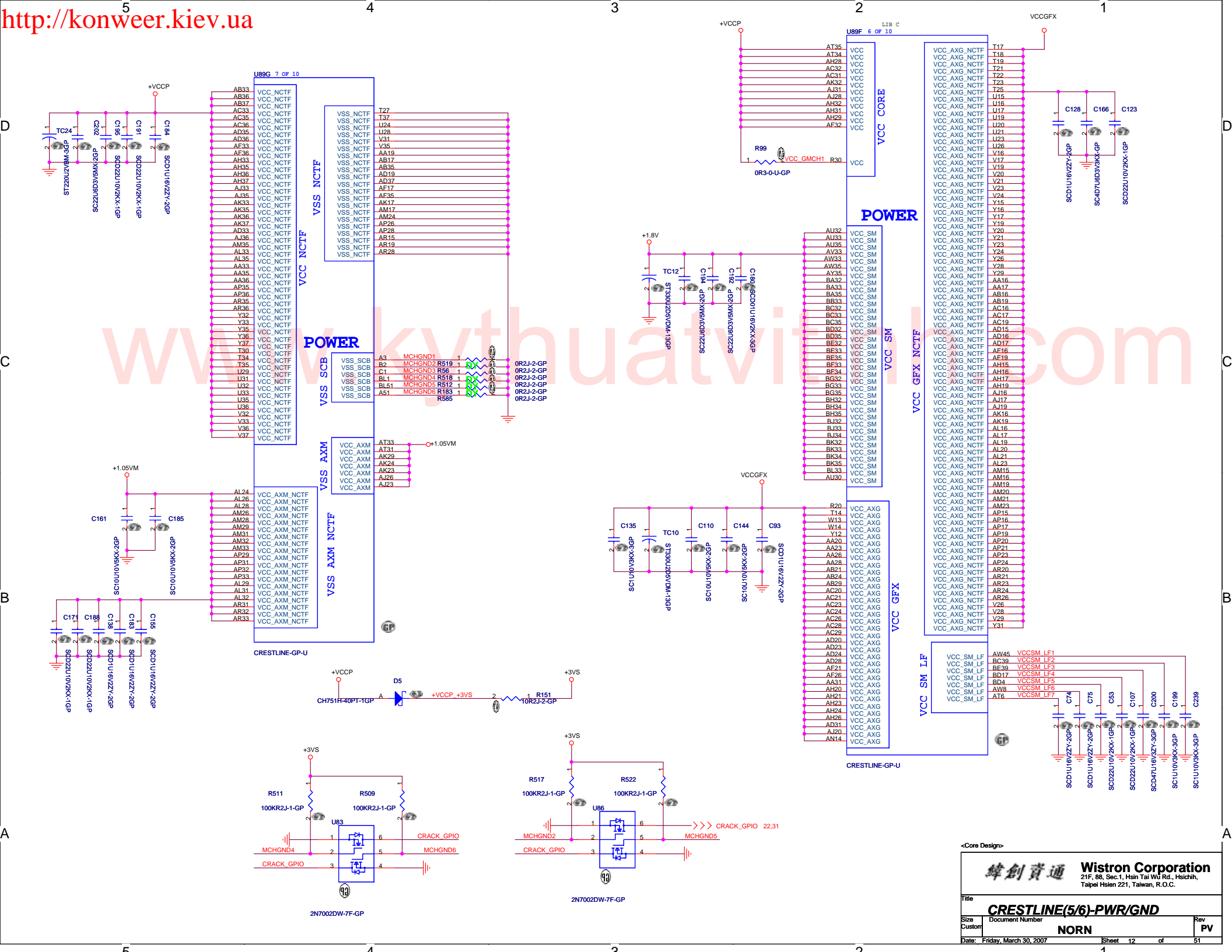
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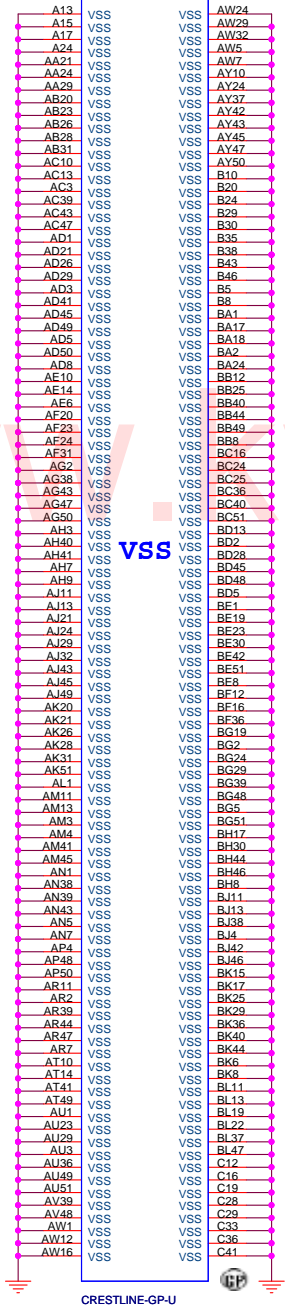
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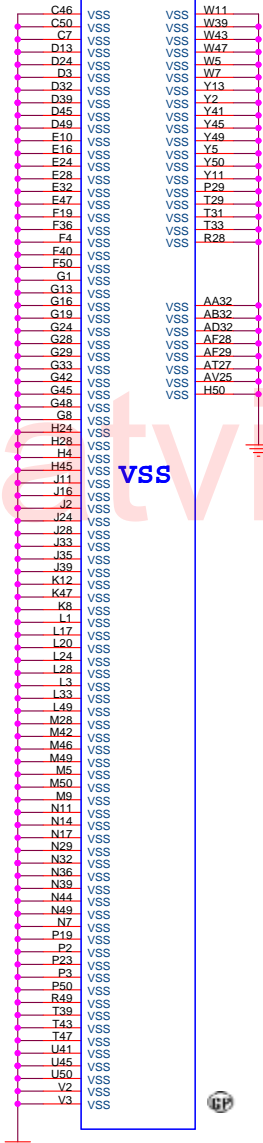


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CRESTLINE-GP-U

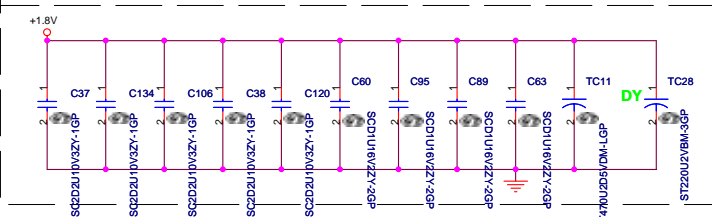
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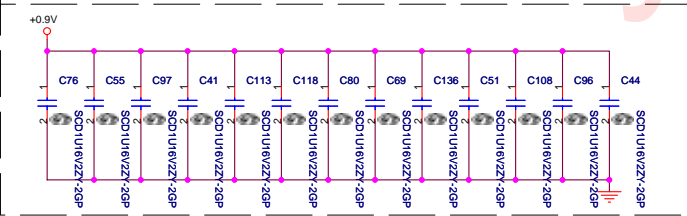
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CRESTLINE(6/6)-PWR/GND			
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- 9 DDR_A_DQS[0..7] <<>>
- 9 DDR_A_DQ[0..63] <<>>
- 9 DDR_A_DM[0..7] <<>>
- 9 DDR_A_DQS[0..7] <<>>
- 9 DDR_A_MA[0..13] <<>>
- 9 DDR_A_BS[0..2] <<>>

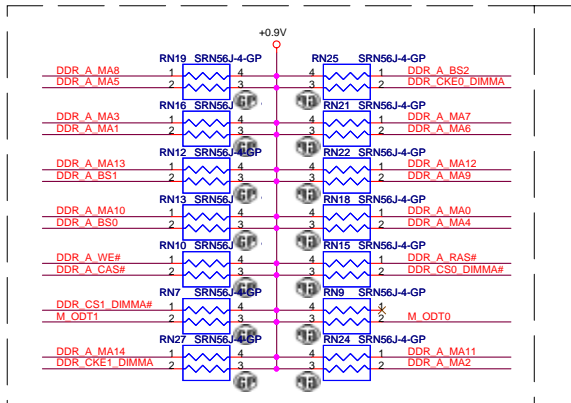
Layout Note:
Place near DM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



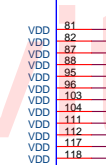
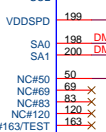
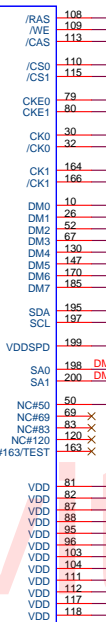
Layout Note:
Place these resistors
closely DM1, all
trace length Max=1.5"



Signal	Pin	Pin	Signal	Pin	Pin
DDR_A MA0	102	A0	DDR_A_RAS#	108	RAM0
DDR_A MA1	101	A1	DDR_A_WE#	109	RAM1
DDR_A MA2	100	A2	DDR_A_CAS#	113	RAM2
DDR_A MA3	99	A3	DDR_CS0_DIMMA#	110	RAM3
DDR_A MA4	98	A4	DDR_CS1_DIMMA#	115	RAM4
DDR_A MA5	97	A5	DDR_CKE0_DIMMA	79	RAM5
DDR_A MA6	96	A6	DDR_CKE1_DIMMA	80	RAM6
DDR_A MA7	95	A7	M_CLK_DDR0	30	RAM7
DDR_A MA8	94	A8	M_CLK_DDR#0	32	RAM8
DDR_A MA9	93	A9	M_CLK_DDR1	164	RAM9
DDR_A MA10	92	A10/AP	M_CLK_DDR#1	166	RAM10
DDR_A MA11	91	A11	DDR_A_DM0	10	RAM11
DDR_A MA12	90	A12	DDR_A_DM1	26	RAM12
DDR_A MA13	89	A13	DDR_A_DM2	52	RAM13
DDR_A MA14	88	A14	DDR_A_DM3	67	RAM14
DDR_A MA14	86	A15	DDR_A_DM4	130	RAM15
DDR_A BS0	85	A16/BA2	DDR_A_DM5	147	RAM16
DDR_A BS1	106	BA0	DDR_A_DM6	170	RAM17
DDR_A D0	107	BA1	DDR_A_DM7	185	RAM18
DDR_A D1	7	DO0	ICH_SMBDATA	195	RAM19
DDR_A D2	7	DO1	ICH_SMBCLK	197	RAM20
DDR_A D3	19	DO2	DM1_SA0	198	RAM21
DDR_A D4	19	DO3	DM1_SA1	200	RAM22
DDR_A D5	4	DO4	DM1_SA1	200	RAM23
DDR_A D6	14	DO5	SA0	50	RAM24
DDR_A D7	14	DO6	SA1	69	RAM25
DDR_A D8	23	DO7	NC#90	83	RAM26
DDR_A D9	23	DO8	NC#91	83	RAM27
DDR_A D10	35	DO9	NC#120	120	RAM28
DDR_A D11	37	DO10	NC#120	120	RAM29
DDR_A D12	20	DO11	NC#163/TEST	163	RAM30
DDR_A D13	22	DO12			
DDR_A D14	36	DO13			
DDR_A D15	38	DO14			
DDR_A D16	43	DO15			
DDR_A D17	45	DO16			
DDR_A D18	55	DO17			
DDR_A D19	57	DO18			
DDR_A D20	44	DO19			
DDR_A D21	46	DO20			
DDR_A D22	56	DO21			
DDR_A D23	58	DO22			
DDR_A D24	61	DO23			
DDR_A D25	63	DO24			
DDR_A D26	73	DO25			
DDR_A D27	75	DO26			
DDR_A D28	62	DO27			
DDR_A D29	64	DO28			
DDR_A D30	74	DO29			
DDR_A D31	76	DO30			
DDR_A D32	123	DO31			
DDR_A D33	125	DO32			
DDR_A D34	135	DO33			
DDR_A D35	137	DO34			
DDR_A D36	124	DO35			
DDR_A D37	126	DO36			
DDR_A D38	134	DO37			
DDR_A D39	136	DO38			
DDR_A D40	141	DO39			
DDR_A D41	143	DO40			
DDR_A D42	141	DO41			
DDR_A D43	153	DO42			
DDR_A D44	140	DO43			
DDR_A D45	142	DO44			
DDR_A D46	152	DO45			
DDR_A D47	154	DO46			
DDR_A D48	157	DO47			
DDR_A D49	159	DO48			
DDR_A D50	173	DO49			
DDR_A D51	175	DO50			
DDR_A D52	168	DO51			
DDR_A D53	169	DO52			
DDR_A D54	174	DO53			
DDR_A D55	176	DO54			
DDR_A D56	179	DO55			
DDR_A D57	181	DO56			
DDR_A D58	189	DO57			
DDR_A D59	191	DO58			
DDR_A D60	180	DO59			
DDR_A D61	192	DO60			
DDR_A D62	192	DO61			
DDR_A D63	194	DO62			
DDR_A D63	194	DO63			
DDR_A DQS#0	11	DO60			
DDR_A DQS#1	29	DO61			
DDR_A DQS#2	49	DO62			
DDR_A DQS#3	68	DO63			
DDR_A DQS#4	129	DO64			
DDR_A DQS#5	146	DO65			
DDR_A DQS#6	167	DO66			
DDR_A DQS#7	186	DO67			
DDR_A DQS0	13	DQS0			
DDR_A DQS1	31	DQS1			
DDR_A DQS2	51	DQS2			
DDR_A DQS3	70	DQS3			
DDR_A DQS4	131	DQS4			
DDR_A DQS5	148	DQS5			
DDR_A DQS6	169	DQS6			
DDR_A DQS7	188	DQS7			
M_ODT0	114	ODT0			
M_ODT1	119	ODT1			
VREF	1	VREF			
GND	201	GND			

DM1

RAM0	108	DDR_A_RAS#
RAM1	109	DDR_A_WE#
RAM2	113	DDR_A_CAS#
RAM3	110	DDR_CS0_DIMMA#
RAM4	115	DDR_CS1_DIMMA#
RAM5	79	DDR_CKE0_DIMMA
RAM6	80	DDR_CKE1_DIMMA
RAM7	30	M_CLK_DDR0
RAM8	32	M_CLK_DDR#0
RAM9	164	M_CLK_DDR1
RAM10	166	M_CLK_DDR#1
RAM11	10	DDR_A_DM0
RAM12	26	DDR_A_DM1
RAM13	52	DDR_A_DM2
RAM14	67	DDR_A_DM3
RAM15	130	DDR_A_DM4
RAM16	147	DDR_A_DM5
RAM17	170	DDR_A_DM6
RAM18	185	DDR_A_DM7
RAM19	195	ICH_SMBDATA
RAM20	197	ICH_SMBCLK
RAM21	198	DM1_SA0
RAM22	200	DM1_SA1
RAM23	50	SA0
RAM24	69	SA1
RAM25	83	NC#90
RAM26	83	NC#91
RAM27	120	NC#120
RAM28	120	NC#120
RAM29	163	NC#163/TEST



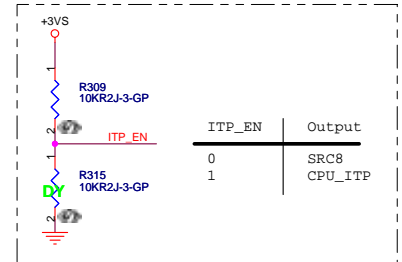
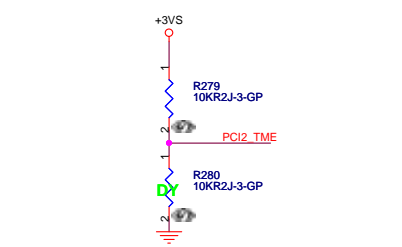
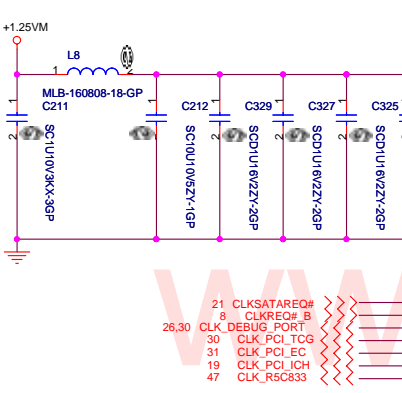
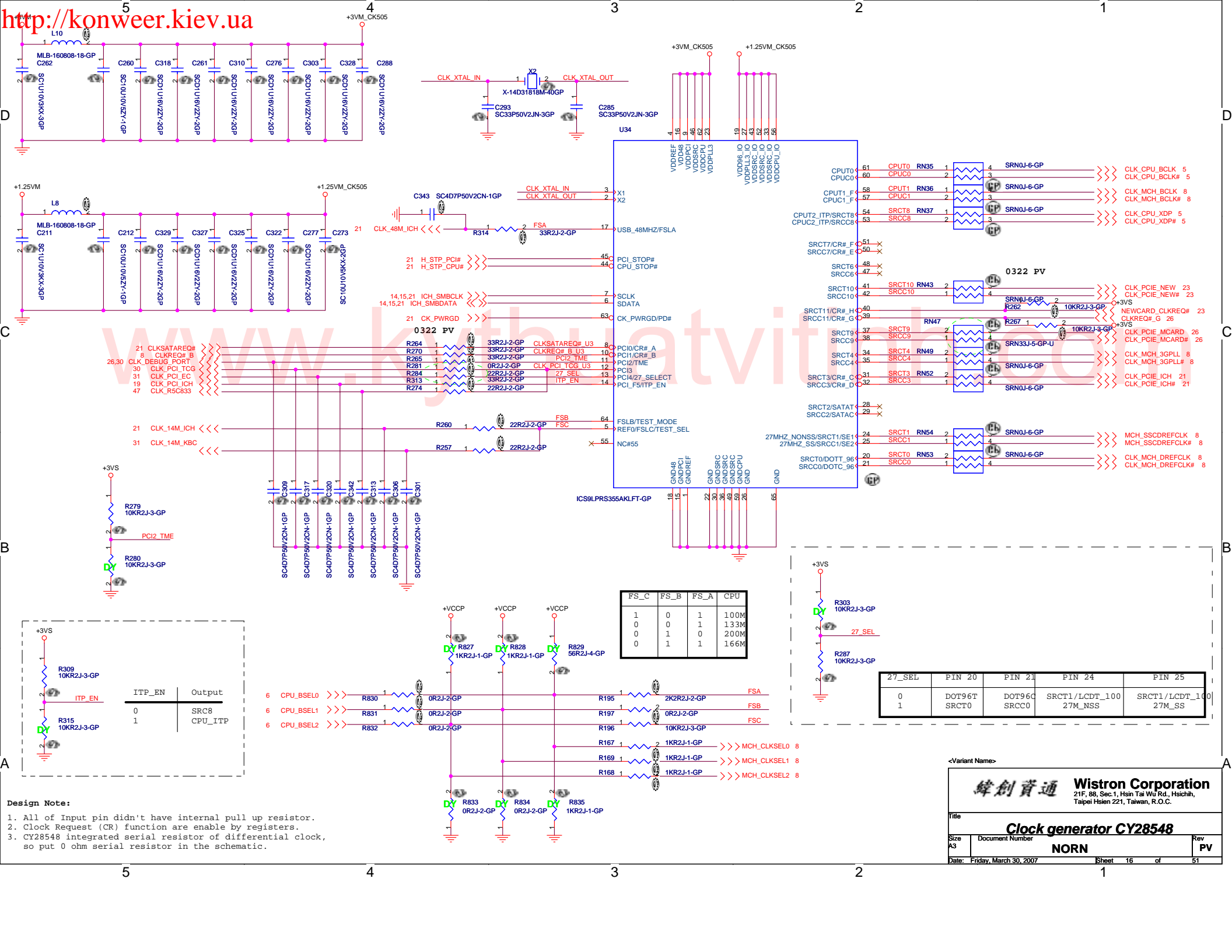
SO-DIMM 1
REVERSE
Foxcon Black
62.10017.E11

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DDRII-SODIMM SLOT1

NORN
PV

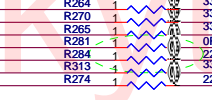
Date: Friday, March 30, 2007



Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

0322 PV



FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T SRCT0	DOT96C SRCC0	SRCT1/LCDDT_100 27M_NSS	SRCT1/LCDDT_100 27M_SS

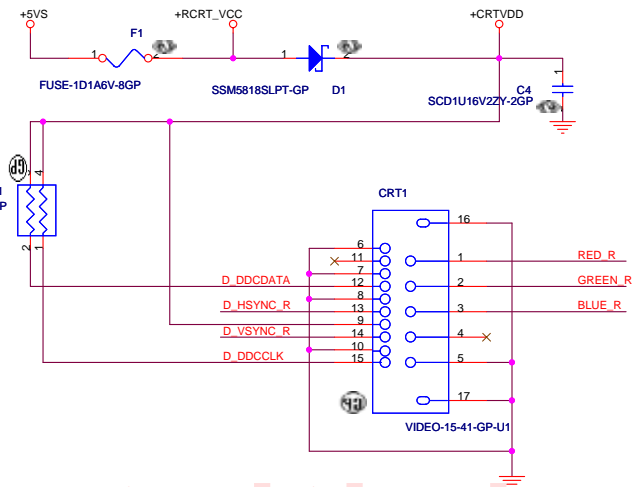
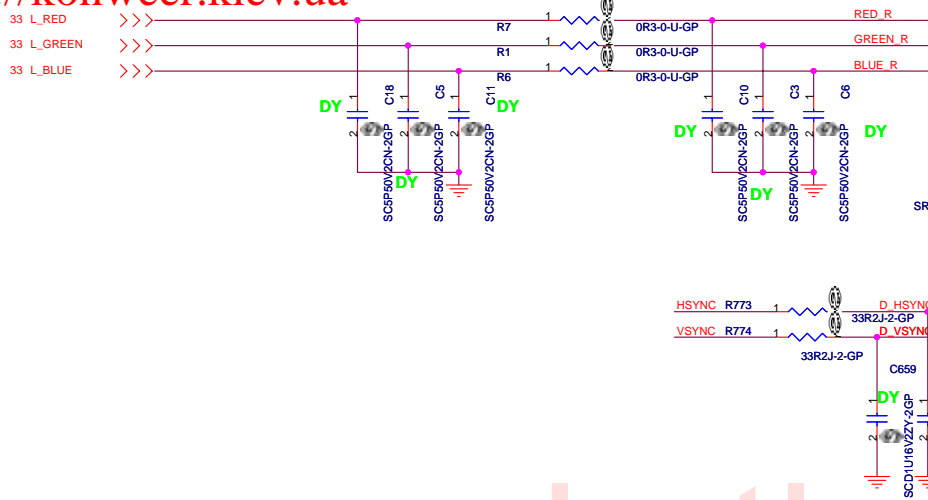
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock generator CY28548**

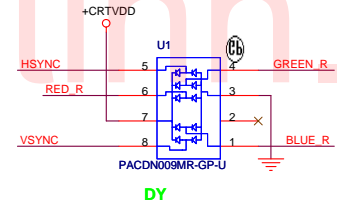
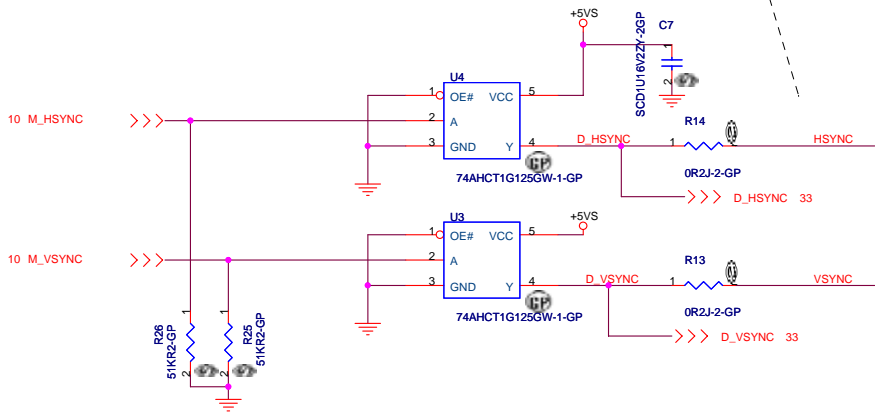
Size A3 Document Number **NORN** Rev **PV**

Date: Friday, March 30, 2007 Sheet 16 of 51

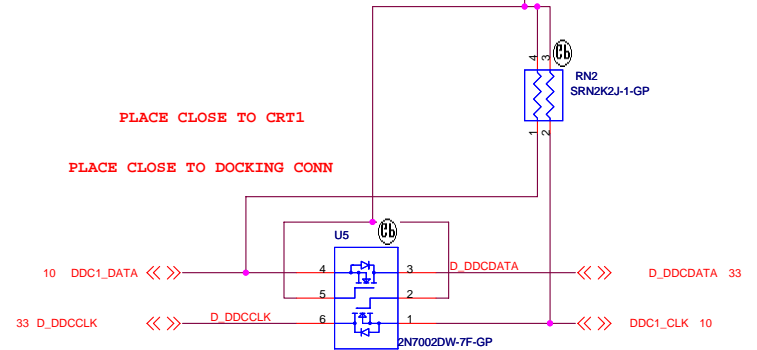


CRT

Layout Note : HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN. , THEN TO SYSTEM CRT CONN.



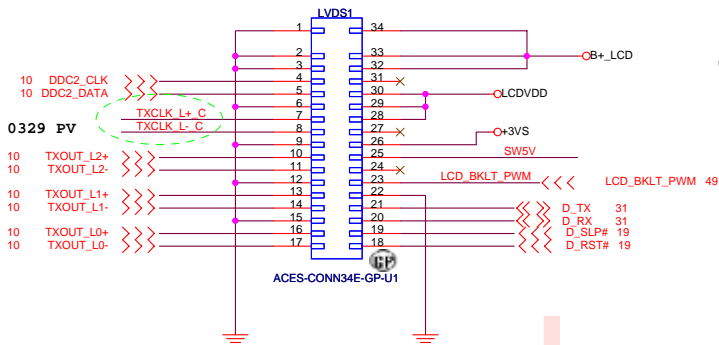
PLACE CLOSE TO CRT1
PLACE CLOSE TO DOCKING CONN



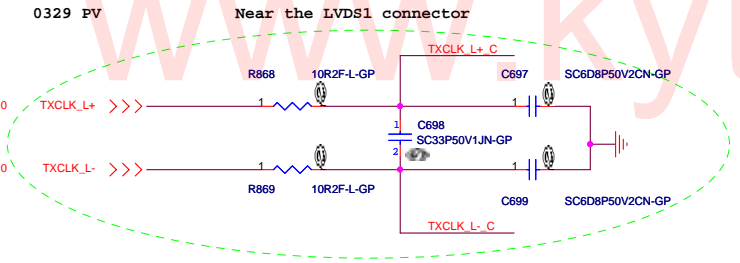
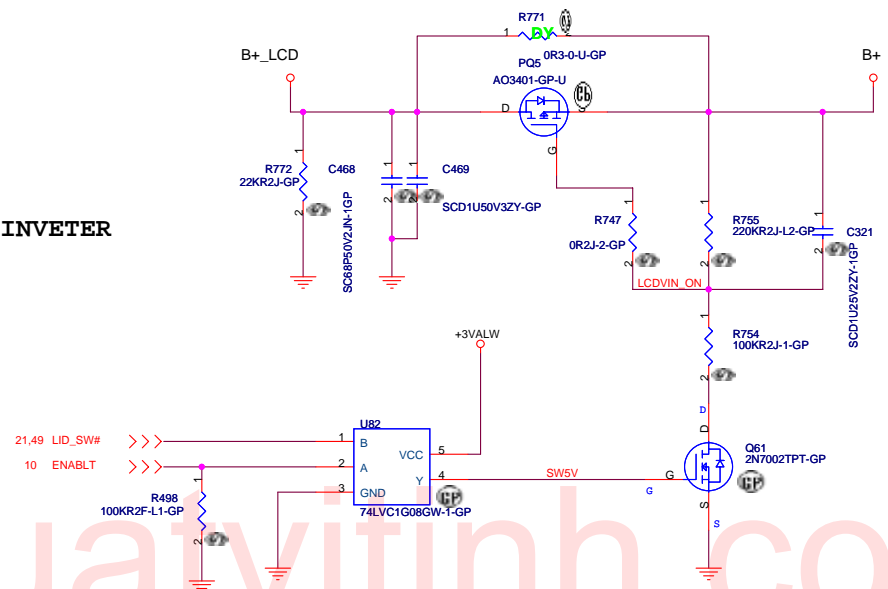
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Taipet Hsien 221, Taiwan, R.O.C.

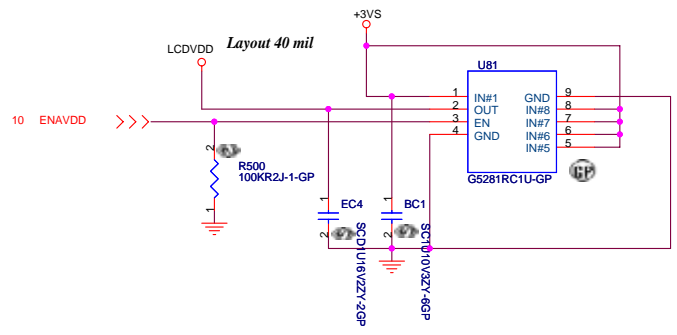
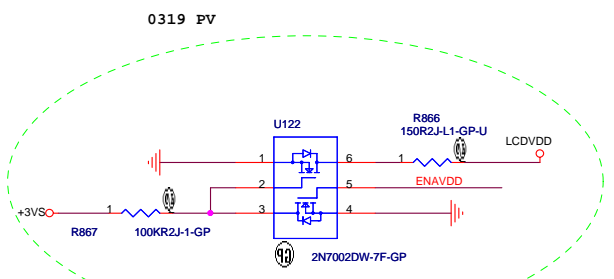
Title			Rev
CRT/TV CONNECTOR			
Size	Document Number	PV	
A3	NORN		
Date:	Friday, March 30, 2007	Sheet	17 of 51



SUPPORT LED INVETER



LCD POWER CIRCUIT



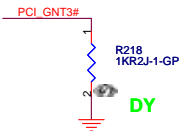
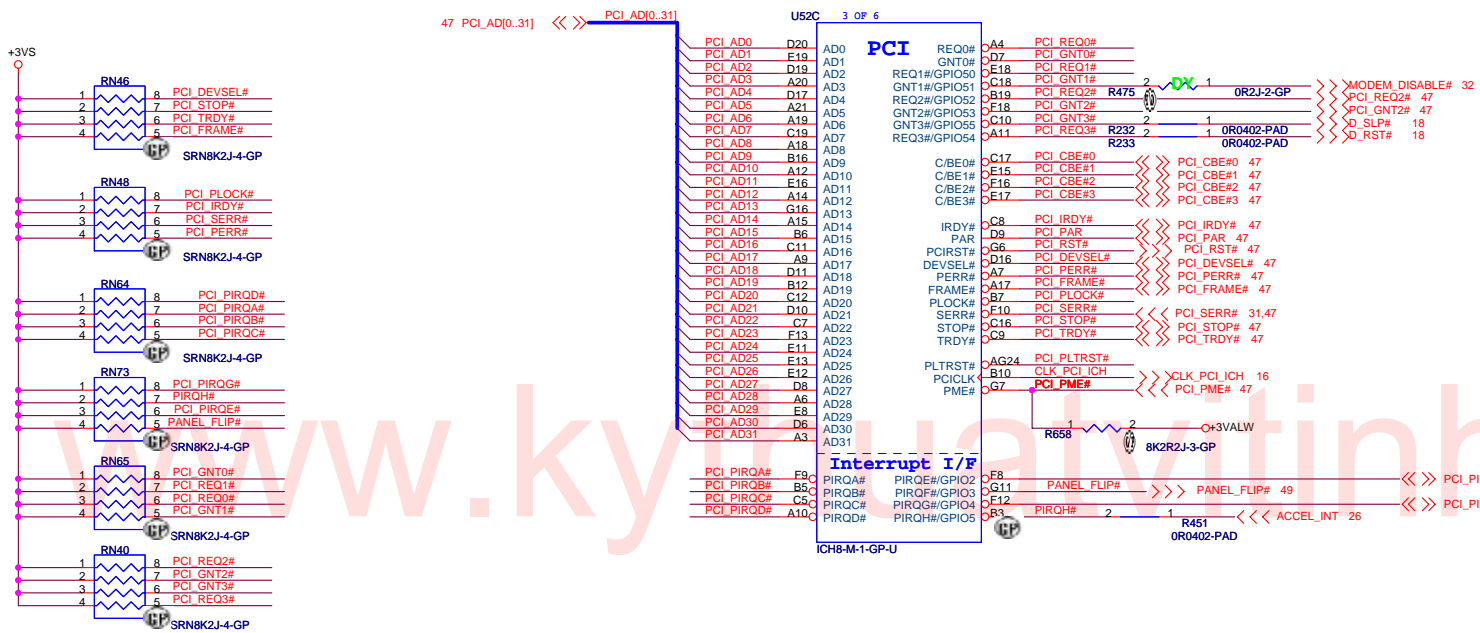
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 Taipei Hsien 221, Taiwan, R.O.C.

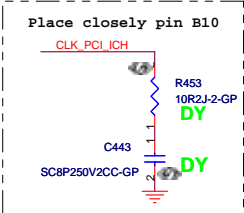
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LCD CONN.

Size A3	Document Number NORN	Rev PV
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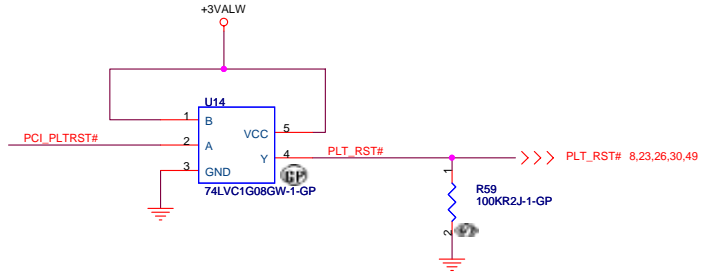
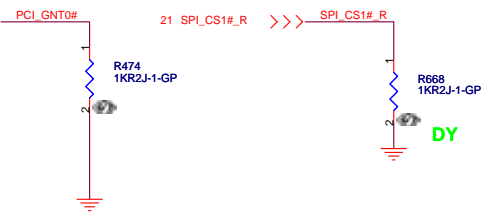
Date: Friday, March 30, 2007 Sheet 18 of 51



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC



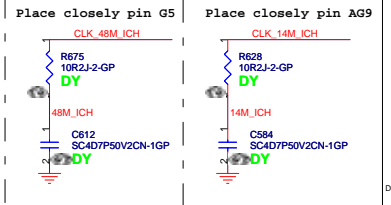
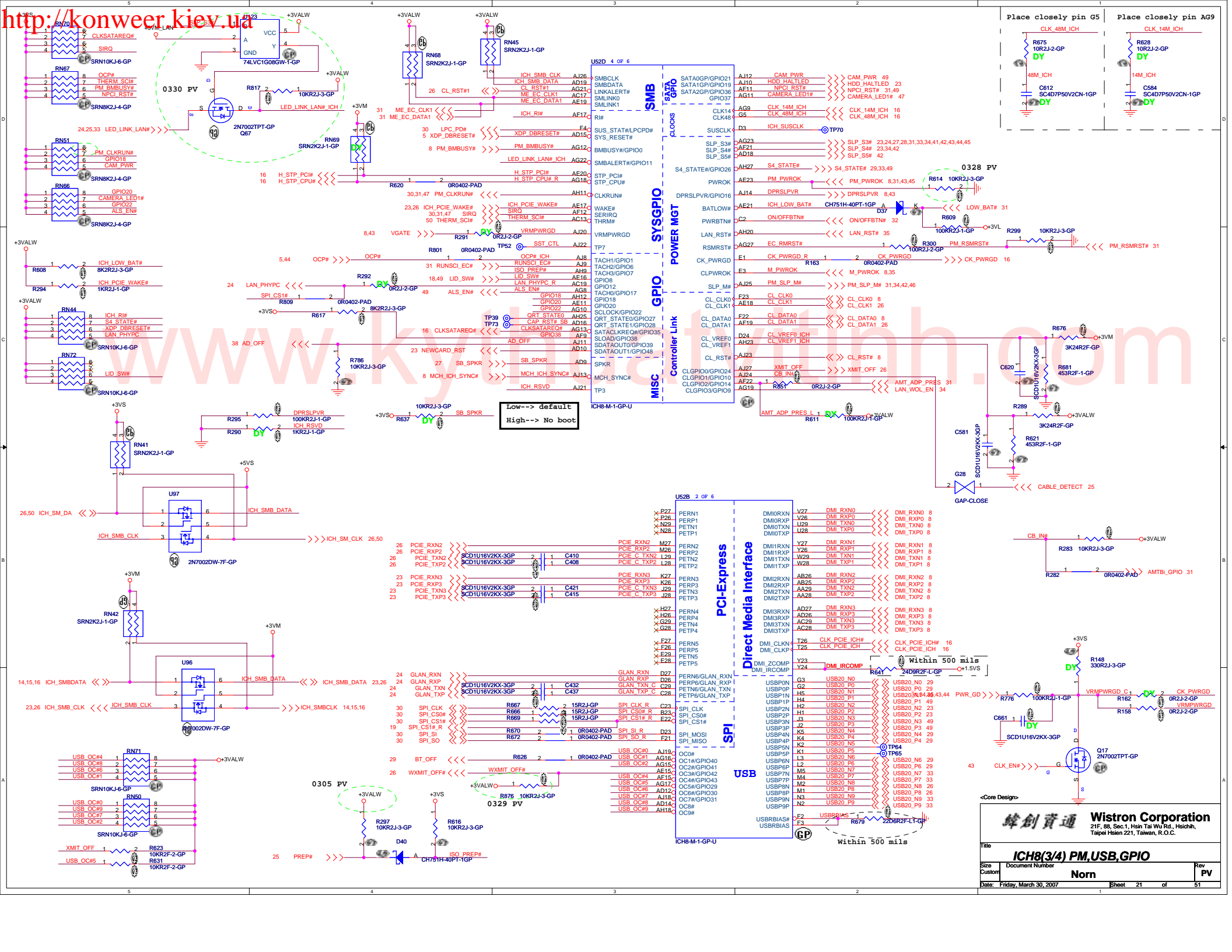
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緯創資通 Wistron Corporation
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Title: **ICH8(1/4)-PCI/INT**

Size: A3 | Document Number: **Norn** | Rev: **PV**

Date: Friday, March 30, 2007 | Sheet: 19 of 51



SMB

SYSGPIO

GPIO

POWER MGT

MISC

Controller Link

USB

PCI-Express

Direct Media Interface

SPI

USB

USB

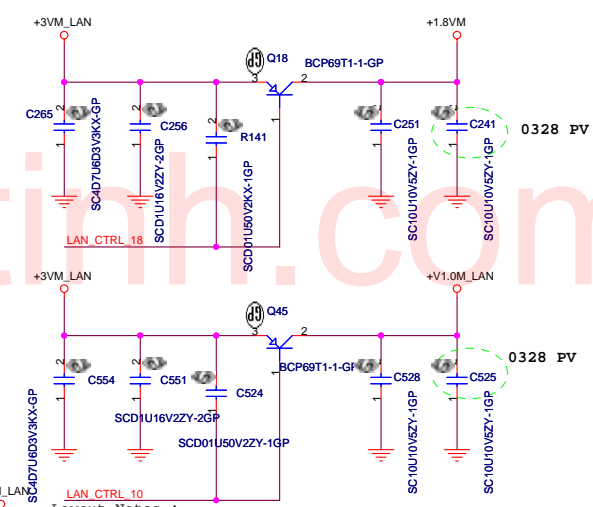
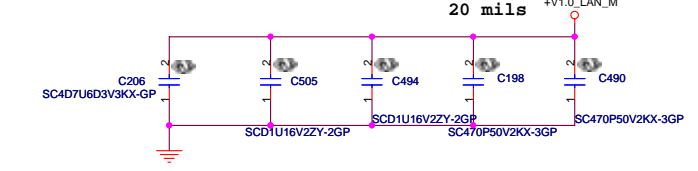
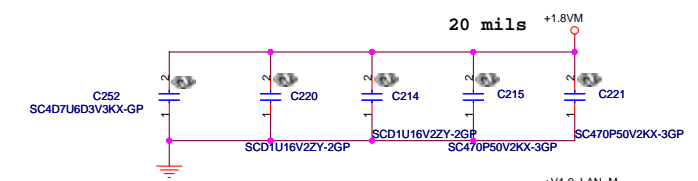
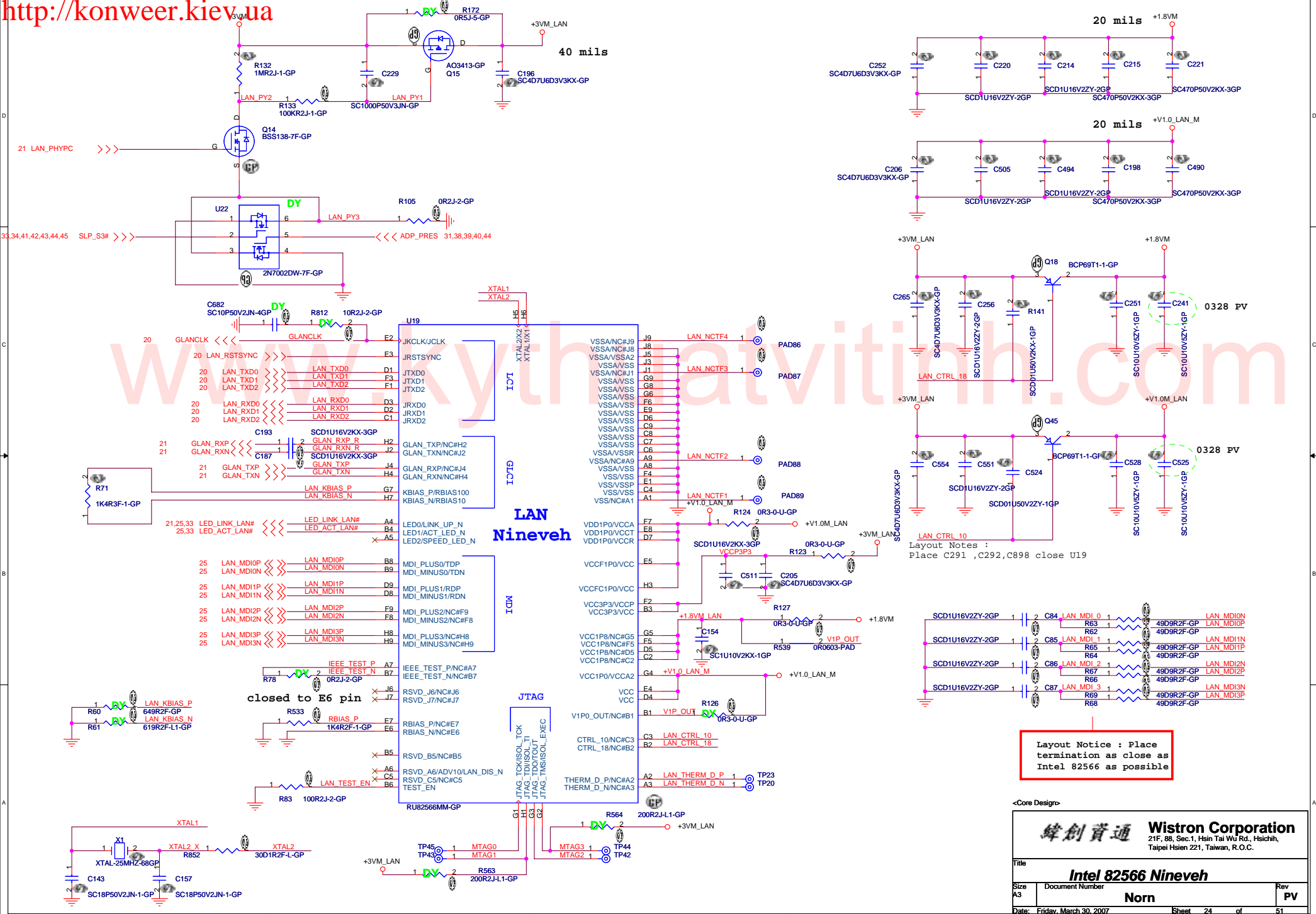
USB

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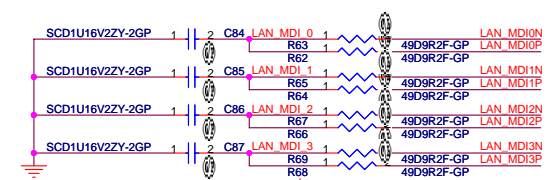
ICH8(3/4) PM,USB,GPIO

Norm
Date: Friday, March 30, 2007

Rev PV
Sheet 21 of 51



Layout Notes :
Place C291 , C292, C898 close U19



Layout Notice : Place termination as close as Intel 82566 as possible

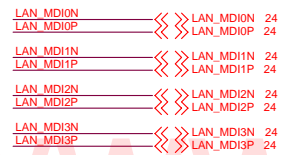
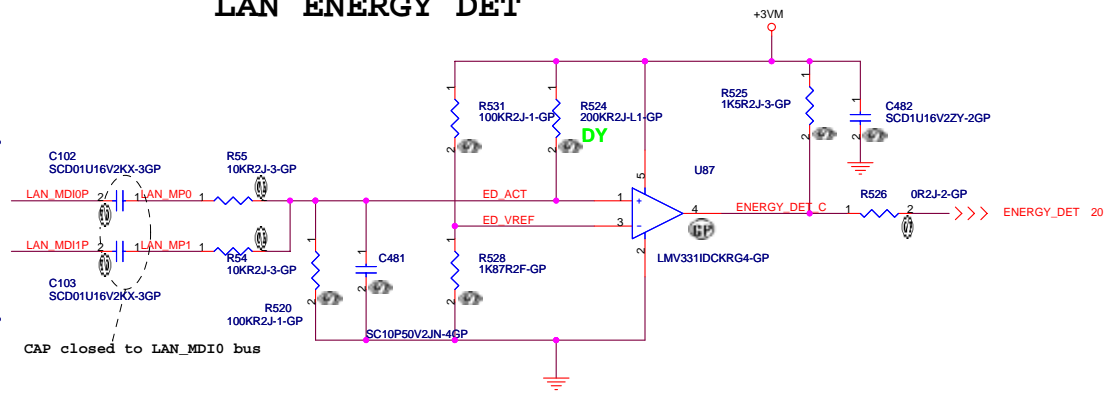
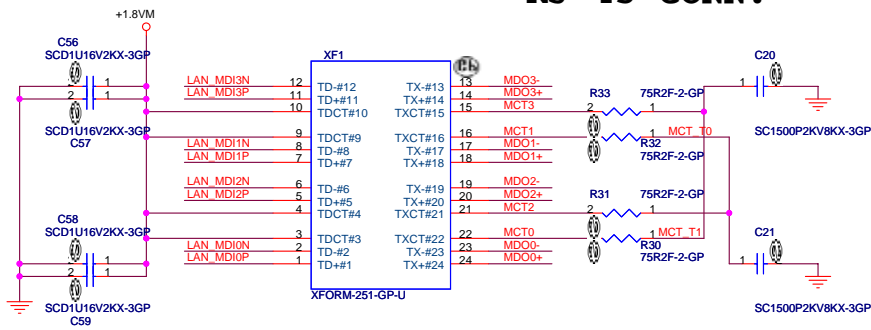
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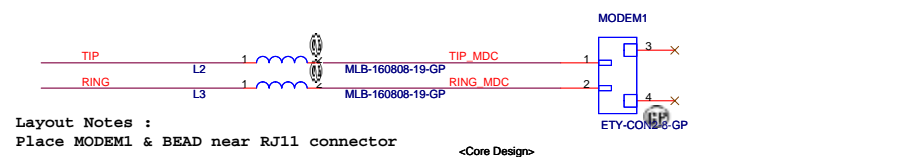
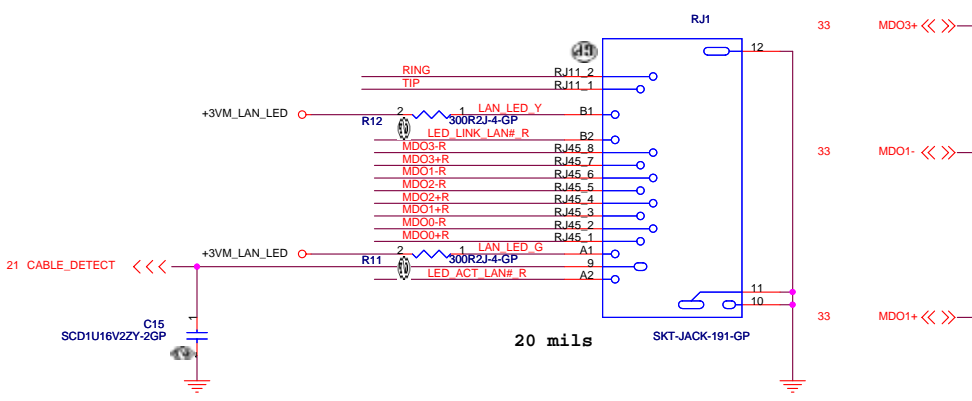
Title	Intel 82566 Nineveh		Rev
Size A3	Document Number	Norn	PV
Date: Friday, March 30, 2007	Sheet	24	of 51

RJ-45 CONN.

LAN ENERGY DET



Note : MDO[3..0]+- signals should route to RJ45 first then to DOCK CONN .



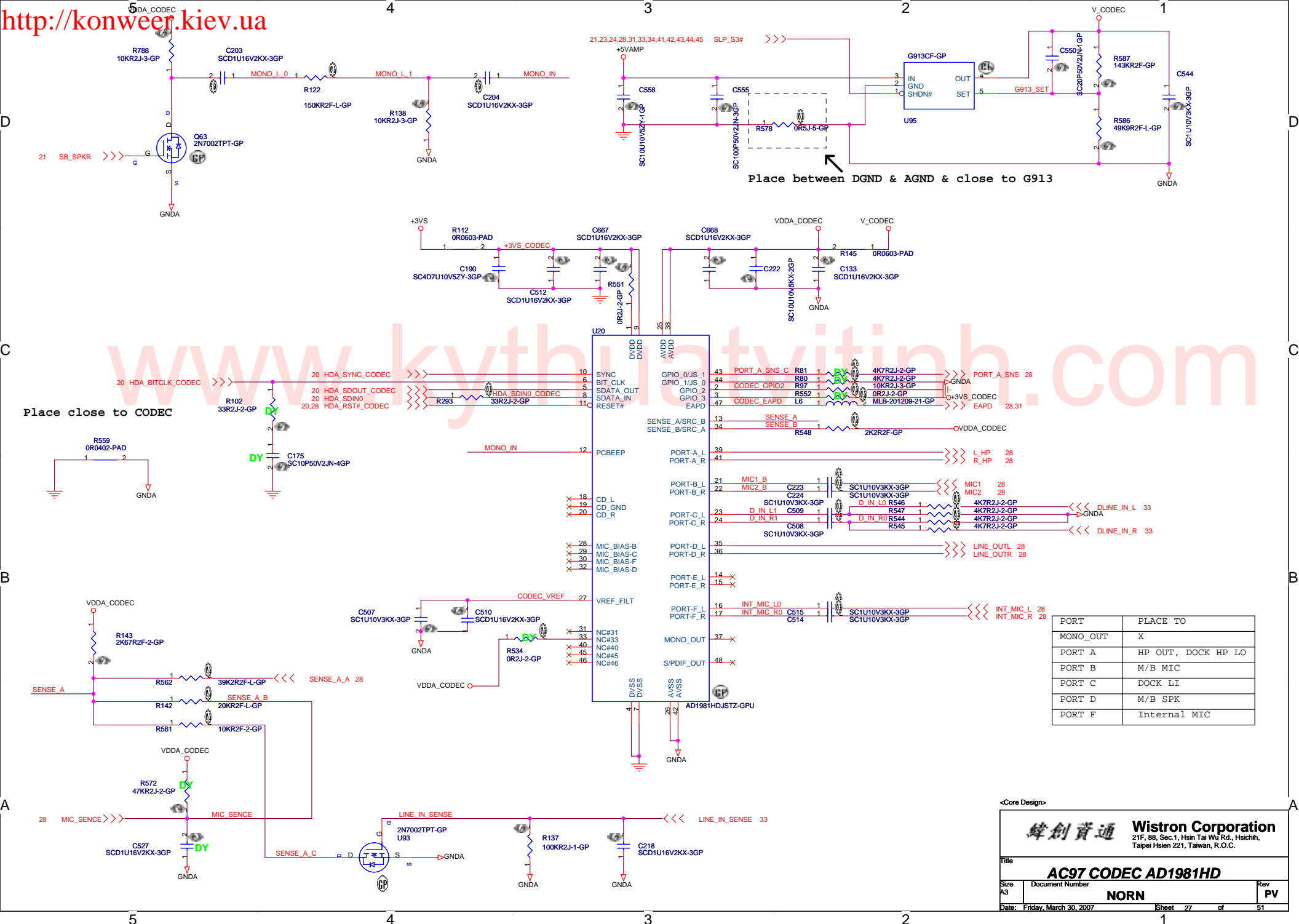
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Magnetic & RJ45/RJ11**

Size: A3 | Document Number: **Norn** | Rev: **PV**

Date: Friday, March 30, 2007 | Sheet: 25 of 51



<Core Design>

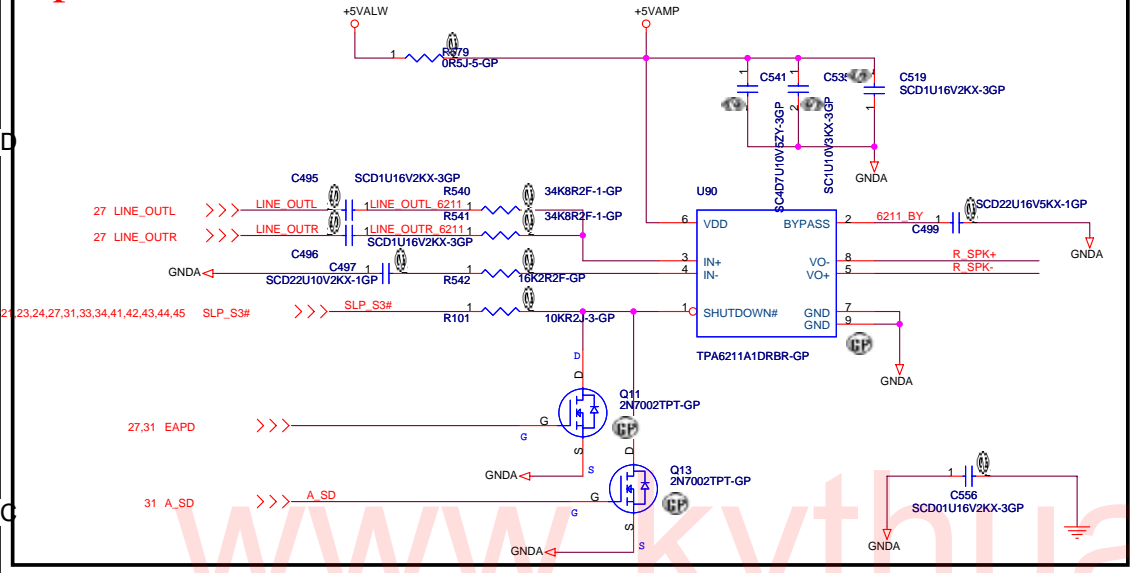
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21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.

Title: **AC97 CODEC AD1981HD**

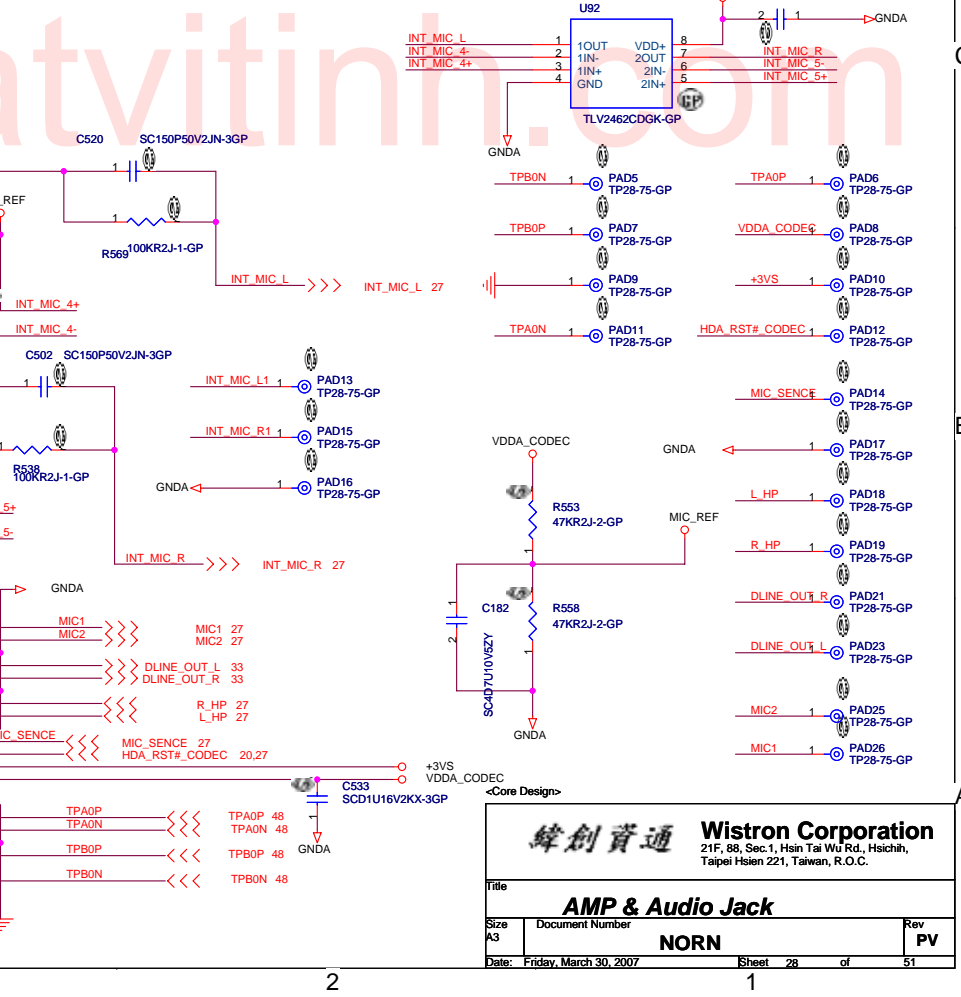
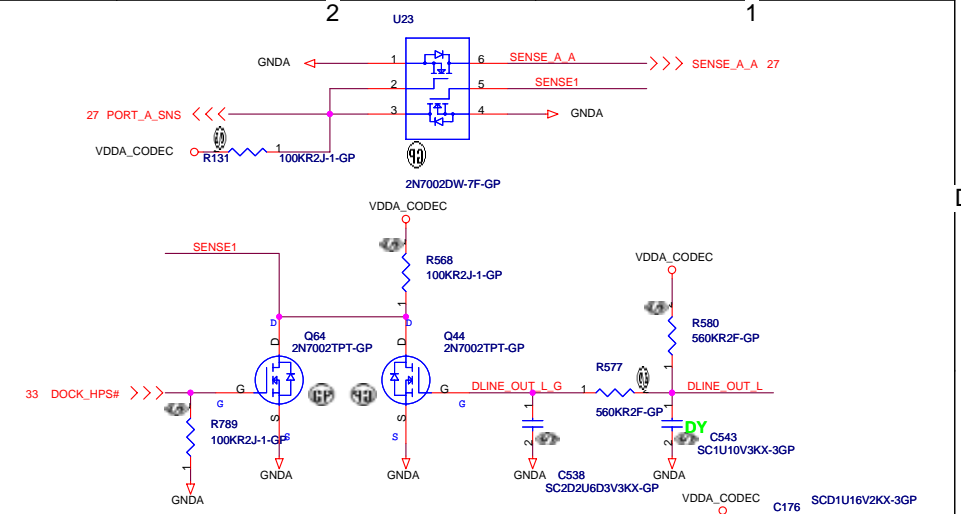
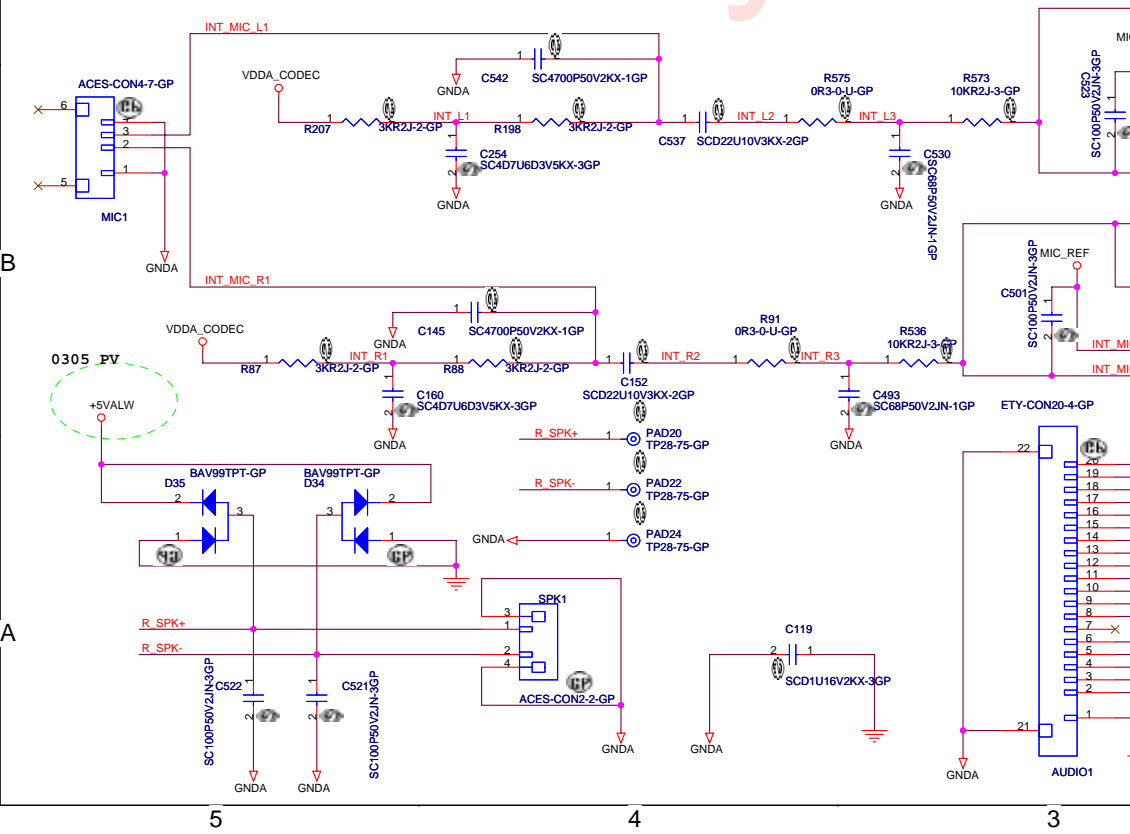
Size A3	Document Number	Rev PV
NORN		

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AMP. FOR INTERNAL SPEAKER



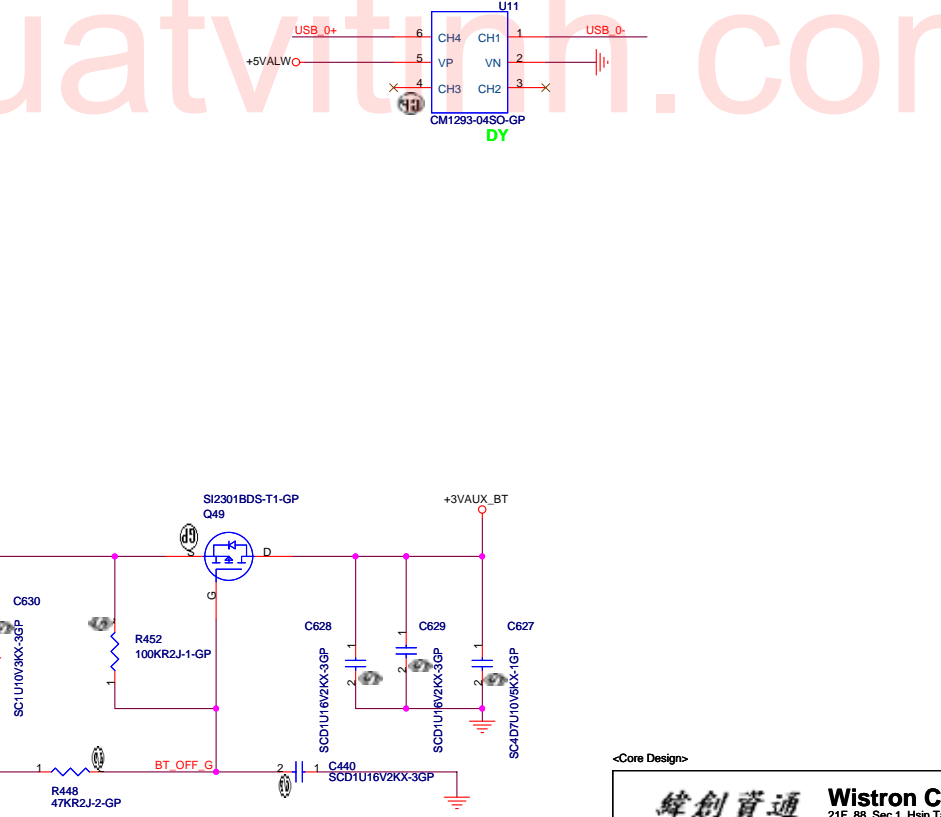
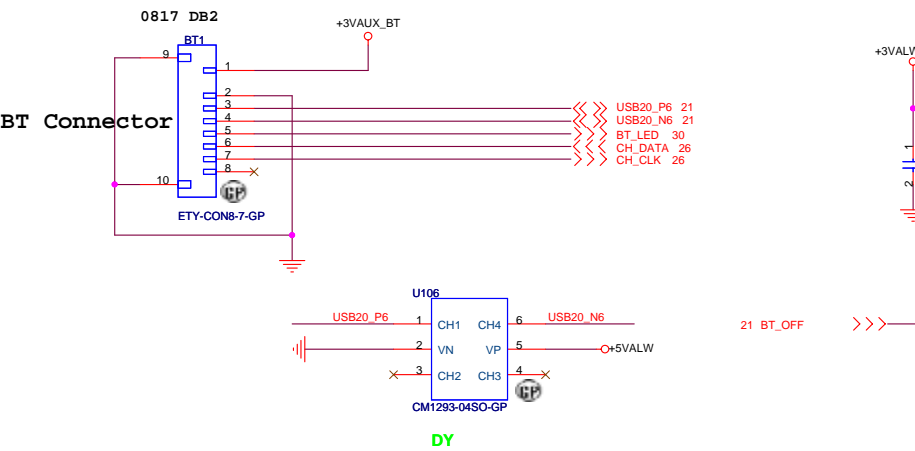
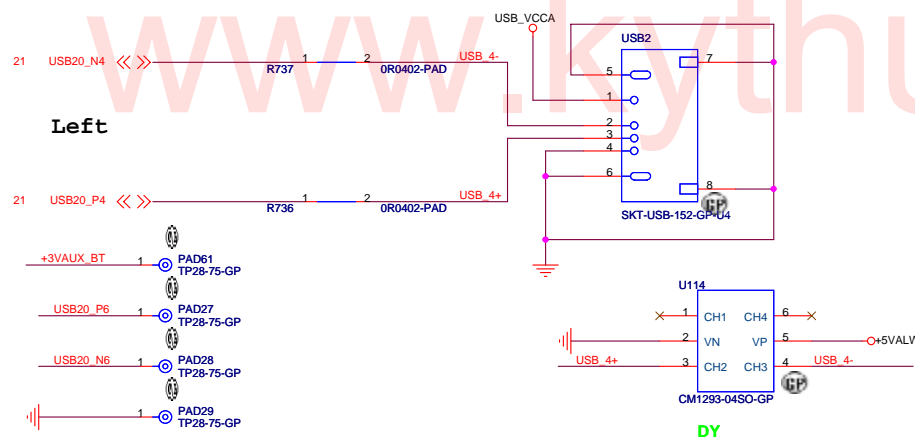
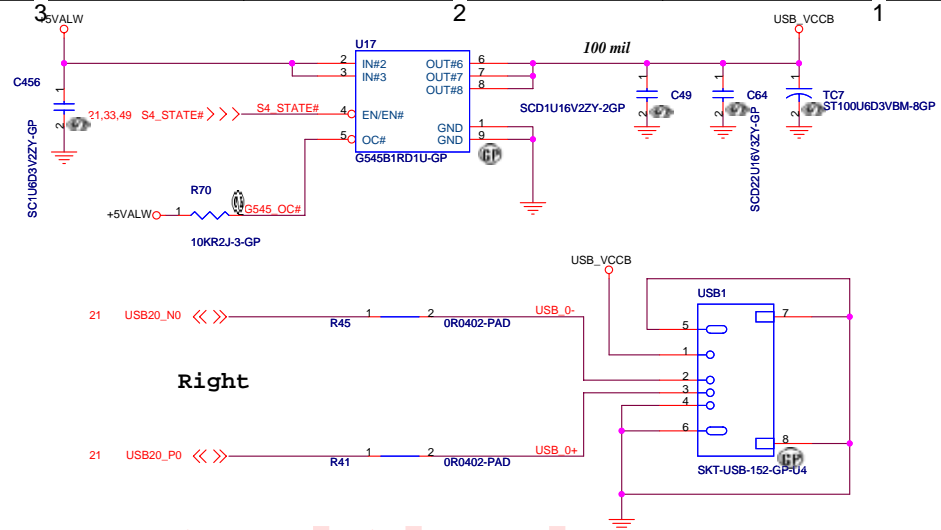
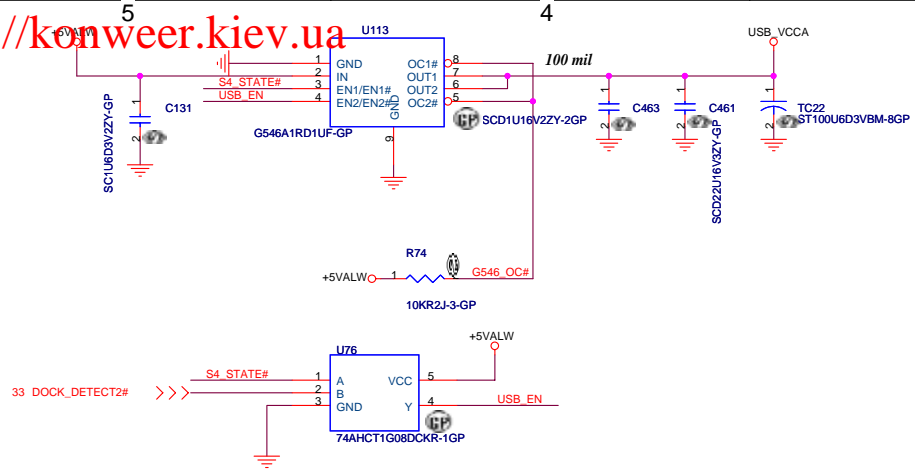
AMP. FOR INTERNAL ARRAY MICROPHONE



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AMP & Audio Jack

Title		Rev	
Size A3	Document Number	PV	
NORN			
Date: Friday, March 30, 2007	Sheet 28	of 51	



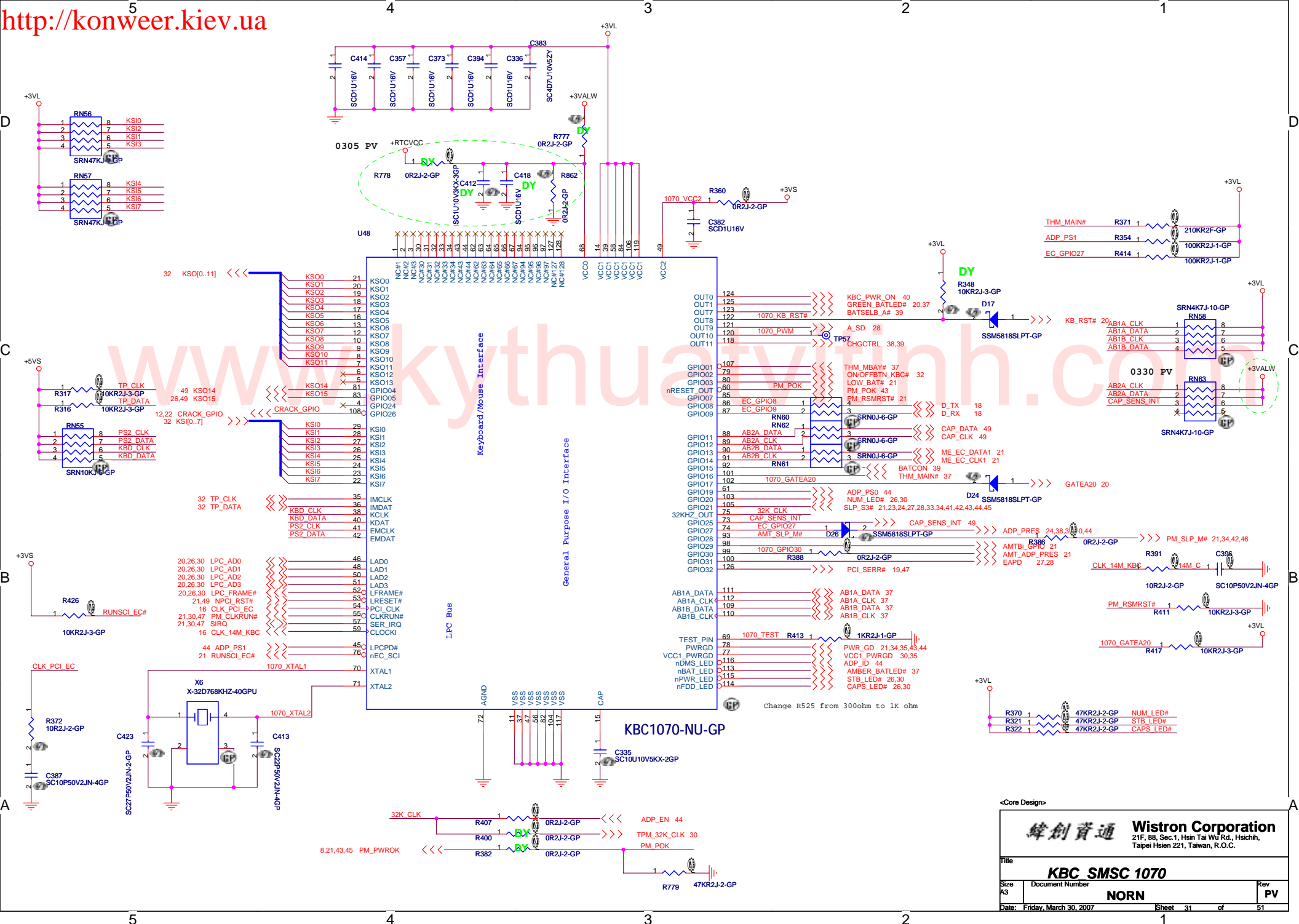
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB&1394 & BT Connector**

Size A3 Document Number **NORN** Rev **PV**

Date: Friday, March 30, 2007 Sheet 29 of 51



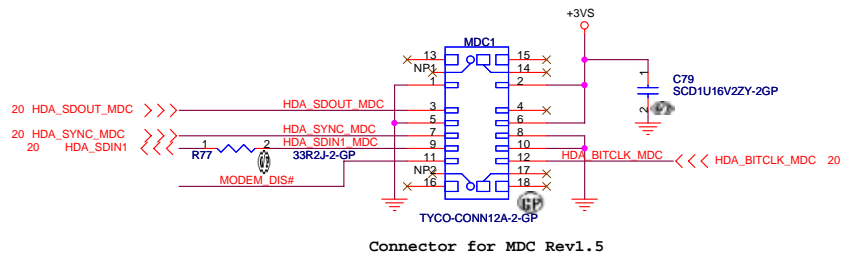
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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsin 221, Taiwan, R.O.C.

Title: **KBC SMC 1070**

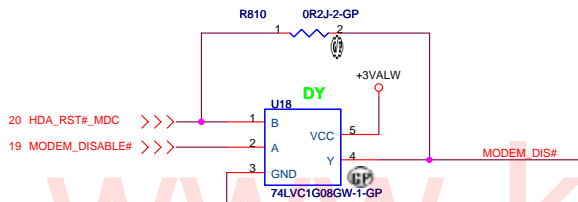
Size A3	Document Number	Rev
	NORN	PV

Date: Friday, March 30, 2007 Sheet 31 of 51

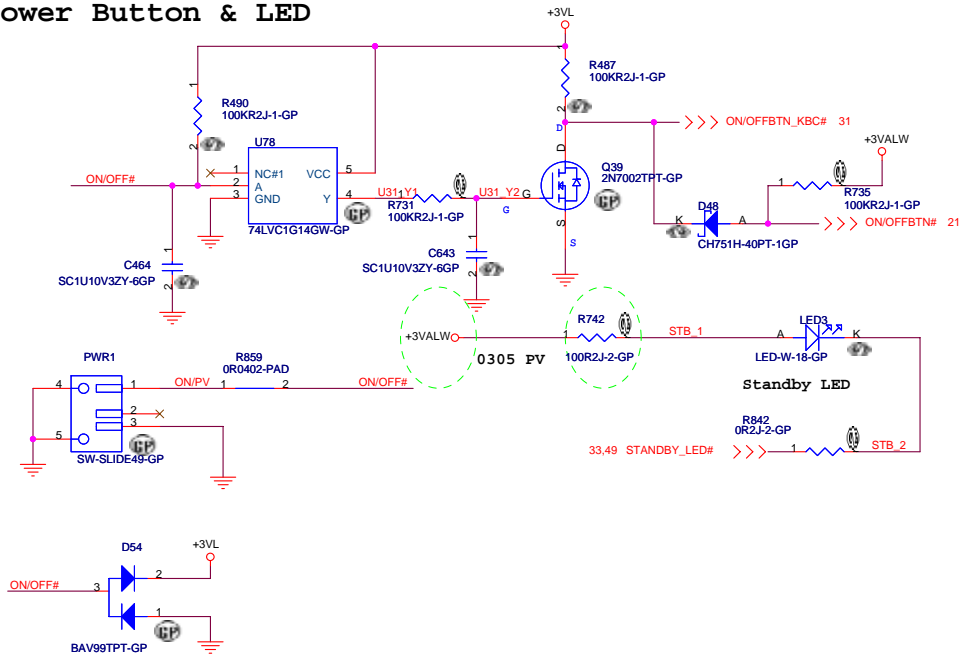
MDC 1.5 Conn.



Connector for MDC Rev1.5

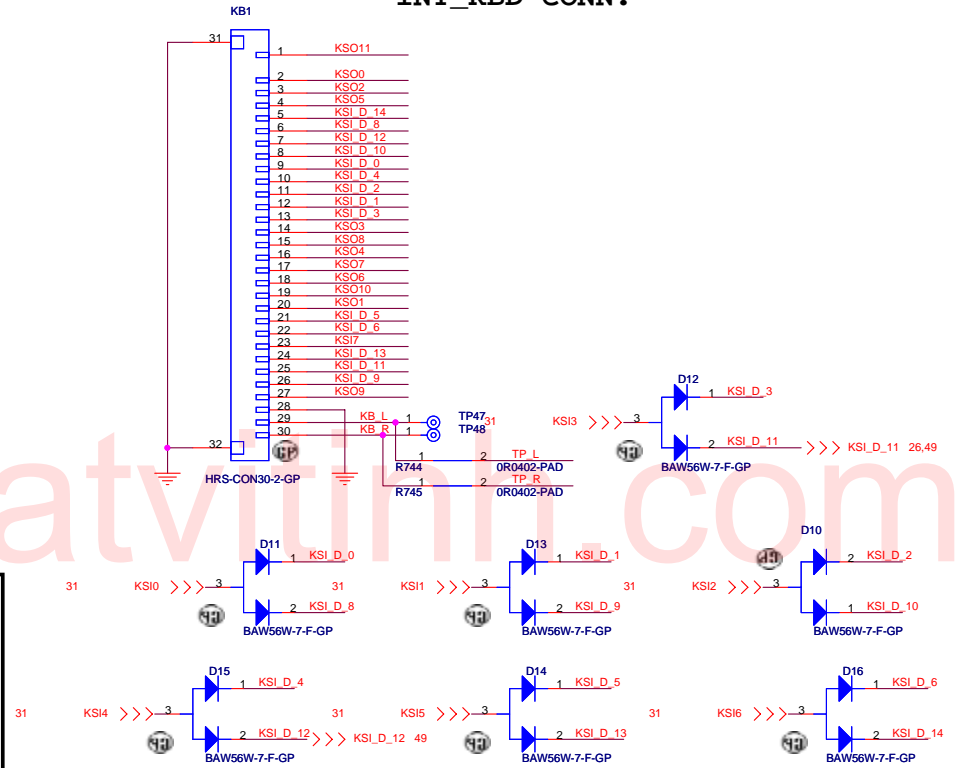


Power Button & LED

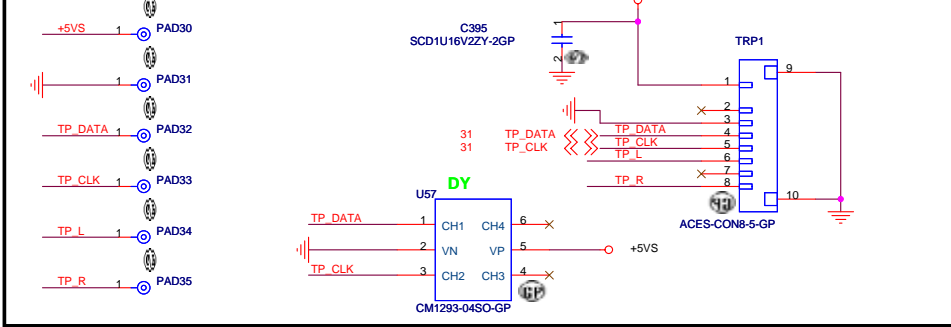


31 KSO[0..11] <<< KSO[0..11]
31 KSI[0..7] <<< KSI[0..7]

INT_KBD CONN.



TrackPoint CONN.



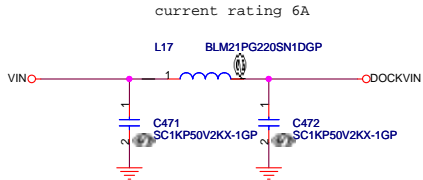
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: MDC/KBD/ON OFF/T.P.

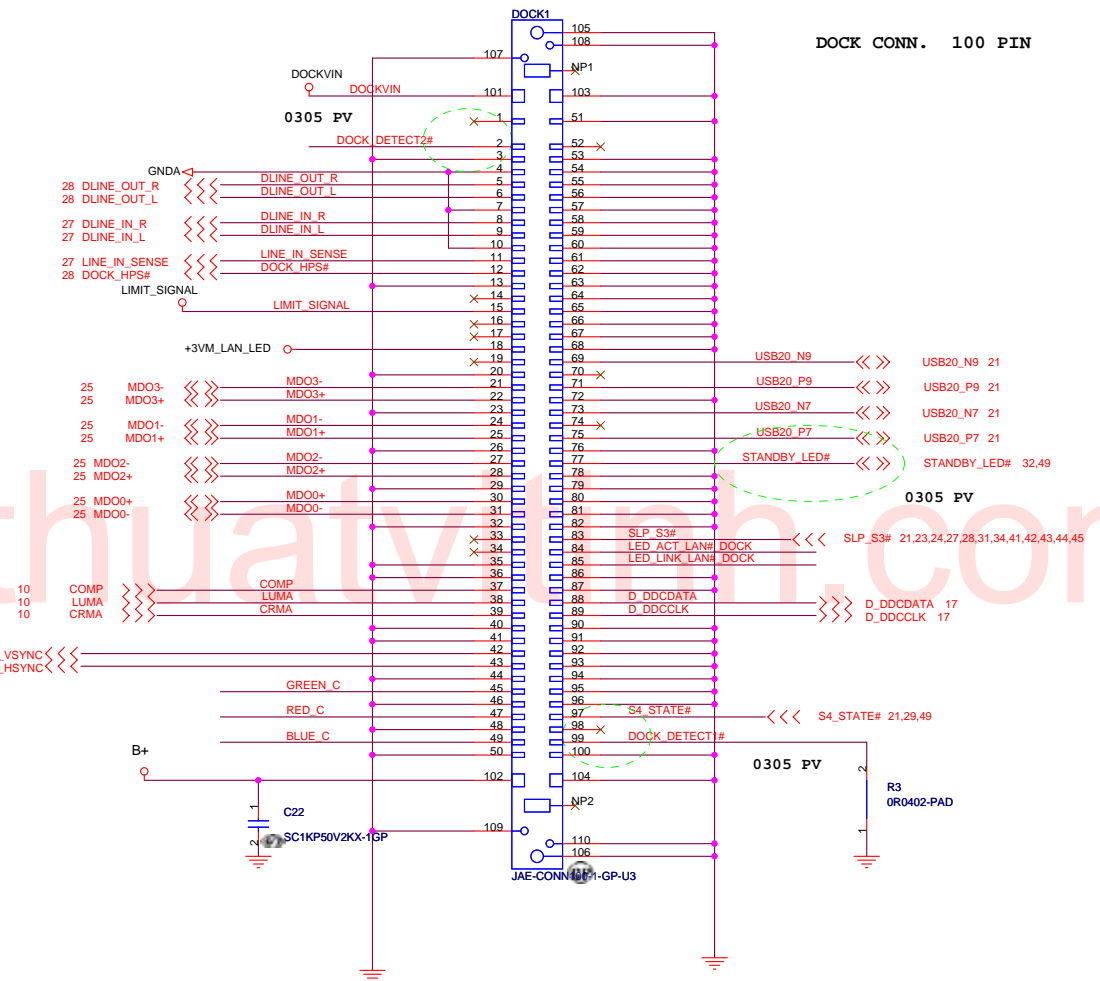
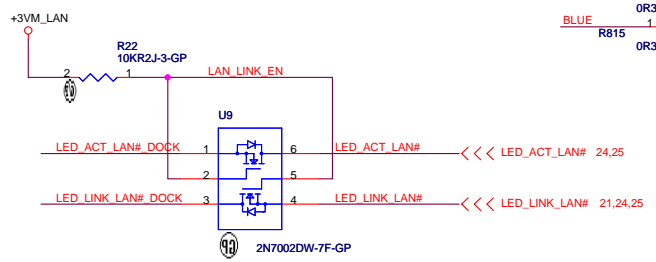
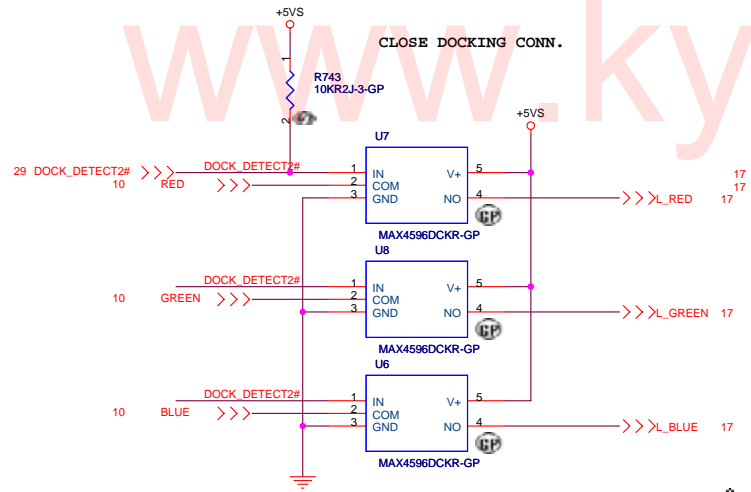
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Date: Friday, March 30, 2007 Sheet: 32 of 51

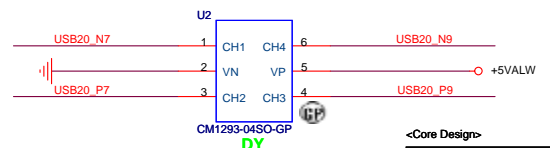


MAX4596

IN	NO TO COM COM TO NO
L	OFF
H	ON



Power Pins
 2 sets
 Set 1 = 18.5V @ 4A per contact
 Set 2 = VBATR @ 3A per contact



<Core Design>

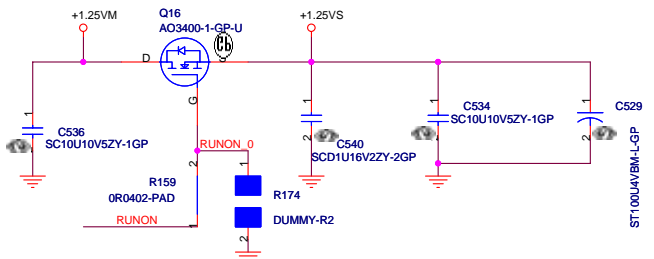
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Docking CONN**

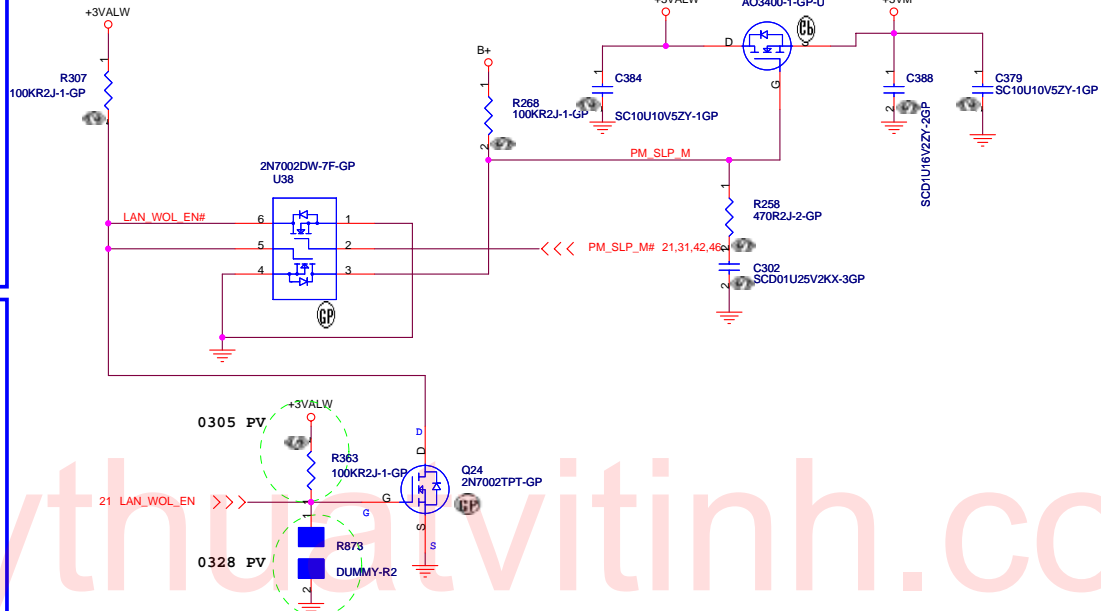
Size A3 Document Number: **Norn** Rev: **PV**

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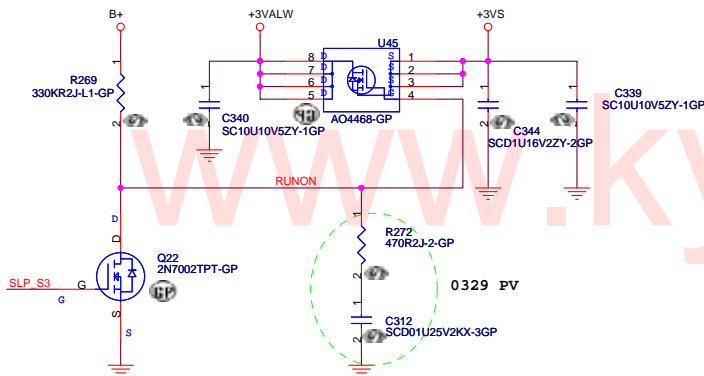
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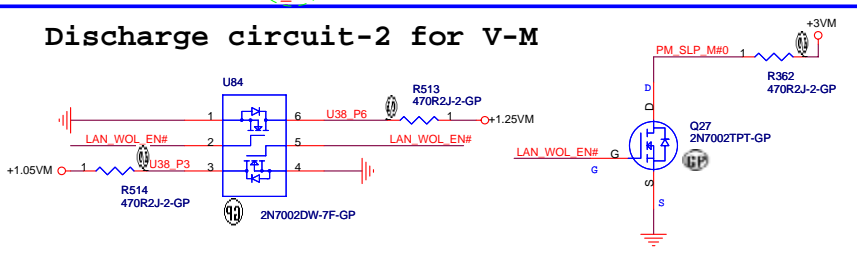
+3VALW to +3VM Transfer



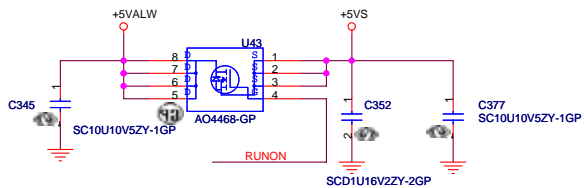
+3VALW to +3VS Transfer



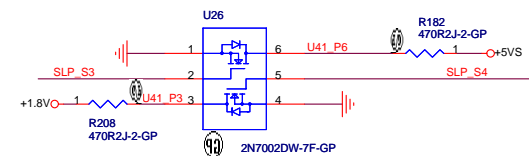
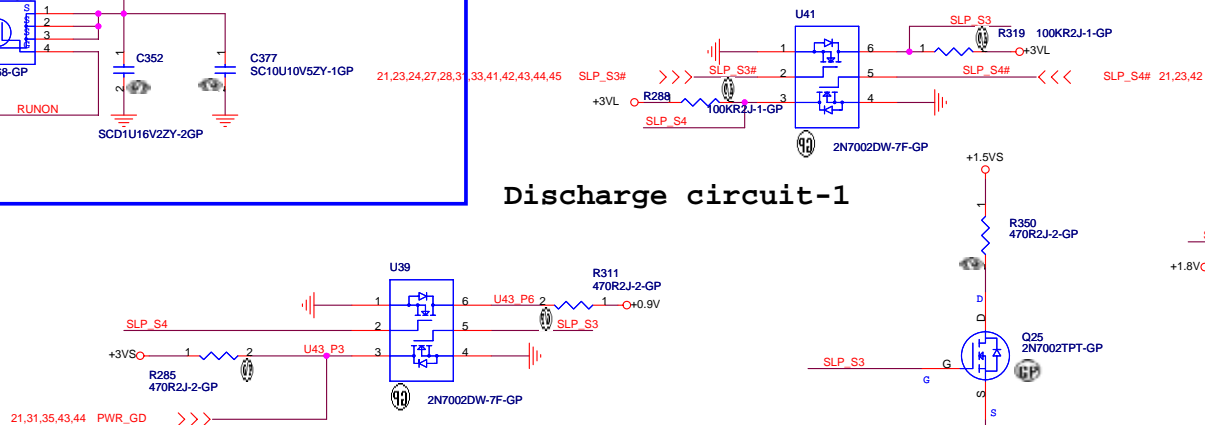
Discharge circuit-2 for V-M



+5VALW to +5VS Transfer



Discharge circuit-1

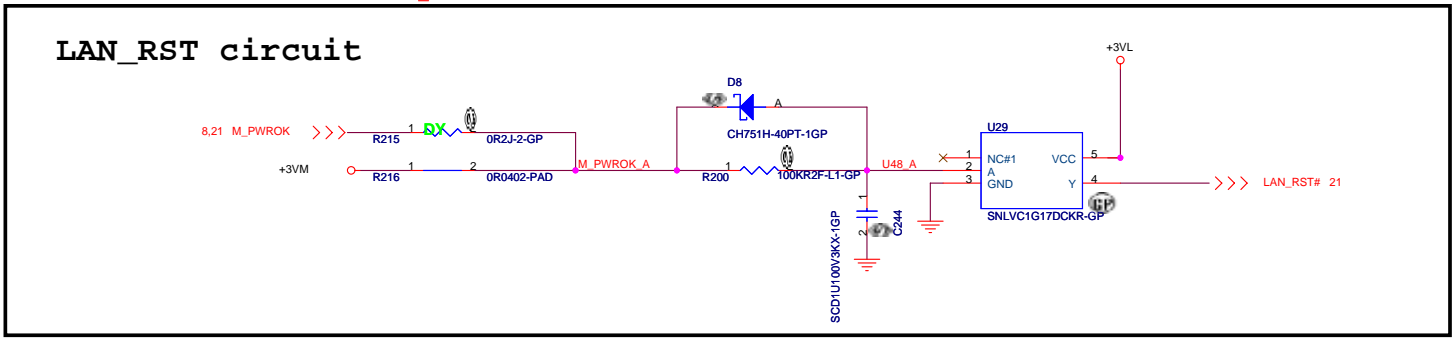
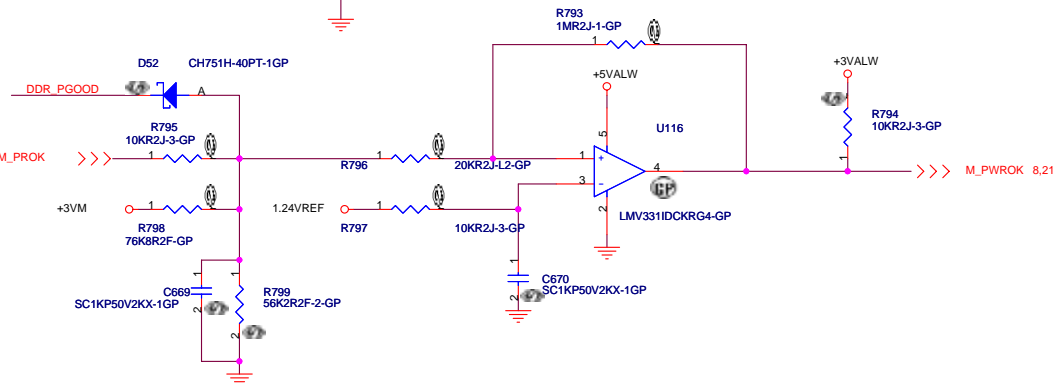
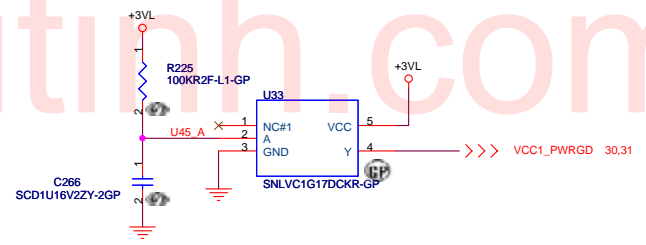
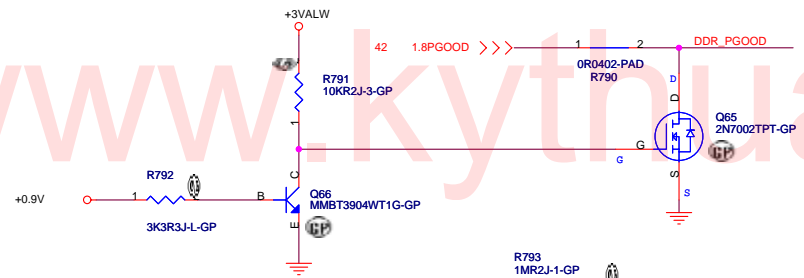
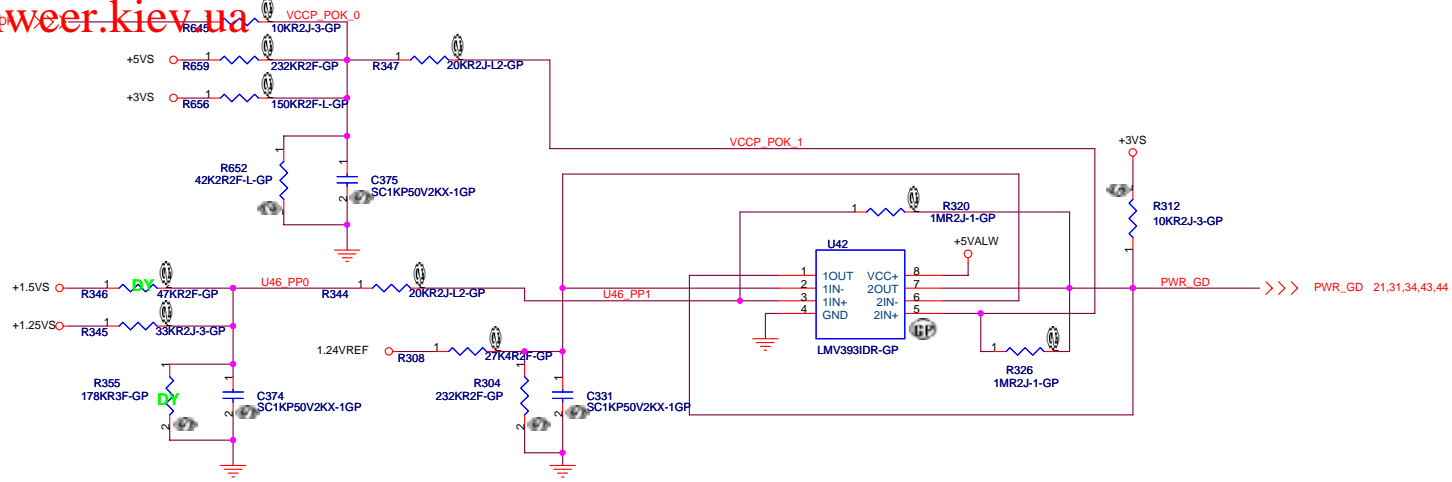


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File: **DC/DC Circuit**

Size: A3 | Document Number: **NORN** | Rev: **PV**

Date: Friday, March 30, 2007 | Sheet: 34 of 51



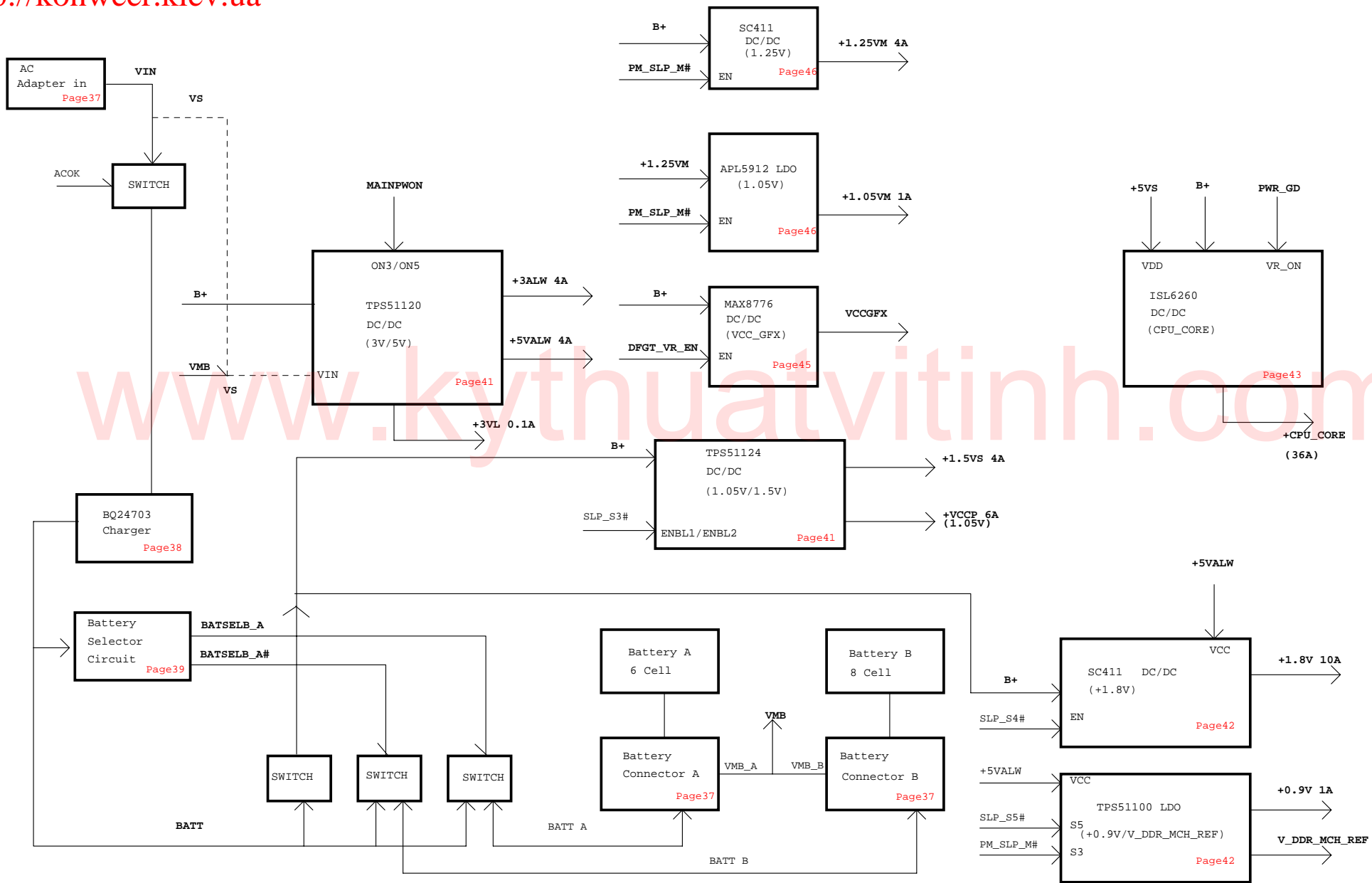
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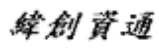
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **POK CKT**

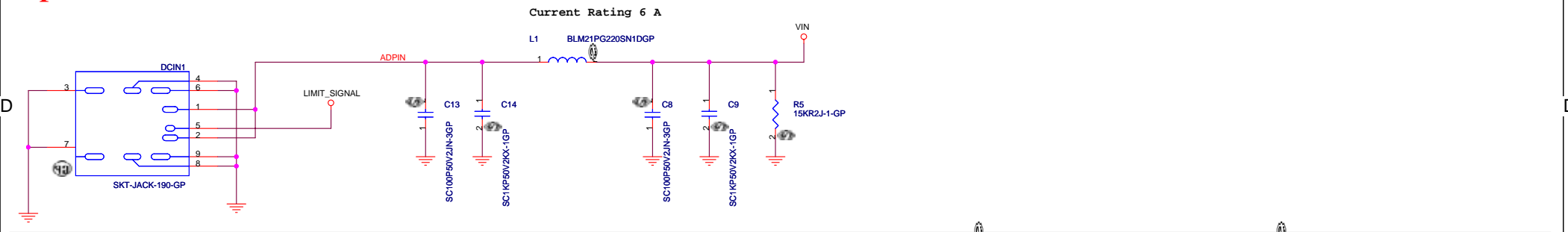
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Date: Friday, March 30, 2007 Sheet 35 of 51

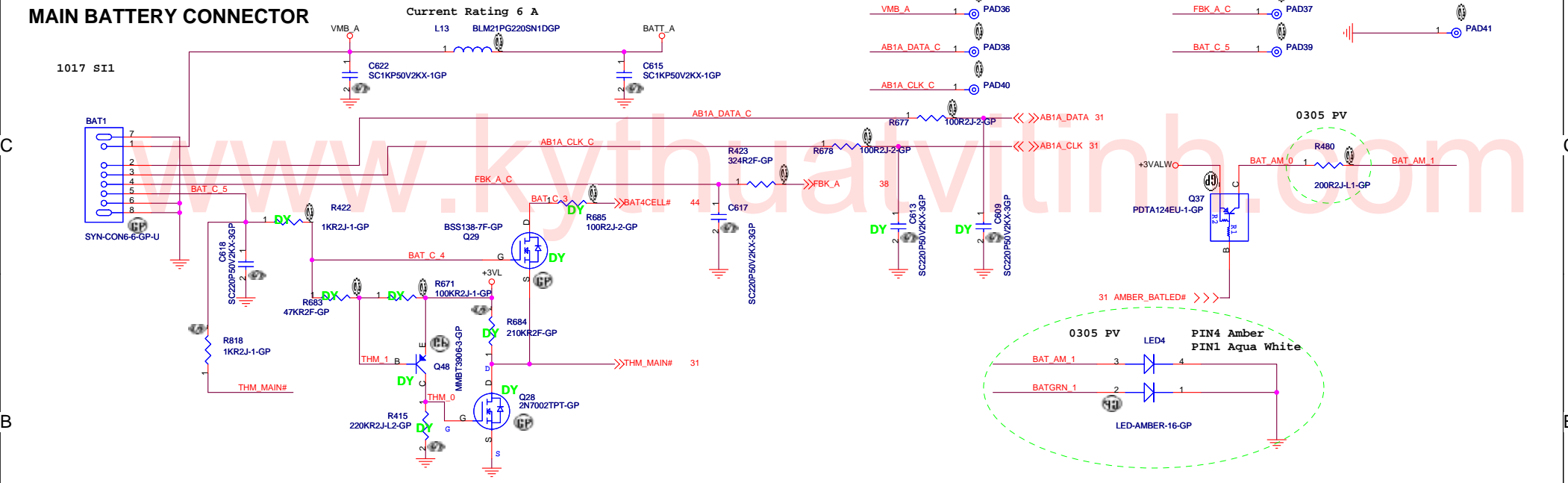



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 Taipei Hsien 221, Taiwan, R.O.C.

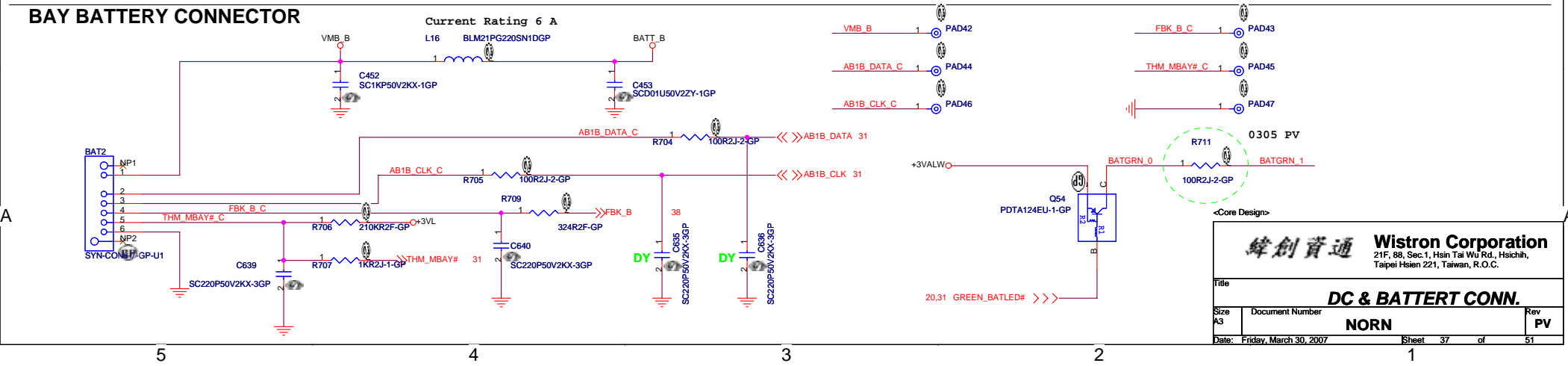
Title: **Power Block Diagram**
 Size: A3 | Document Number: **NORN** | Rev: **PV**
 Date: Friday, March 23, 2007 | Sheet: 36 of 51



MAIN BATTERY CONNECTOR



BAY BATTERY CONNECTOR

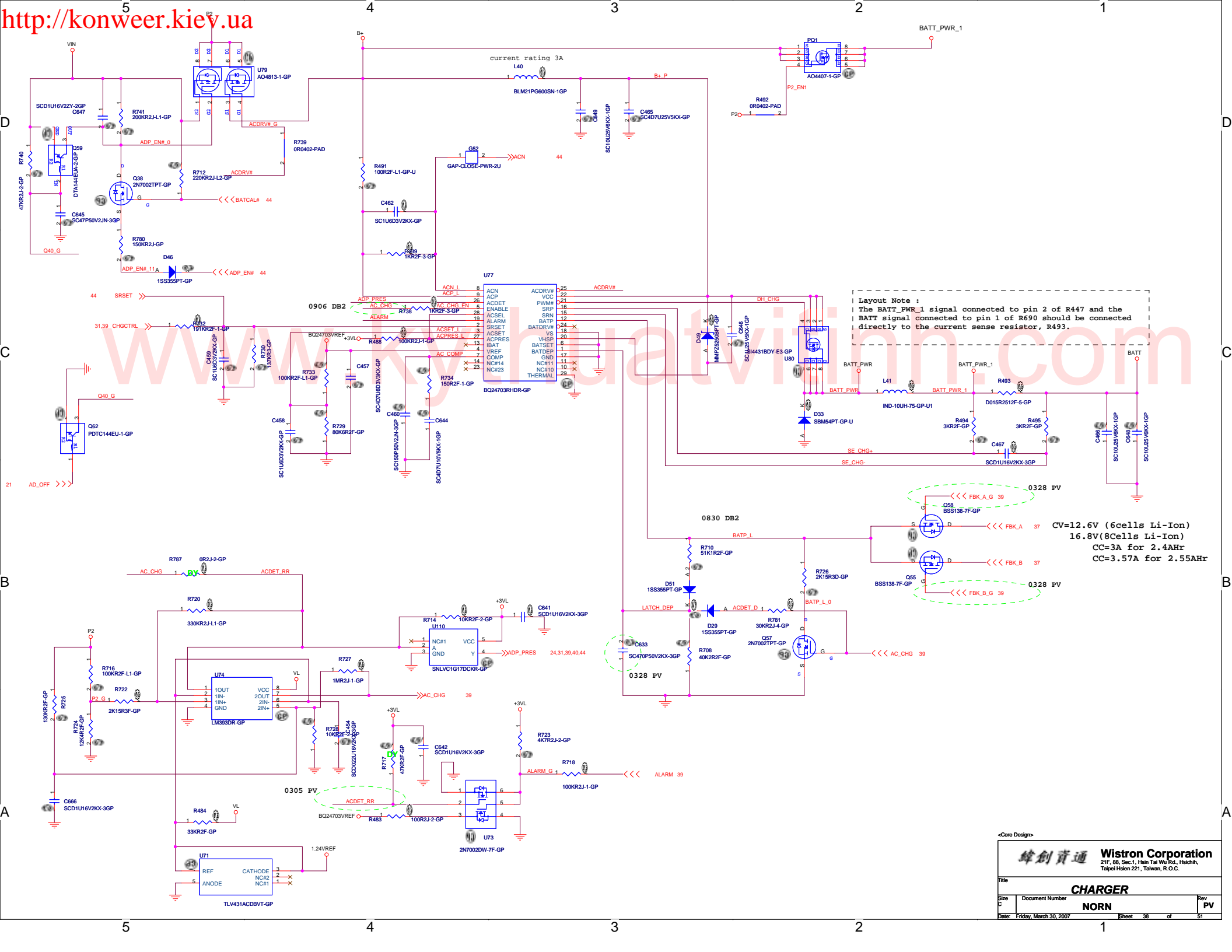


緯創資通 **Wistron Corporation**
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Title: **DC & BATTERY CONN.**

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Layout Note :
The BATT_PWR_1 signal connected to pin 2 of R447 and the BATT signal connected to pin 1 of R690 should be connected directly to the current sense resistor, R493.

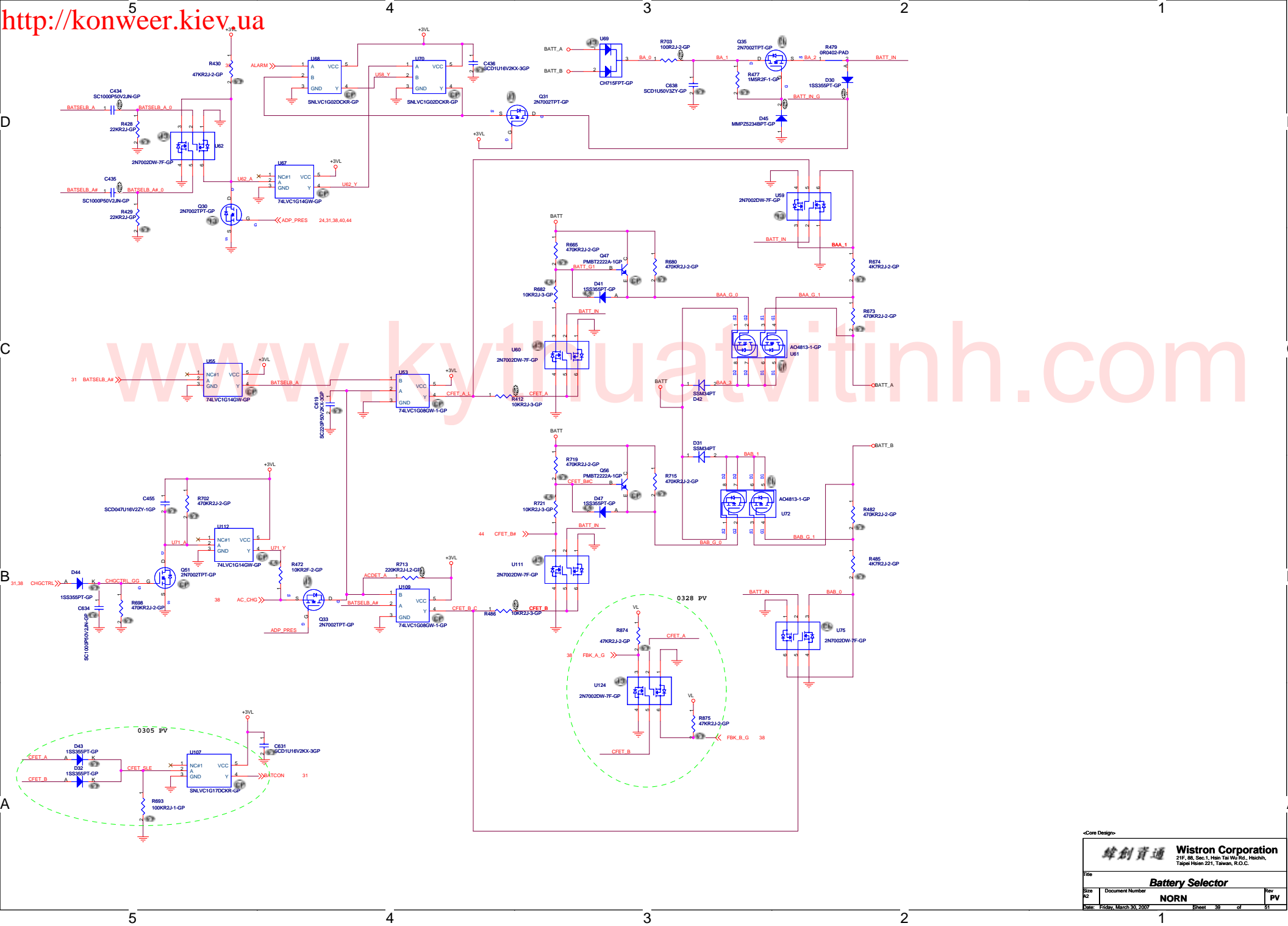
CV=12.6V (6cells Li-Ion)
16.8V(8Cells Li-Ion)
CC=3A for 2.4Ahr
CC=3.57A for 2.55Ahr

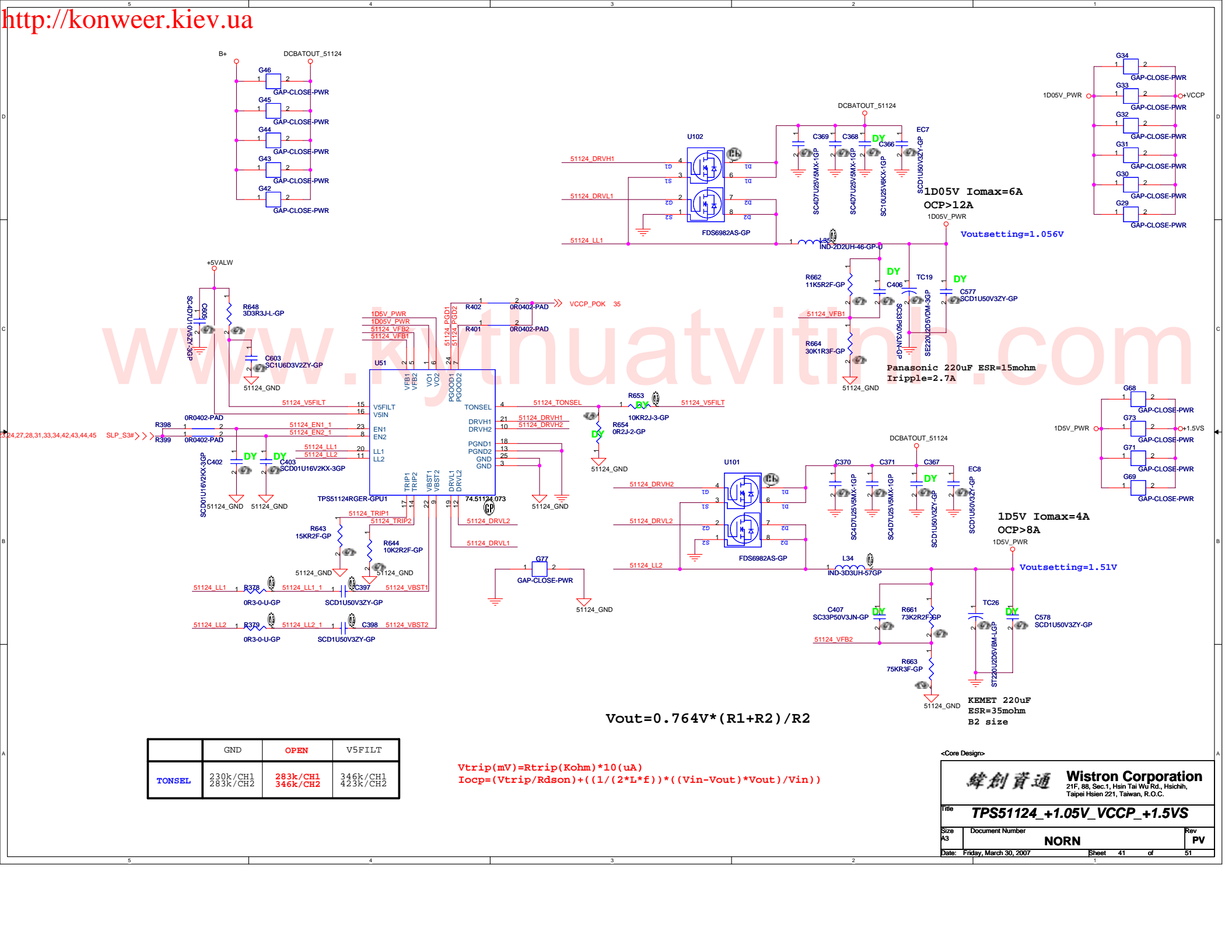
D

C

B

A





	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	345k/CH1 423k/CH2

$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$

$V_{out} = 0.764V * (R1+R2) / R2$

<Core Design>

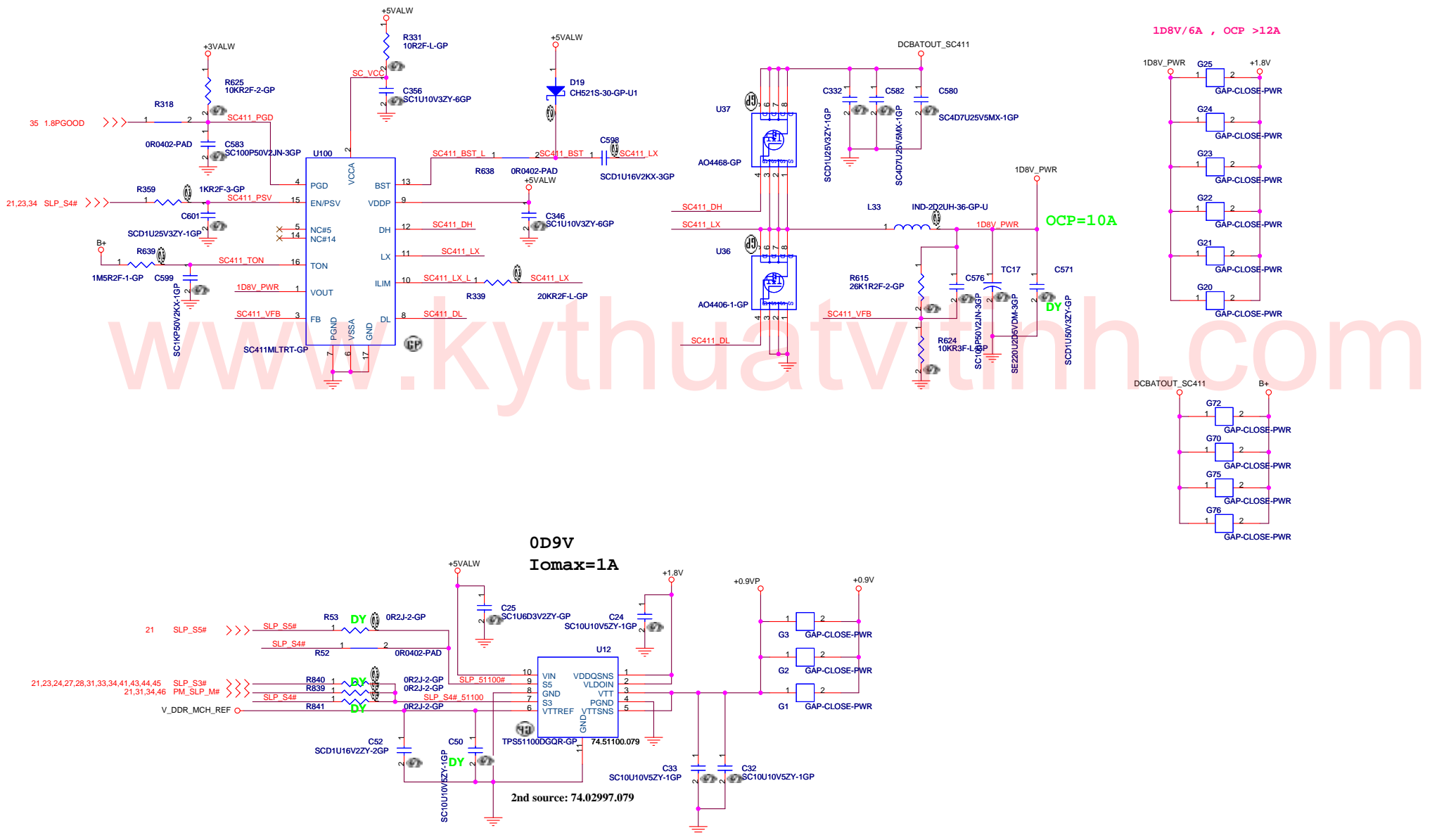
緯創資通 Wistron Corporation
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Title: **TPS51124 +1.05V_VCCP_+1.5V**

Size A3 Document Number **NORN** Rev **PV**

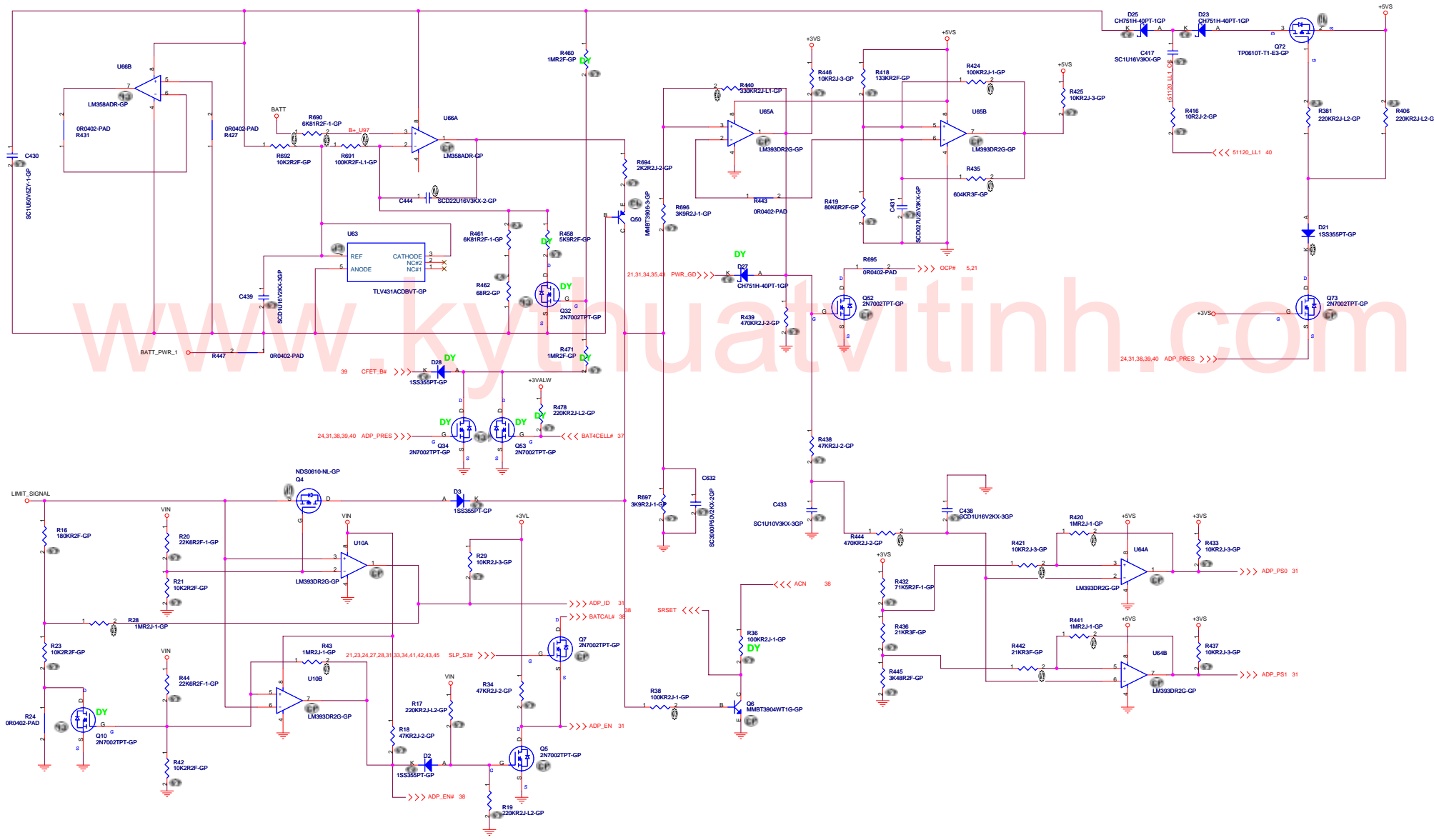
Date: Friday, March 30, 2007 Sheet 41 of 51

SC411 for 1D8V /TPS51110_0D9V

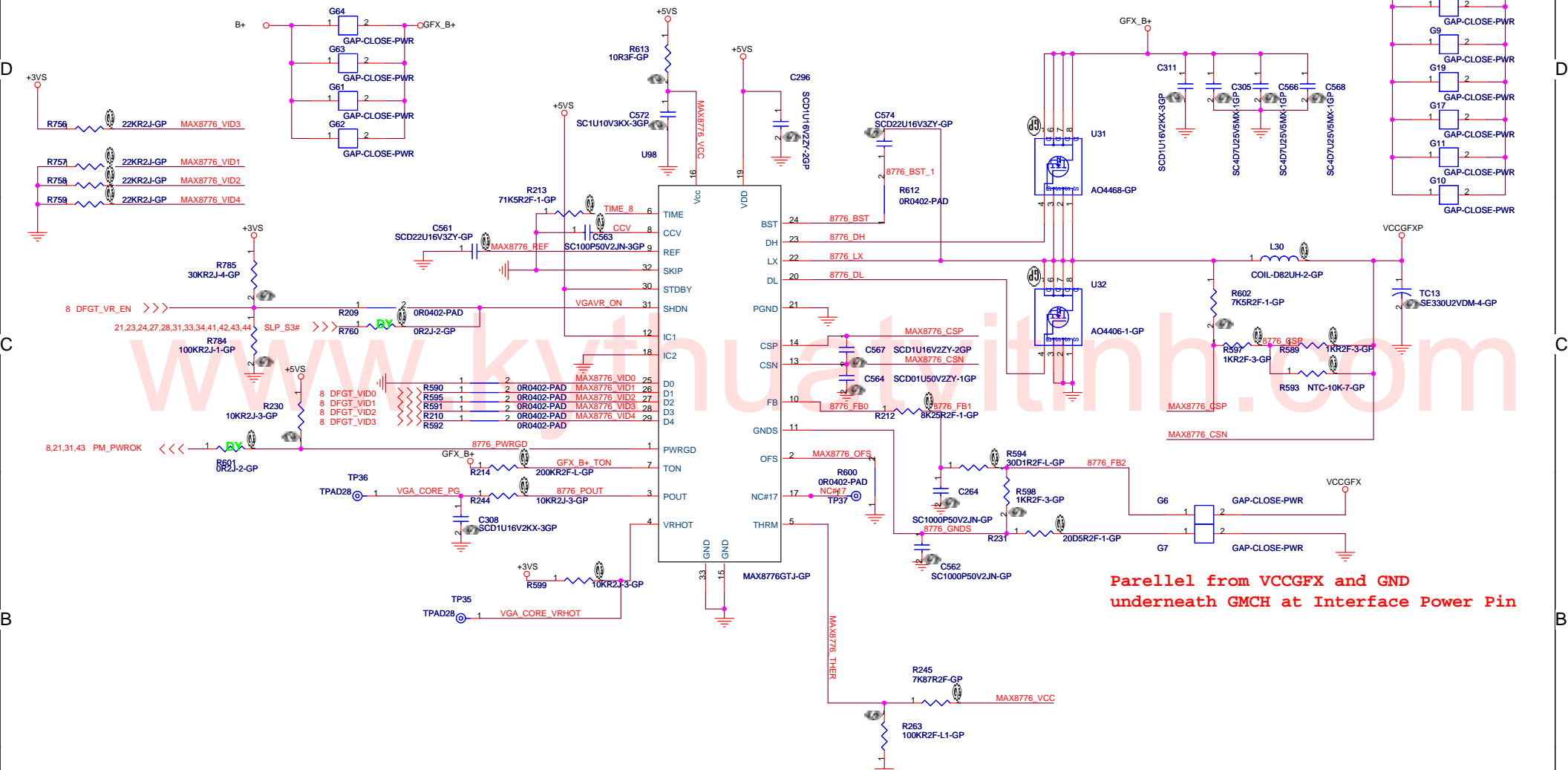


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緯創資通 Wistron Corporation	
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Title: SC 411 1D8V/0.9VP TPS51100	
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MAX8776



Parallel from VCCGFX and GND
underneath GMCH at Interface Power Pin

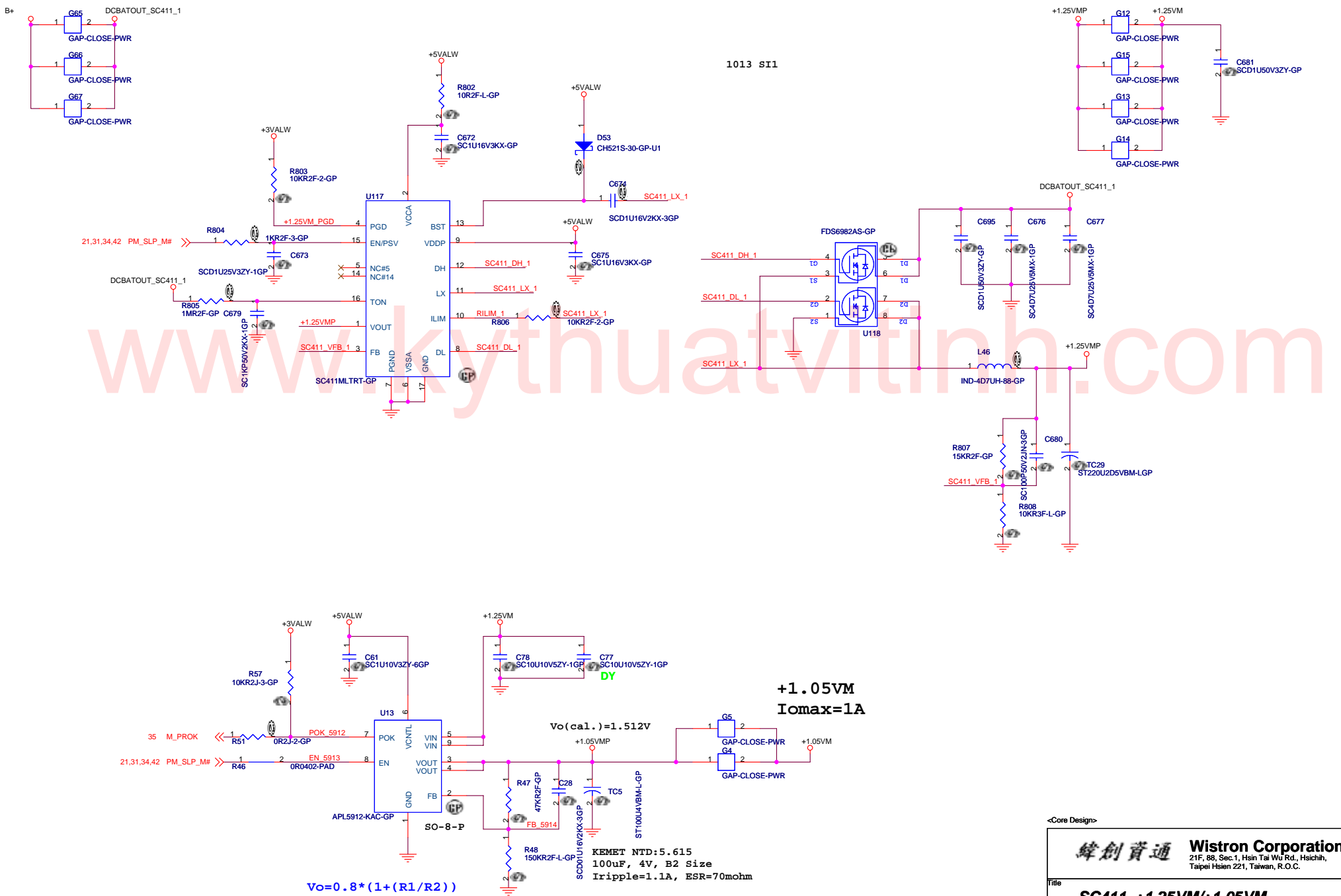
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsin 221, Taiwan, R.O.C.

Title: **MAX8776_VCCGFX**

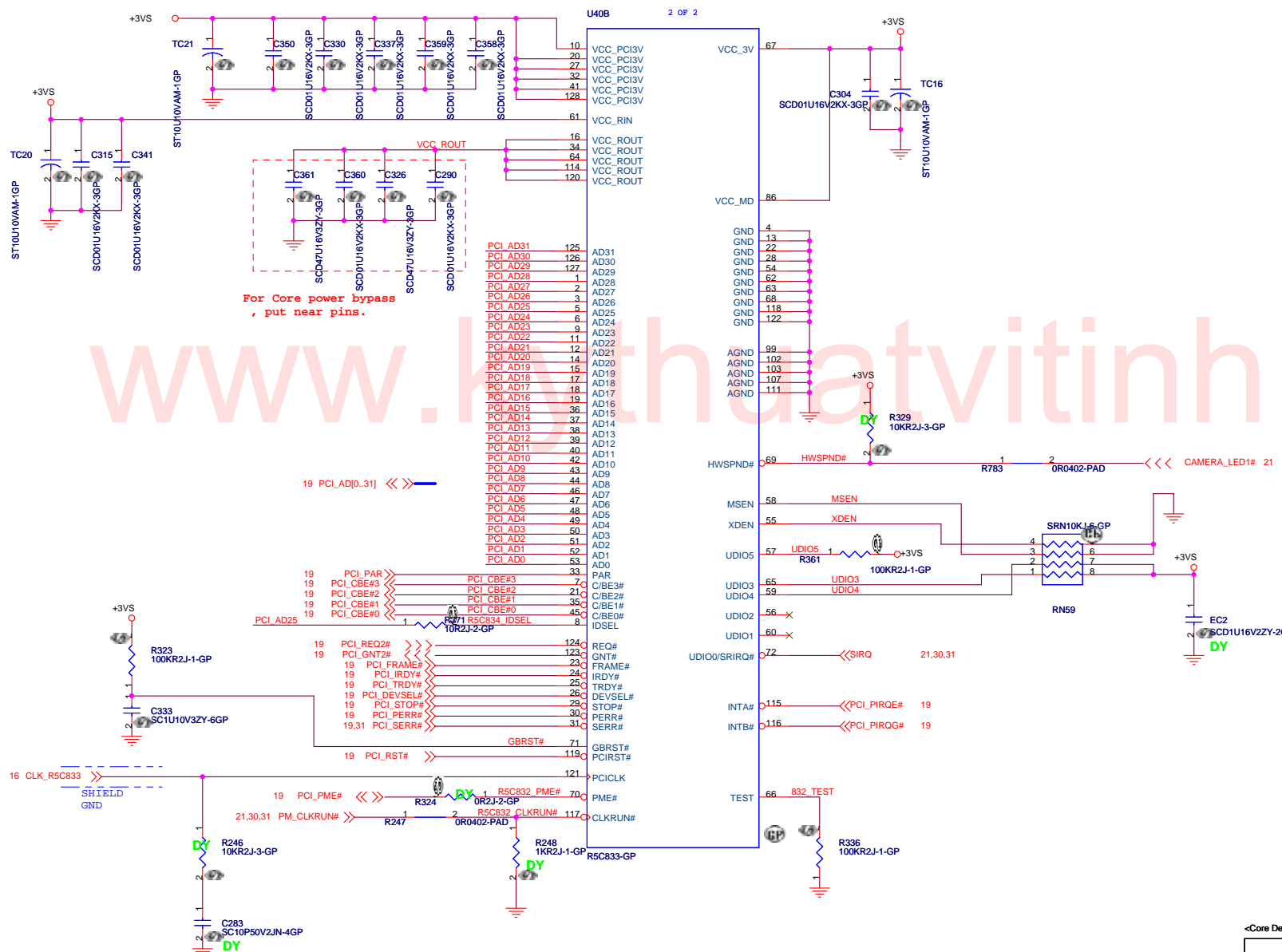
Size A3	Document Number	Rev
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緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title SC411 +1.25VM/+1.05VM	
Size A3	Document Number NORN
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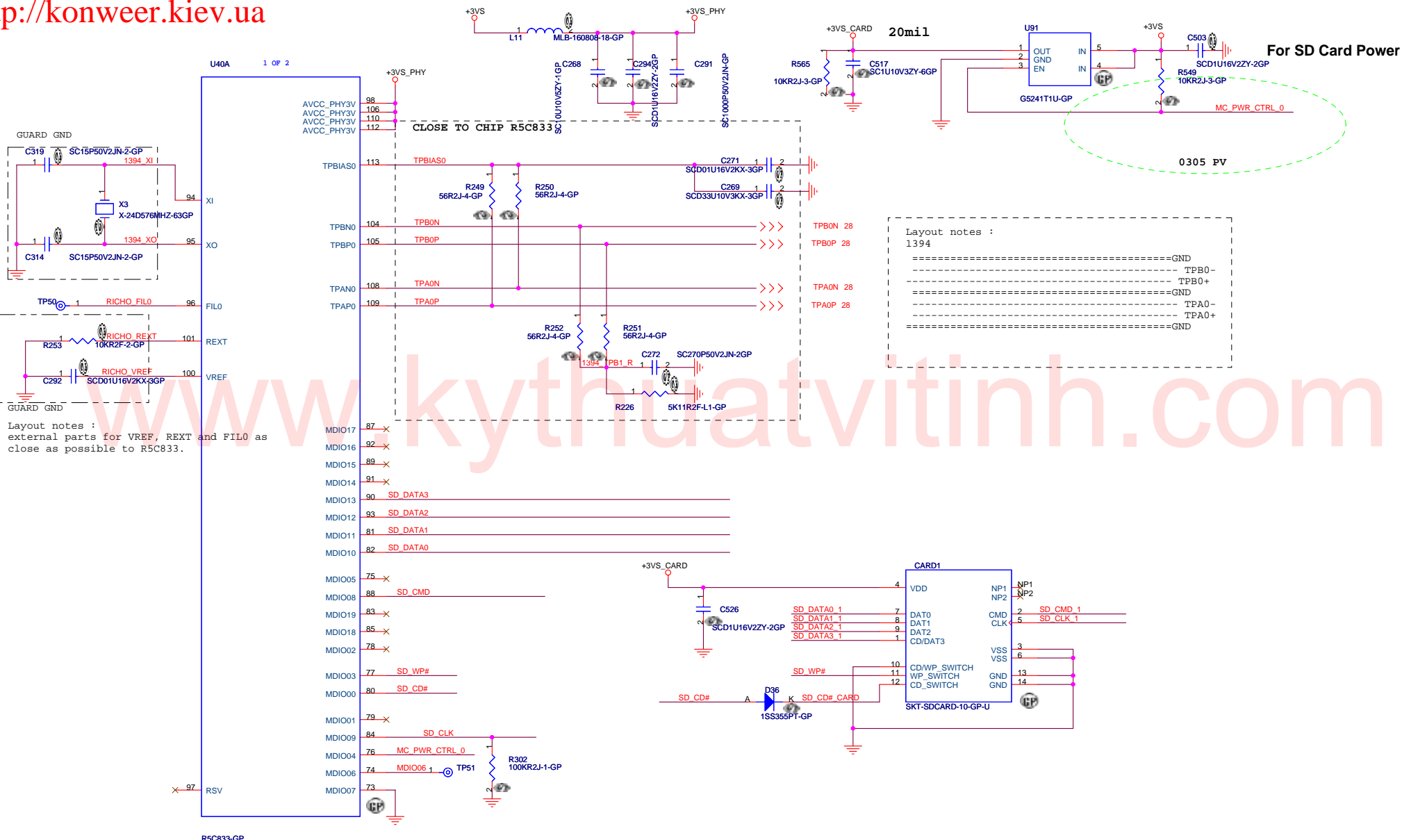


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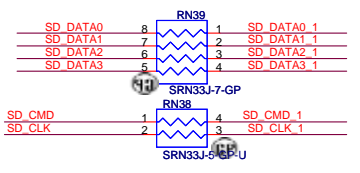
Title: **R5C833/PCI**

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Layout notes :
external parts for VREF, REXT and FIL0 as close as possible to R5C833.

Layout notes :
1394
=====GND
-----TPB0-
-----TPB0+
=====GND
-----TPA0-
-----TPA0+
=====GND



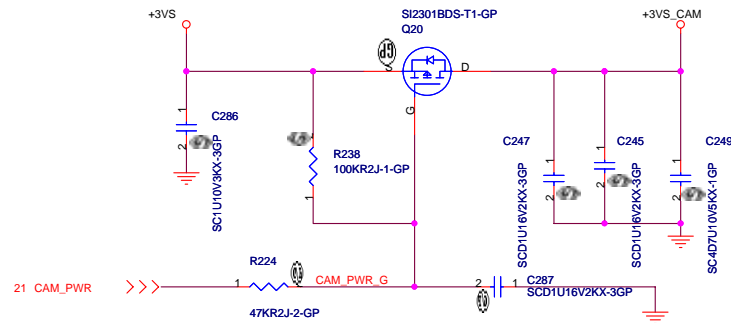
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緯創資通 Wistron Corporation
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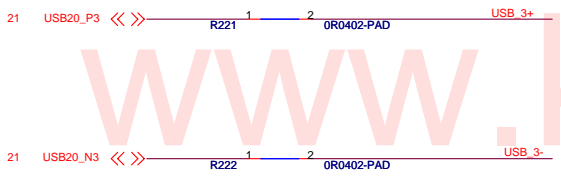
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Size A3	Document Number	NORN	Rev PV
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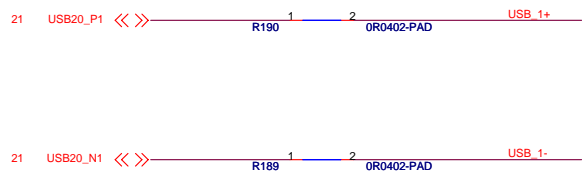
Date: Friday, March 30, 2007 Sheet 48 of 51



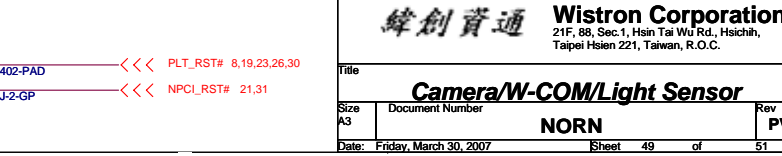
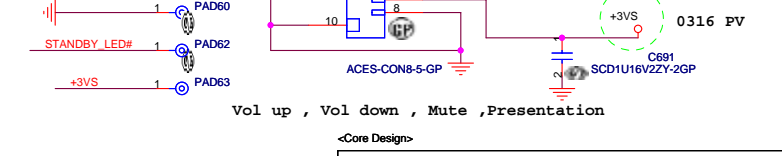
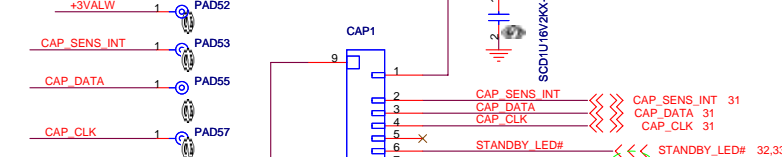
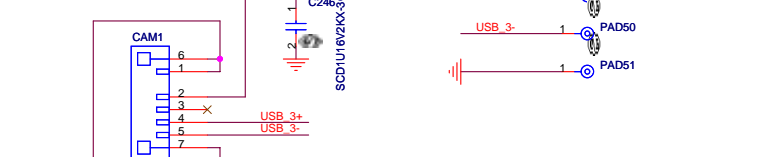
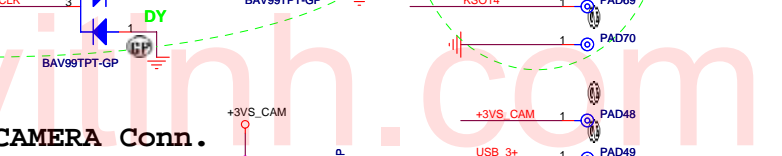
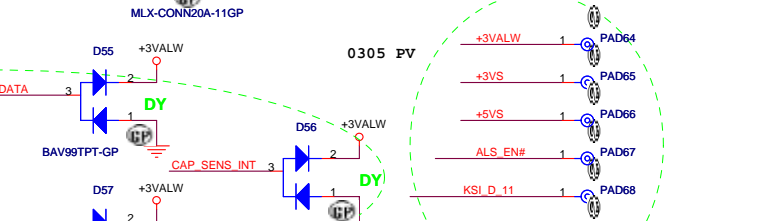
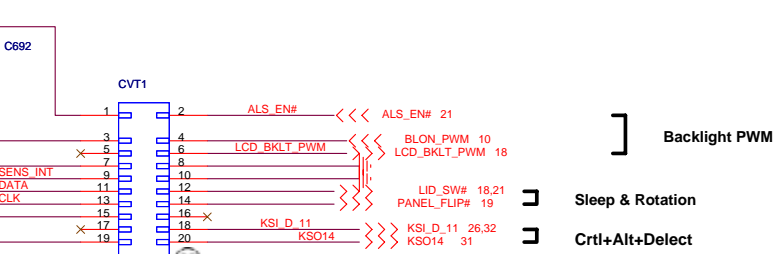
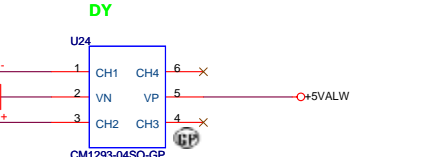
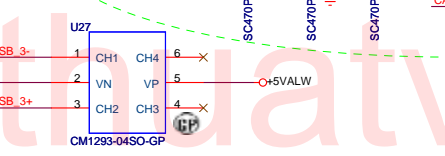
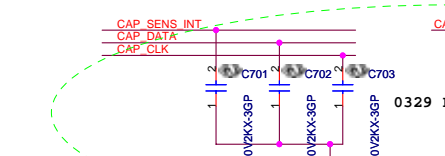
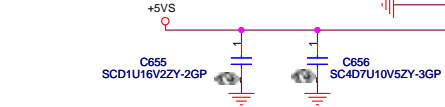
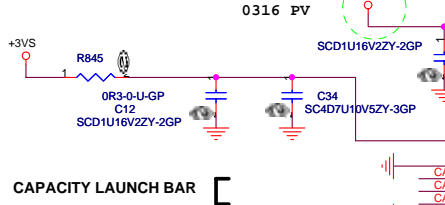
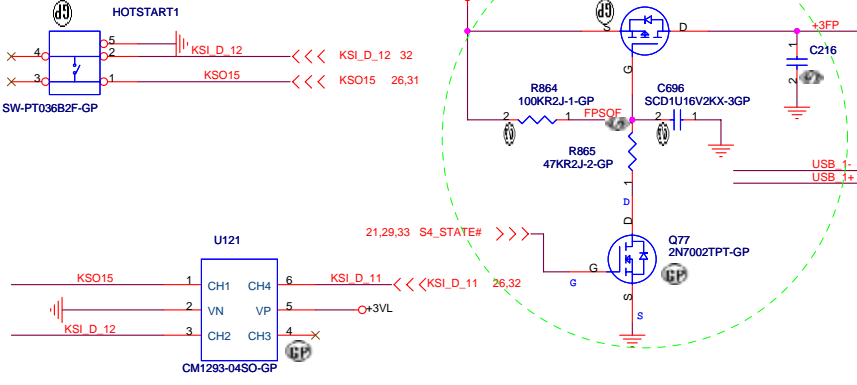
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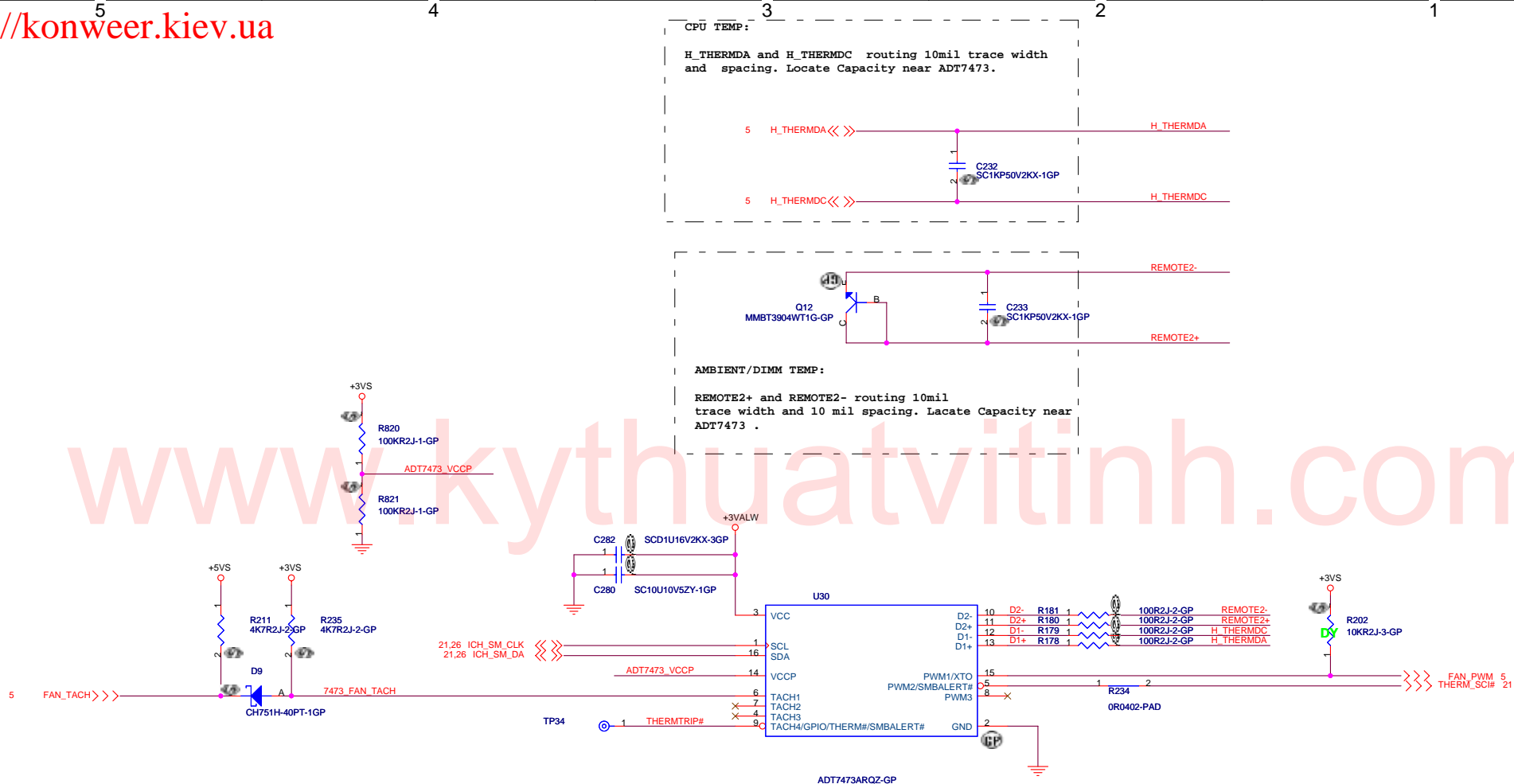
FingerPrint



HOTSTART



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Camera/W-COM/Light Sensor
 Title: **NORN** Rev: **PV**
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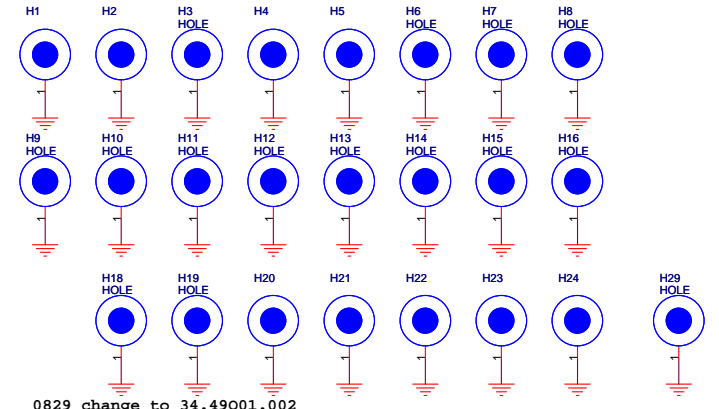
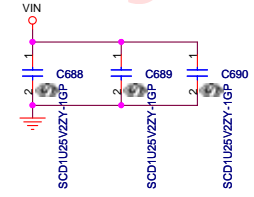
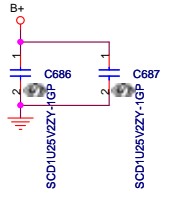


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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
ADT7473 Thermal Sensor			
Title	Document Number		Rev
Size A3	NORN		PV
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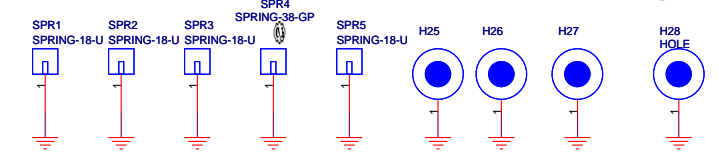
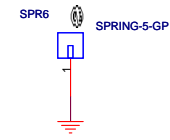
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1101 HOLE H1,H2 change part to 34.4R836.001
1101 HOLE H4,H5 change part to 34.4R837.001
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1101 HOLE H20,H21 change part to 34.4R841.001
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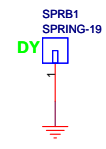


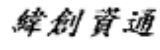
0829 change to 34.49Q01.002

0814 ME update drawing



1018 change SPR4 to 34.47R31.001
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UNUSED PARTS/EMI Capacitors	
Title	
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A3	Norn
Date: Tuesday, March 27, 2007	Rev PV
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