

MODEL REV

CHANGE LIST

Model CT3/5 MB BOARD

Page FROM TO

CT3/5 MB
31CT3MB0015
31CT3MB0031

1A

PAGE 2 --- Enable CLK48M from clokc generator for the PLL circuit of 7411, and disable the ocsillator circuit of PCI7411 PLL.

PAGE 3 --- Remove H/W shutdown circuit that supported ADM1032.

PAGE 4 --- Use X7R type to replace Y5V type for CPU Decoupling/Bypass capacitor.

PAGE 10 --- Add a terminal resistor R706 for -CODE_RST# to improve signal quality.

PAGE 11 --- 1. Add a 10K pull-up resistor on MCH_SYNC# for booting.
2. Change the power plane of PCIE_WAKE# from 3VSUS to 3V_S5 to solve system can't turn off issue.
3. Change the power plane of ICH_THRM# and SCI_# from 3VSUS to +3V to reduce leakage.

PAGE 12 --- We can also use 5VSUS to instead of 5V_S5 to save cost of MOSFET(A06402).

PAGE 15 --- Add a level-shift cicuit for EDID interface.

PAGE 17 --- 1. Add a off-page and a EMI solution for CLK48M.
2. Remove the reserve resistors (R693-R695) of parallel interface for PCI1510.

PAGE 18 --- Remove R696, connect controller and power switch directly .

PAGE 19 --- Change R682&R683 value from 56 ohms to 0 ohm cause of BOM error at A-test.

PAGE 22 --- 1. Change MC3 type from Y5V to X7R to improve singal quality.
2. Connect H1/H3 to AGND via a 0 ohm resistor by Conexant's comment.

PAGE 23 --- 1. Add a terminal resistor R707 for RTL8100/8110 id selection.
2. Add a 0.1uF to make Q40 turn on slowly to aviod 3VPCU drop issue.

PAGE 24 --- Modified transformer circuit cause of CT can't connect each other on 10/100M application.

PAGE 26 --- Add a flashrom as PLCC32 type for BIOS debugging.

PAGE 27 --- 1. Change R352 value from 120K ohms to 20M ohms.
2. Add a LPC debug port for software team to debug convenient.

PAGE 30 --- Add GMT fan controller for B-test to costdown.

PAGE 31 --- 1. Add ESD protection circuit for S-VIDEO signal to Docking.
2. Add R713 to enable the mux in the Tampa-2 cable

PAGE 33 --- Change PR143 value from 100K to 10K to solve display abnormal issue.

PAGE 35 --- 1. Move 5V_S5 circuit to Page 36.
2. De-popuplate PQ129 and PR182.
3. Change PR178 value from 22 ohm to 47 ohm.

PAGE 36 --- Remove PC170 and PQ127 but reserve 5V_S5 power circuit.

1	1A	
2	1A	2A
3	1A	2A
4	1A	2A
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	2A
11	1A	2A
12	1A	2A
13	1A	
14	1A	
15	1A	2A
16	1A	
17	1A	2A
18	1A	2A
19	1A	2A
20	1A	
21	1A	
22	1A	2A
23	1A	2A
24	1A	2A
25	1A	
26	1A	2A
27	1A	2A
28	1A	
29	1A	
30	1A	2A
31	1A	2A
32	1A	
33	1A	2A
34	1A	
35	1A	2A
36	1A	2A
37	1A	
38	1A	
39	1A	

MODEL REV

CHANGE LIST

CT3/5 MB
31CT3MB0015
31CT3MB0031

2A

PAGE 2 --- 1. Add C1048 for CLK48M to get better EMI performance.

PAGE 3 --- 1. Add R733 as pull-up resistor for FREQ#.

PAGE 11 --- 1. Add RF_OFF# and BT_OFF#

PAGE 17 --- 1. Populate R704 and C1046 to get better EMI performance.

2. Remove R701 & R702 for unused PCI1510RVGF circuit.

PAGE 18 --- 1. Disconnect SM_PHYS_WP on controller side.

2. Tie SM_EL_WP with SM_PHYS_WP on conn side to allow for normal operation of SD and SM.

3. Add a discharge circuit for media card power.

4. Add R718 to solve cross-talk issue of MS-Pro card.

5. Add R717 to solve SM card can't write protect issue.

6. Add R719~R736 as terminal on all multi-function pins.

7. Add pull-up circuit.

PAGE 27 --- 1. Reserve 0R for RF_OFF# and BT_OFF# circuit.

2. Modify LPC pin name.

PAGE 28 --- 1. Change HDD and ODD select definition.

PAGE 30 --- Adjust Capacitors and Bead to improve CRT timing issue.

1. Change L66, L67, L68 from BK1608HM470 to 0R.

2. Remove C931, C932, C933.

3. Change C934, C935, C936 from 22P to 5.6P.

4. Change C6, C14, C350 from 10P to 5.6P.

5. Change L1, L26, L27 from BK1608HM470 to BLM18BA750SN1T.

PAGE 31 --- 1. Change L5,L6,L7,C57,C58,C64,C77,C113,C121 value to improve S-video quality.

2. Reserve S-video impedance match circuit.

Page	CT3/5 MB BOARD	
	FROM	TO
1	1A	
2	2A	3A
3	2A	3A
4	2A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	2A	
11	2A	
12	1A	
13	1A	
14	1A	
15	2A	
16	1A	
17	2A	3A
18	2A	3A
19	2A	
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21	1A	
22	2A	
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26	2A	2A
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31	2A	
32	1A	
33	2A	
34	2A	
35	2A	
36	2A	
37	2A	
38	2A	
39	2A	

CT3 BLOCK DIAGRAM

PENTIUM-M / ALVISO / ICH6-M

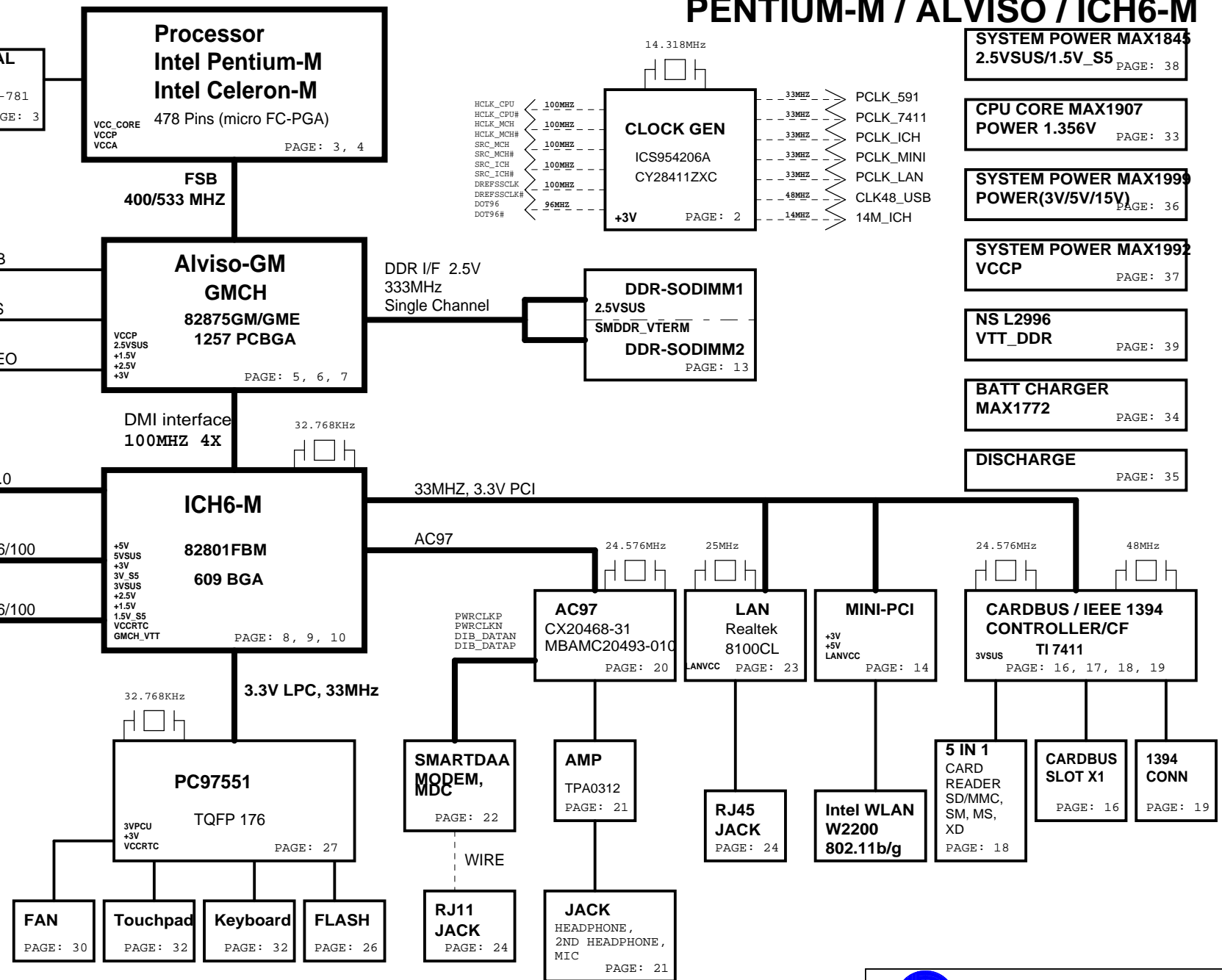
PCB STACK UP

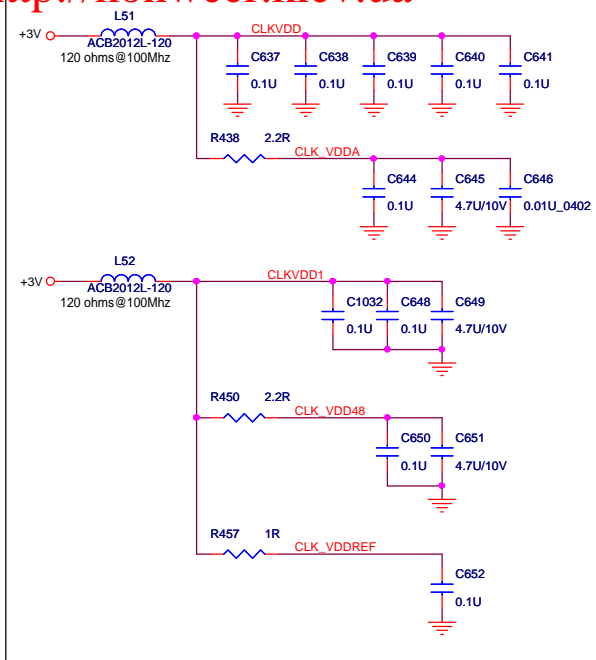
- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

PCB THICKNESS: 1.2mm

PCI DEVICES IRQ ROUTING

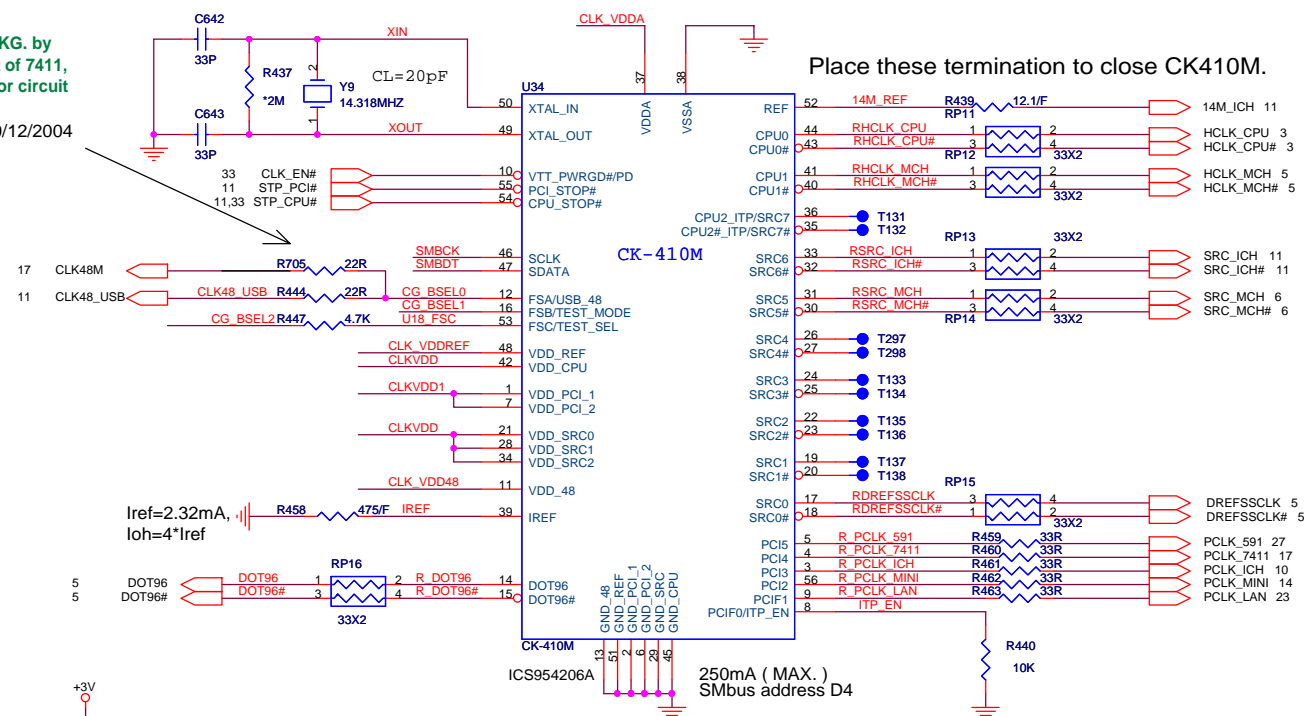
DEVICE	IDSEL #	REQ/GNT #	PCI_INT
GBIT ETHERNET AD16		2	A
MINIPCI SLOT AD22		1	C,D
CardBus/1394 AD25		0	E,F,G





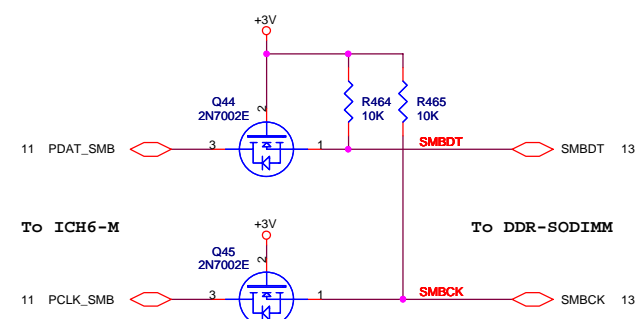
SI stage:
Enable CLK48M from CKG. by R705 for the PLL circuit of 7411, and disable the oscillator circuit at PCI7411 side.

Sting 10/12/2004



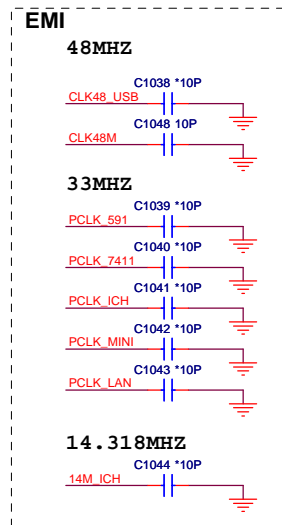
FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	DOTHAN FSB 400
0	0	1	133	100	33	DOTHAN FSB 533
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	RESERVED			

* Frequency select by CPU auto sense.

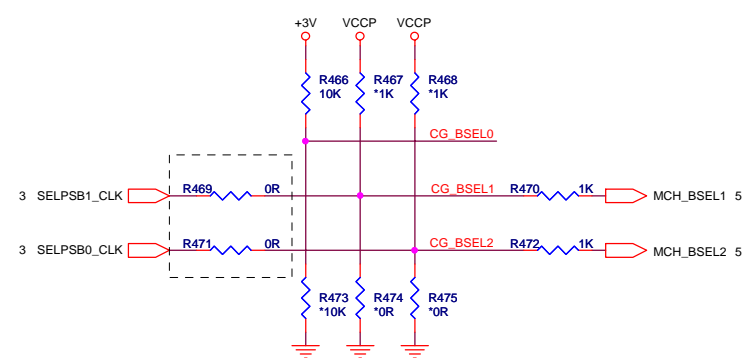


PV stage:
Add C1048 for CLK48M to get better EMI performance.

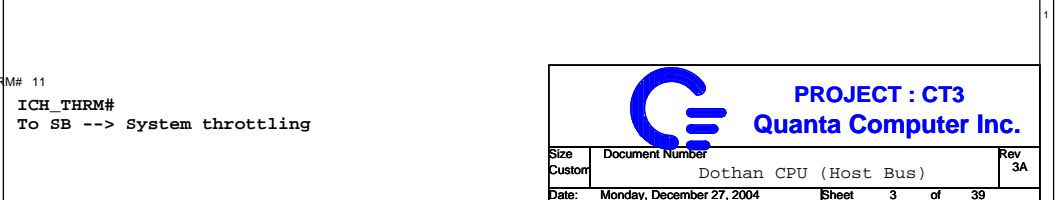
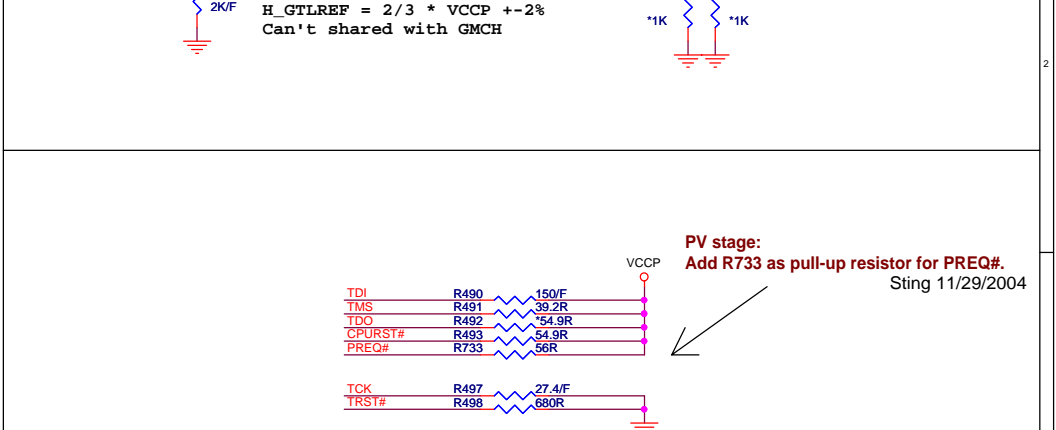
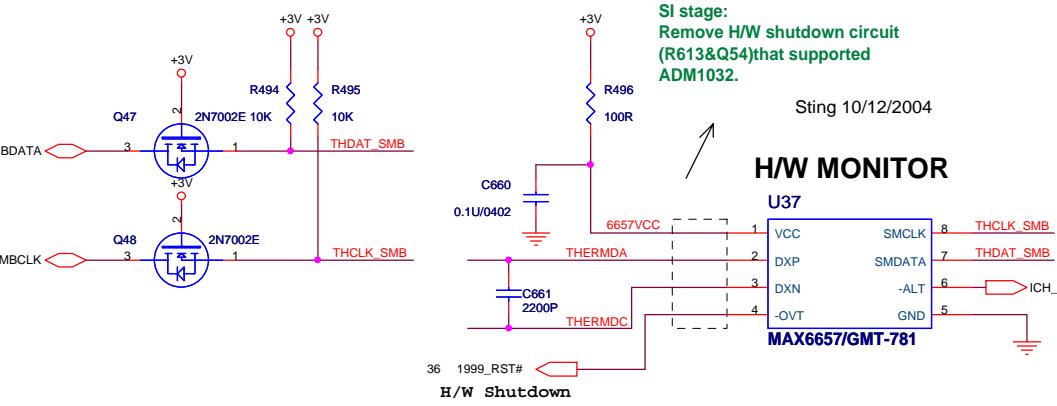
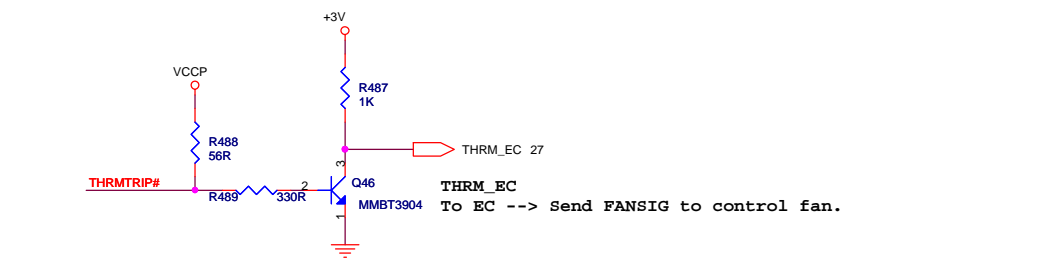
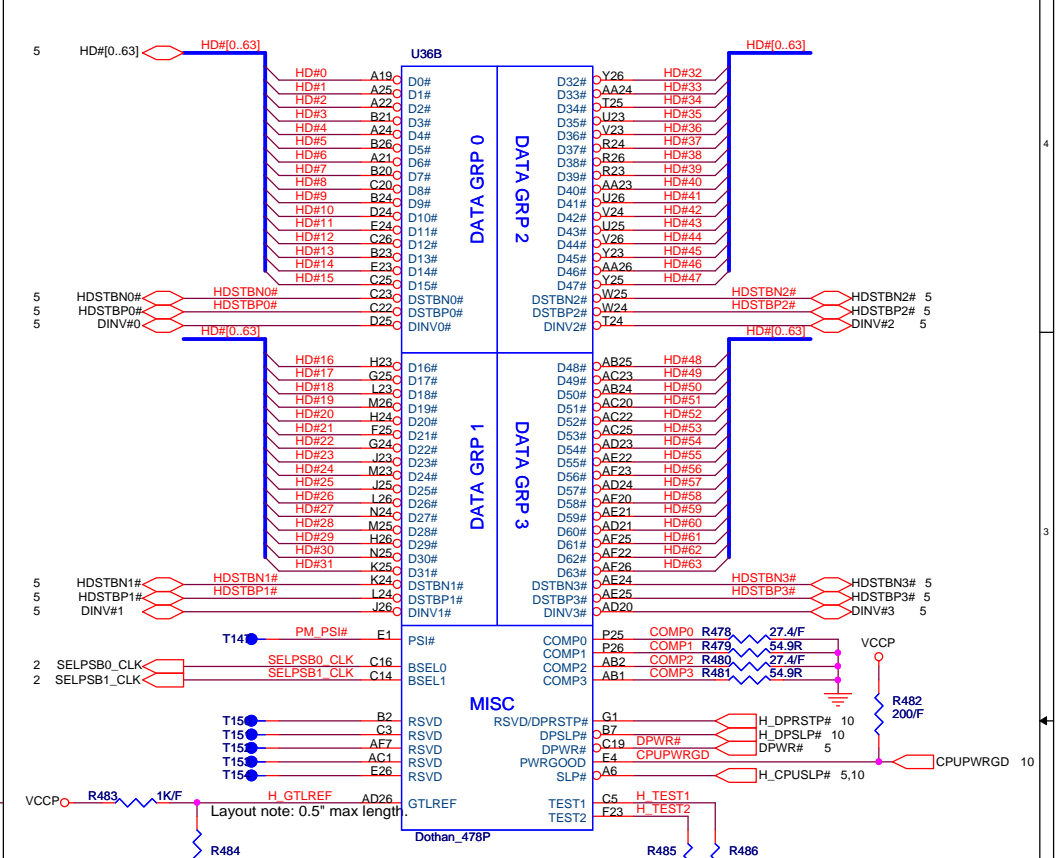
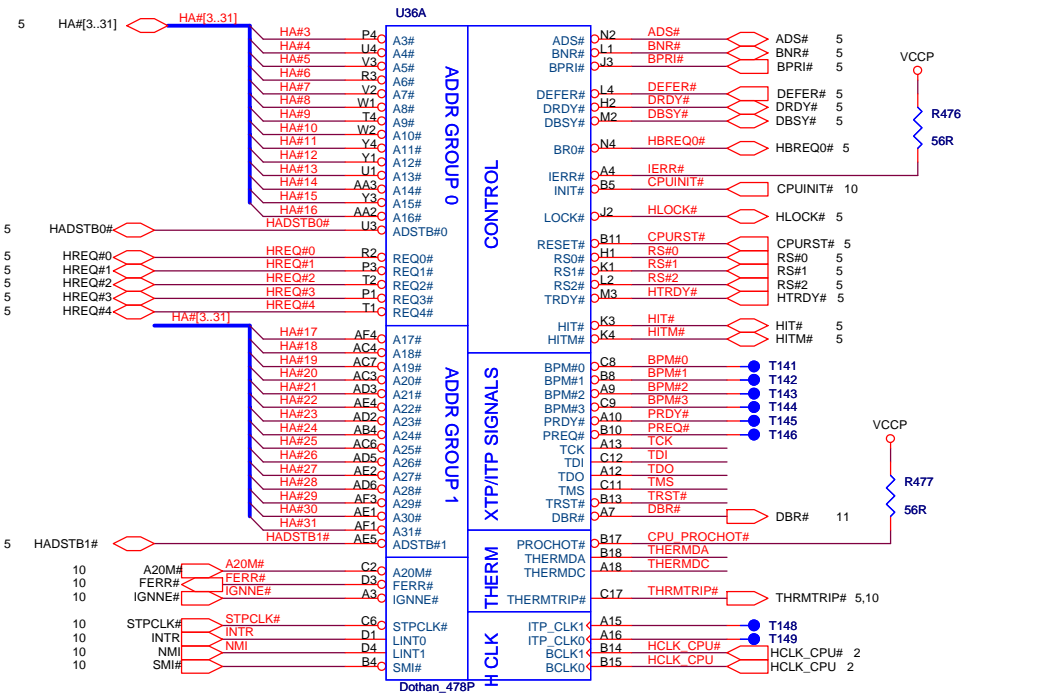
Sting 11/29/2004

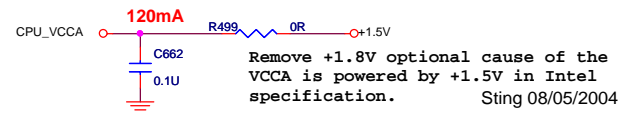
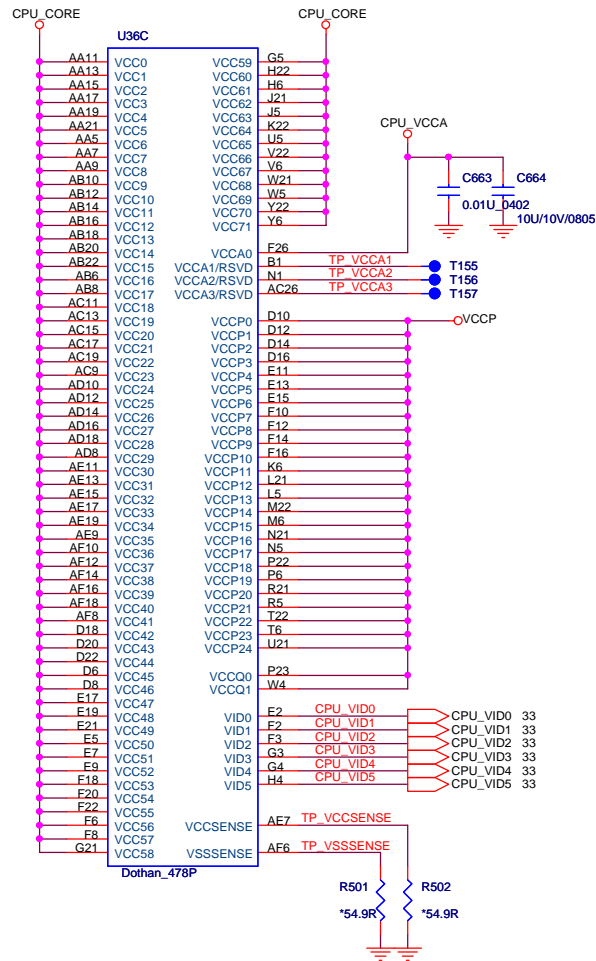


R_PCLK_LAN ITP_EN
0: SRCCLK=96MHZ 0: SRC_7 Pair
1: SRCCLK=100MHZ 1: CPU_2 ITP Pair

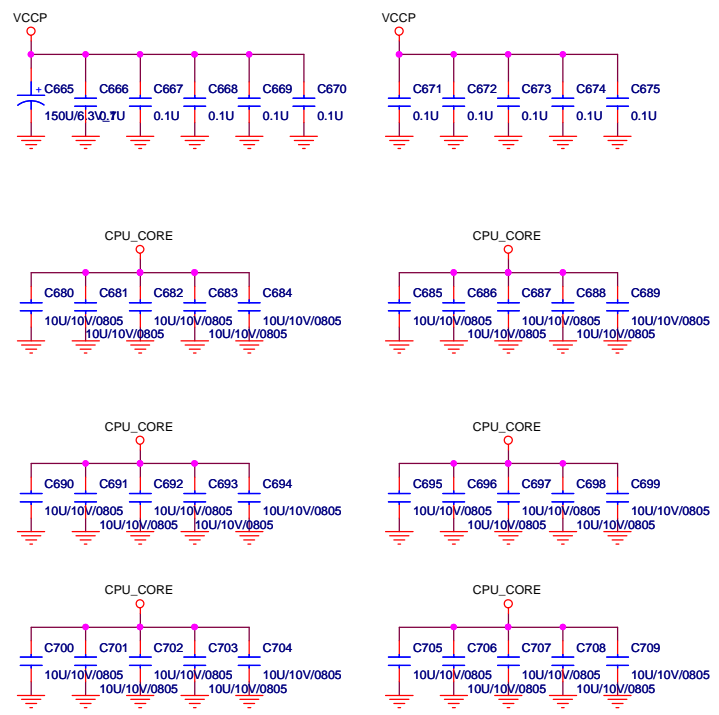


R469,R471
Dothan-A can remove so that the FSB frequency will be selected by hardware setting(R474,R475,R467,R468).
Dothan-B should be populated.

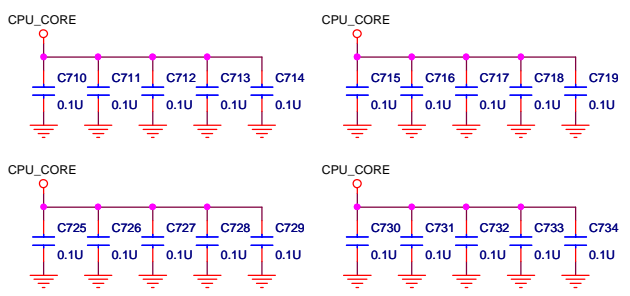




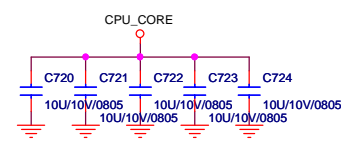
SI stage:
Use X7R type to replace Y5V type for Decoupling/Bypass capacitor.
Sting 10/12/2004



CPU de-coupling capacitor



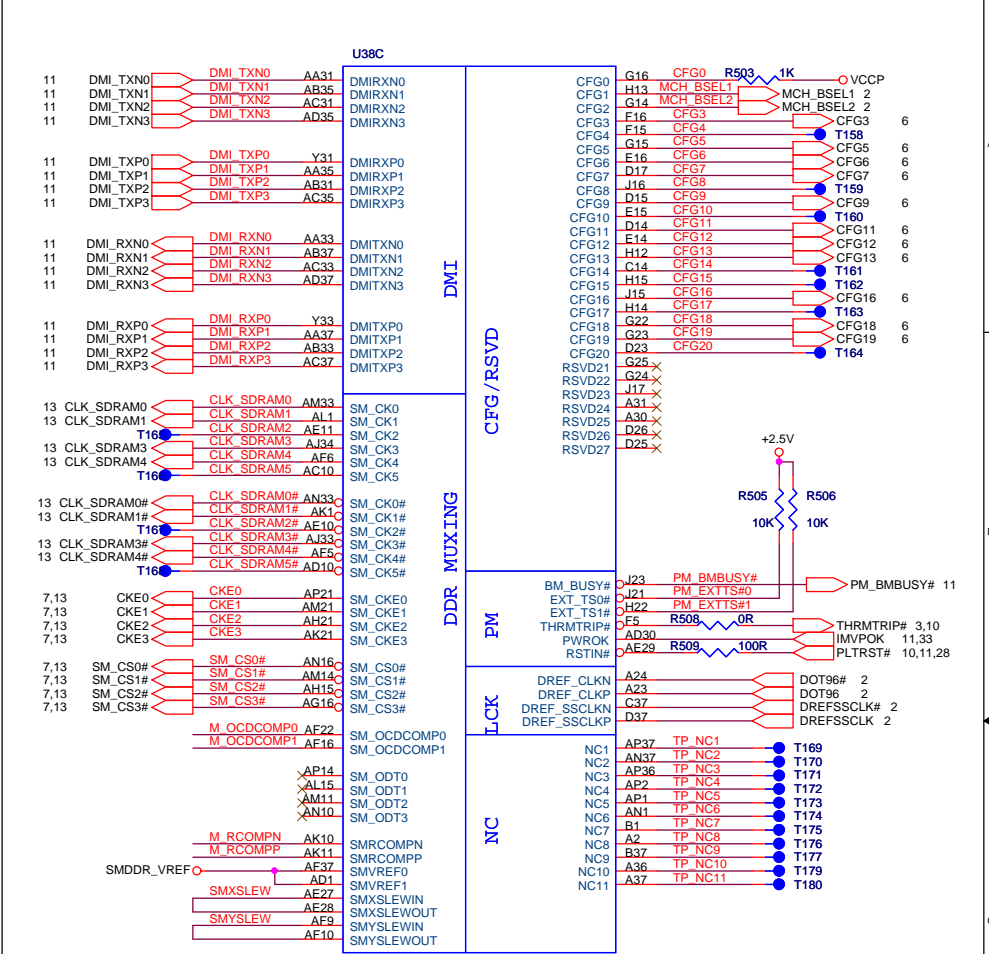
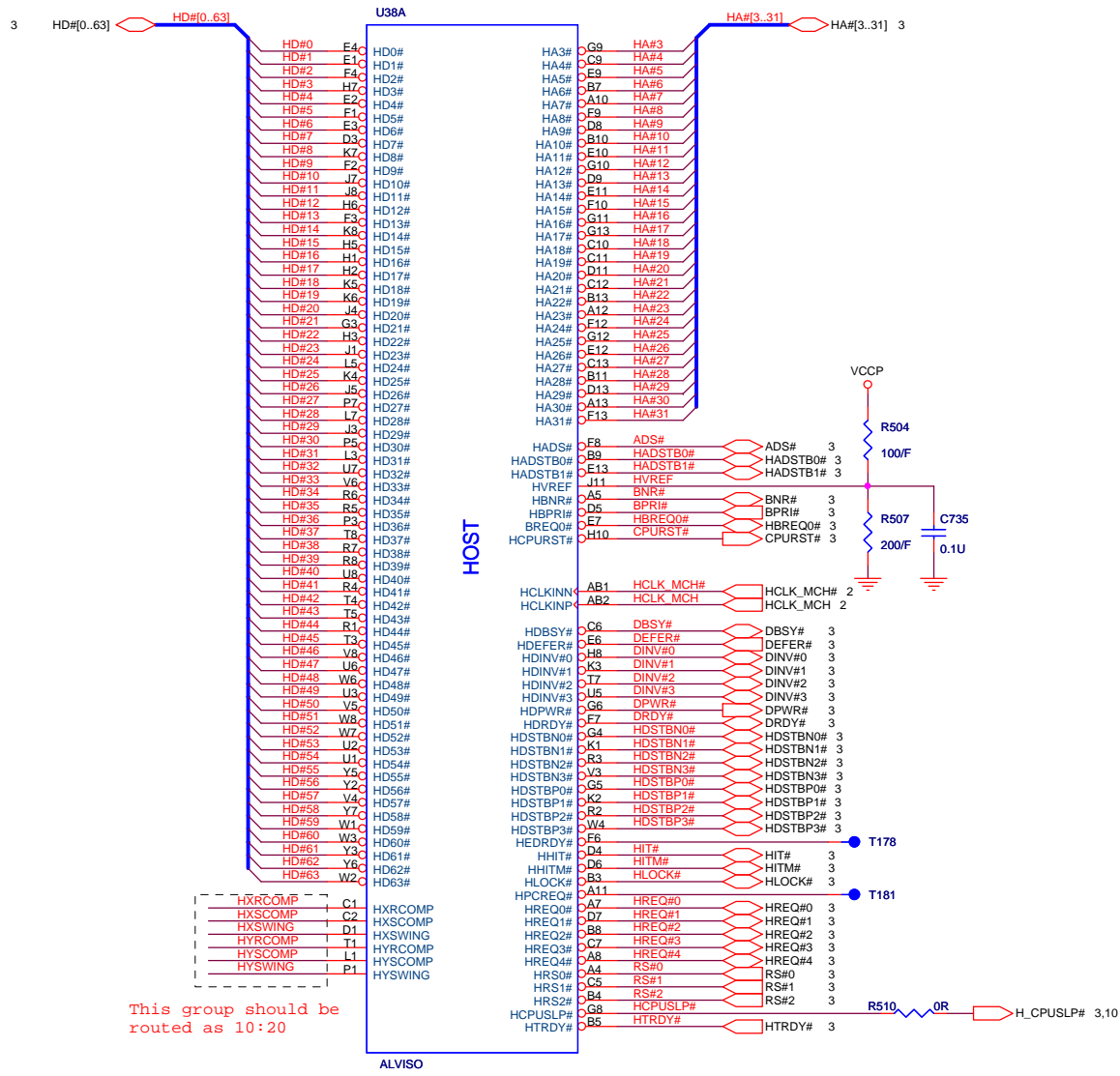
CPU Bypass capacitor



U36D		
A2	VSS0	D13
A5	VSS1	D14
A8	VSS2	D17
A11	VSS3	D19
A14	VSS4	D21
A17	VSS5	D23
A20	VSS6	D26
A23	VSS7	E3
A26	VSS8	E4
AA1	VSS9	E8
AA4	VSS10	E10
AA6	VSS11	E12
AA8	VSS12	E14
AA10	VSS13	E16
AA12	VSS14	E18
AA14	VSS15	E20
AA16	VSS16	E22
AA18	VSS17	E25
AA20	VSS18	F1
AA22	VSS19	F4
AA25	VSS20	F5
AB3	VSS21	F7
AB5	VSS22	F9
AB7	VSS23	F11
AB9	VSS24	F13
AB11	VSS25	F15
AB13	VSS26	F17
AB15	VSS27	F19
AB17	VSS28	F21
AB19	VSS29	F24
AB21	VSS30	G2
AB23	VSS31	G6
AB26	VSS32	G22
AC2	VSS33	G23
AC5	VSS34	G26
AC8	VSS35	H3
AC10	VSS36	H5
AC12	VSS37	H21
AC14	VSS38	H25
AC16	VSS39	J1
AC18	VSS40	J4
AC21	VSS41	J6
AC24	VSS42	J22
AD1	VSS43	J24
AD4	VSS44	K2
AD7	VSS45	K5
AD9	VSS46	K21
AD11	VSS47	K23
AD13	VSS48	K26
AD15	VSS49	L3
AD17	VSS50	L6
AD19	VSS51	L22
AD22	VSS52	L25
AD25	VSS53	M1
AE3	VSS54	M4
AE6	VSS55	M5
AE8	VSS56	M21
AE10	VSS57	M24
AE12	VSS58	N6
AE14	VSS59	N22
AE16	VSS60	N23
AE18	VSS61	N26
AE20	VSS62	P2
AE23	VSS63	P5
AE26	VSS64	P21
AE28	VSS65	P24
AF9	VSS66	P63
AF11	VSS67	R1
AF12	VSS68	R4
AF13	VSS69	R6
AF15	VSS70	R22
AF17	VSS71	R25
AF19	VSS72	T3
AF21	VSS73	T5
AF24	VSS74	T21
B3	VSS75	T23
B6	VSS76	T26
B9	VSS77	U2
B12	VSS78	U6
B16	VSS79	U22
B19	VSS80	U24
B22	VSS81	V1
B25	VSS82	V4
C1	VSS83	V5
C4	VSS84	V21
C7	VSS85	V25
C10	VSS86	W3
C15	VSS87	W22
C18	VSS88	W23
C21	VSS89	W26
C24	VSS90	Y2
D2	VSS91	Y5
D5	VSS92	Y21
D7	VSS93	Y24
D9	VSS94	
D11	VSS95	
	VSS96	

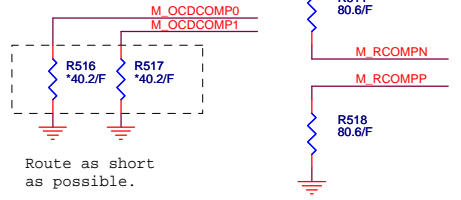
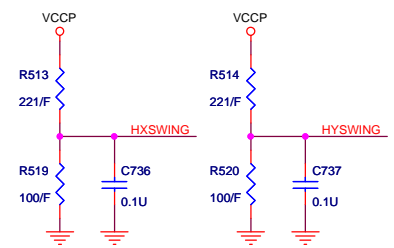
PROJECT : CT3
Quanta Computer Inc.

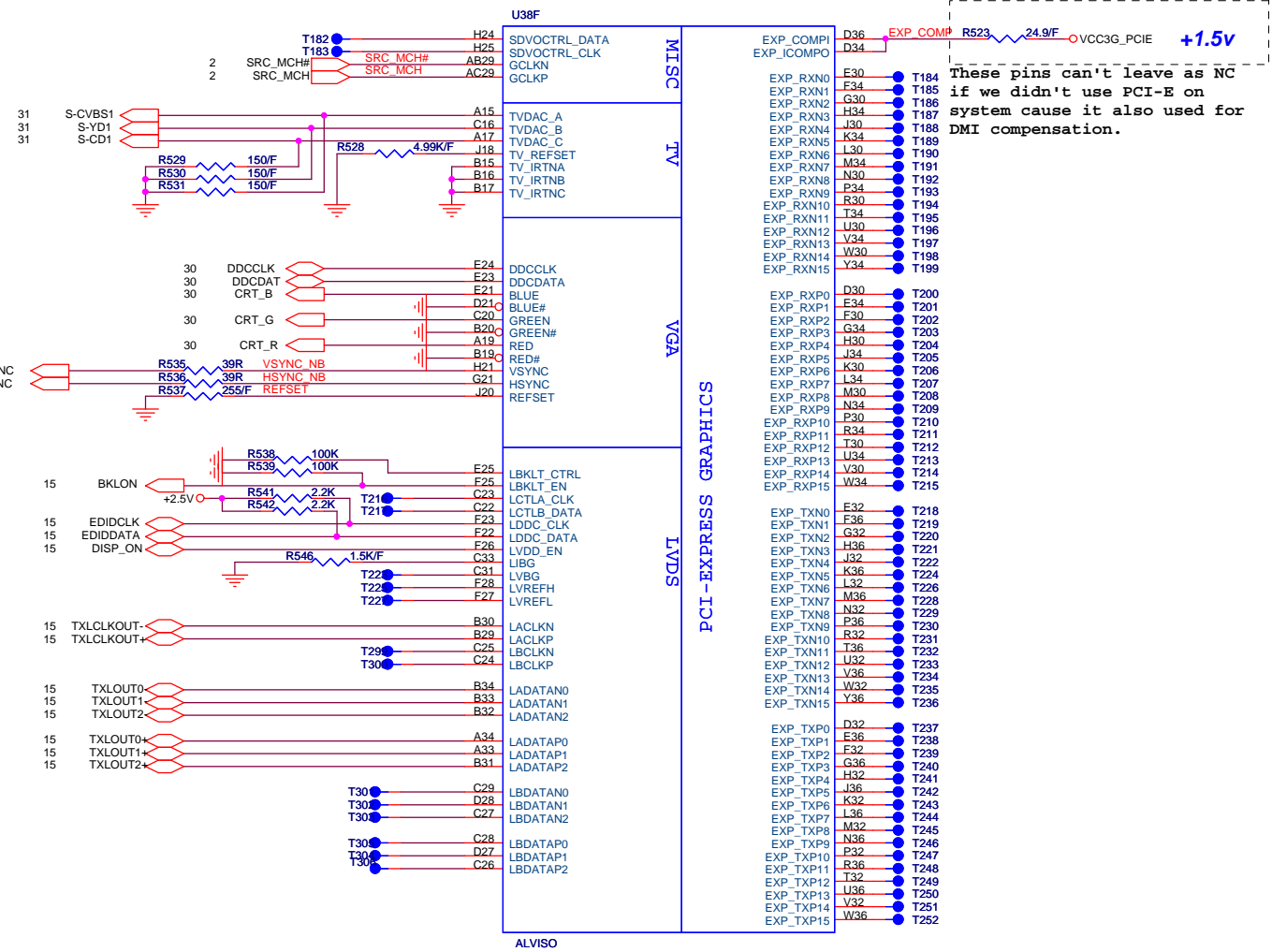
Size	Document Number	Rev
Customer	CPU POWER / GND	2A
Date:	Monday, December 27, 2004	Sheet 4 of 39



It's point to point, 55ohm trace, keep as short as possible.

This group should be routed as 10:20

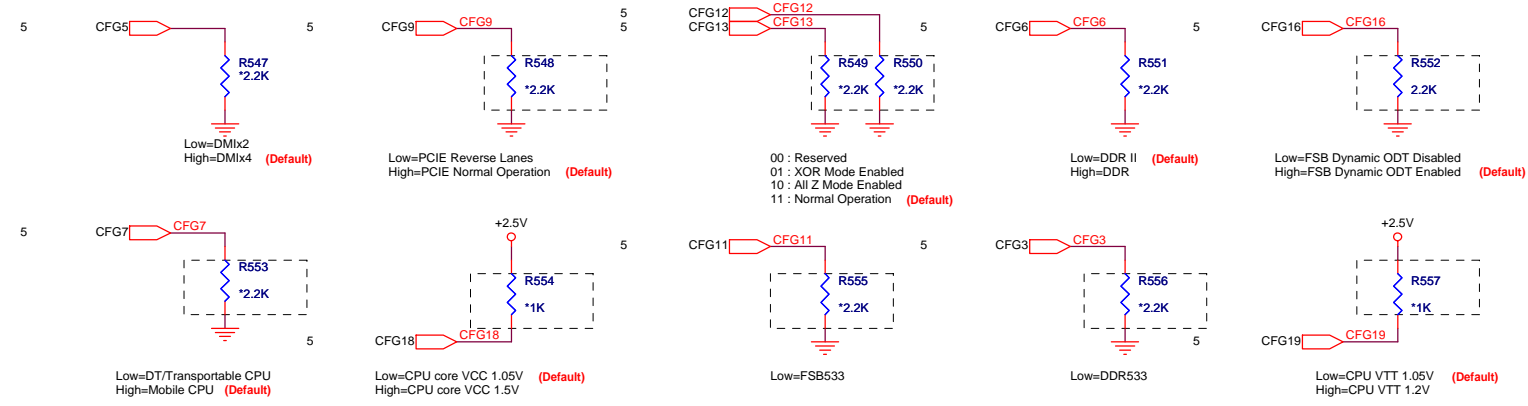




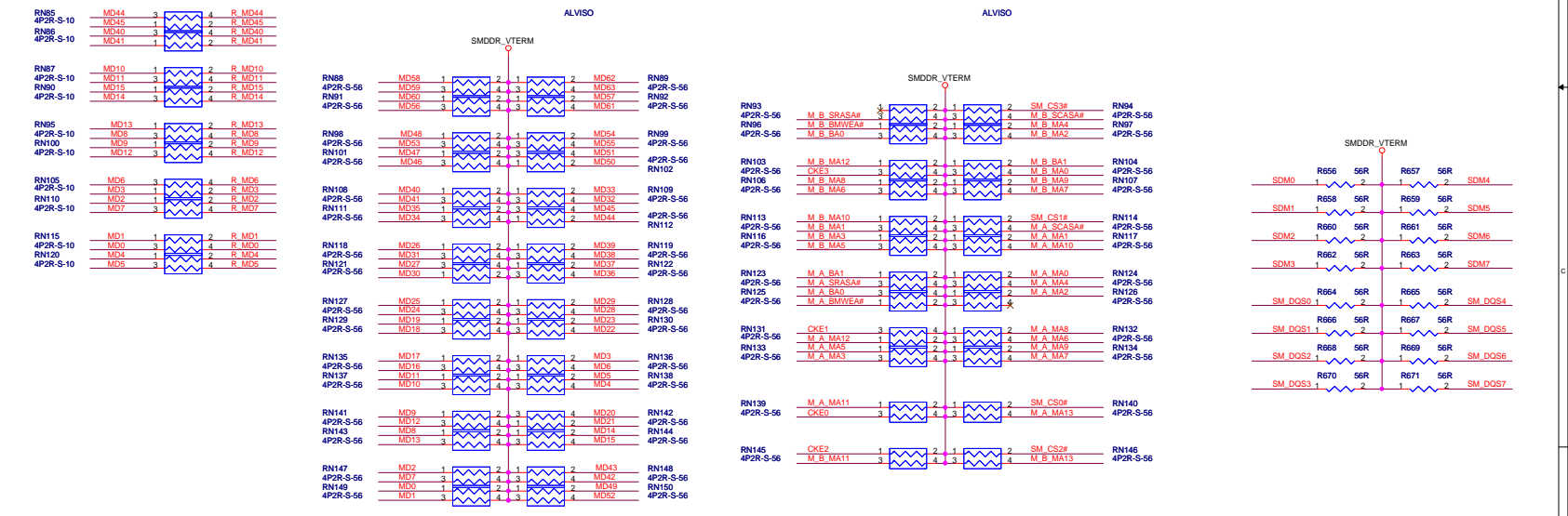
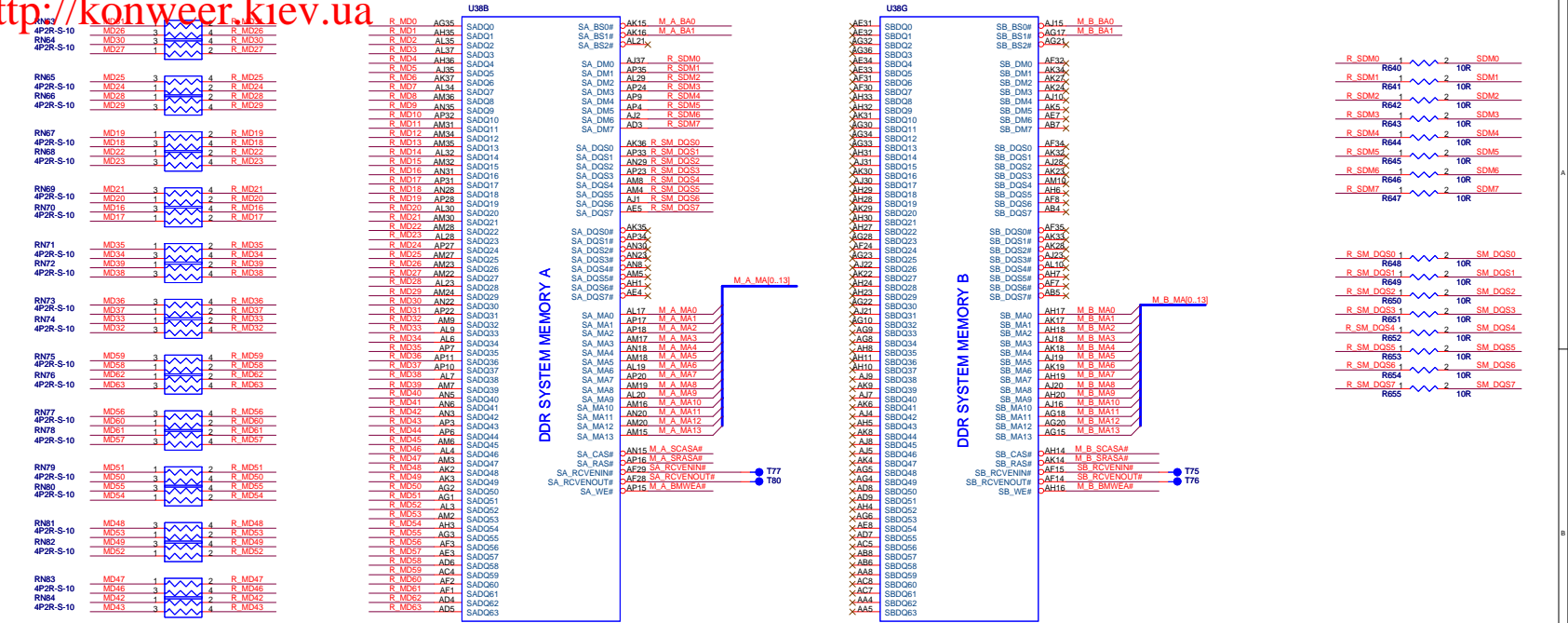
These pins can't leave as NC if we didn't use PCI-E on system cause it also used for DMI compensation.

CRT B R532 150/F
 CRT G R533 150/F
 CRT R R534 150/F
 Place near chip

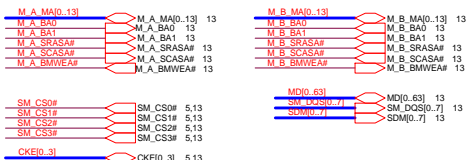
Strapping

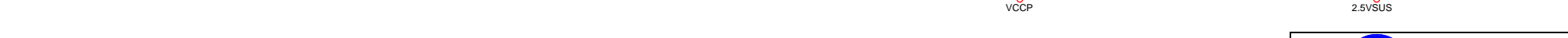
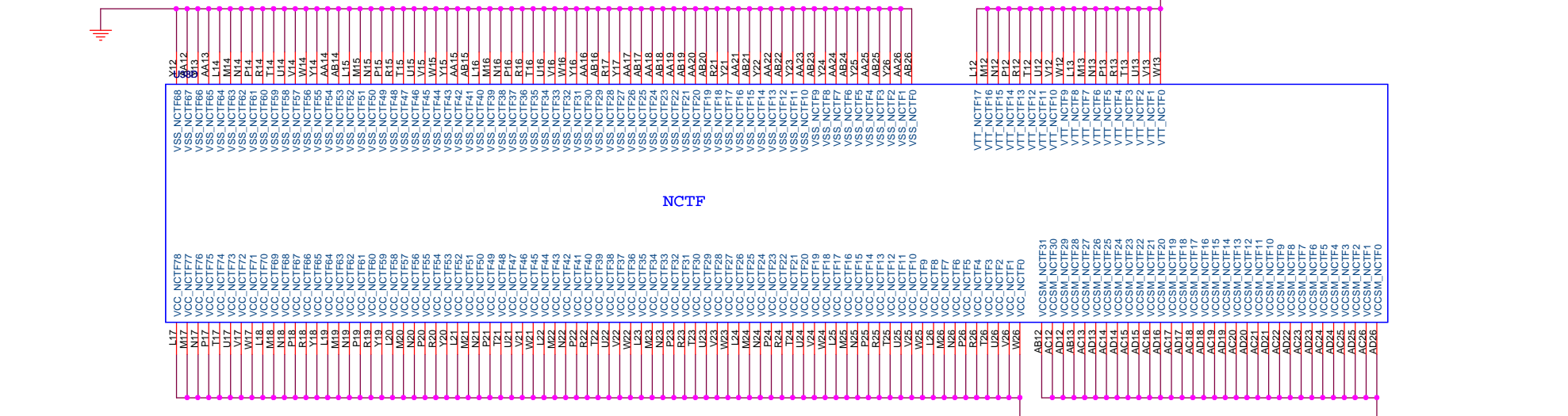
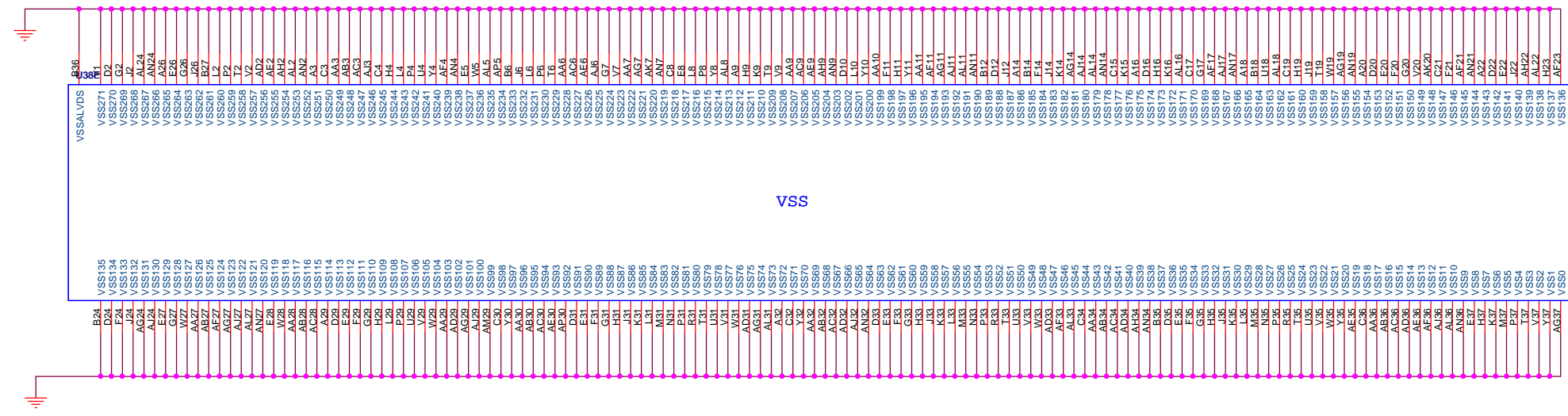



CFG[2:0]
 001=533MT/S FSB
 101=400MT/S FSB
 CFG[3:17] have internal pullup.
 CFG[18:19] have internal pulldown.



For terminal R-pack.

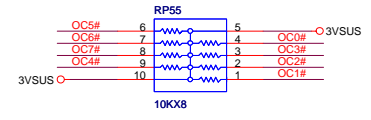
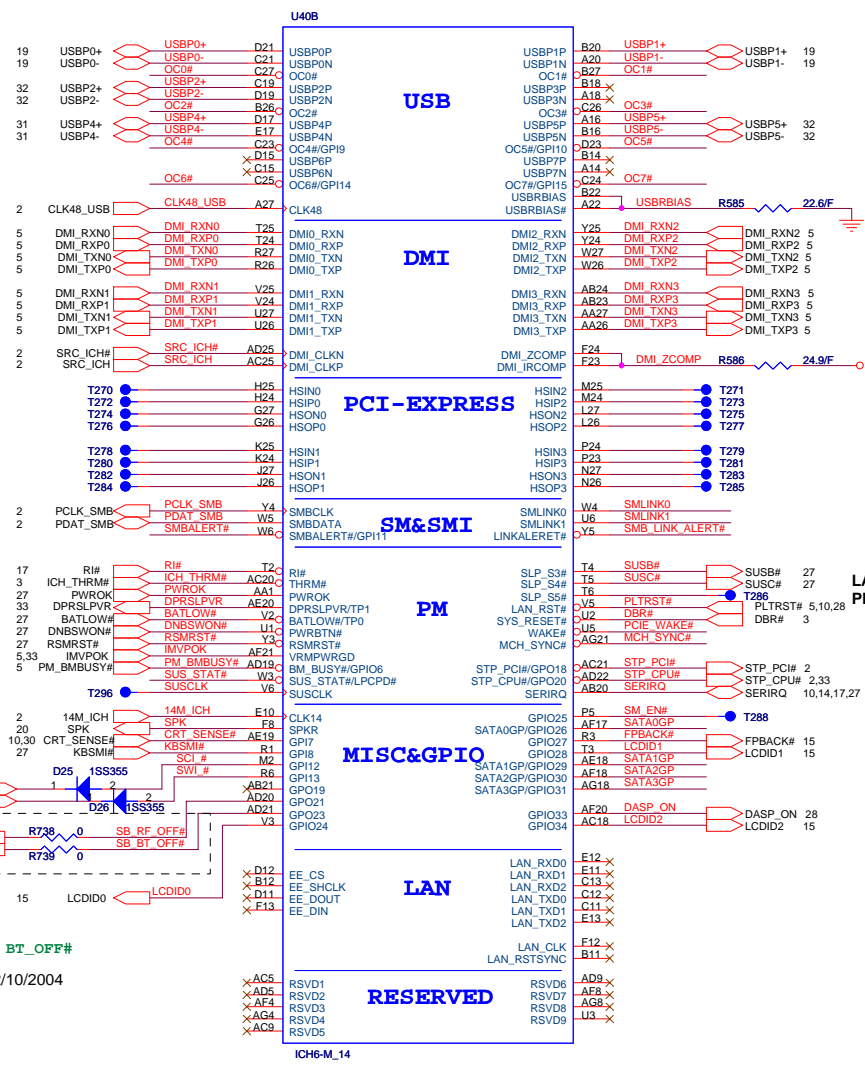
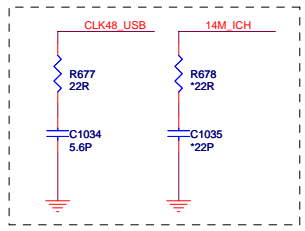






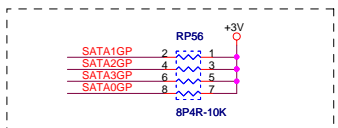
PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALVISO VSS/NCTF	1A
Date:	Monday, December 27, 2004	Sheet 9 of 39



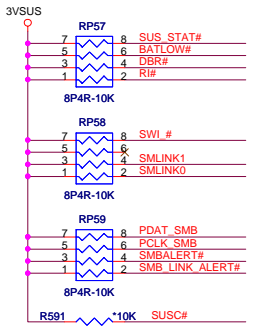
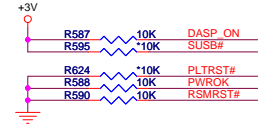
Place within 500mils of ICH-6

Place within 500mils of ICH-6

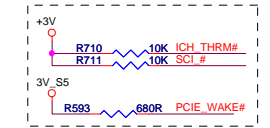


These signals should be pulled-up to +3V via a 8.2K-10K if didn't used as S-ATA interlock switch or GPI signals.

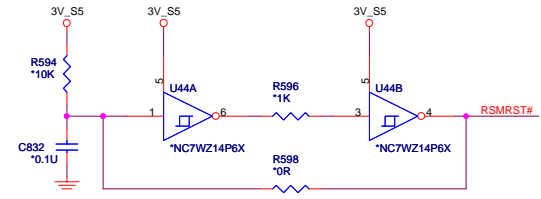
LAN_RST# should be connected to PLTRST# if internal LAN didn't use.



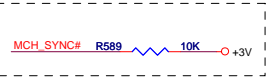
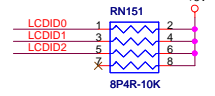
PV stage:
1. Add RF_OFF# and BT_OFF# circuit.
Griffey 12/10/2004



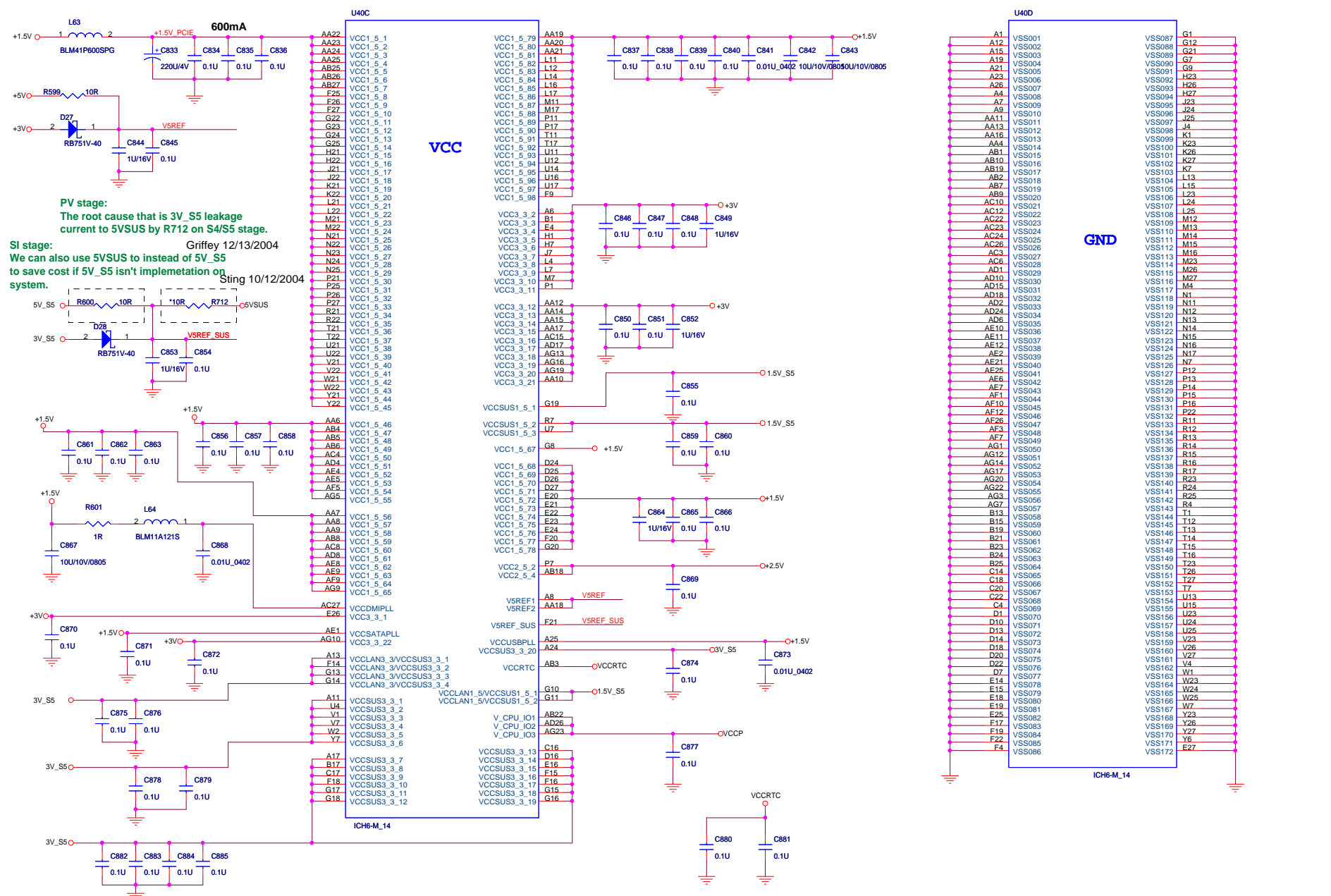
1. Change the power plane of PCIE_WAKE# from 3VSUS to 3V_S5 to solve system can't turn off issue.
2. Change the power plane of ICH_THRM# and SCTI_# from 3VSUS to +3V to solve leakage issue.
Sting 10/06/2004

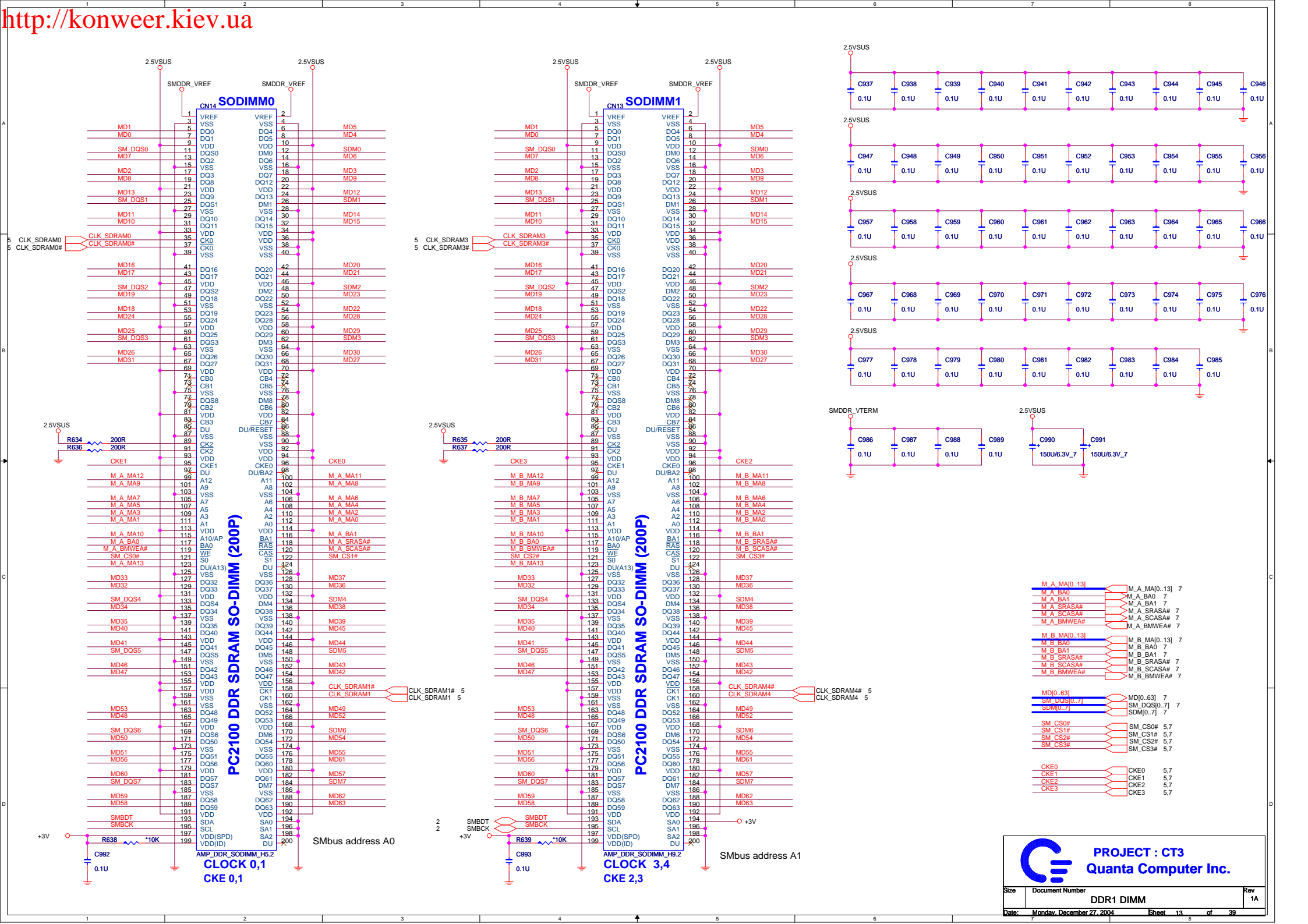


Enable Cable ID



SI stage:
R589 should be populated, because MCH_SYNC# is internally ANDed with PWROK.system will not booting without this pulled-up resistor.
Sting 09/24/2004





SODIMM0

SODIMM1

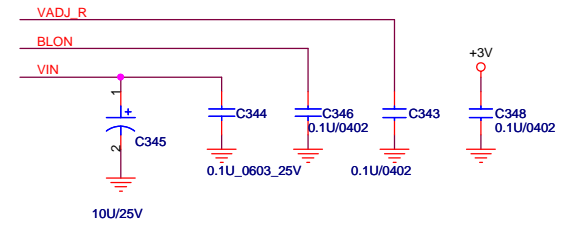
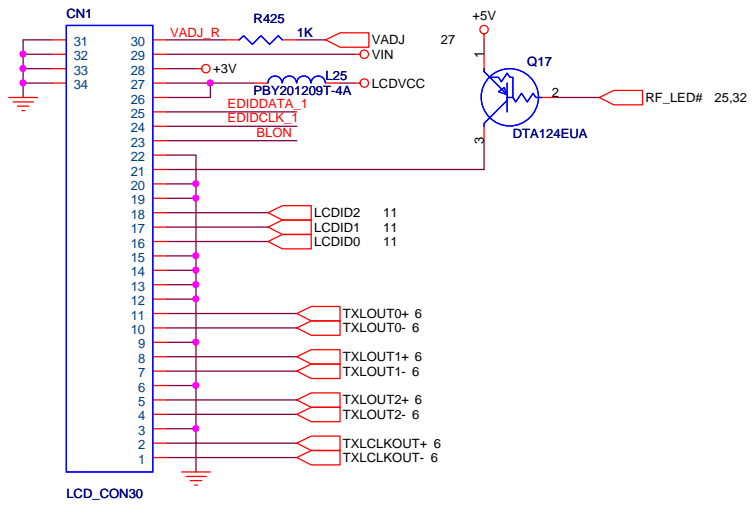
PC2100 DDR SDRAM SO-DIMM (200P)

PC2100 DDR SDRAM SO-DIMM (200P)

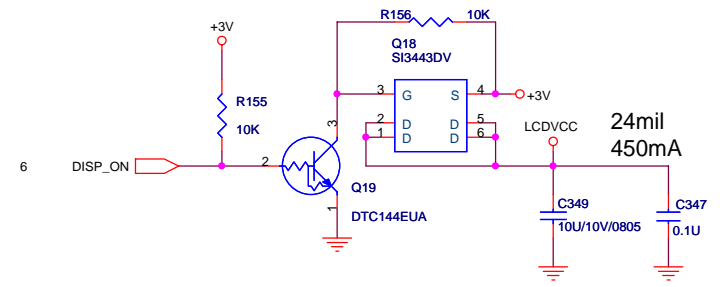
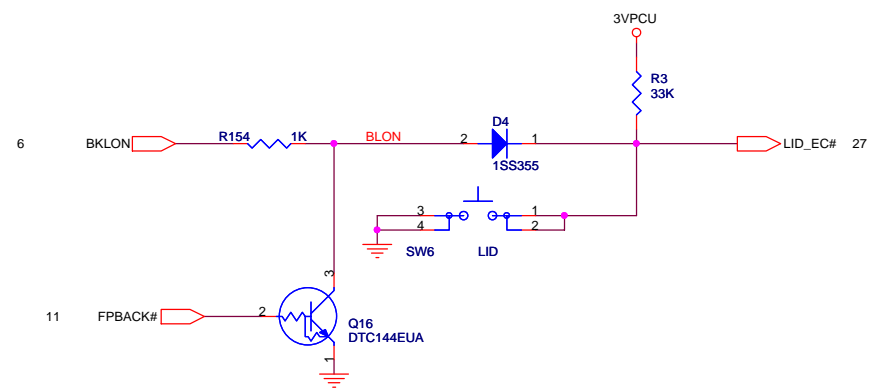
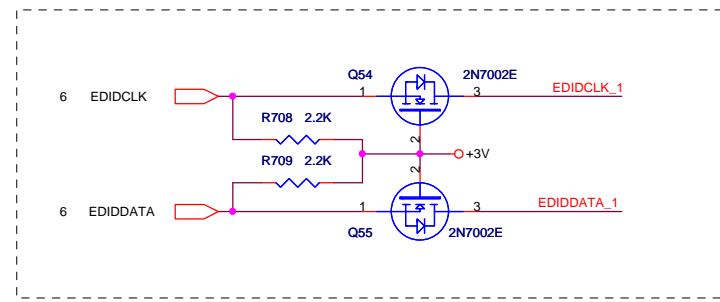
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- M A BA0 M A BA0 7
- M A BA1 M A BA1 7
- M A SRASA# M A SRASA# 7
- M A SCASA# M A SCASA# 7
- M A BMWEA# M A BMWEA# 7
- M B MA0[0..13] M B MA0[0..13] 7
- M B BA0 M B BA0 7
- M B BA1 M B BA1 7
- M B SRASA# M B SRASA# 7
- M B SCASA# M B SCASA# 7
- M B BMWEA# M B BMWEA# 7
- MD0[6,3] MD0[6,3] 7
- SM_DQS0[7] SM_DQS0[7] 7
- SDM0[7] SDM0[7] 7
- SM_CS0# SM_CS0# 5,7
- SM_CS1# SM_CS1# 5,7
- SM_CS2# SM_CS2# 5,7
- SM_CS3# SM_CS3# 5,7
- CKE0 CKE0 5,7
- CKE1 CKE1 5,7
- CKE2 CKE2 5,7
- CKE3 CKE3 5,7

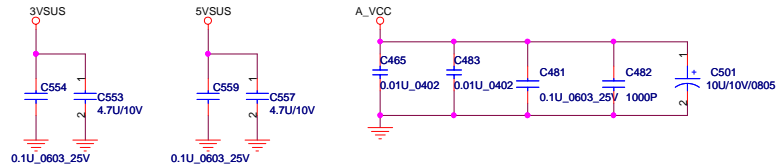
PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
	DDR1 DIMM	1A
Date:	Monday, December 27, 2004	Sheet 13 of 39



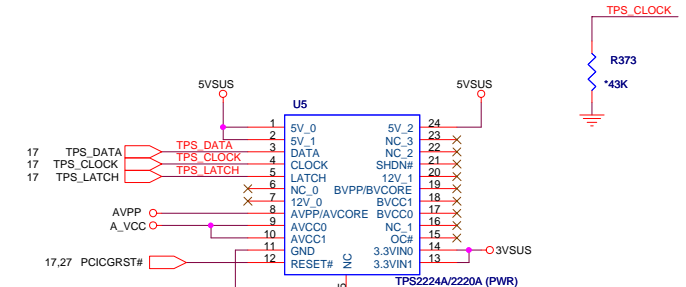
SI stage:
Add a level-shift circuit for EDID interface.
Sting 10/04/2004





CARDBUS POWER SWITCH

For PCI7411



For PCI1510

PV stage:
Remove unused PCI1510RVGF circuit.

Griffey 12/08/2004

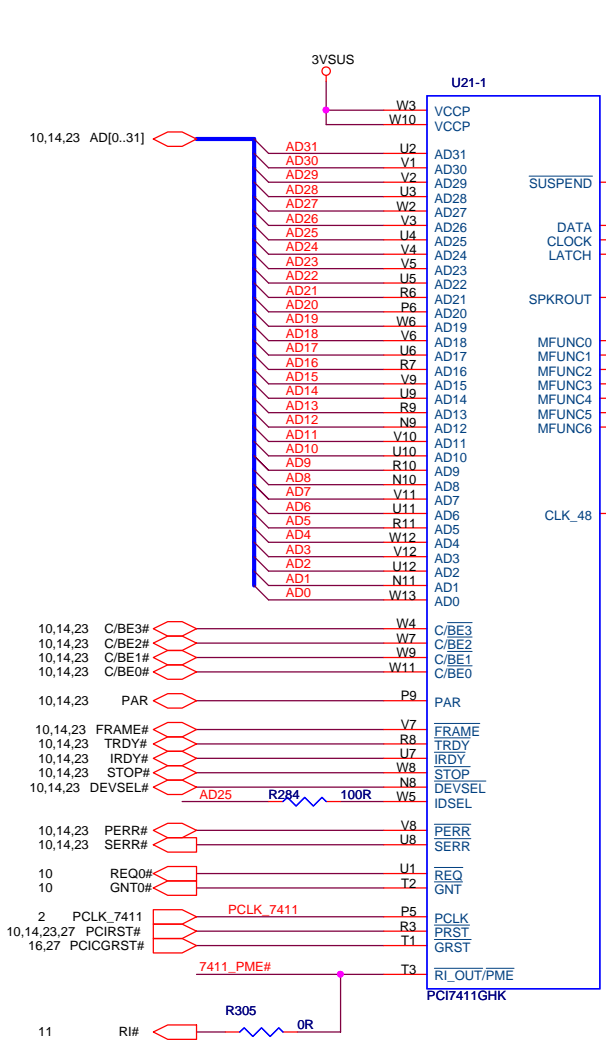
U21-3	U21-2
VCCB D19	VCCA A5
VCCB K19	VCCA A11
B_CAD31/B D10	A_CAD31/A D10
B_CAD30/B D9	A_CAD30/A D9
B_CAD29/B D8	A_CAD29/A D8
B_CAD28/B D8	A_CAD28/A D8
B_CAD27/B D0	A_CAD27/A D0
B_CAD26/B_A0	A_CAD26/A_A0
B_CAD25/B_A1	A_CAD25/A_A1
B_CAD24/B_A2	A_CAD24/A_A2
B_CAD23/B_A3	A_CAD23/A_A3
B_CAD22/B_A4	A_CAD22/A_A4
B_CAD21/B_A5	A_CAD21/A_A5
B_CAD20/B_A6	A_CAD20/A_A6
B_CAD19/B_A25	A_CAD19/A_A25
B_CAD18/B_A7	A_CAD18/A_A7
B_CAD17/B_A24	A_CAD17/A_A24
B_CAD16/B_A17	A_CAD16/A_A17
B_CAD15/B_IOWR	A_CAD15/A_IOWR
B_CAD14/B_A9	A_CAD14/A_A9
B_CAD13/B_IORD	A_CAD13/A_IORD
B_CAD12/B_A11	A_CAD12/A_A11
B_CAD11/B_OE	A_CAD11/A_OE
B_CAD10/B_CE2	A_CAD10/A_CE2
B_CAD9/B_A10	A_CAD9/A_A10
B_CAD8/B_D15	A_CAD8/A_D15
B_CAD7/B_D7	A_CAD7/A_D7
B_CAD6/B_D13	A_CAD6/A_D13
B_CAD5/B_D6	A_CAD5/A_D6
B_CAD4/B_D12	A_CAD4/A_D12
B_CAD3/B_D5	A_CAD3/A_D5
B_CAD2/B_D11	A_CAD2/A_D11
B_CAD1/B_D4	A_CAD1/A_D4
B_CAD0/B_D3	A_CAD0/A_D3
B_CC/BE3/B_REG	A_CC/BE3/A_REG
B_CC/BE2/B_A12	A_CC/BE2/A_A12
B_CC/BE1/B_A8	A_CC/BE1/A_A8
B_CC/BE0/B_CE1	A_CC/BE0/A_CE1
B_CPAR/A_A13	A_CPAR/A_A13
B_CFRAME/B_A23	A_CFRAME/A_A23
B_CTRDY/B_A22	A_CTRDY/A_A22
B_CIRDY/B_A15	A_CIRDY/A_A15
B_CSTOP/B_A20	A_CSTOP/A_A20
B_CDEVSL/B_A21	A_CDEVSL/A_A21
B_CBLOCK/B_A19	A_CBLOCK/A_A19
B_CPERR/B_A14	A_CPERR/A_A14
B_CSERR/B_WAIT	A_CSERR/A_WAIT
B_CREQ/B_INPACK	A_CREQ/A_INPACK
B_CGNT/B_WE	A_CGNT/A_WE
B_CSTSCHG/B_BVD1(STSCHG/R)	A_CSTSCHG/A_BVD1(STSCHG/R)
B_CCLKRUN/B_WP(OIS16)	A_CCLKRUN/A_WP(OIS16)
B_CCLK/B_A16	A_CCLK/A_A16
B_CINT/B_READY(IREQ)	A_CINT/A_READY(IREQ)
B_CRST/B_RESET	A_CRST/A_RESET
B_CAUDIO/B_BVD2(SPKR)	A_CAUDIO/A_BVD2(SPKR)
B_CCD1/B_CDT	A_CCD1/A_CDT
B_CCD2/B_CD2	A_CCD2/A_CD2
B_CVS1/B_VS1	A_CVS1/A_VS1
B_CVS2/B_VS2	A_CVS2/A_VS2
B_RSVD/B_D14	A_RSVD/A_D14
B_RSVD/B_D2	A_RSVD/A_D2
B_RSVD/B_A18	A_RSVD/A_A18

U21-2	U21-1
A5	A_VCC
A11	A_VCC
D1	A_D10
C1	A_D9
D3	A_D8
C2	A_D7
B1	A_D0
B4	A_A0
A4	A_A1
E6	A_A2
B5	A_A3
C6	A_A4
B6	A_A5
G9	A_A6
C7	A_A25
B7	A_A7
A7	A_A24
A10	A_A17
E11	A_IOWR#
G11	A_A9
C11	A_IORD#
B11	A_A11
C12	A_OE#
B12	A_CE2#
E12	A_A10
C13	A_D7
M15	A_D13
A13	A_D8
C14	A_D12
E13	A_D5
A14	A_D11
A14	A_D4
E14	A_D3
C5	A_REG#
F9	A_A12
B10	A_A8
G12	A_CE1#
G10	A_A13
C8	A_A23
A8	A_A22
B8	A_A15
A9	A_A20
C9	A_A21
E10	A_A19
A14	A_A14
A14	A_WAIT#
B3	A_INPACK#
E7	A_INPACK#
B9	A_WE#
B2	A_STSCHG_P
C3	A_OIS16#
E9	A_A16
C4	A_IREQ#
A6	A_RESET
A2	A_SPKR_P
C15	A_CD1#
E5	A_CD2#
A3	A_VS1#
E8	A_VS2#
B13	A_D14
D2	A_D2
C10	A_A18

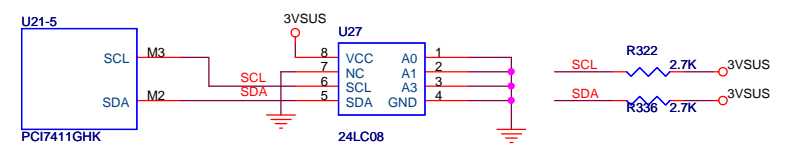
U21-1	U21-2	U21-3	U21-4
A_D3	2	SKTAA0/D3	
A_D4	3	SKTAA1/D4	
A_D11	37	SKTAA2/D11	
A_D5	4	SKTAD3/D5	
A_D12	38	SKTAD4/D12	
A_D6	5	SKTAD5/D6	
A_D13	39	SKTAD6/D13	
A_D7	6	SKTAD7/D7	
A_D15	41	SKTAD8/D15	
A_D10	8	SKTAD9/D10	
A_OE#	9	SKTAA10/OE#	
A_A11	10	SKTAA11/A11	
A_IORD#	44	SKTAA12/IORD#	
A_A17	45	SKTAA13/IORD#	
A_IOWR#	11	SKTAA14/A9	
A_A9	46	SKTAA15/IOWR#	
A_A24	55	SKTAA16/A17	
A_A7	22	SKTAA17/A24	
A_A6	56	SKTAA18/A7	
A_A5	24	SKTAA19/A25	
A_A4	25	SKTAA20/A6	
A_A3	27	SKTAA21/A5	
A_A2	23	SKTAA22/A4	
A_A1	28	SKTAA23/A3	
A_A0	29	SKTAA24/A2	
A_D0	30	SKTAA25/A1	
A_D8	64	SKTAA26/A0	
A_D1	31	SKTAA27/D0	
A_D9	65	SKTAA28/D8	
A_D10	66	SKTAA29/D1	
A_D10	66	SKTAA30/D9	
A_D10	66	SKTAA31/D10	
A_CE1#	7	SKTACBE0/CE1#	
A_A8	12	SKTACBE1/A8	
A_A12	21	SKTACBE2/A12	
A_REG#	61	SKTACBE3/REG#	
A_A23	19	SKTAPCLK/A16	
A_A15	20	SKTAFRAME/A23	
A_A22	53	SKTATRDIY/A15	
A_A21	50	SKTATRDIY/A22	
A_A20	49	SKTADVSEL/A21	
A_A13	13	SKTASTOP/A20	
A_A14	23	SKTAPARA/A13	
A_WAIT#	14	SKTAPERR/A14	
A_INPACK#	60	OSKTASERR/WAIT#	
A_WE#	15	SKTAREQ/INPACK#	
A_IREQ#	16	SKTAGNT/WE#	
A_A19	48	SKTALOCK/A19	
A_OIS16#	33	SKTACLKRUN/WP	
A_RESET	58	SKTARST/RESET	
A_D14	40	SKTARSVD/D14	
A_A18	47	SKTARSVD/A18	
A_VS1#	43	SKTAVS1/VS1#	
A_VS2#	57	SKTAVS2/VS2#	
A_CD1#	36	SKTACD1/CD1#	
A_CD2#	62	SKTACD2/CD2#	
A_SPKR_P	67	SKTAAUDIO/BVD2	
A_STSCHG_P	63	SKTASTSCHG/BVD1	
A_D2	32	SKTARSVD/D2	

CARDBUS SLOT

FOX=WZ21131-G2



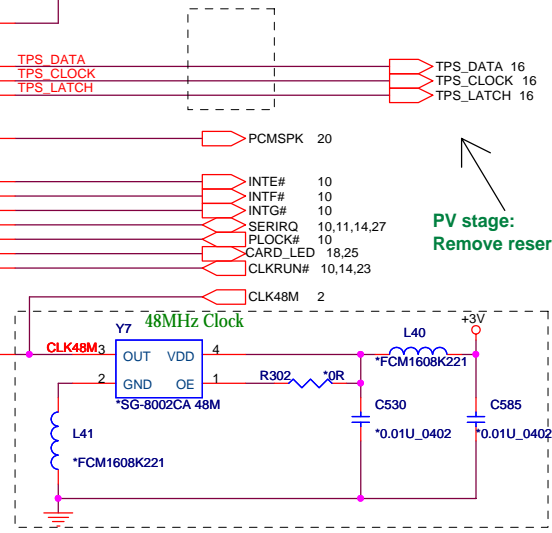
SI stage:
Remove reserve resistor R693~R695 for
PC11510RVGF
Sting 09/24/2004



PV stage:
Remove R701 & R702 for unused PCI1510RVGF
circuit.
Griffey 12/10/2004

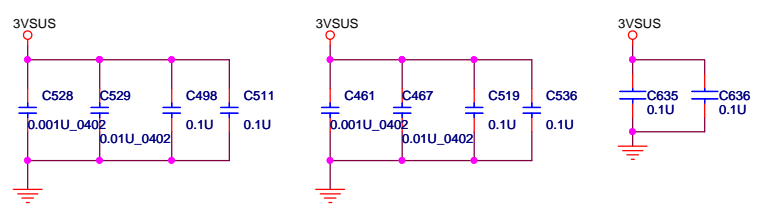
When -VCCD0 and -VCCD1 asserted high,
PLOCK# and INTF# will provide a SDA
signaling for I2C bus, PLOCK# will provide a
SCL signaling for I2C bus.

PV stage:
Remove reserve related circuit for PCI1510RVGF.
Griffey 12/08/2004

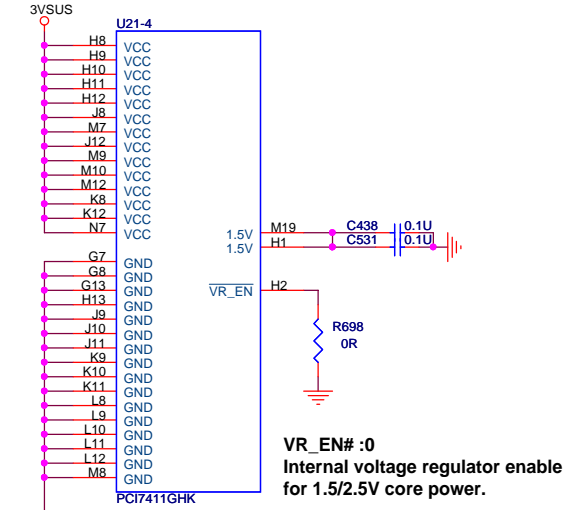


SI stage:
Remove all component of PLL circuit and Add
CLK48M input from CKG.

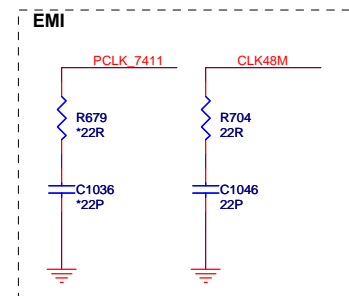
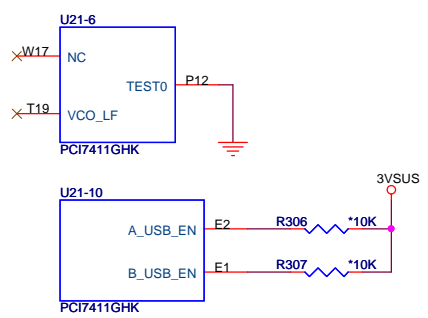
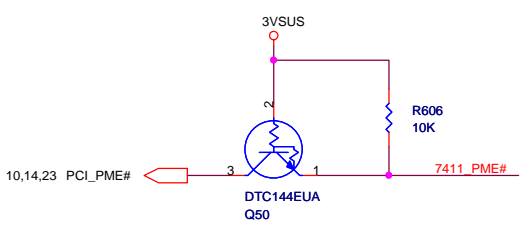
Sting 10/12/2204



PCIXX21 Power Terminals

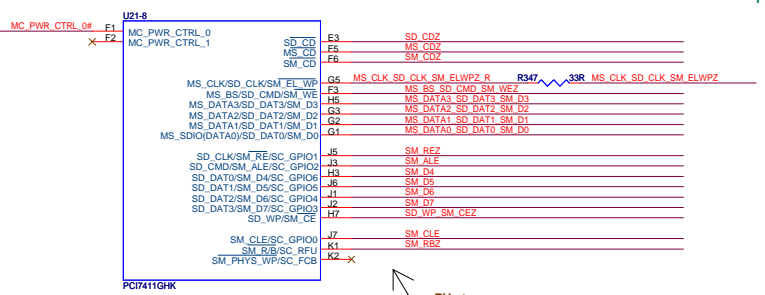


VR_EN# :0
Internal voltage regulator enable
for 1.5/2.5V core power.



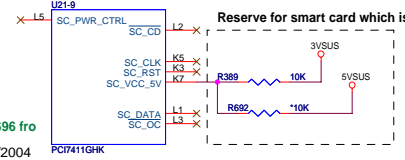
PV stage:
Populate R704 and C1045 for getting better
EMI performance.
Sting 11/19/2004

CARD POWER CONTROL



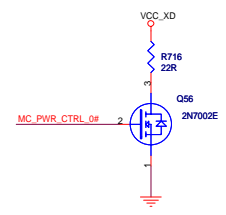
PV stage:
Remove reserve related circuit for
PCI1510RVGF.
Griffey 12/08/2004

SI stage:
Remove reserve resistor R696 fro
PCI1510RVGF.
Sting 10/12/2004

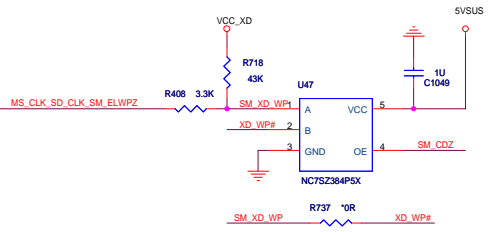


Reserve for smart card which is powered by 5V.

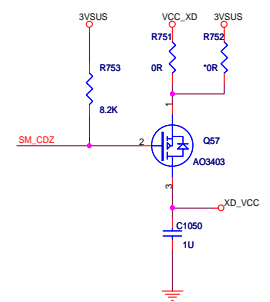
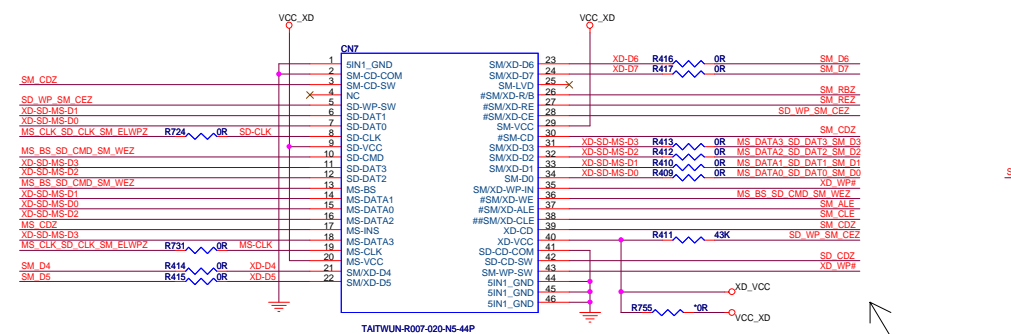
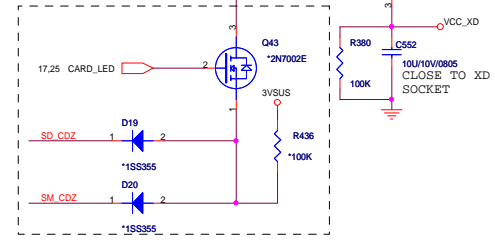
PV stage:
Add a discharge circuit for media
card power.
Sting 11/19/2004



PV stage:
1. Disconnect SM_PHYS_WP.
2. Tie SM_EL_WP with SM_PHYS_WP of SM card to allow
for normal operation of SD and SM.
Sting 11/19/2004



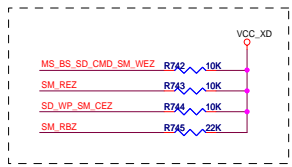
PV stage:
1. Add quick switch circuit.
Griffey 12/10/2004

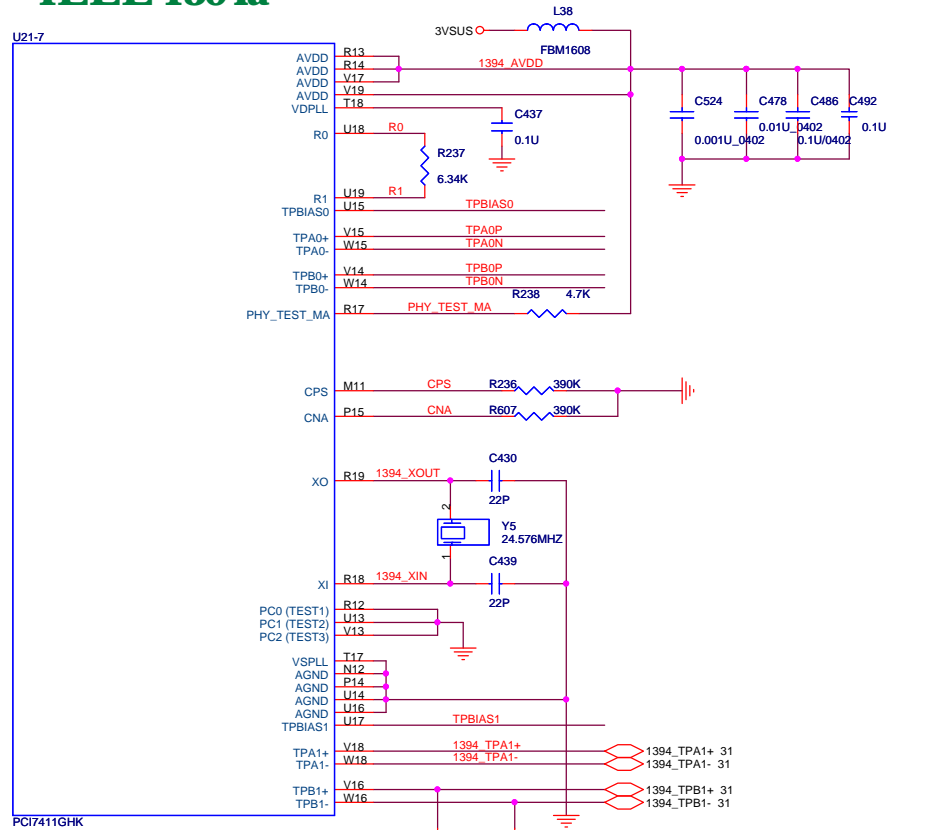


5 IN1 CARD READER

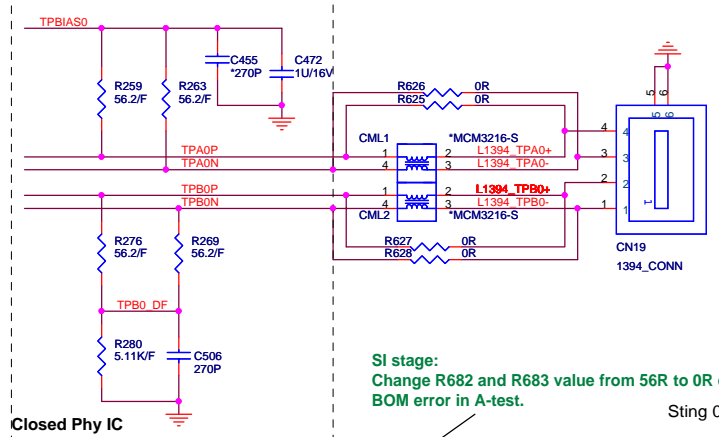
PV stage:
1. Add pull-up circuit.
Griffey 12/20/2004

PV stage:
1. Add R717 to solve SM card can't write protect issue.
2. Add R718 to solve cross-talk issue of MS-PRO card.
3. Add R719-R736 as terminal on all multi-funtion pin.
Sting 11/19/2004





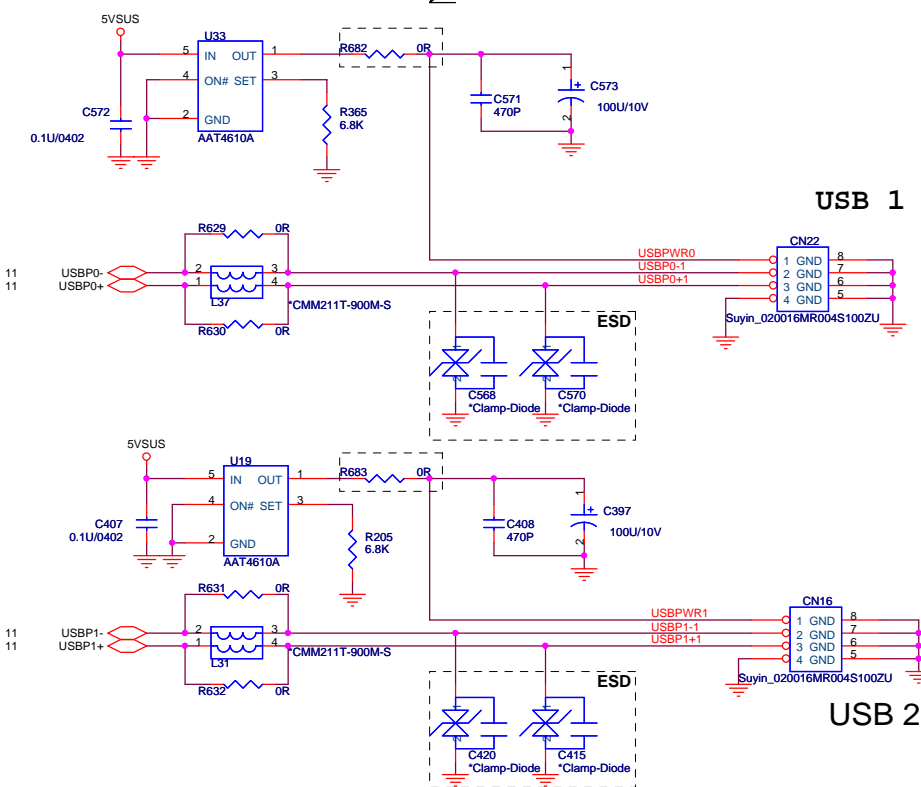
IEEE 1394 CONNECTOR



SI stage:
Change R682 and R683 value from 56R to 0R cause of BOM error in A-test.

Sting 09/24/2004

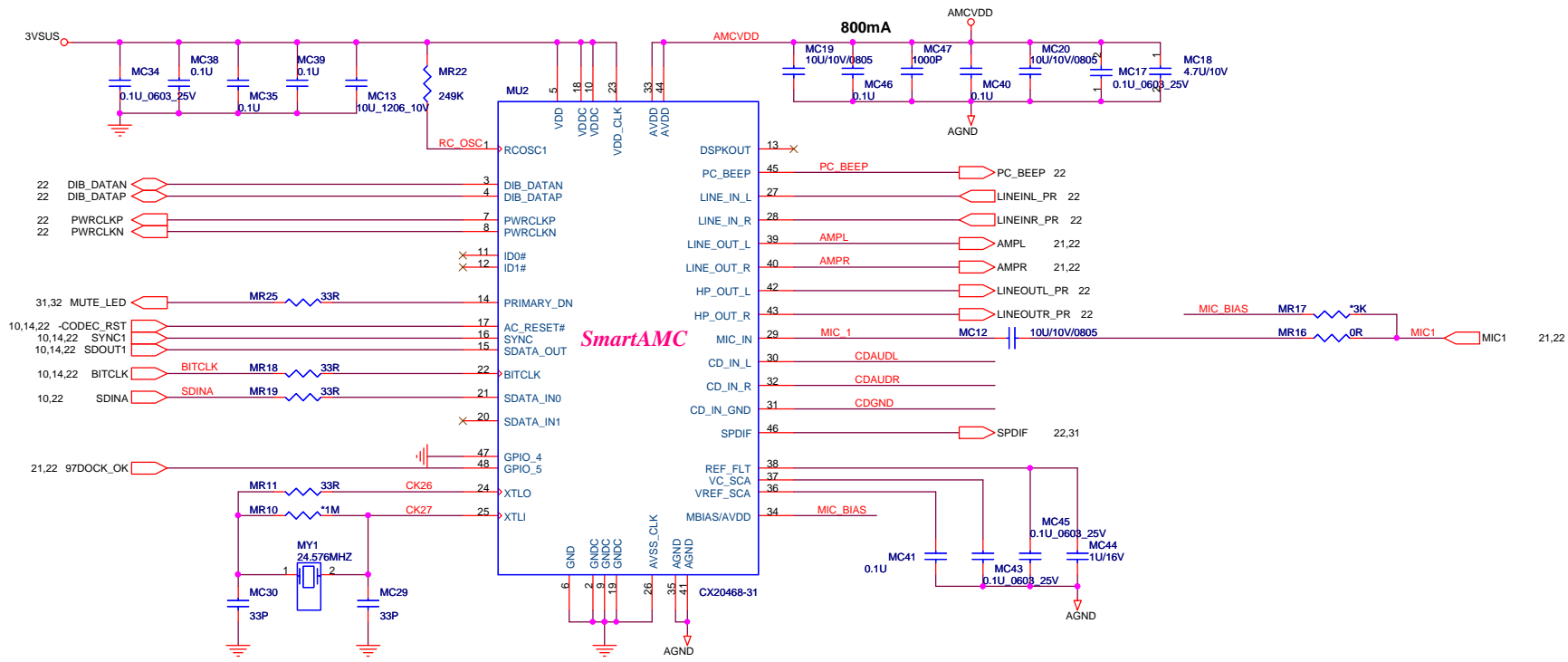
Closed Phy IC



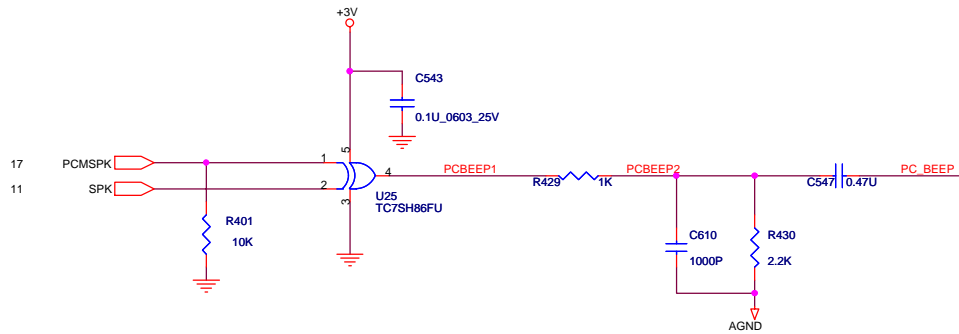
USB 1

USB 2

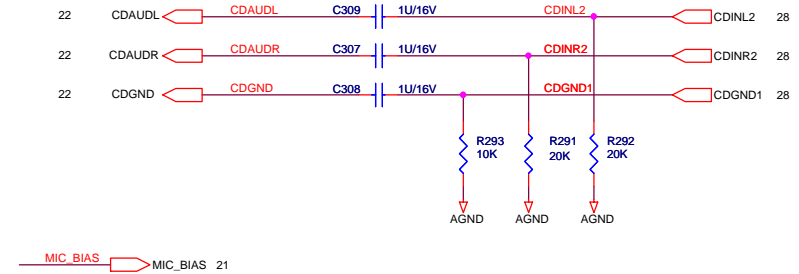
The AMC20493-001 modem is used for mother board family MBAMC20493-010.



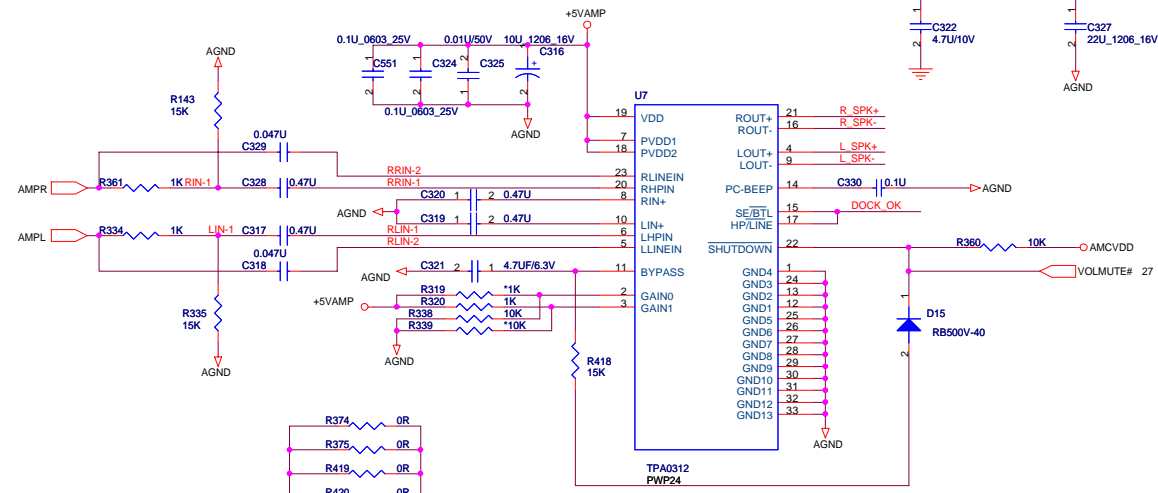
PC SPEAKER



FROM CD-ROM



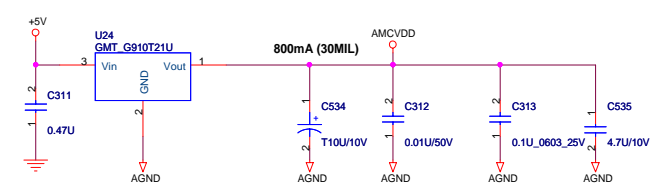
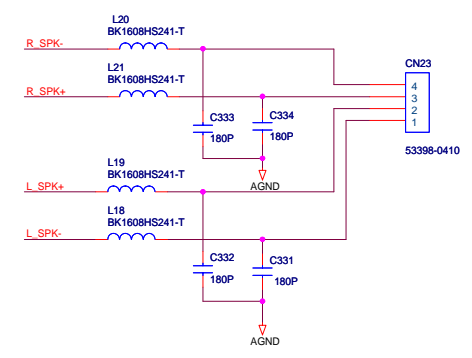
AUDIO AMPLIFIER



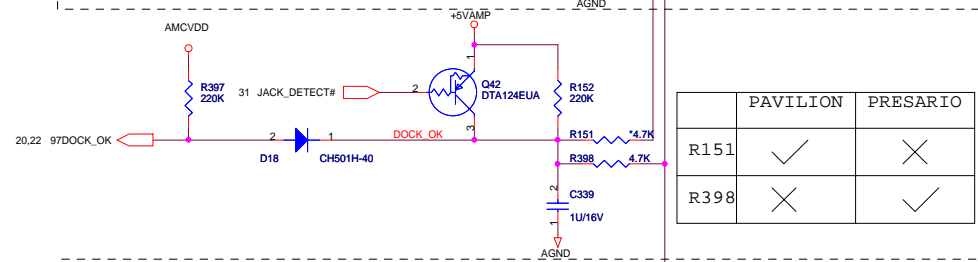
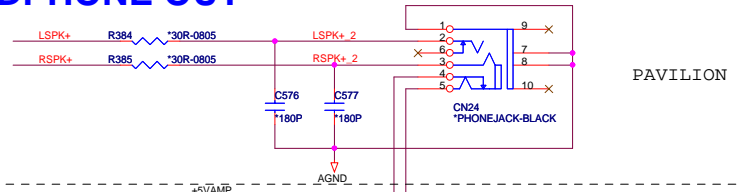
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

SPEAKER OUT

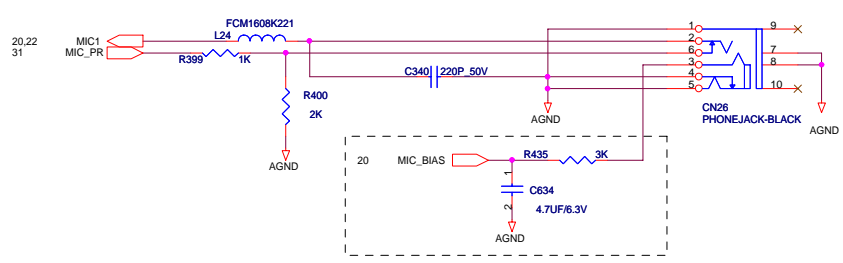


2ND HEADPHONE OUT

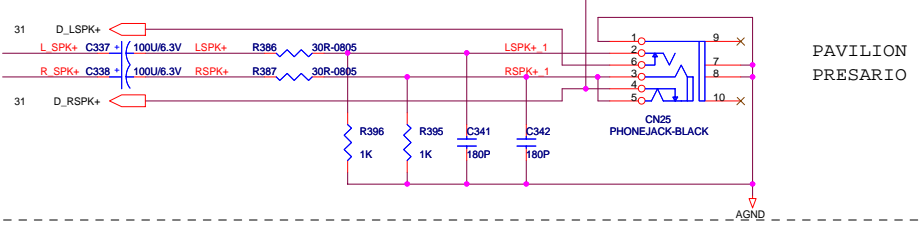


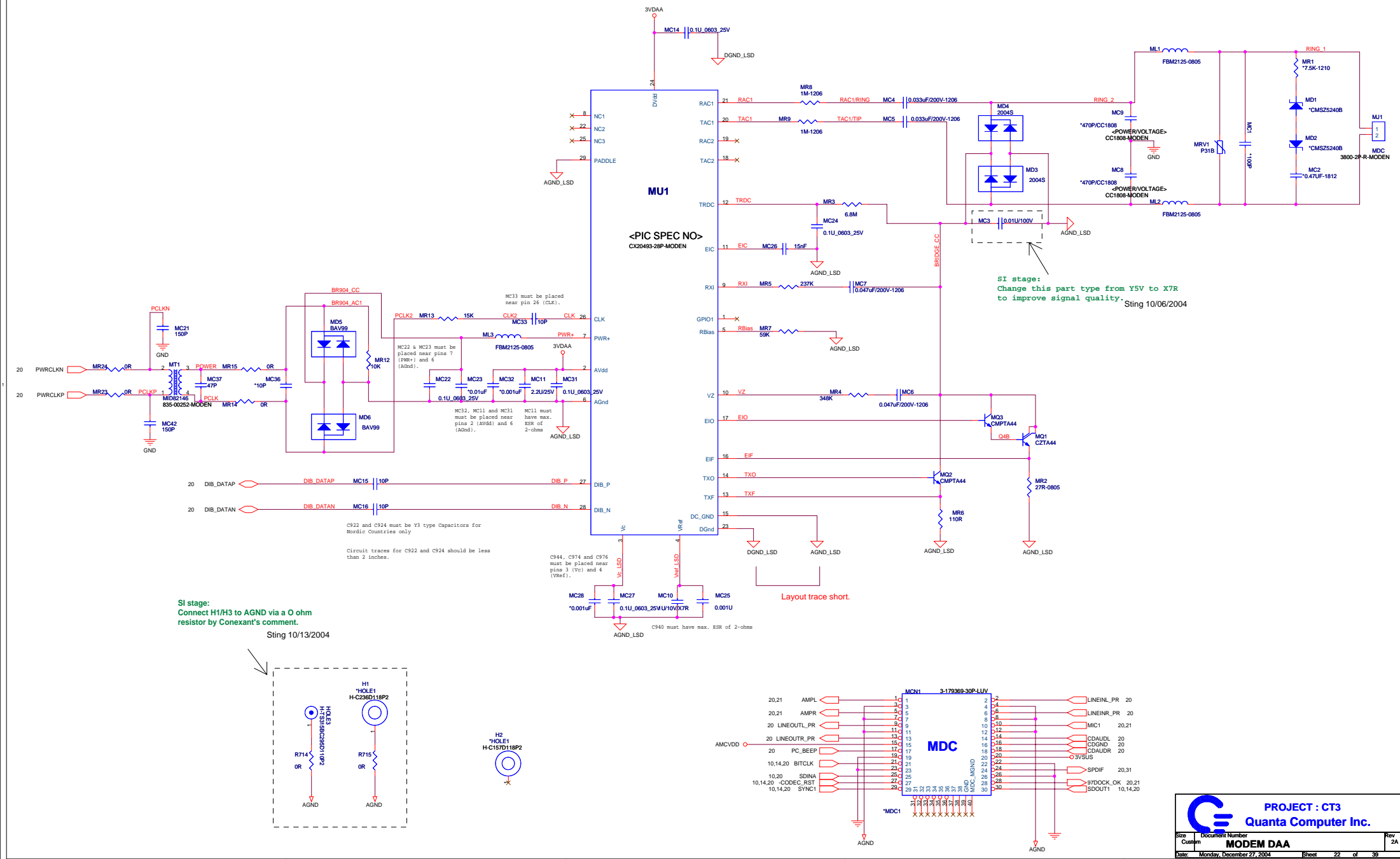
	PAVILION	PRESARIO
R151	✓	✗
R398	✗	✓

MICROPHONE



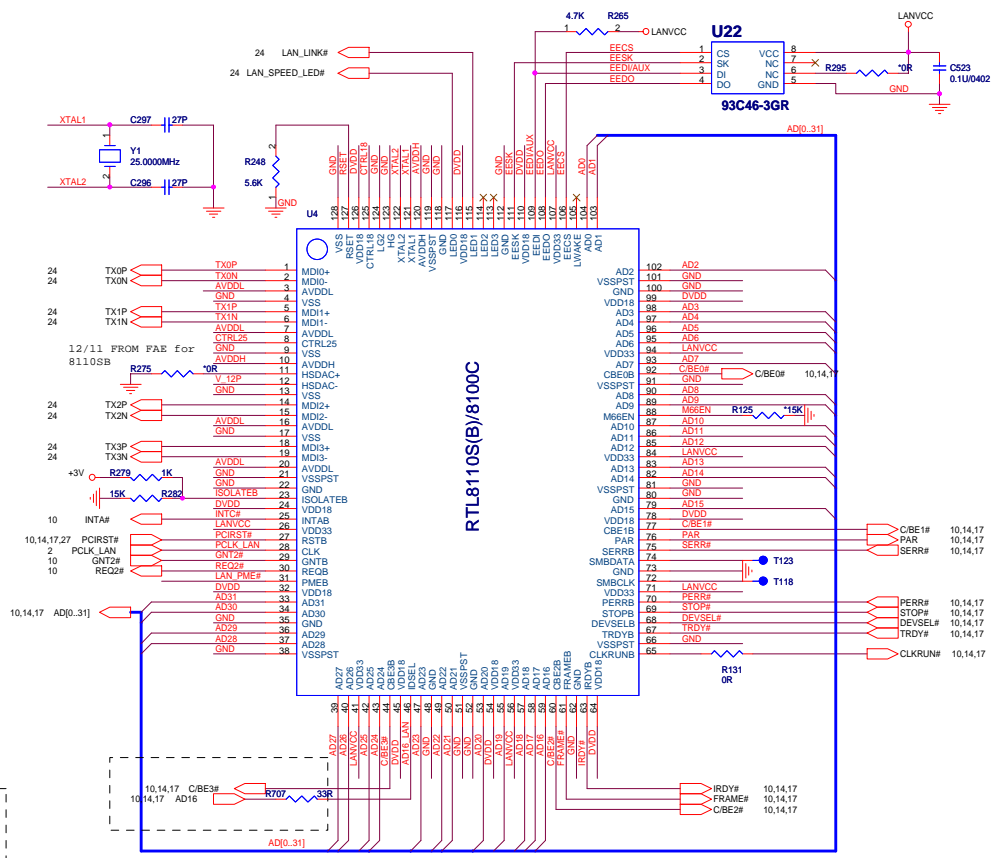
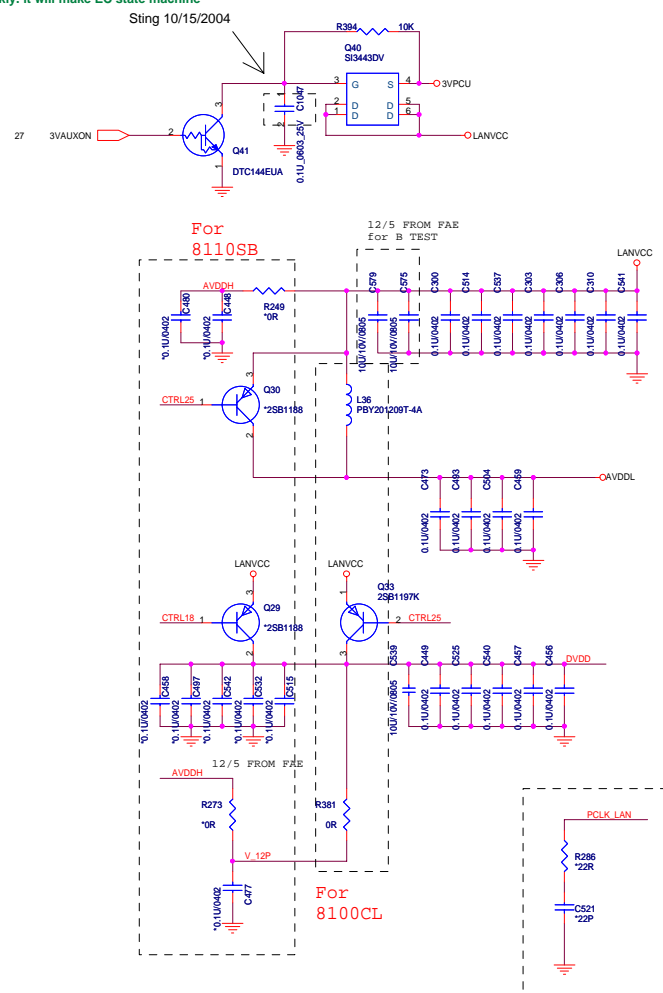
HEADPHONE OUT



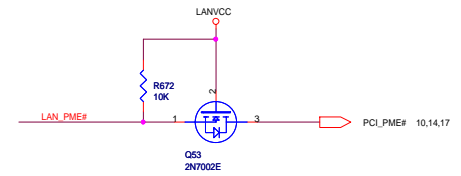


	8100CL(10/100M)	8110SB(1G)
DVDD33	3.3VD 26,41,56,71,84,94,107	3.3VD 26,41,56,71,84,94,107
AVDDL	3.3VA 3,7,20	2.5VA 3,7,20,16
DVDD	2.5VD 32,54,78,99	1.8VD 32,54,78,99,24,45,64,110,116,126
AVDD25	2.5VA 12	NC
AVDDH	NC	3.3VA 10,120

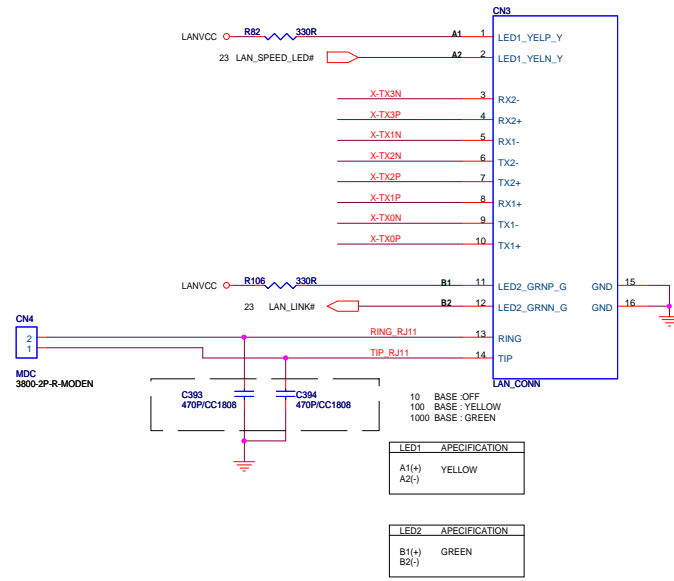
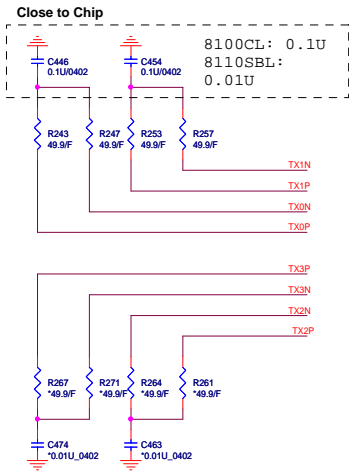
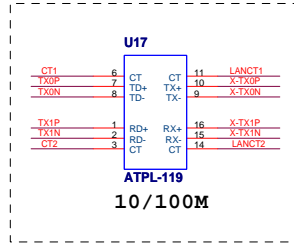
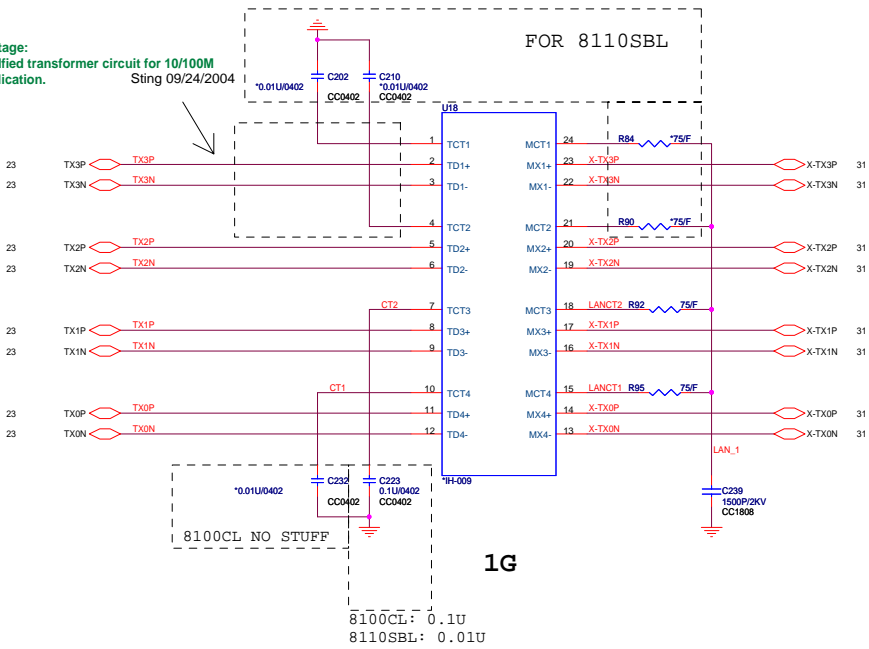
SI stage:
Add a 0.1uF to make Q40 turn on slowly, because 3VPCU will drop when LANVCC turned on quickly. it will make EC state machine crazy.

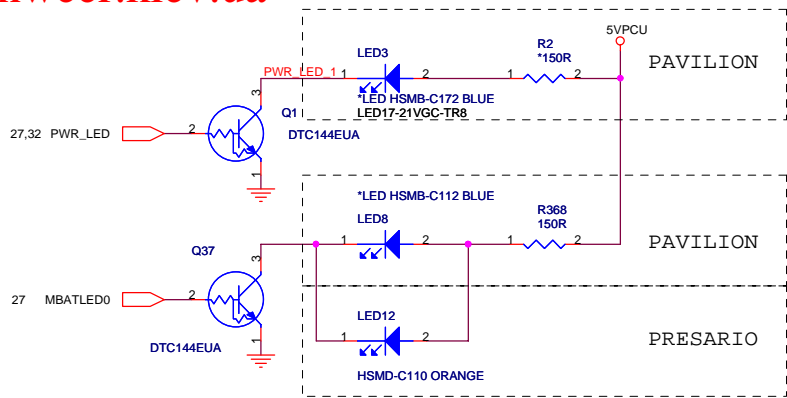


SI stage:
Add R707 for ID selection of Lan controller.

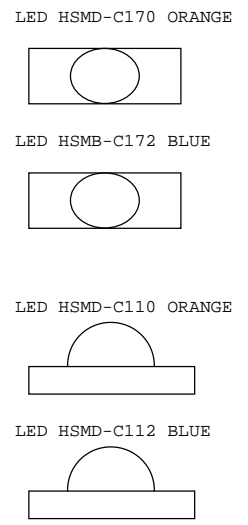
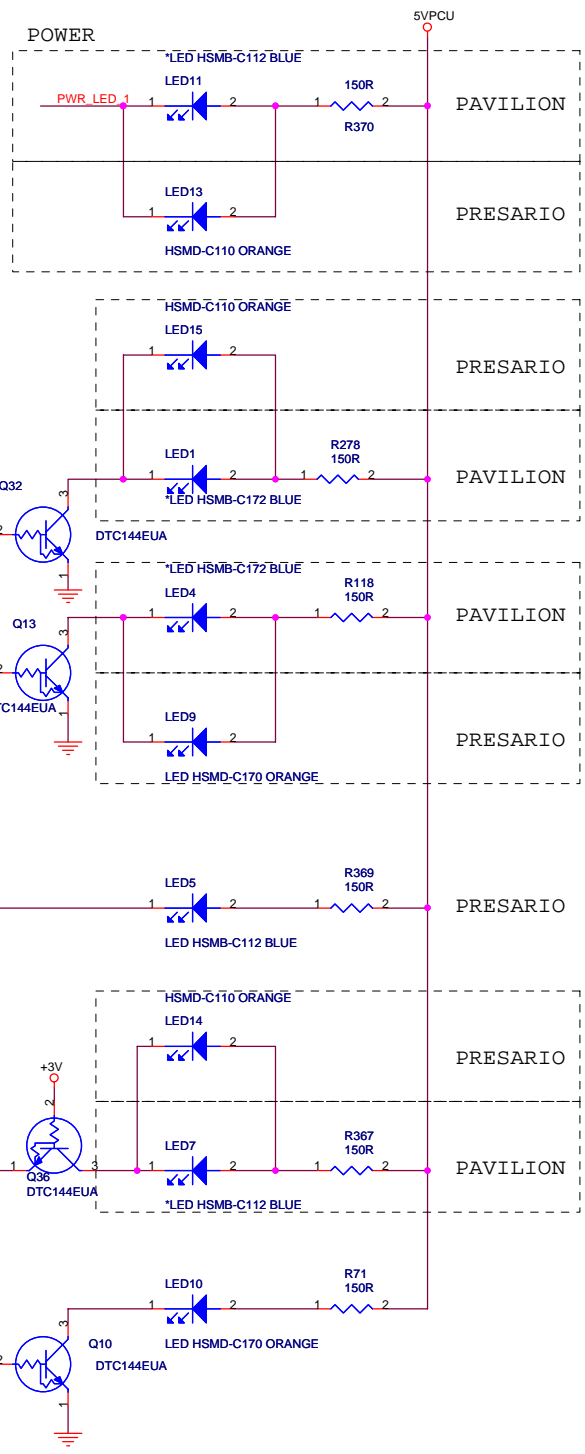
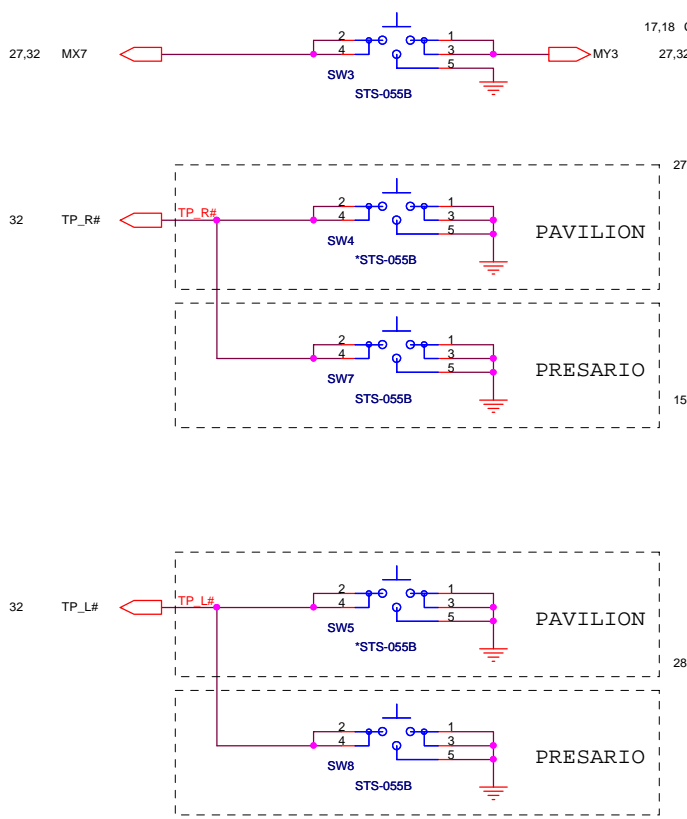


SI stage:
Modified transformer circuit for 10/100M application.
Sting 09/24/2004

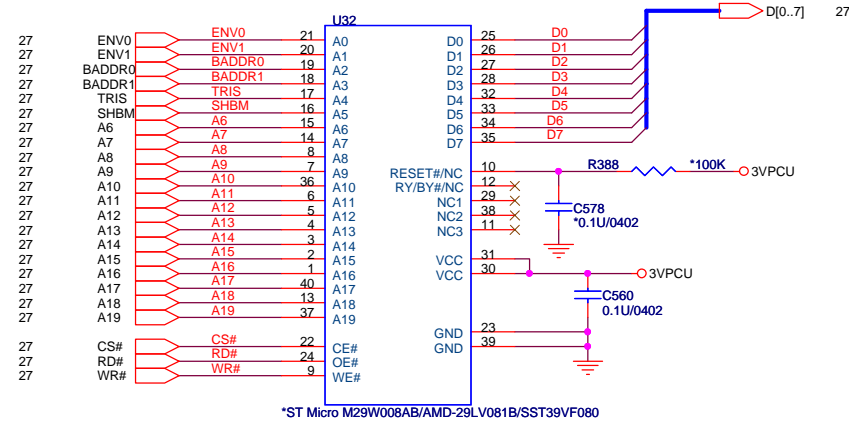




Touchpad control



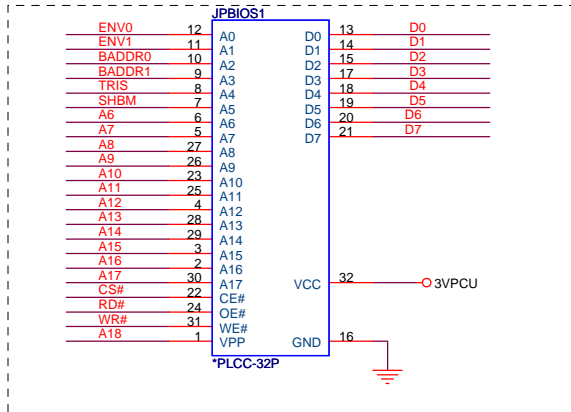
8Mbit (1M Byte), TSSOP40



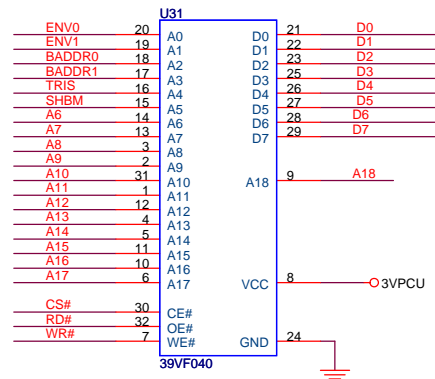
1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326 UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
 2.SIO has internal 20 mS delay of VCC1_PWROK

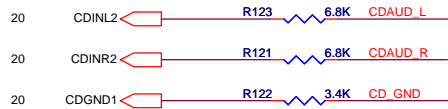
AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
 SST :Pin10,12 are NC

SI stage:
 Add PLCC32 cause of it is convenient for Bios debugging.
 Sting 10/01/2004

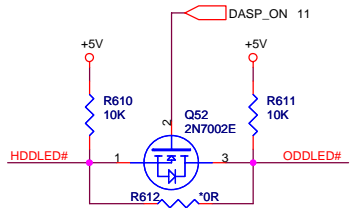
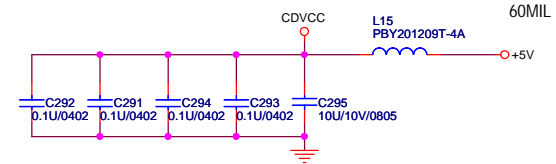
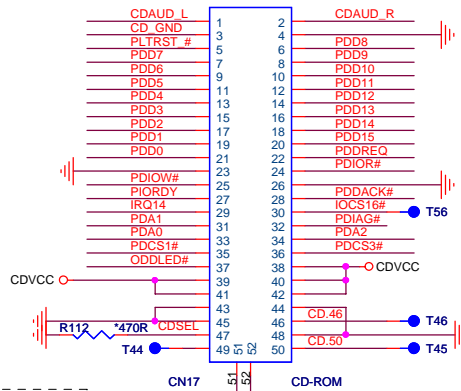


4Mbit (512k Byte), TSSOP32



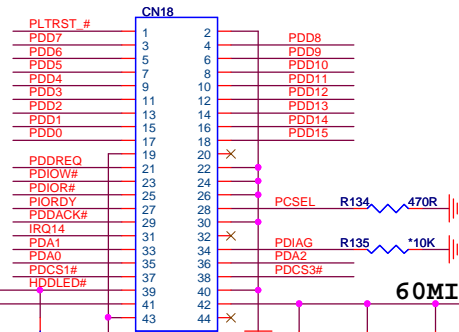
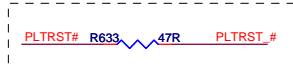
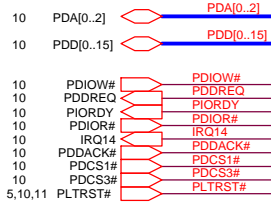


CD-ROM



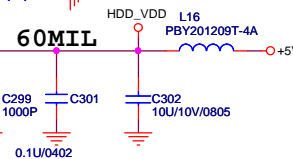
ADD DASP_ON FOR IDE CABLE SELECT

CDSEL
--> NC, Slave device
--> Low, Master device

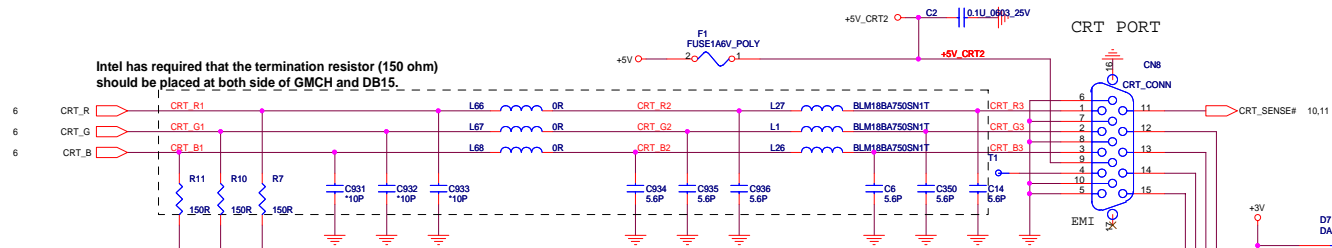


PCSEL
--> NC, Slave device
--> Low, Master device

HDD CONNECTOR



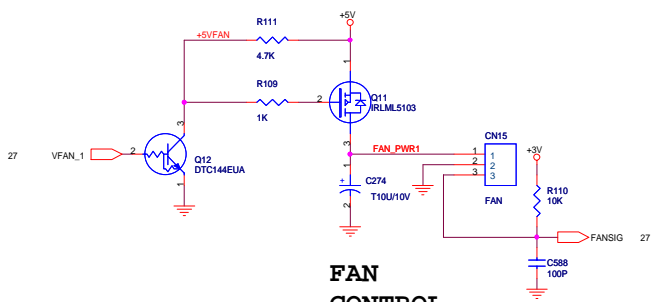
Intel has required that the termination resistor (150 ohm) should be placed at both side of GMCH and DB15.



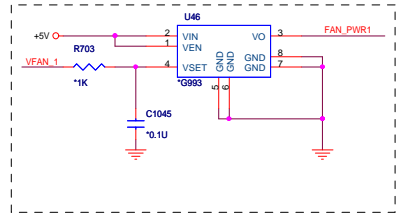
PV stage: Adjust Capacitors and Bead to improve CRT timing issue.

Griffey 12/09/2004

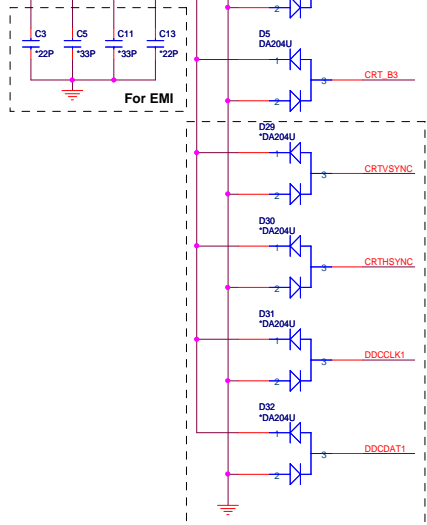
FAN CONTROL



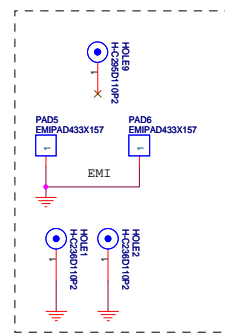
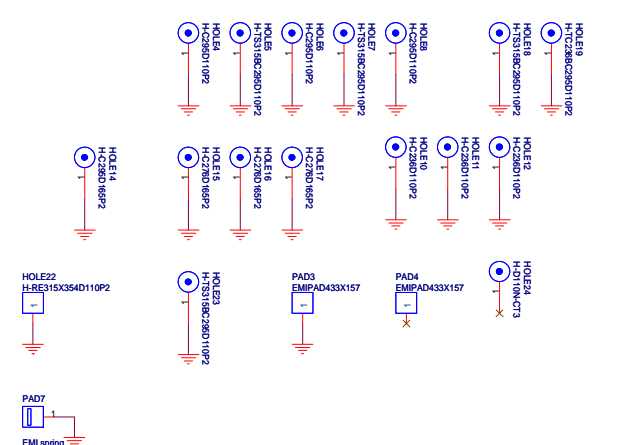
SI stage: Add GMT solution for B-test to costdown. Sting 09/24/2004

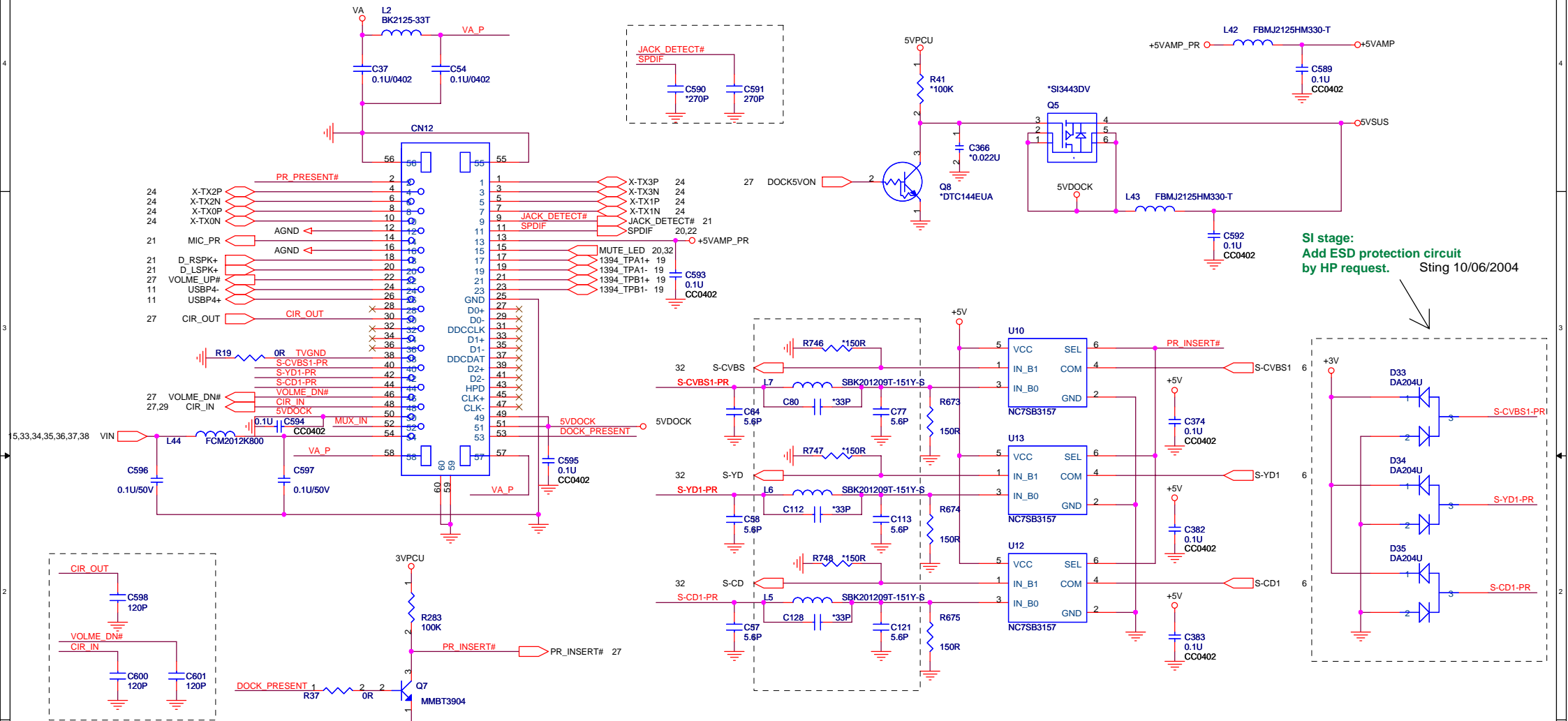


For EMI



Add ESD protection by Sting 08/03/2004





SI stage:
Add ESD protection circuit
by HP request. Sting 10/06/2004

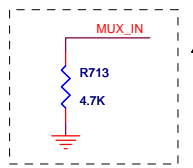
PV stage:
1. Change L5,L6,L7,C57,C58,C64,C77,C113,C121 value to improve S-video quality.
2. Reserve S-video impedance match circuit.

SEL	FUNCTION (COM)
HIGH	IN_B1

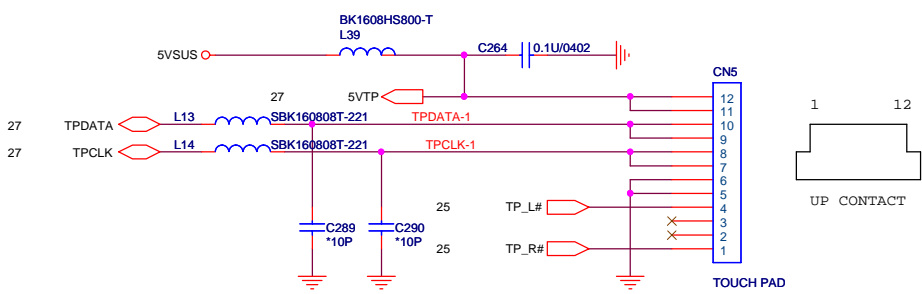
Griffey 12/22/2004

SI stage:
Add R713 to enable the mux in the Tampa-2 cable.
(connects the component TV output to the composite/Svideo output lines).

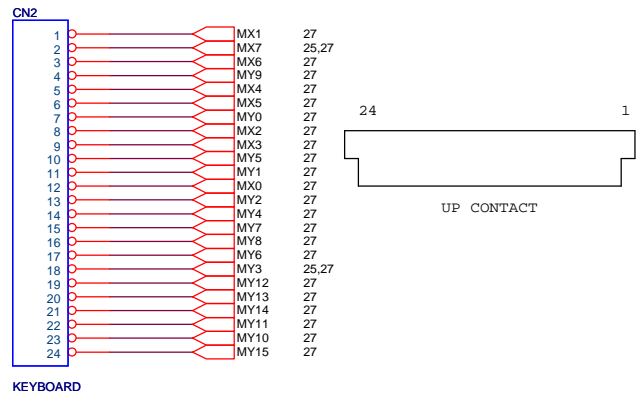
Sting 10/12/2004



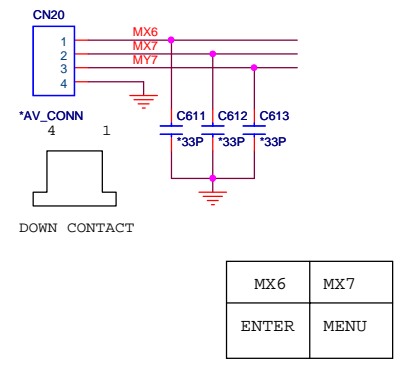
TOUCH PAD CONNECTOR



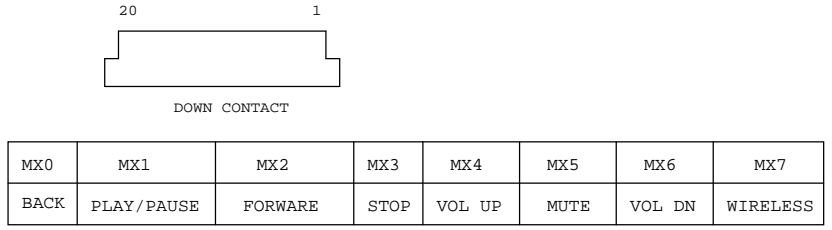
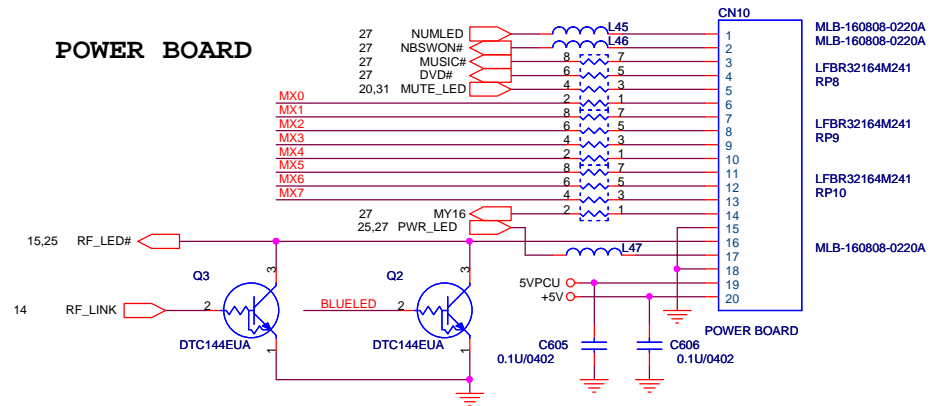
KEYBOARD CONNECTOR



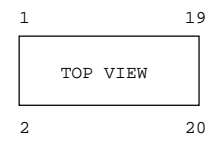
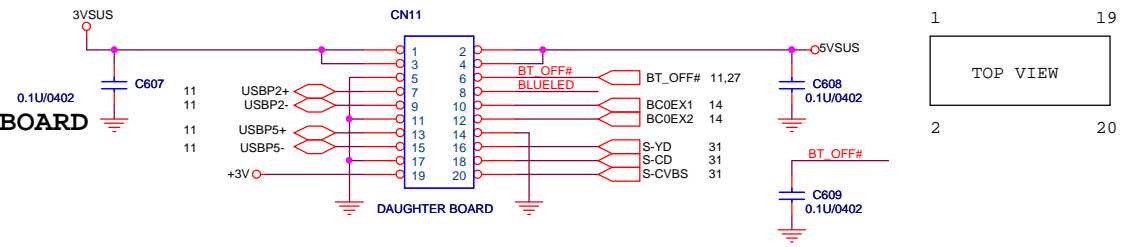
AV BOARD



POWER BOARD



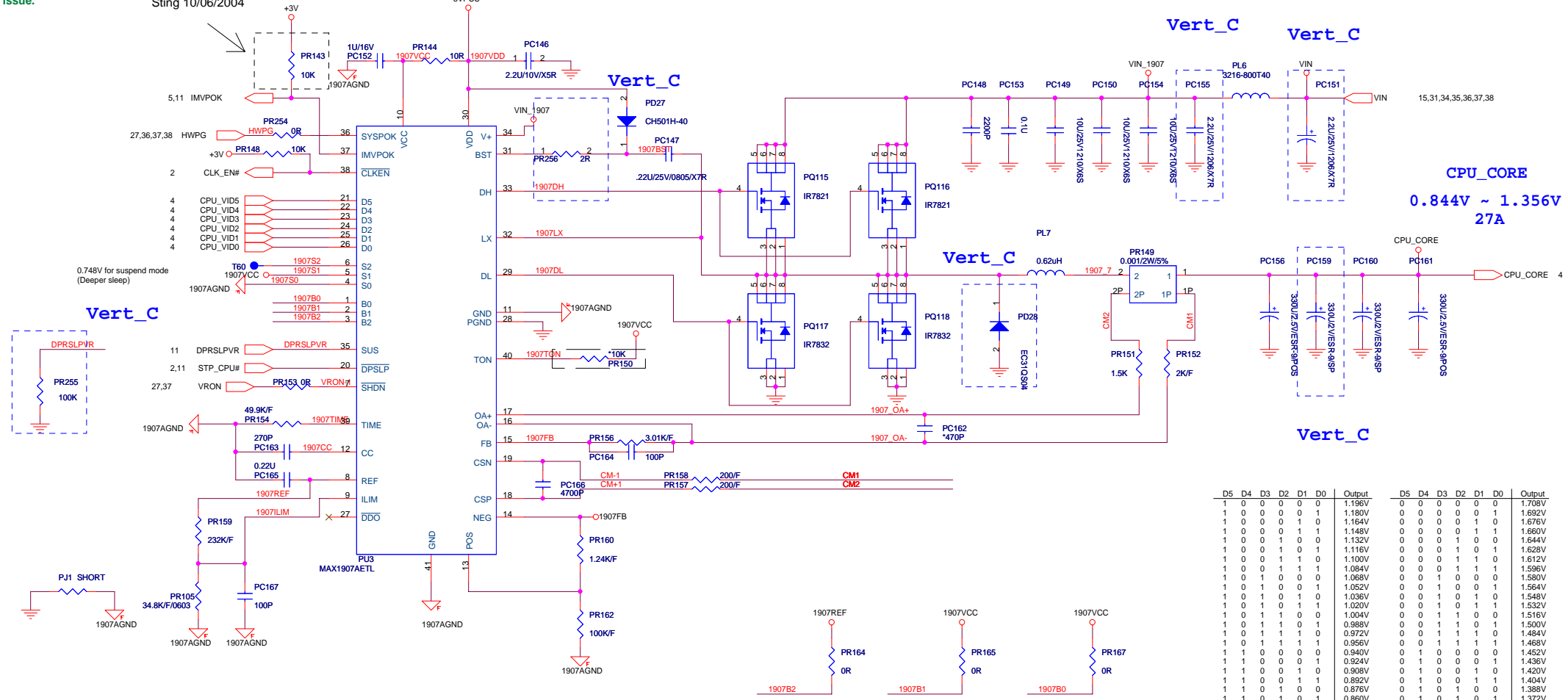
DAUGHTER BOARD



CPU VCC_CORE (MAX1907)

SI stage:
Change PR143 value from 100K ohms to
10K ohm to solve panel display abnormal
issue.

Sting 10/06/2004



D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	1	0	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	1	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	1	0	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	1	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

SUSPEND MODE (SUS=HIGH)				
S2	S1	S0	Output	
✓	OPEN	VCC	GND	0.748V

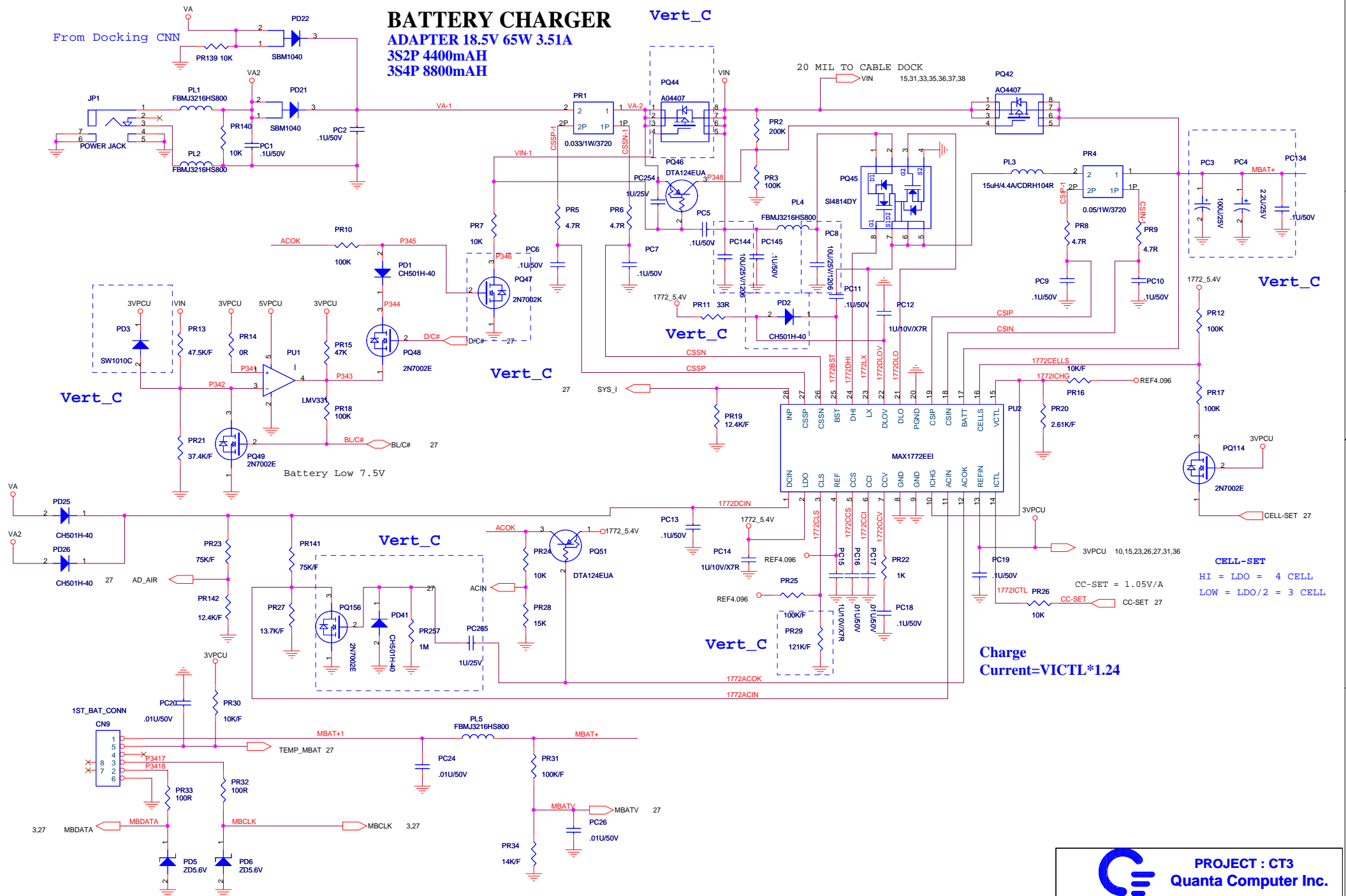
VCC_BOOT				
B2	B1	B0	Output	
✓	GND	GND	GND	1.708V
✓	REF	REF	REF	1.372V
✓	OPEN	OPEN	OPEN	1.036V
✓	VCC	VCC	VCC	0.700V
✓	REF	VCC	VCC	1.212V

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU CORE POWER	2A
Date:	Monday, December 27, 2004	Sheet 33 of 39

BATTERY CHARGER

ADAPTER 18.5V 65W 3.51A
3S2P 4400mAh
3S4P 8800mAh

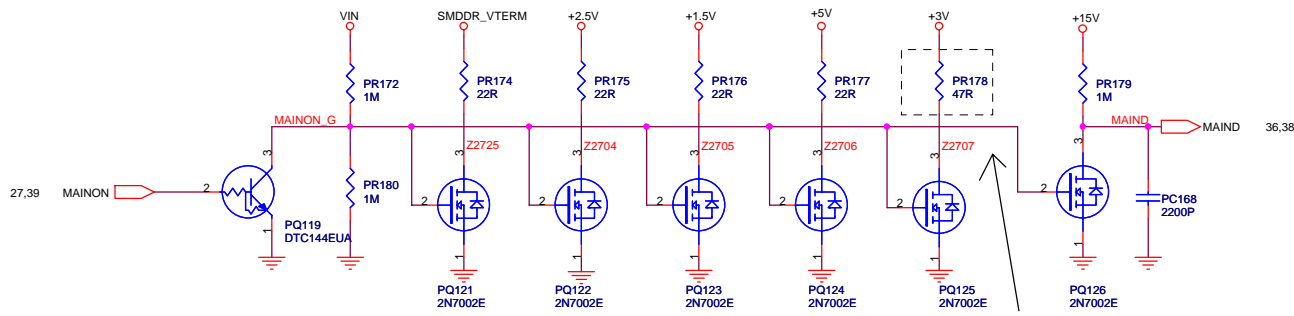


Charge
Current=VICTL*1.24

CELL-SET
HI = LDO = 4 CELL
LOW = LDO/2 = 3 CELL

PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX1772/CHARGING	2A
Date:	Monday, December 27, 2004	Sheet 34 of 39

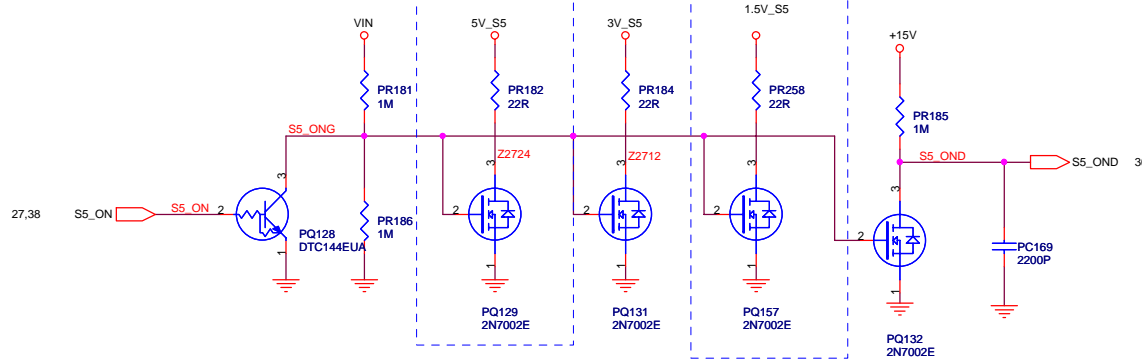


Vert_C

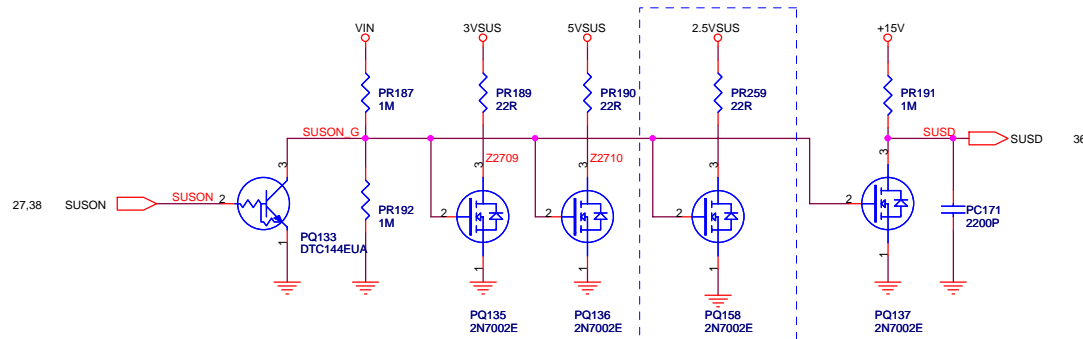
Vert_C

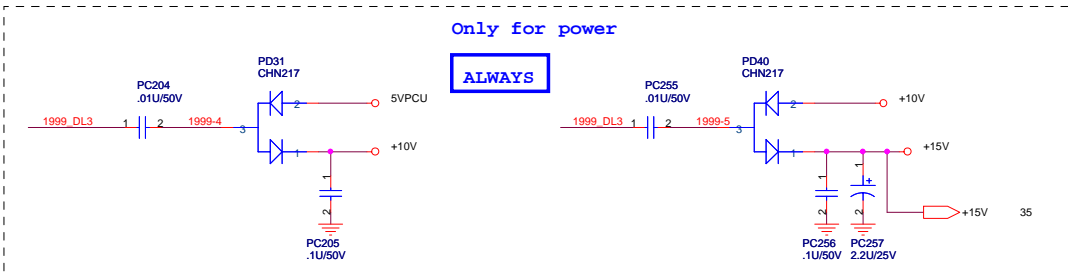
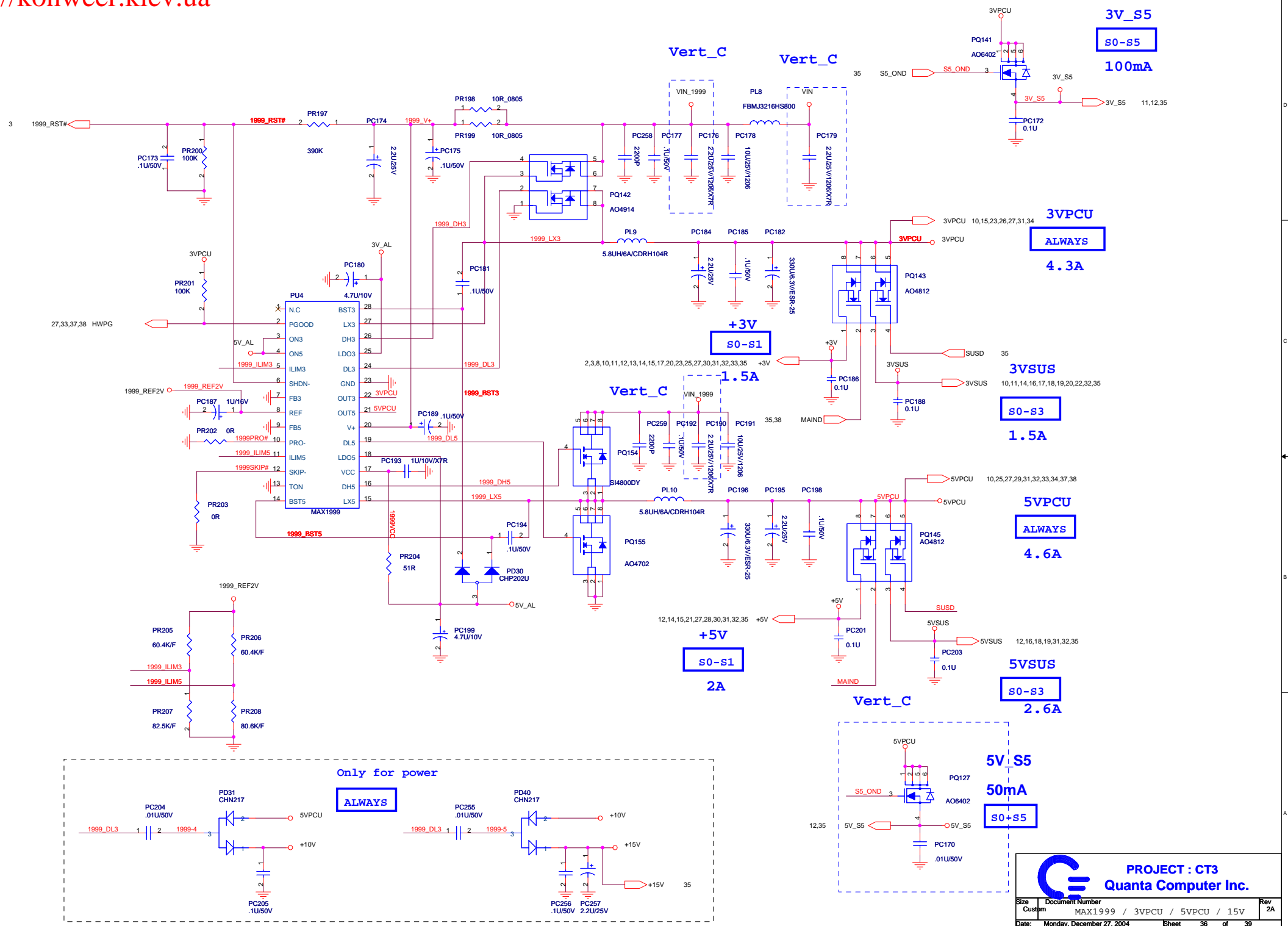
SI stage:
Change PR178 value from 22 ohm to 47 ohm, Intel has required the timing sequence of +1.5V and +3V in the system, we'd like to increase the value to make +3V discharge slowly to meet the specification of falling time.

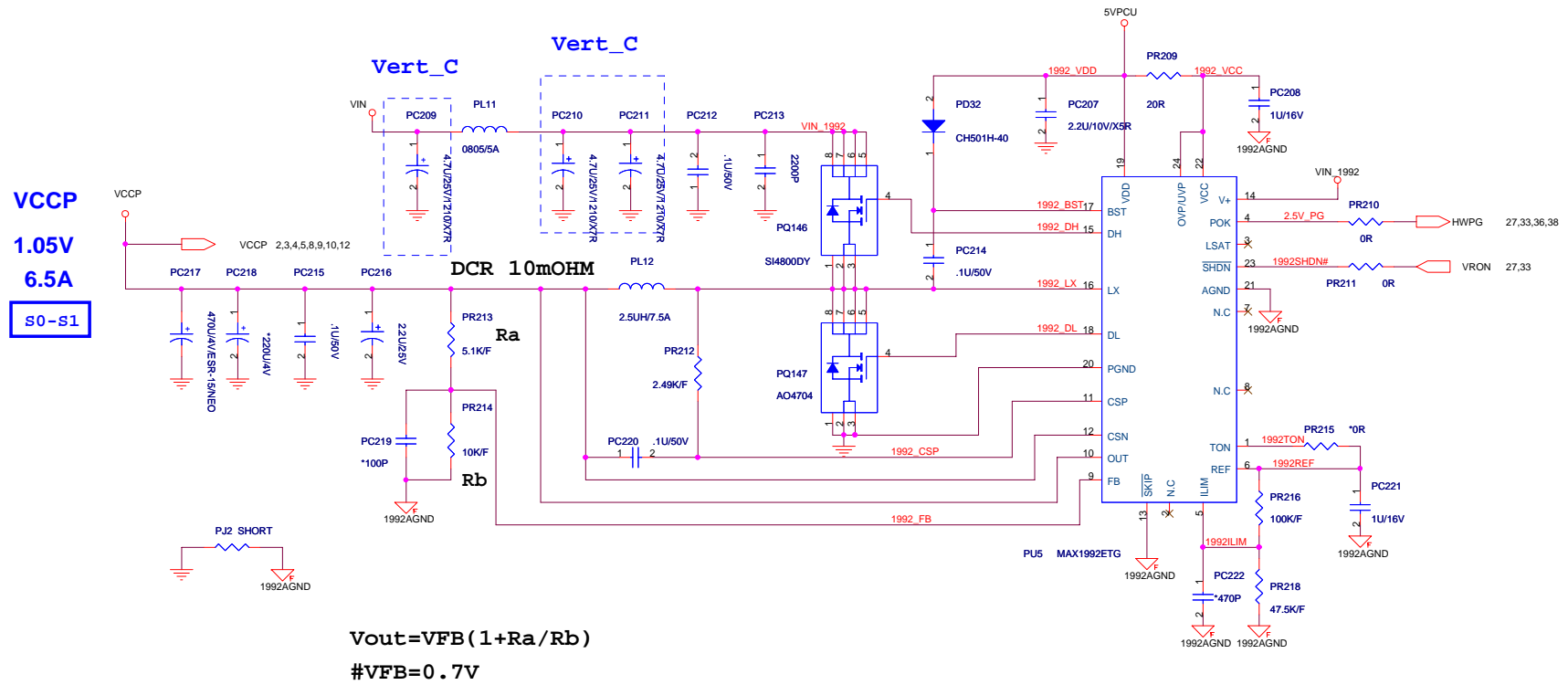
Sting 10/19/2004



Vert_C







DDR

