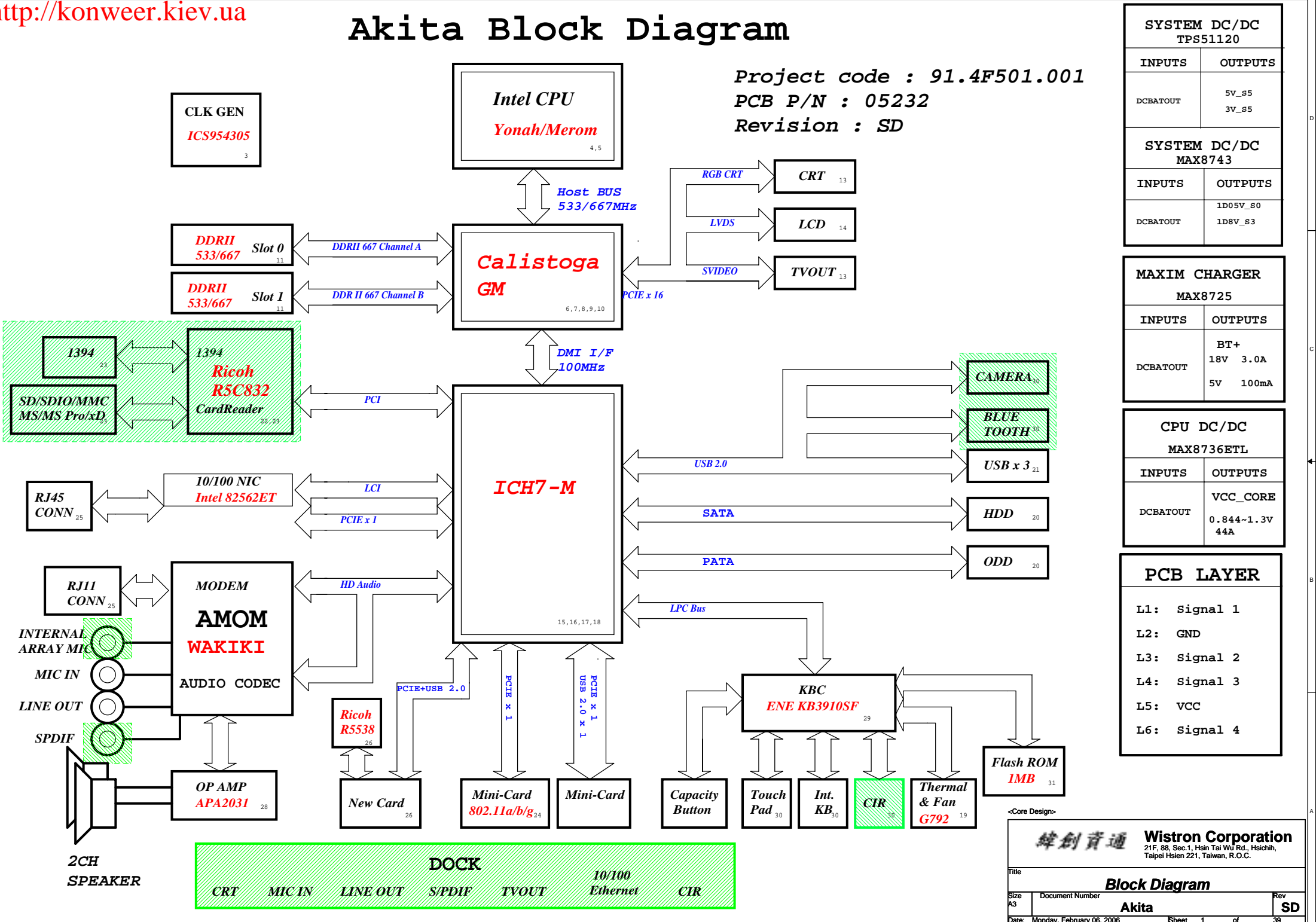


# Akita Block Diagram

Project code : 91.4F501.001  
 PCB P/N : 05232  
 Revision : SD



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4



<Core Design>

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Title: **Block Diagram**

Size: A3   Document Number: **Akita**   Rev: **SD**

Date: Monday, February 06, 2006   Sheet: 1 of 39

# Calistoga Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6		0=Moby Dick 1=Calistoga
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	Reserved	
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORX In signal.

## History

11.18.2004: mini card not ready

# 125CV Spread Spectrum Select

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+0.3
1	0	0	1	+0.4
1	0	1	0	+0.5
1	0	1	1	+0.6
1	1	0	0	+0.8
1	1	0	1	+1.0
1	1	1	0	+1.25
1	1	1	1	+1.5

## PCI Routing

	IDSEL	IRQ	REQ/GNT
R5C832	25		0

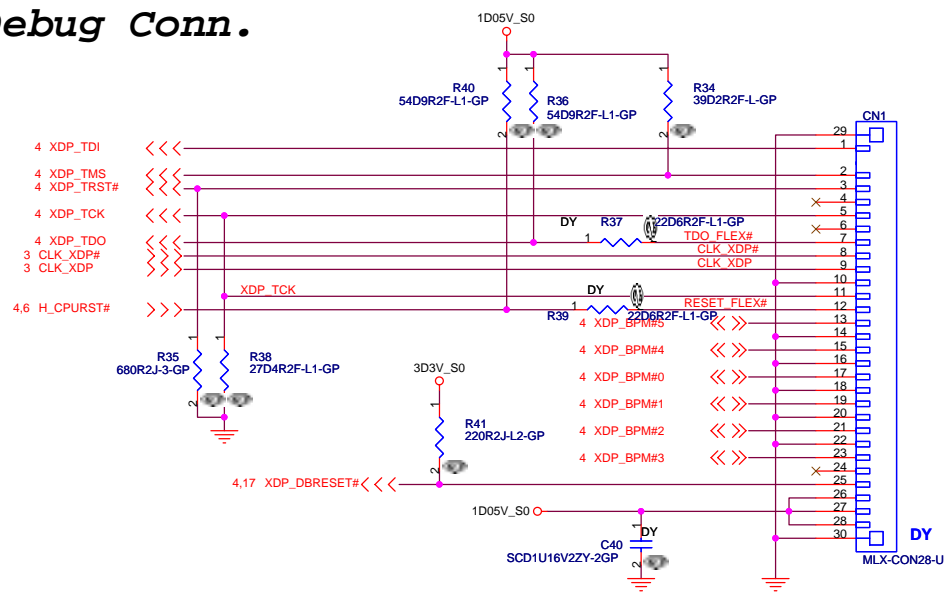
# ICH7M Integrated Pull-up and Pull-down Resistors

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDRQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

## ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

## ITP Debug Conn.



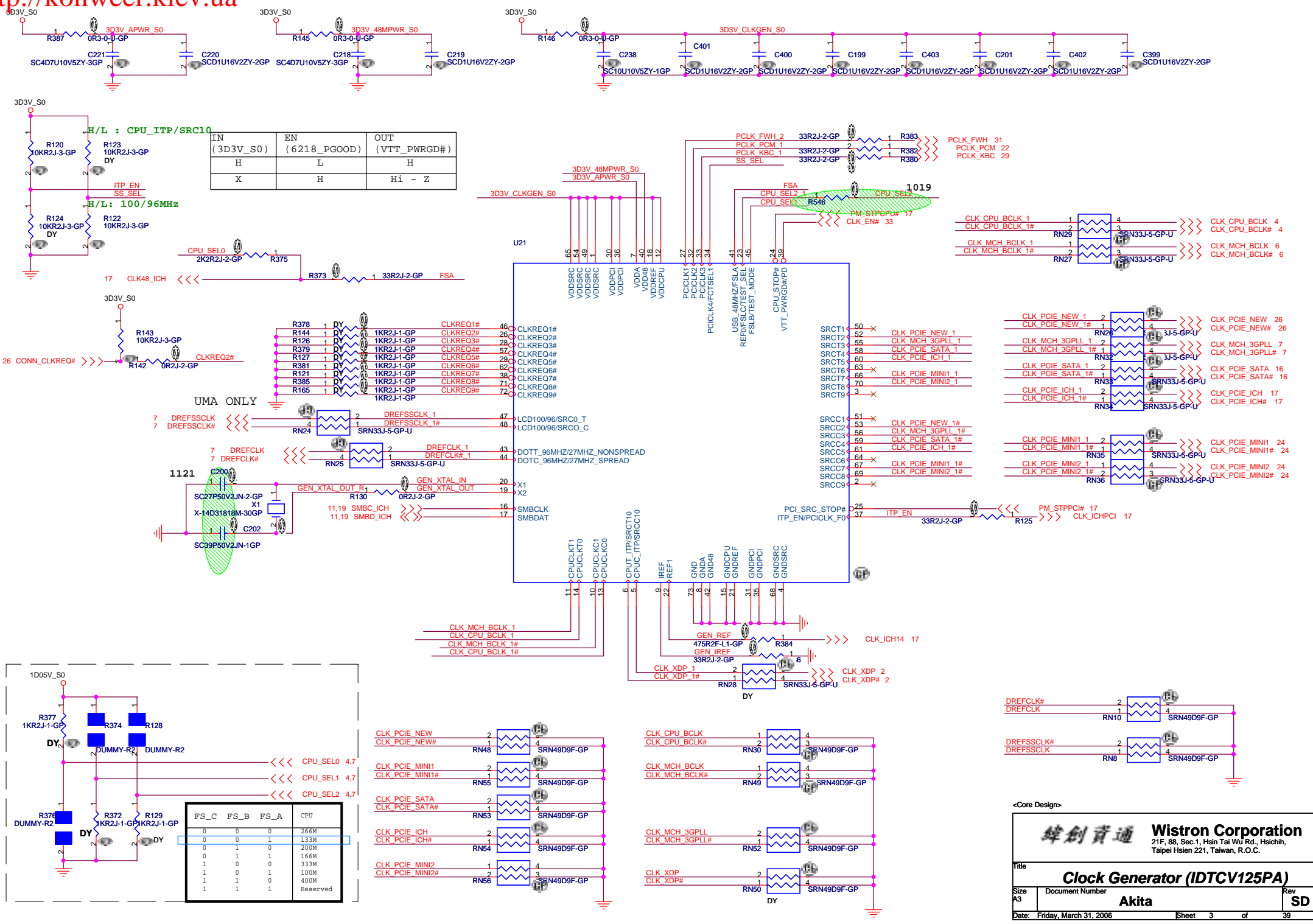
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Title: **ITP**

Size A3 Document Number: **Akita** Rev: **SD**

Date: Friday, March 31, 2006 Sheet 2 of 39



IN (3D3V_S0)	EN (6218_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

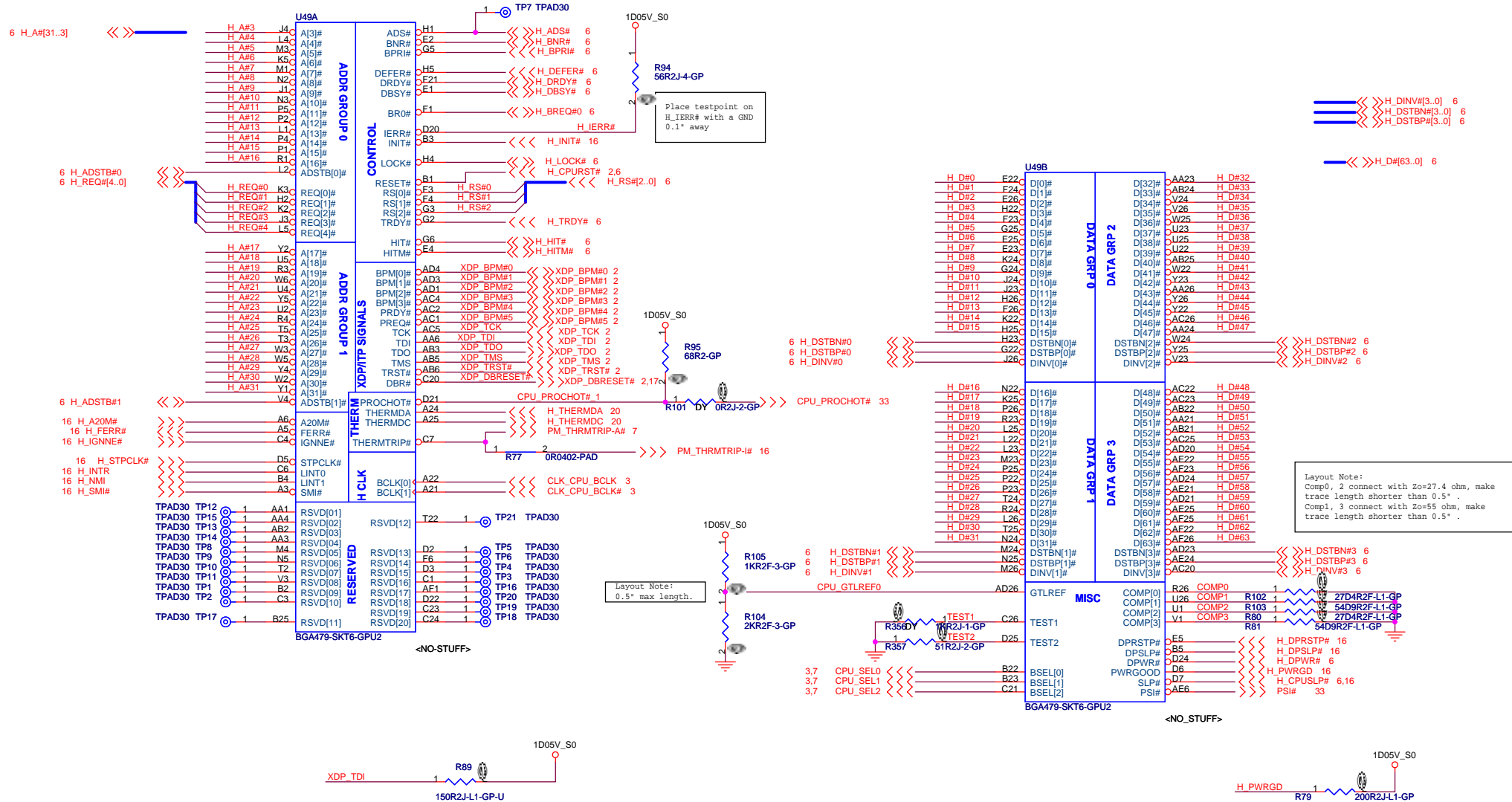
FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

<Core Design>

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Title: **Clock Generator (IDTCV125PA)**

Size A3	Document Number Akita	Rev SD
Date: Friday, March 31, 2006	Sheet 3 of 39	



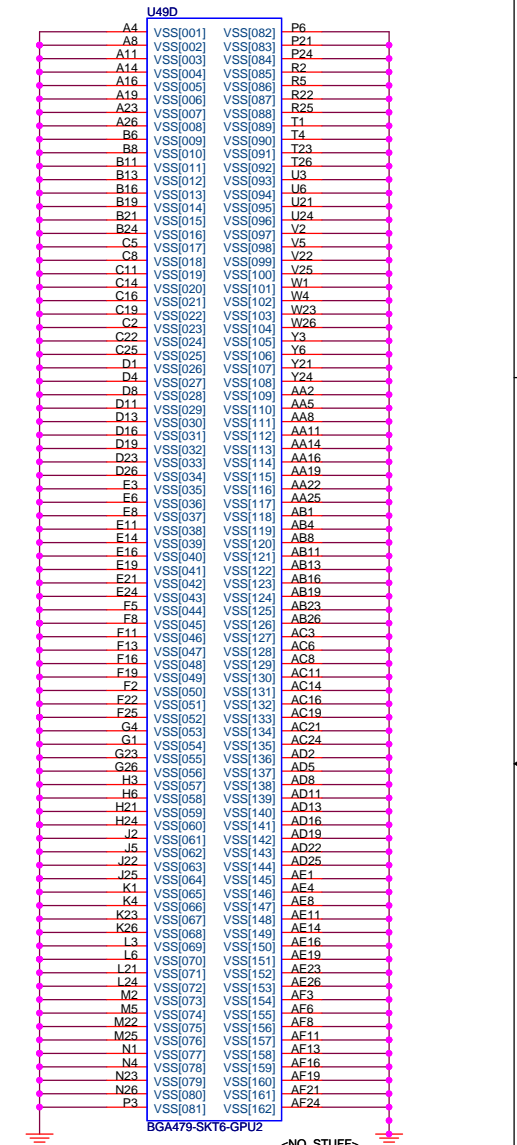
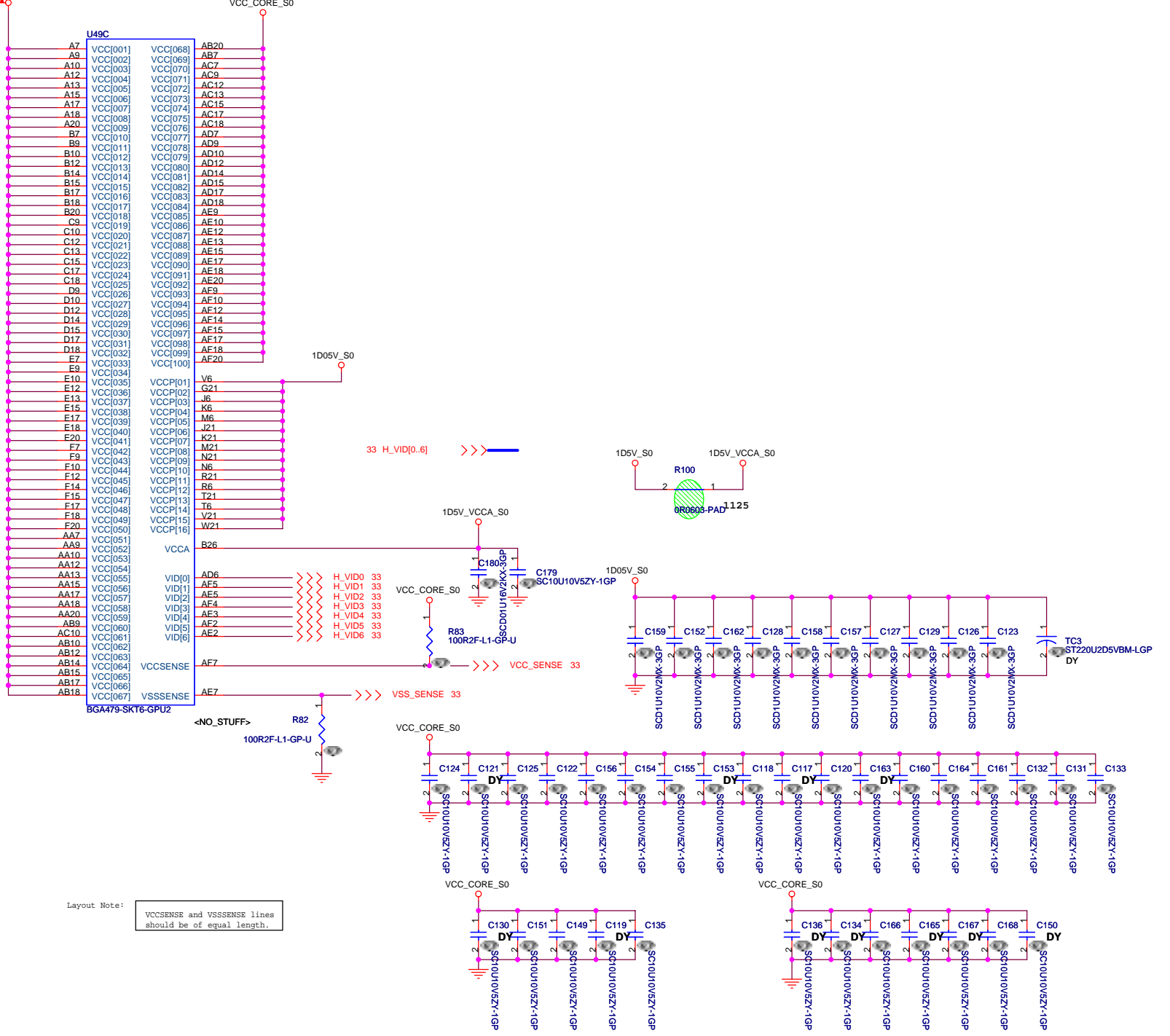
>>> H\_DINV#[3..0] 6  
 >>> H\_DSTBN#[3..0] 6  
 >>> H\_DSTBP# [3..0] 6  
 >>> H\_D# [63..0] 6

**Layout Note:**  
 Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".  
 Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

**<Core Design>**

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Title: **CPU (1 of 2)**  
 Size: A3  
 Document Number: **Akita**  
 Date: Friday, March 31, 2006  
 Sheet: 4 of 39  
 Rev: **SD**



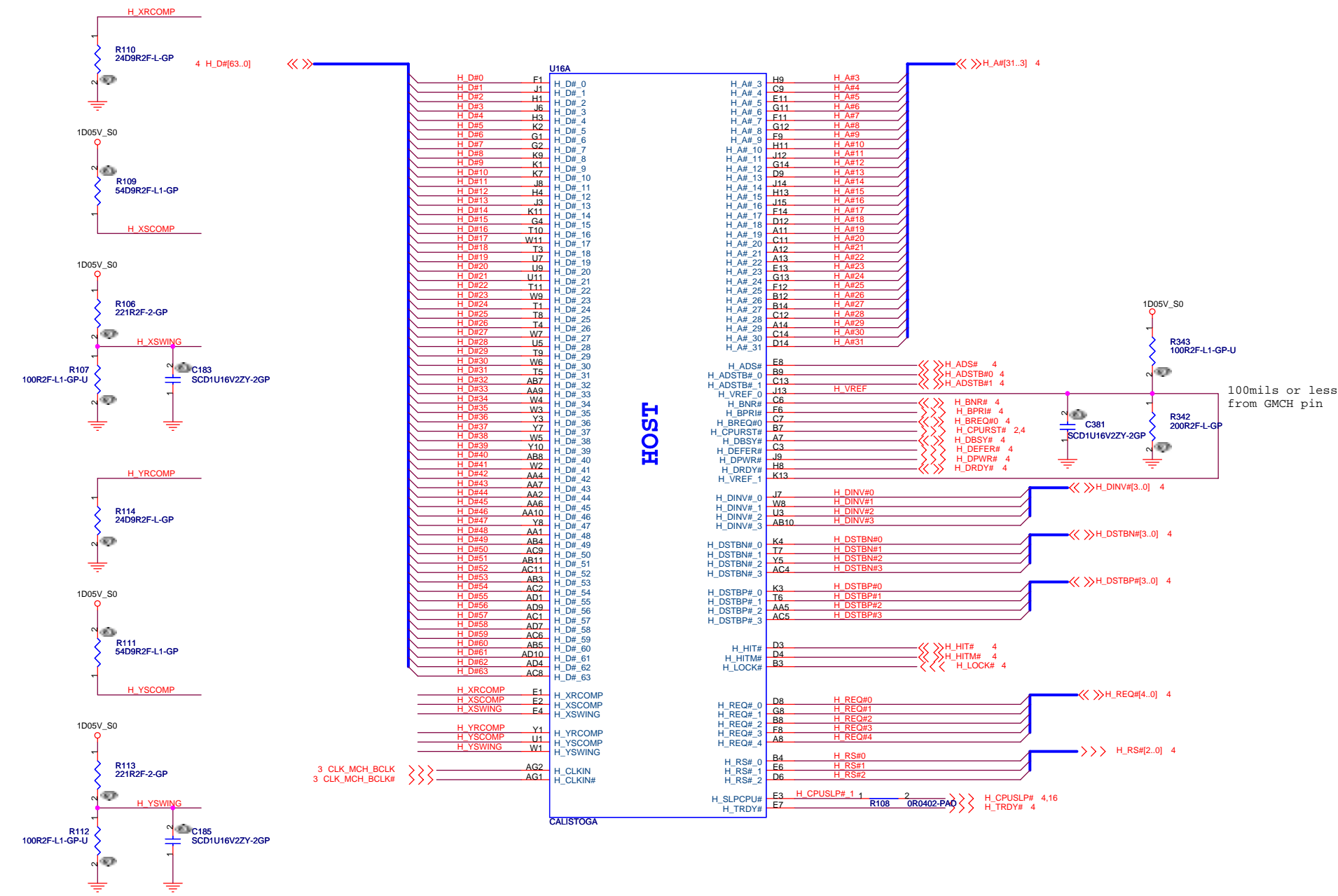
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Title: **CPU (2 of 2)**

Size: A3 Document Number: **Akita** Rev: **SD**

Date: Friday, March 31, 2006 Sheet 5 of 39



Place them near to the chip

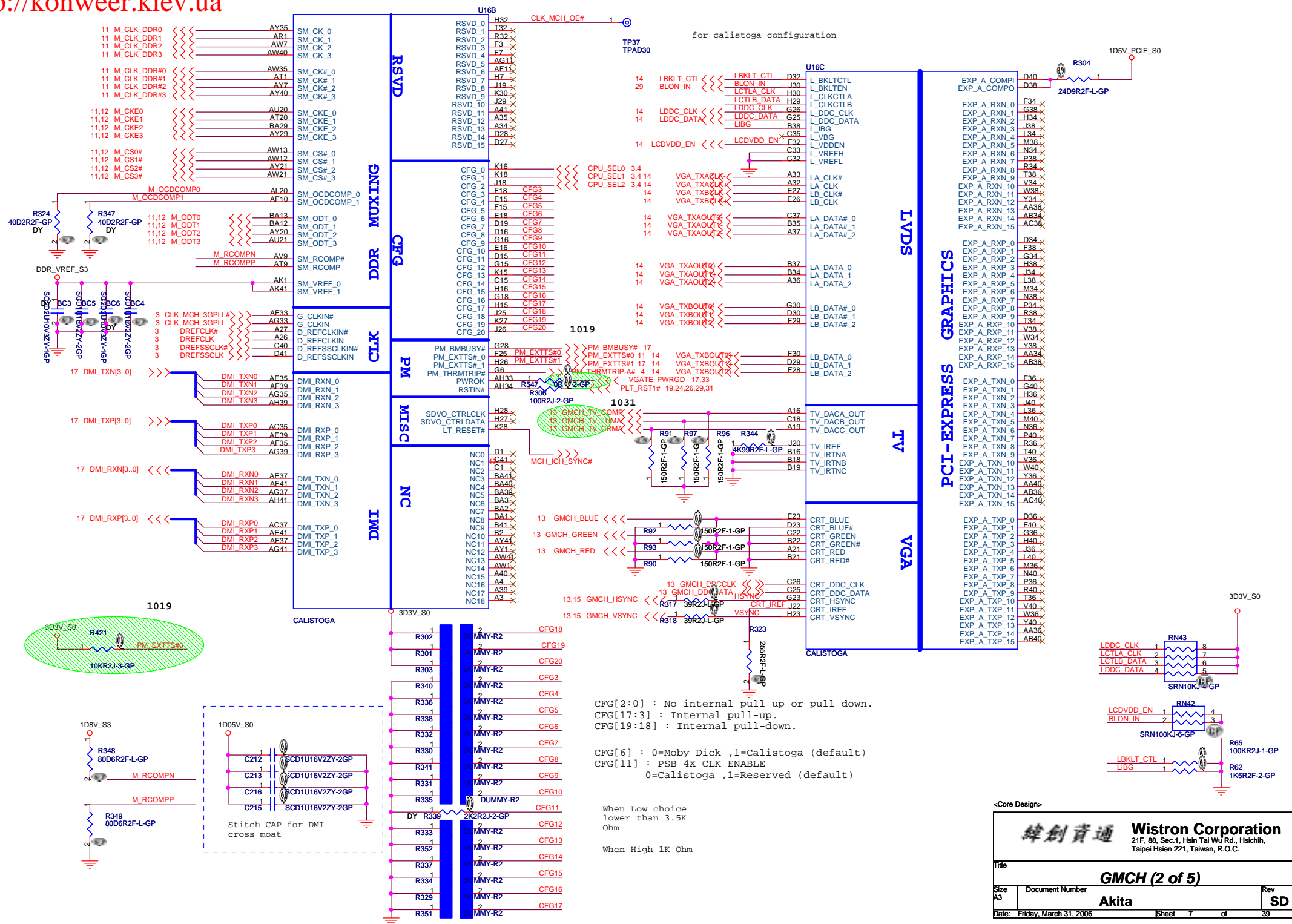
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Title: **GMCH (1 of 5)**

Size: A3 Document Number: Akita Rev: SD

Date: Monday, February 06, 2006 Sheet: 6 of 39



CFG[2:0] : No internal pull-up or pull-down.  
 CFG[17:3] : Internal pull-up.  
 CFG[19:18] : Internal pull-down.

CFG[6] : 0=Moby Dick ,1=Calistoga (default)  
 CFG[11] : PSB 4X CLK ENABLE  
 0=Calistoga ,1=Reserved (default)

When Low choice lower than 3.5K Ohm

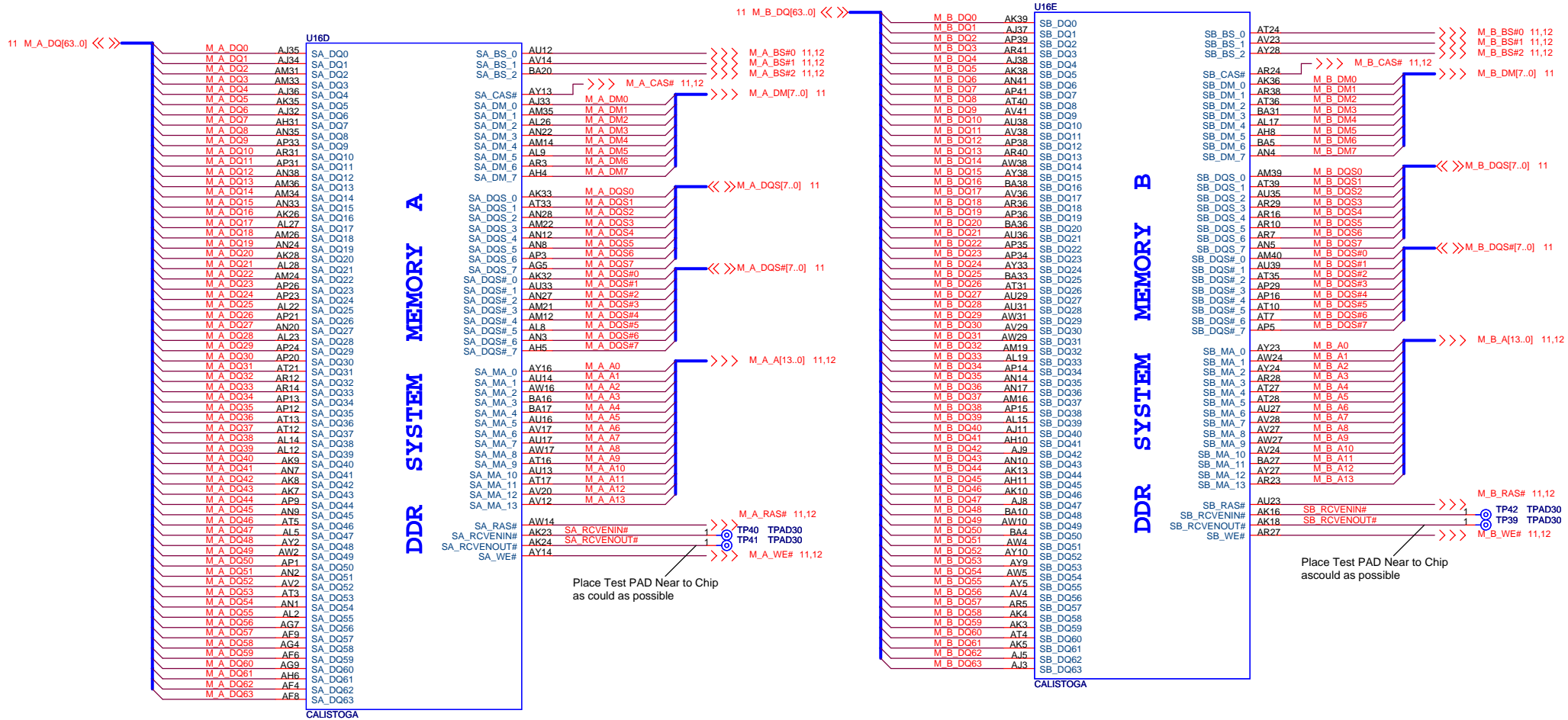
When High 1K Ohm

<Core Design>

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Size A3		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Date: Friday, March 31, 2006		Sheet 7 of 39	

**GMCH (2 of 5)**

Akita SD



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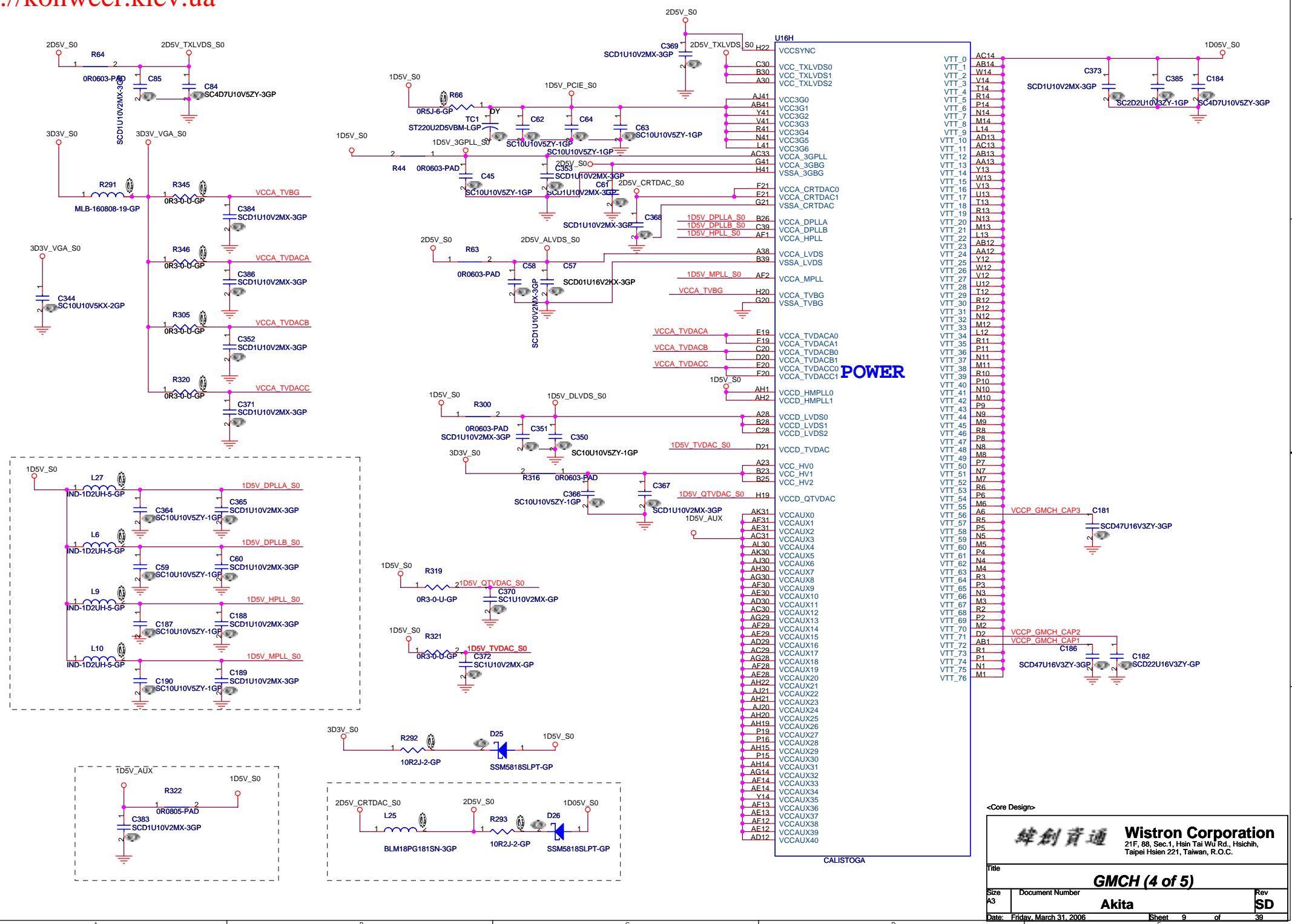
緯創資通 **Wistron Corporation**  
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 Taipei Hsien 221, Taiwan, R.O.C.

Title

**GMCH (3 of 5)**

Size A3 Document Number Akita Rev SD

Date: Monday, February 06, 2006 Sheet 8 of 39



**POWER**

**<Core Design>**

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Title: **GMCH (4 of 5)**

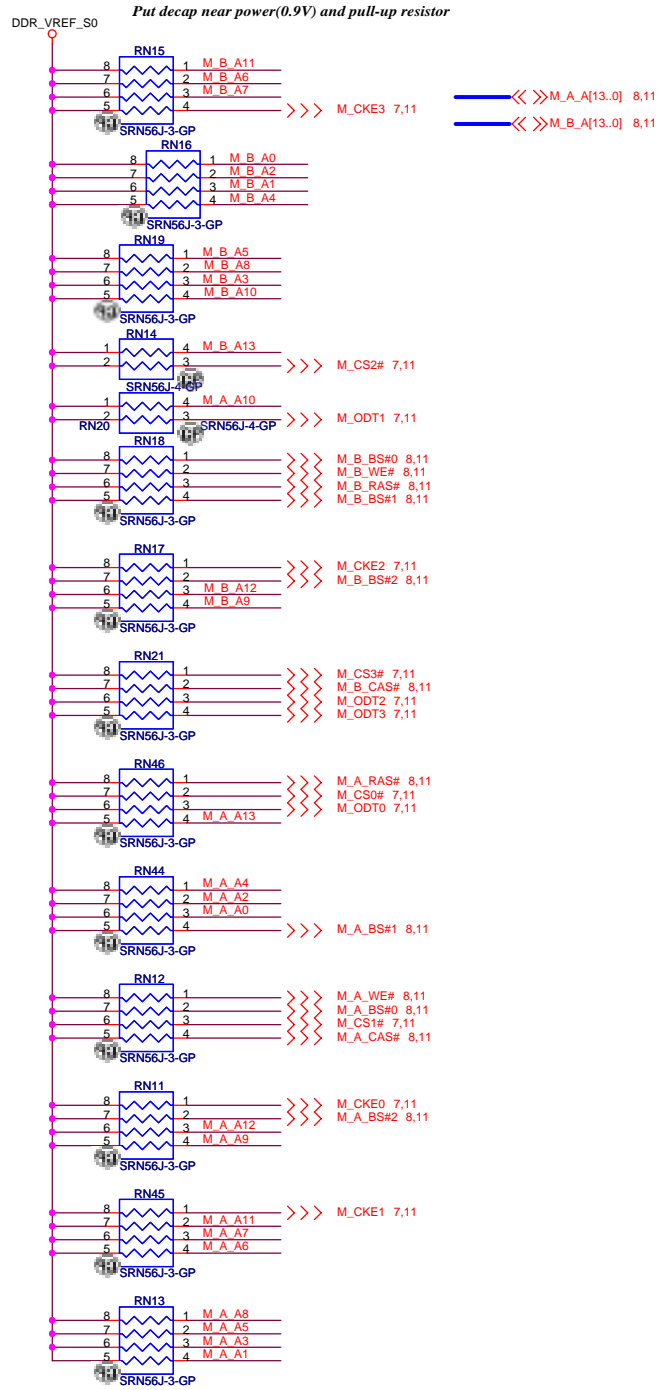
Size: A3 Document Number: **Akita** Rev: **SD**

Date: Friday, March 31, 2006 Sheet: 9 of 39

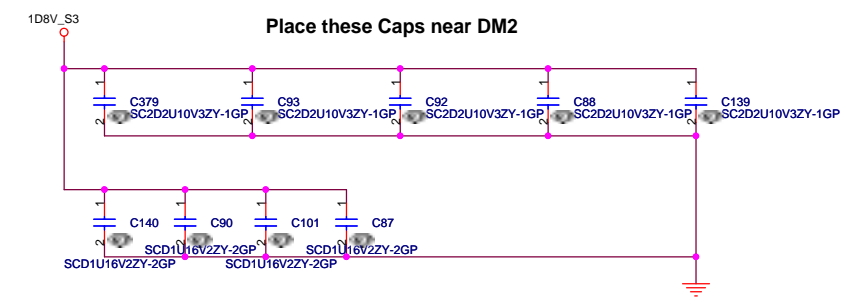
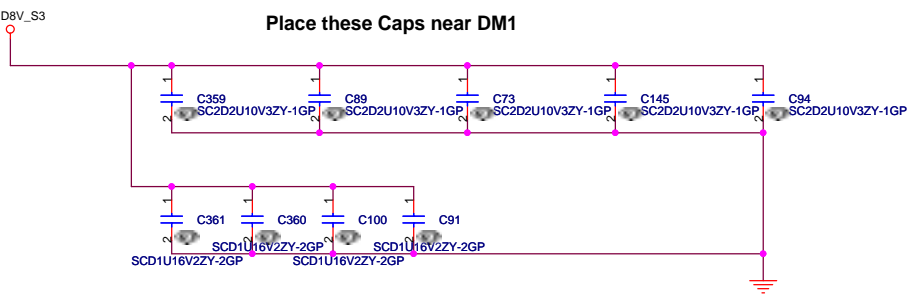
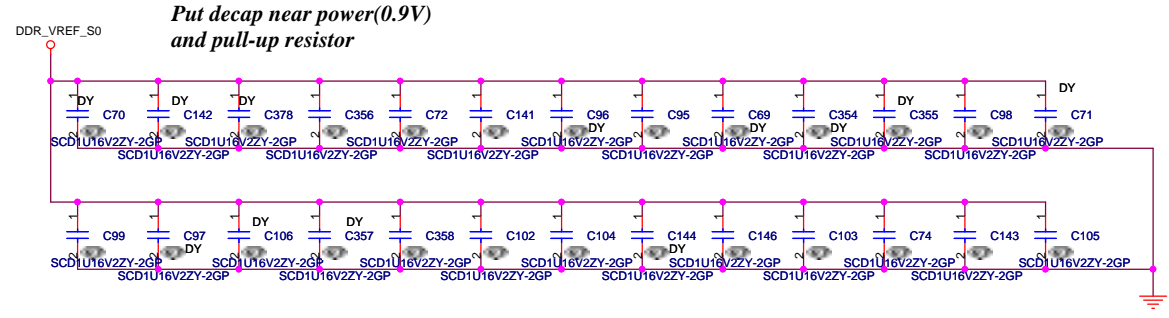




# PARALLEL TERMINATION

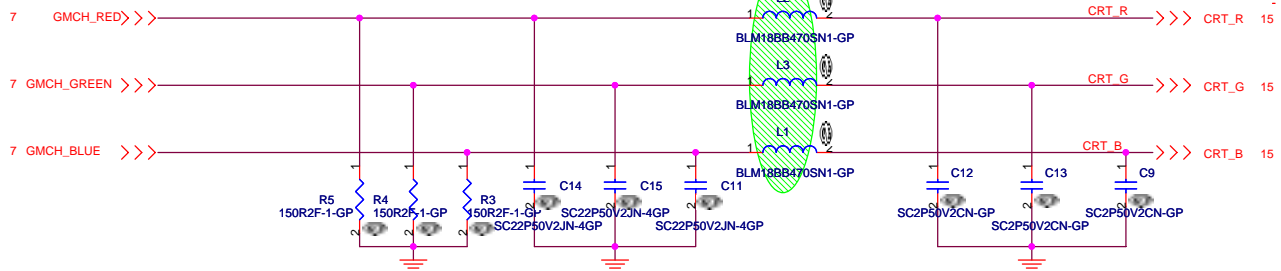


# Decoupling Capacitor



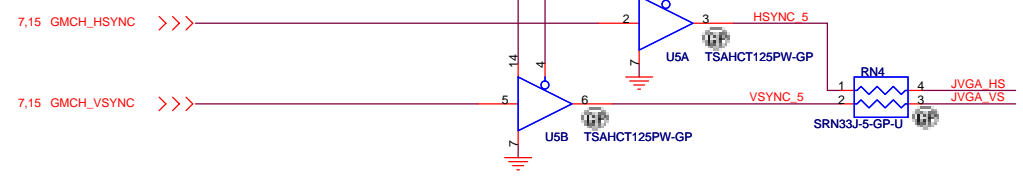
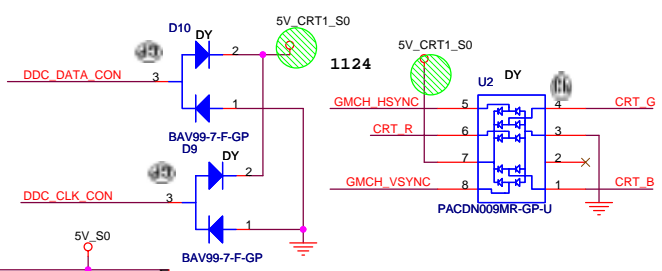
# CRT I/F & CONNECTOR

Layout Note:  
Place these resistors  
close to the CRT-out  
connector

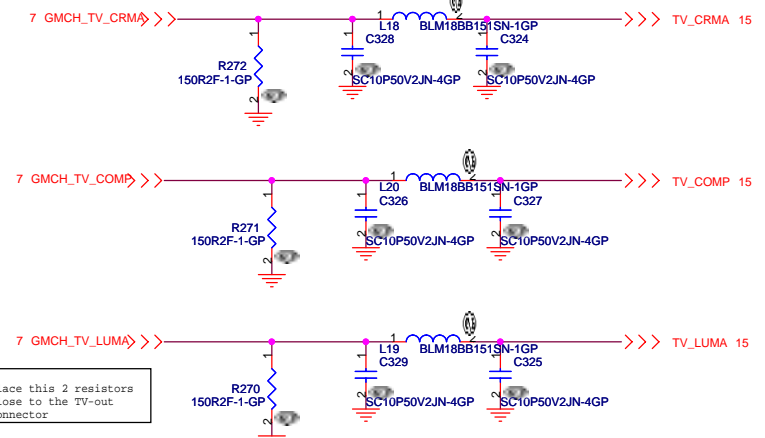


**Layout Note:**  
 \* Must be a ground return path between this ground and the ground on the VGA connector.  
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

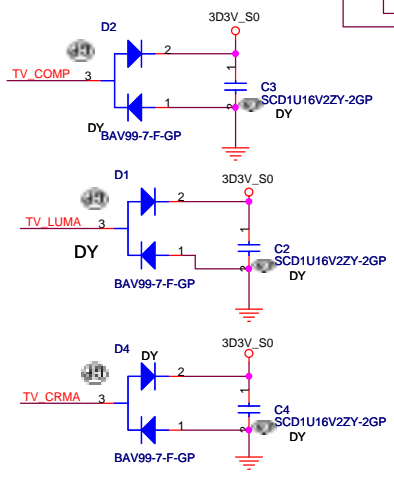
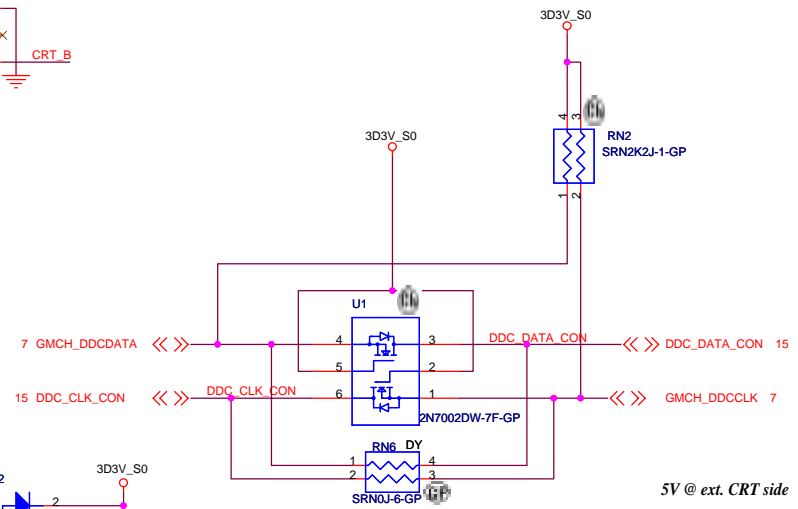
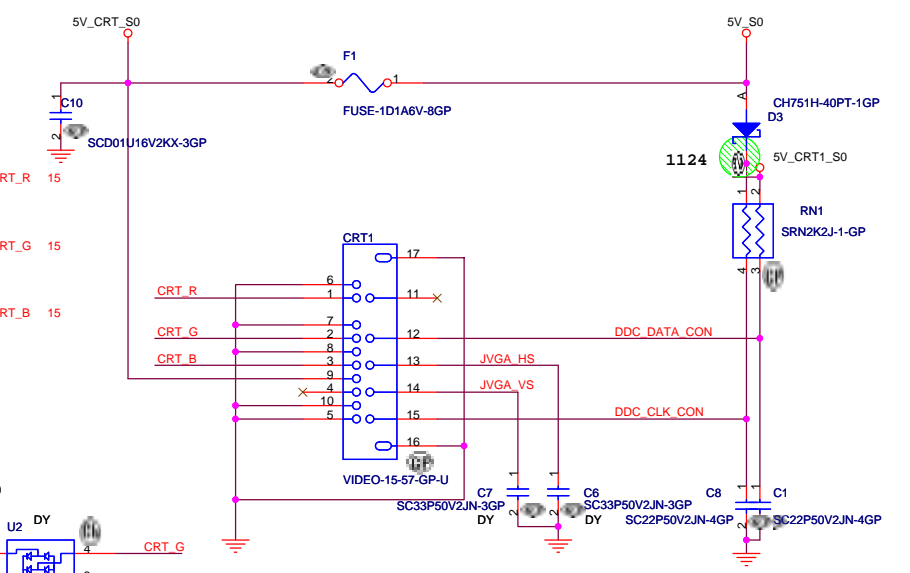
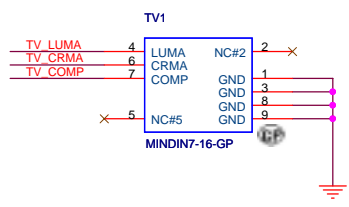
Hsync & Vsync level shift



## TV OUT CONN



Place this 2 resistors  
close to the TV-out  
connector



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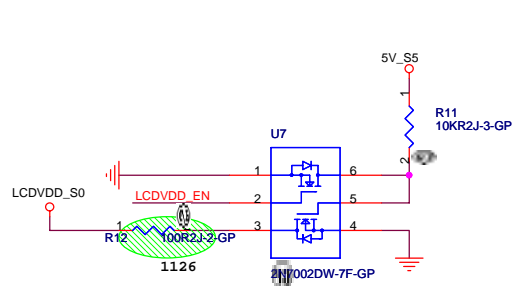
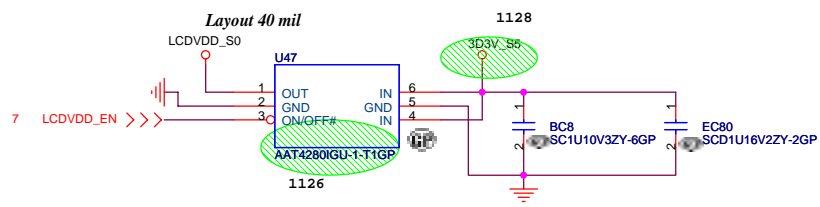
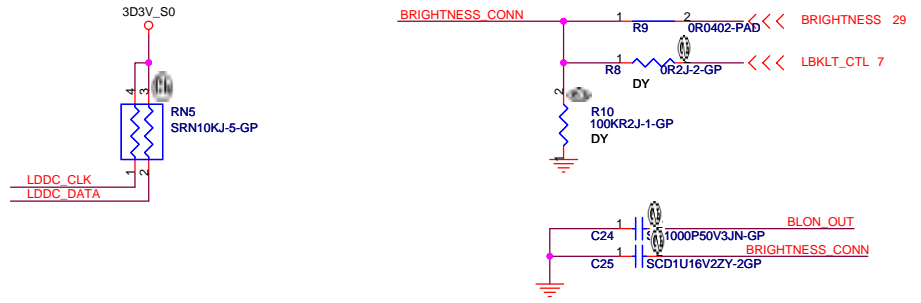
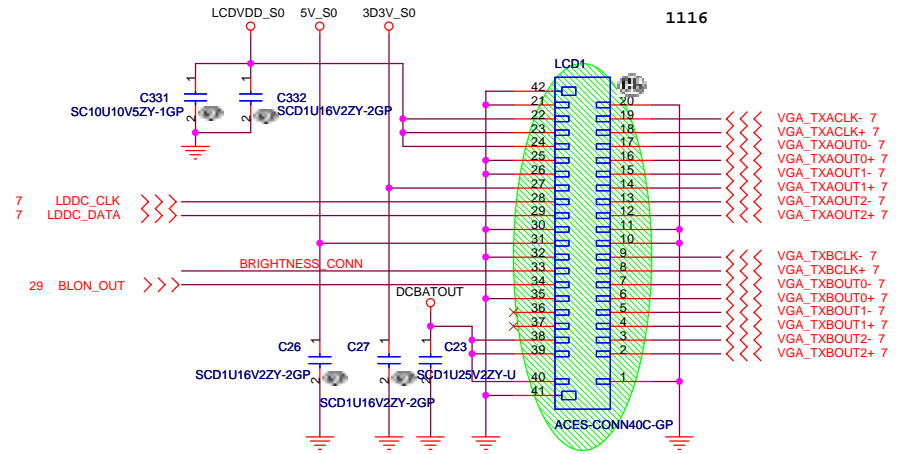
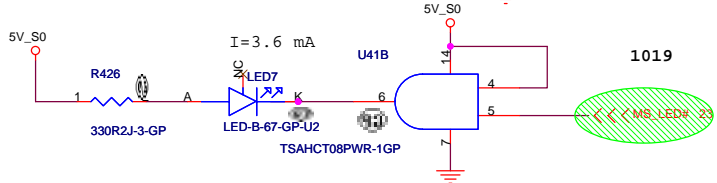
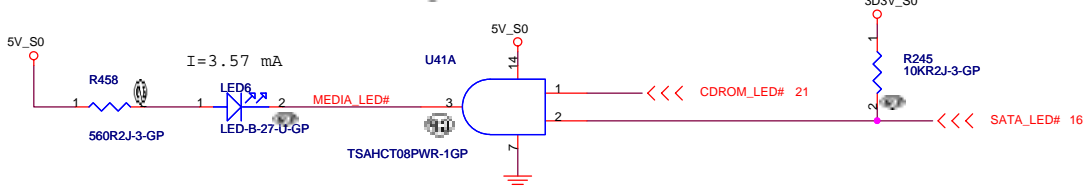
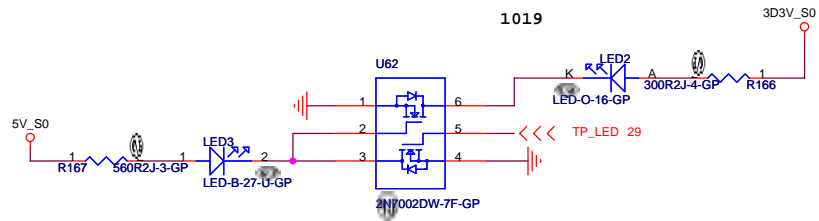
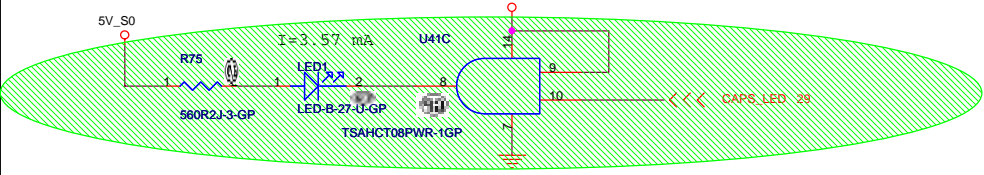
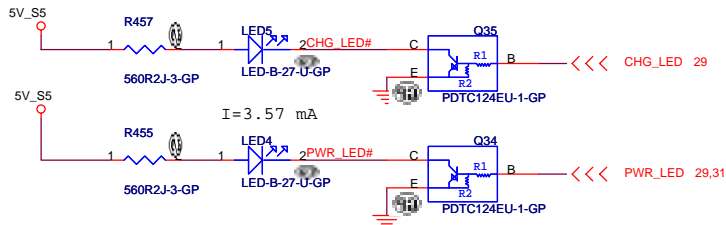
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Title: **CRT/TV Connector**

Size A3	Document Number	Rev
	<b>Akita</b>	<b>SD</b>
Date: Saturday, April 01, 2006	Sheet 13 of 39	

# LED / INVERTER INTERFACE

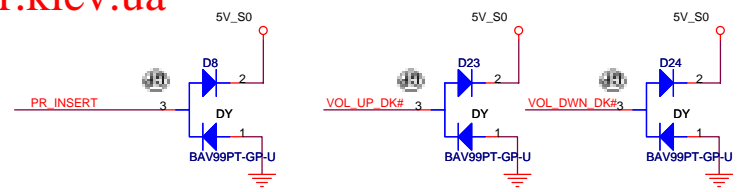
## LCD/INV CONN



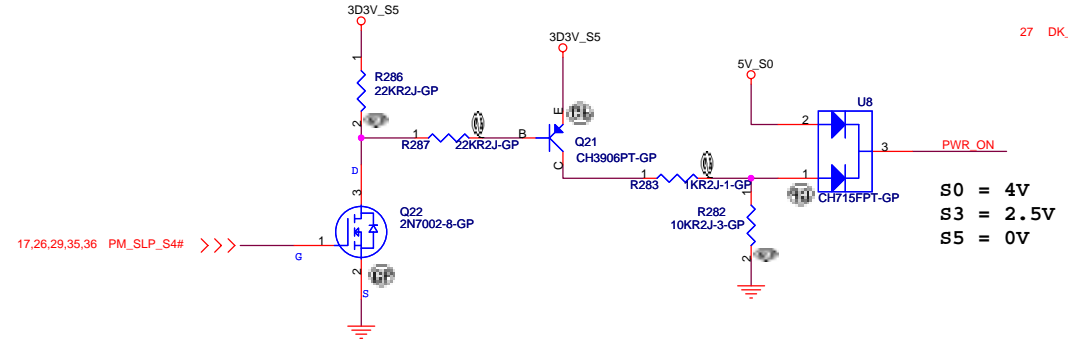
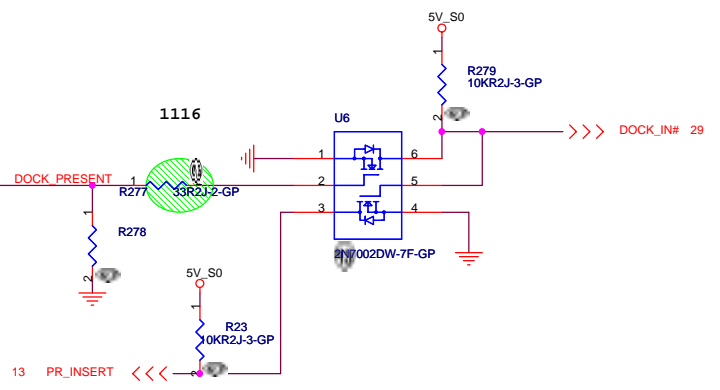
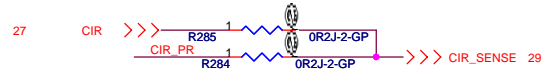
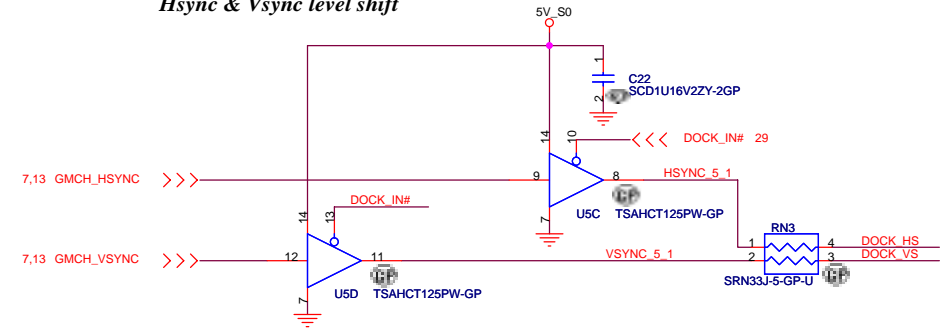
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Title	
<b>LCD/Inverter Connector</b>	
Size	Document Number
Custom	<b>Akita</b>
Date: Saturday, April 01, 2006	Rev <b>SD</b>
Sheet 14	of 39

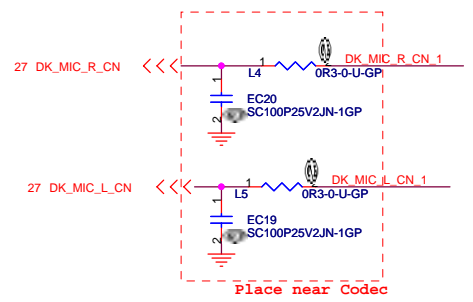
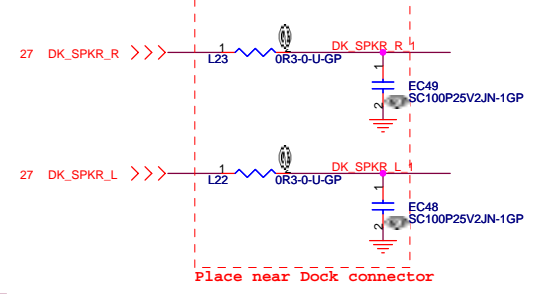
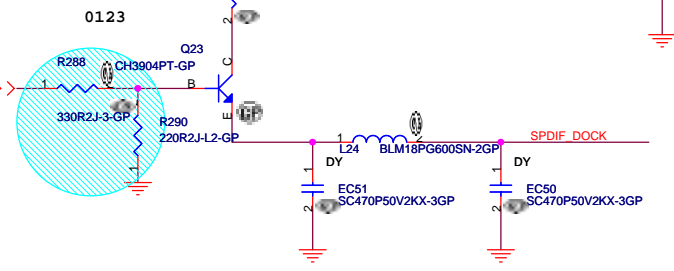
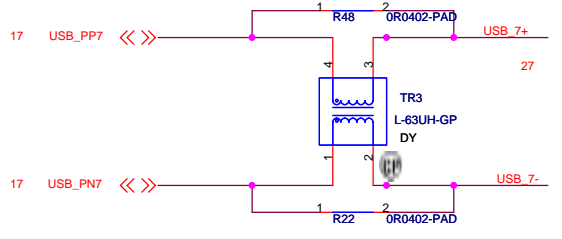
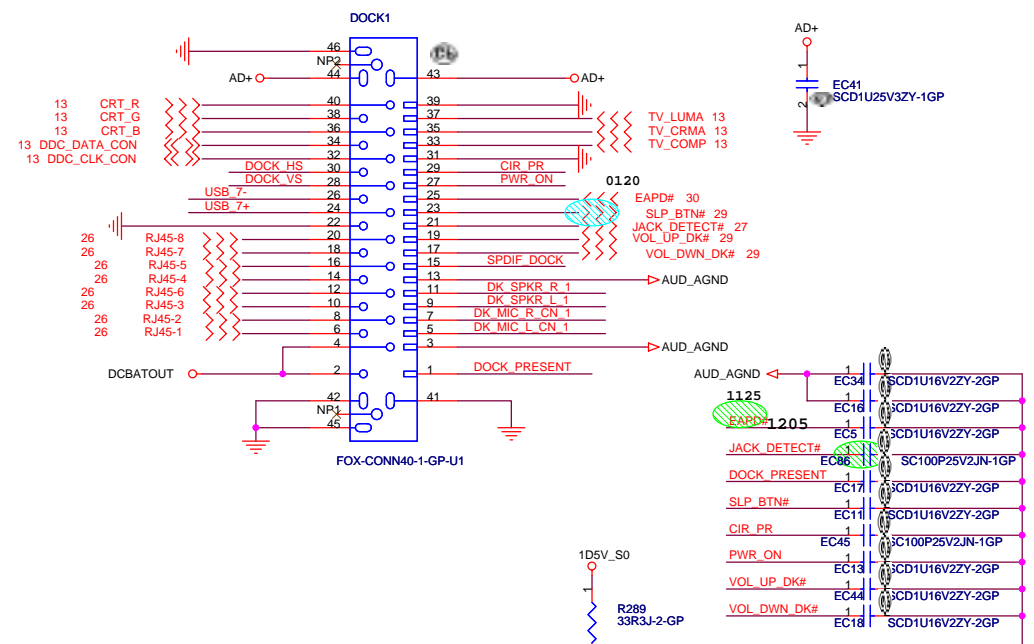
# Docking Connector



## Hsync & Vsync level shift



S0 = 4V  
S3 = 2.5V  
S5 = 0V



Place near Dock connector

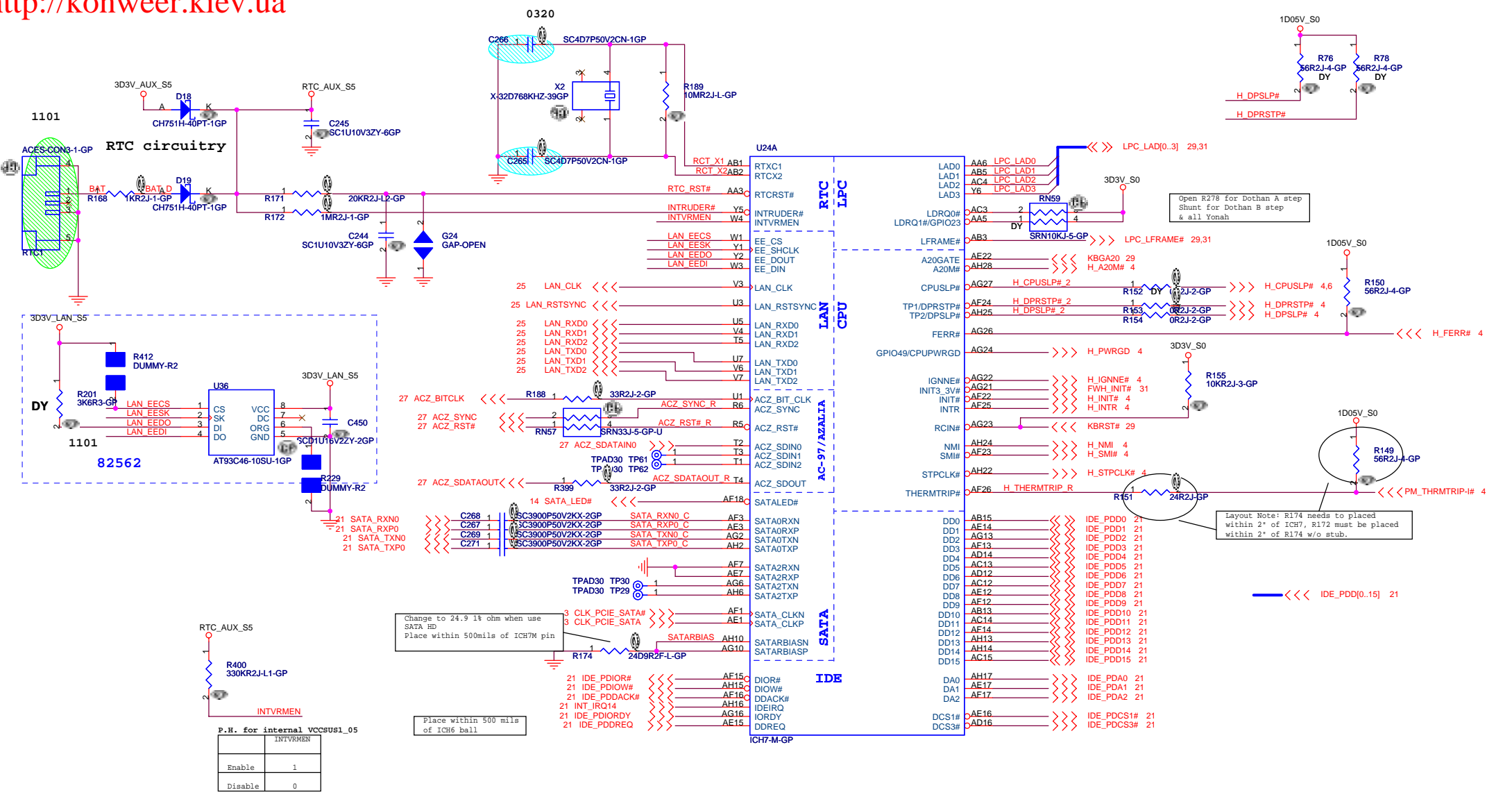
Place near Codec

<Core Design>

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Title: **Board to board conn/ Docking**

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Akita		
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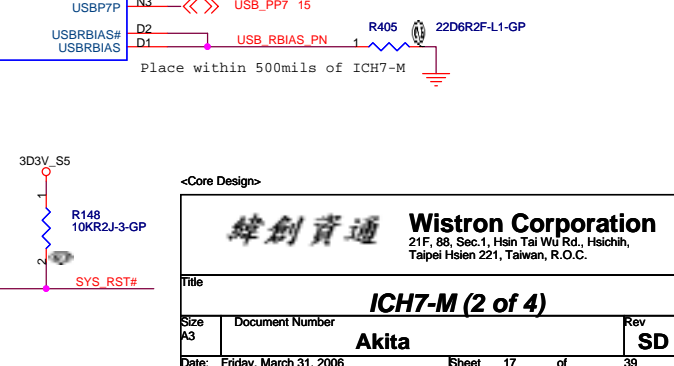
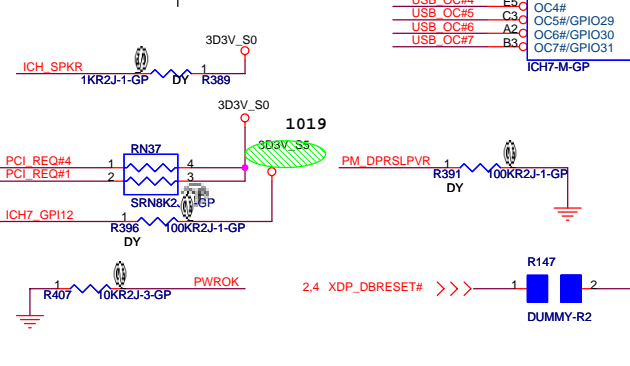
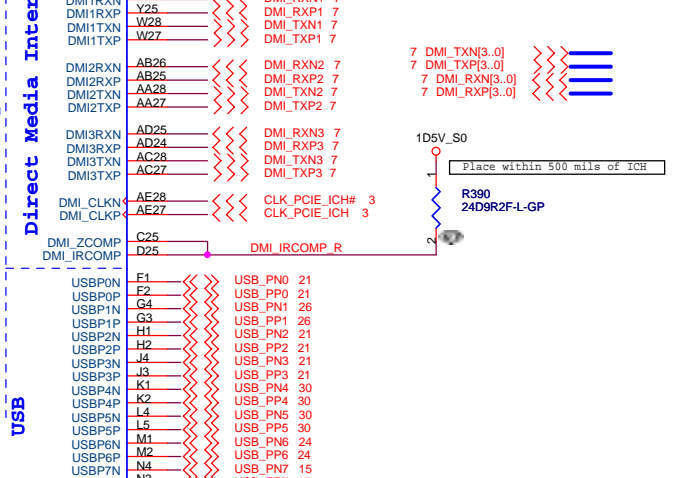
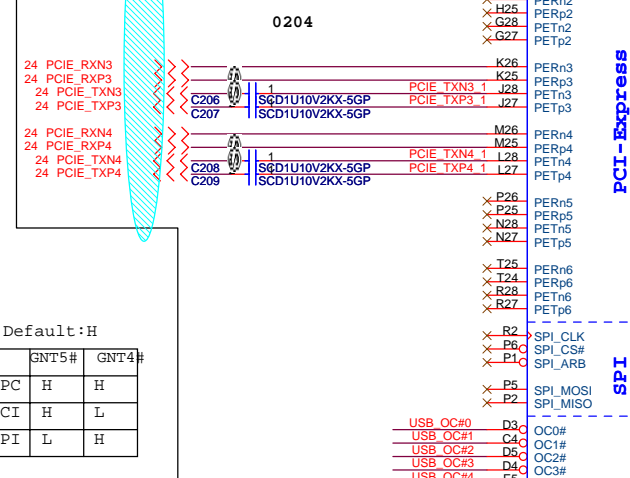
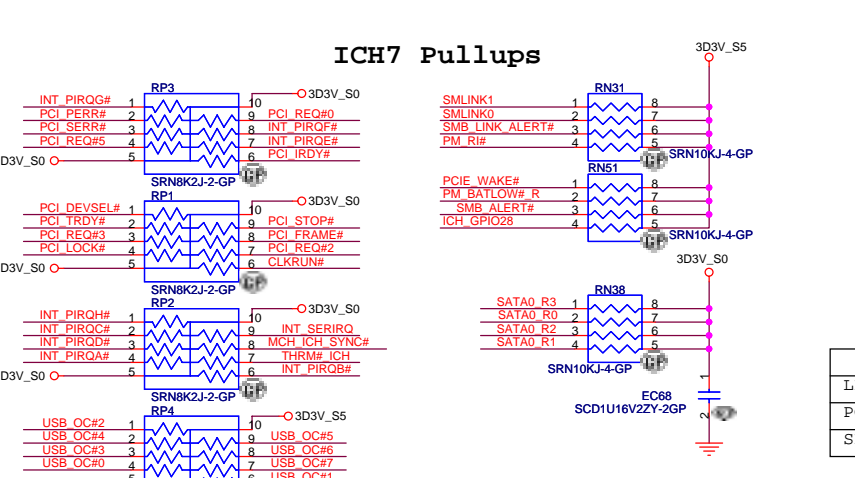
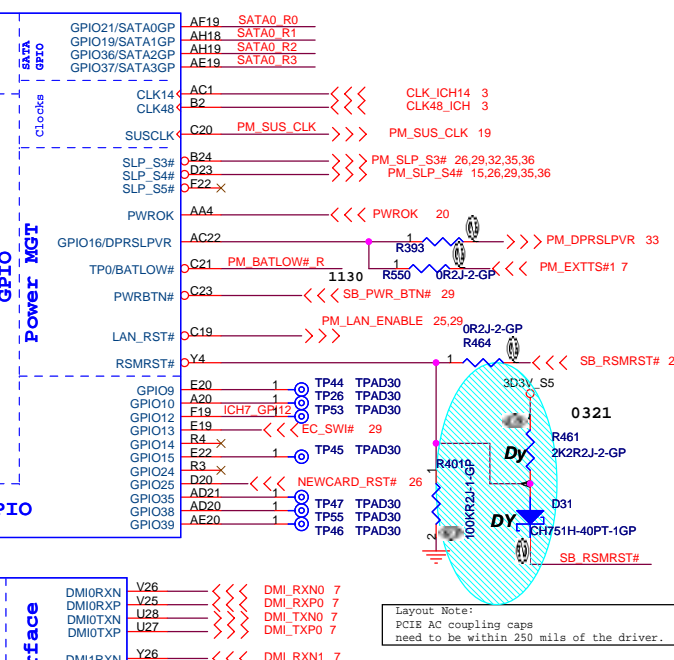
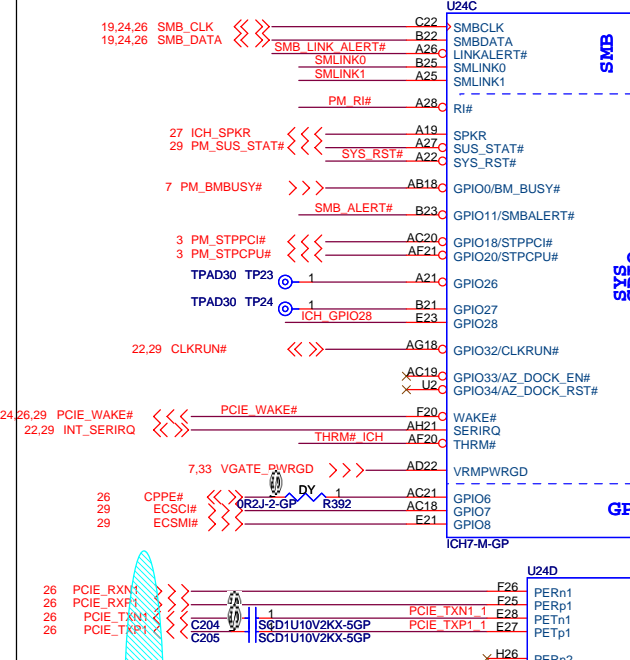
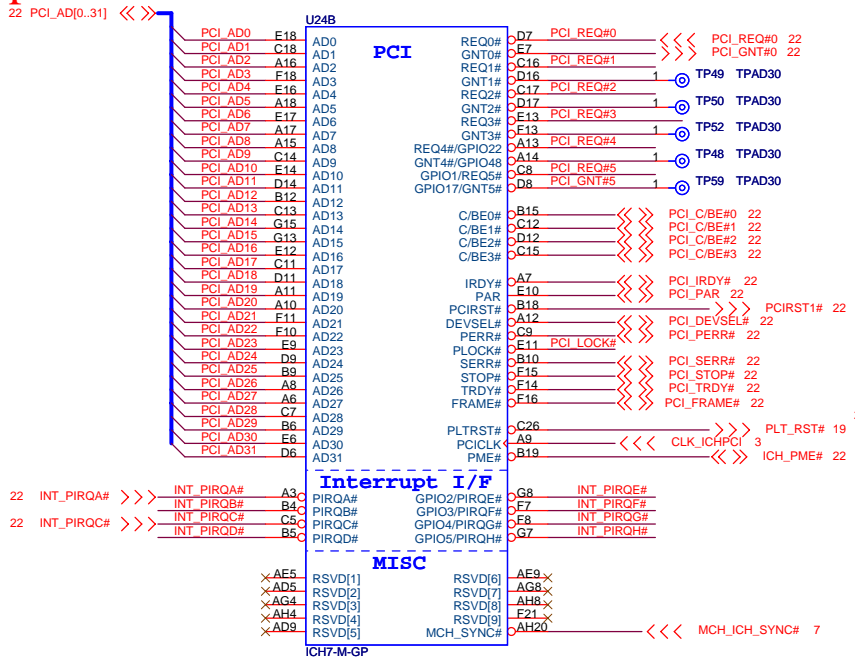
**<Core Design>**

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Title: **ICH7-M (1 of 4)**

Size: A3 Document Number: **Akita** Rev: **SD**

Date: Friday, March 31, 2006 Sheet: 16 of 39



Layout Note:  
 PCB AC coupling caps  
 need to be within 250 mils of the driver.

Default: H

LPC	H	H
PCI	H	L
SPI	L	H

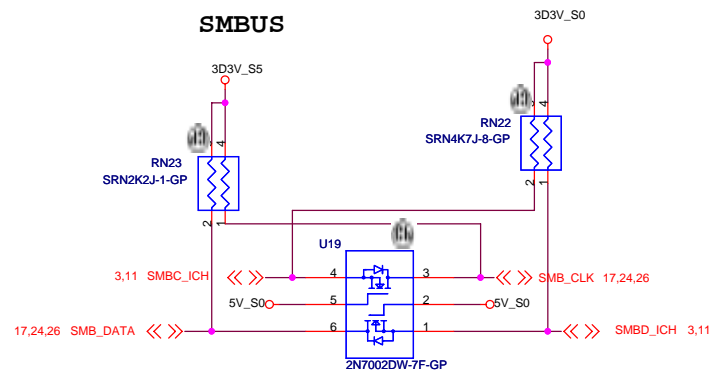
**Wistron Corporation**  
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 Taipei Hsein 221, Taiwan, R.O.C.

**ICH7-M (2 of 4)**

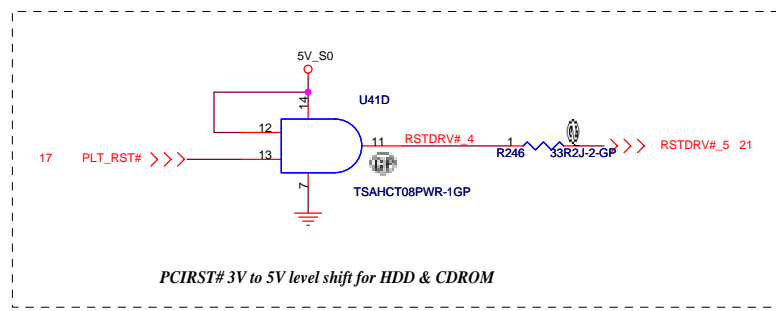
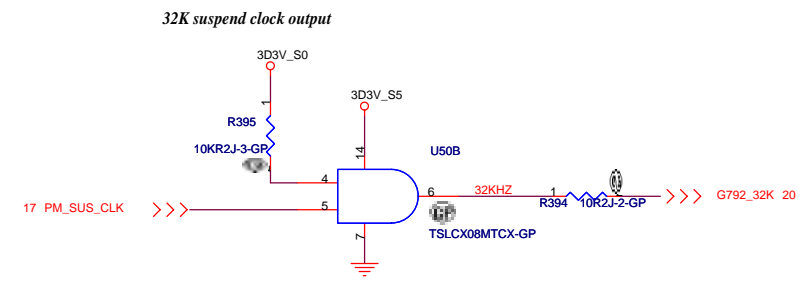
Date: Friday, March 31, 2006

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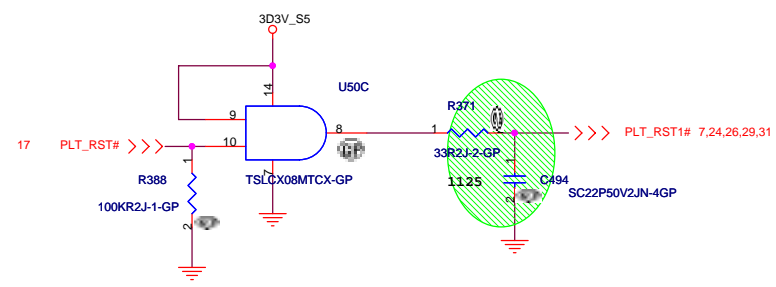




Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance



PCIRST# 3V to 5V level shift for HDD & CDROM



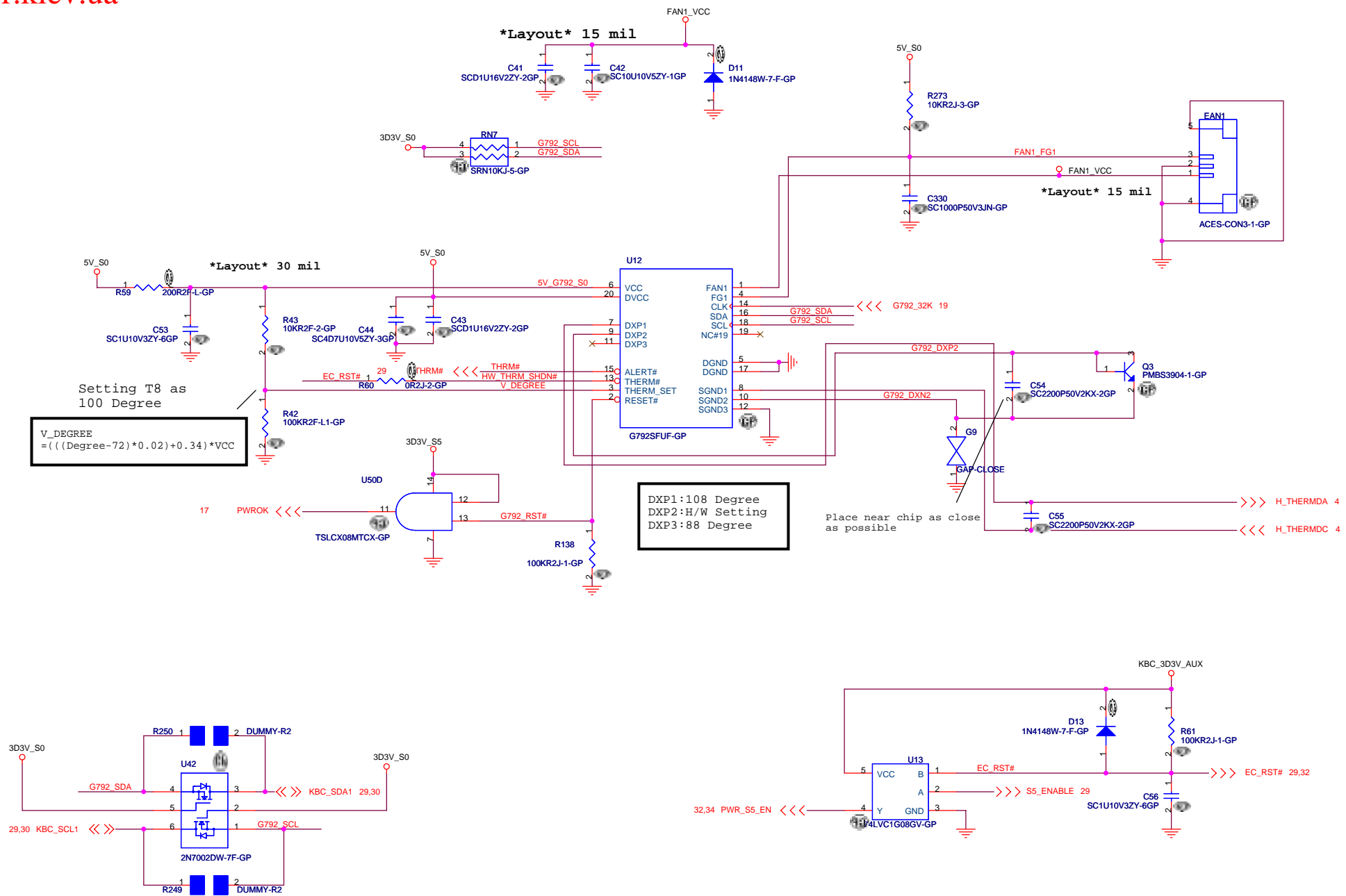
A4	VSS1[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
B11	VSS[5]	VSS[102]	R13
B14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B28	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T15
D18	VSS[16]	VSS[113]	T16
D21	VSS[17]	VSS[114]	T17
D24	VSS[18]	VSS[115]	U4
E1	VSS[19]	VSS[116]	U12
E2	VSS[20]	VSS[117]	U13
E4	VSS[21]	VSS[118]	U14
E8	VSS[22]	VSS[119]	U15
E15	VSS[23]	VSS[120]	U16
F3	VSS[24]	VSS[121]	U17
F4	VSS[25]	VSS[122]	U24
F5	VSS[26]	VSS[123]	U25
F12	VSS[27]	VSS[124]	U26
F27	VSS[28]	VSS[125]	V2
F28	VSS[29]	VSS[126]	V13
G1	VSS[30]	VSS[127]	V15
G2	VSS[31]	VSS[128]	V24
G5	VSS[32]	VSS[129]	V27
G6	VSS[33]	VSS[130]	V28
G9	VSS[34]	VSS[131]	W6
G14	VSS[35]	VSS[132]	W24
G18	VSS[36]	VSS[133]	W25
G21	VSS[37]	VSS[134]	W26
G24	VSS[38]	VSS[135]	Y3
G25	VSS[39]	VSS[136]	Y24
G26	VSS[40]	VSS[137]	Y28
H3	VSS[41]	VSS[138]	AA1
H4	VSS[42]	VSS[139]	AA24
H5	VSS[43]	VSS[140]	AA25
H24	VSS[44]	VSS[141]	AA26
H27	VSS[45]	VSS[142]	AB4
H28	VSS[46]	VSS[143]	AB6
J1	VSS[47]	VSS[144]	AB11
J2	VSS[48]	VSS[145]	AB14
J5	VSS[49]	VSS[146]	AB16
J24	VSS[50]	VSS[147]	AB19
J25	VSS[51]	VSS[148]	AB21
J26	VSS[52]	VSS[149]	AB24
K24	VSS[53]	VSS[150]	AB27
K27	VSS[54]	VSS[151]	AB28
K28	VSS[55]	VSS[152]	AC2
L13	VSS[56]	VSS[153]	AC5
L15	VSS[57]	VSS[154]	AC9
L24	VSS[58]	VSS[155]	AC11
L25	VSS[59]	VSS[156]	AD1
L26	VSS[60]	VSS[157]	AD3
M3	VSS[61]	VSS[158]	AD4
M4	VSS[62]	VSS[159]	AD7
M5	VSS[63]	VSS[160]	AD8
M12	VSS[64]	VSS[161]	AD11
M13	VSS[65]	VSS[162]	AD15
M14	VSS[66]	VSS[163]	AD19
M15	VSS[67]	VSS[164]	AD23
M16	VSS[68]	VSS[165]	AE2
M17	VSS[69]	VSS[166]	AE4
M24	VSS[70]	VSS[167]	AE8
M27	VSS[71]	VSS[168]	AE11
M28	VSS[72]	VSS[169]	AE18
N1	VSS[73]	VSS[170]	AE21
N2	VSS[74]	VSS[171]	AE24
N5	VSS[75]	VSS[172]	AE25
N6	VSS[76]	VSS[173]	AF2
N11	VSS[77]	VSS[174]	AF4
N12	VSS[78]	VSS[175]	AF8
N13	VSS[79]	VSS[176]	AF11
N14	VSS[80]	VSS[177]	AF21
N15	VSS[81]	VSS[178]	AF27
N16	VSS[82]	VSS[179]	AF28
N17	VSS[83]	VSS[180]	AG3
N18	VSS[84]	VSS[181]	AG7
N24	VSS[85]	VSS[182]	AG11
N25	VSS[86]	VSS[183]	AG17
N26	VSS[87]	VSS[184]	AG20
P3	VSS[88]	VSS[185]	AG25
P4	VSS[89]	VSS[186]	AH1
P12	VSS[90]	VSS[187]	AH3
P13	VSS[91]	VSS[188]	AH7
P14	VSS[92]	VSS[189]	AH12
P15	VSS[93]	VSS[190]	AH23
P16	VSS[94]	VSS[191]	AH27
P17	VSS[95]	VSS[192]	
P24	VSS[96]	VSS[193]	
P27	VSS[97]	VSS[194]	

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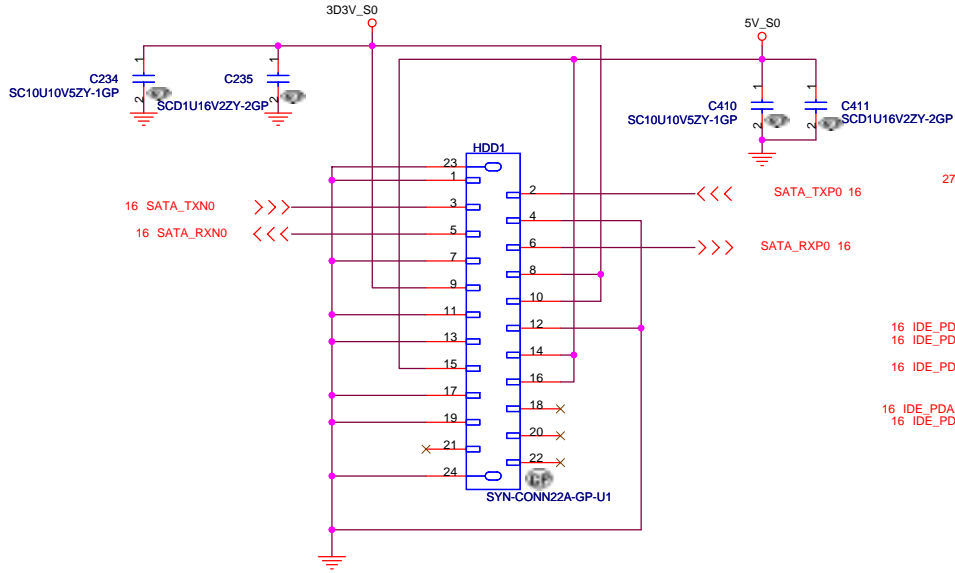
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Title: ICH7-M (4 of 4)

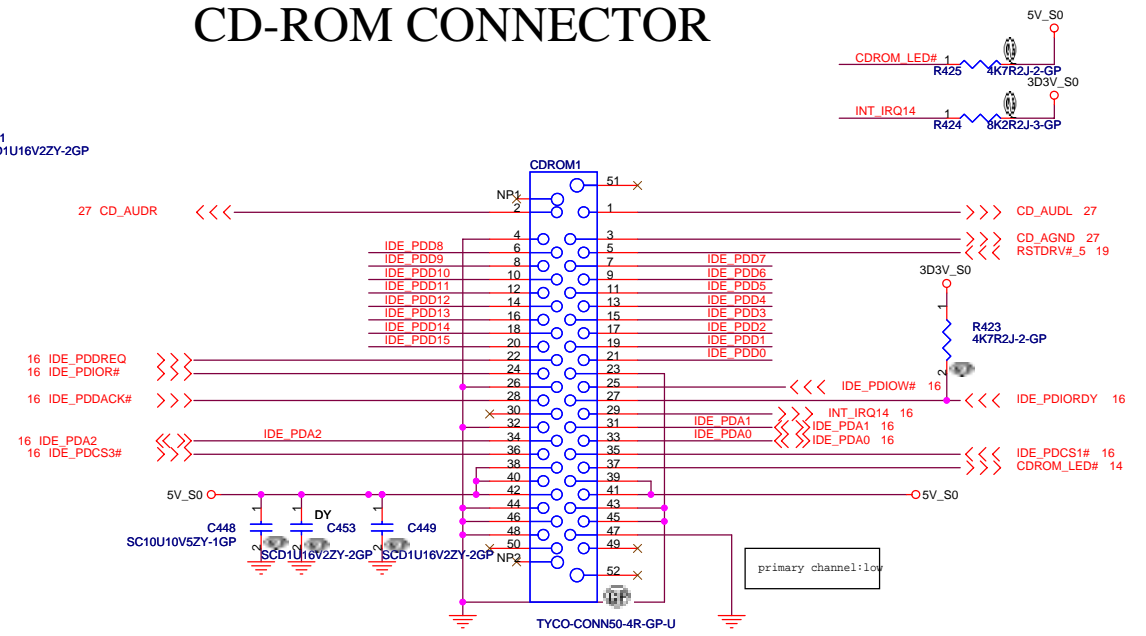
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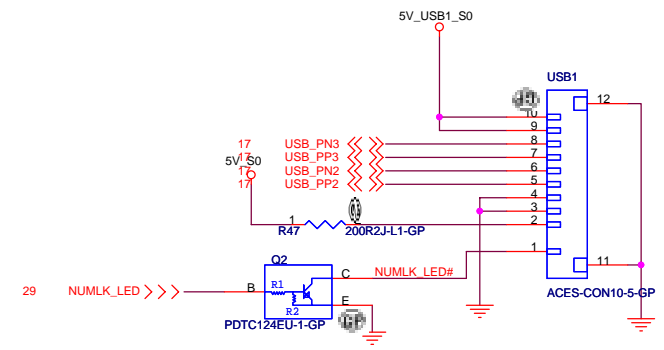
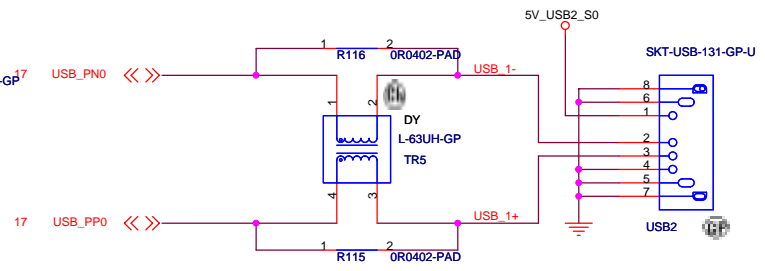
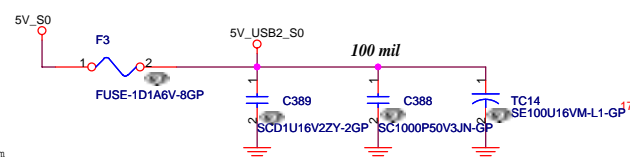
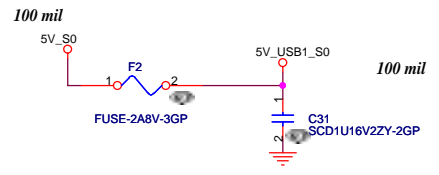
# SATA HD Connector



# CD-ROM CONNECTOR



# USB PORT



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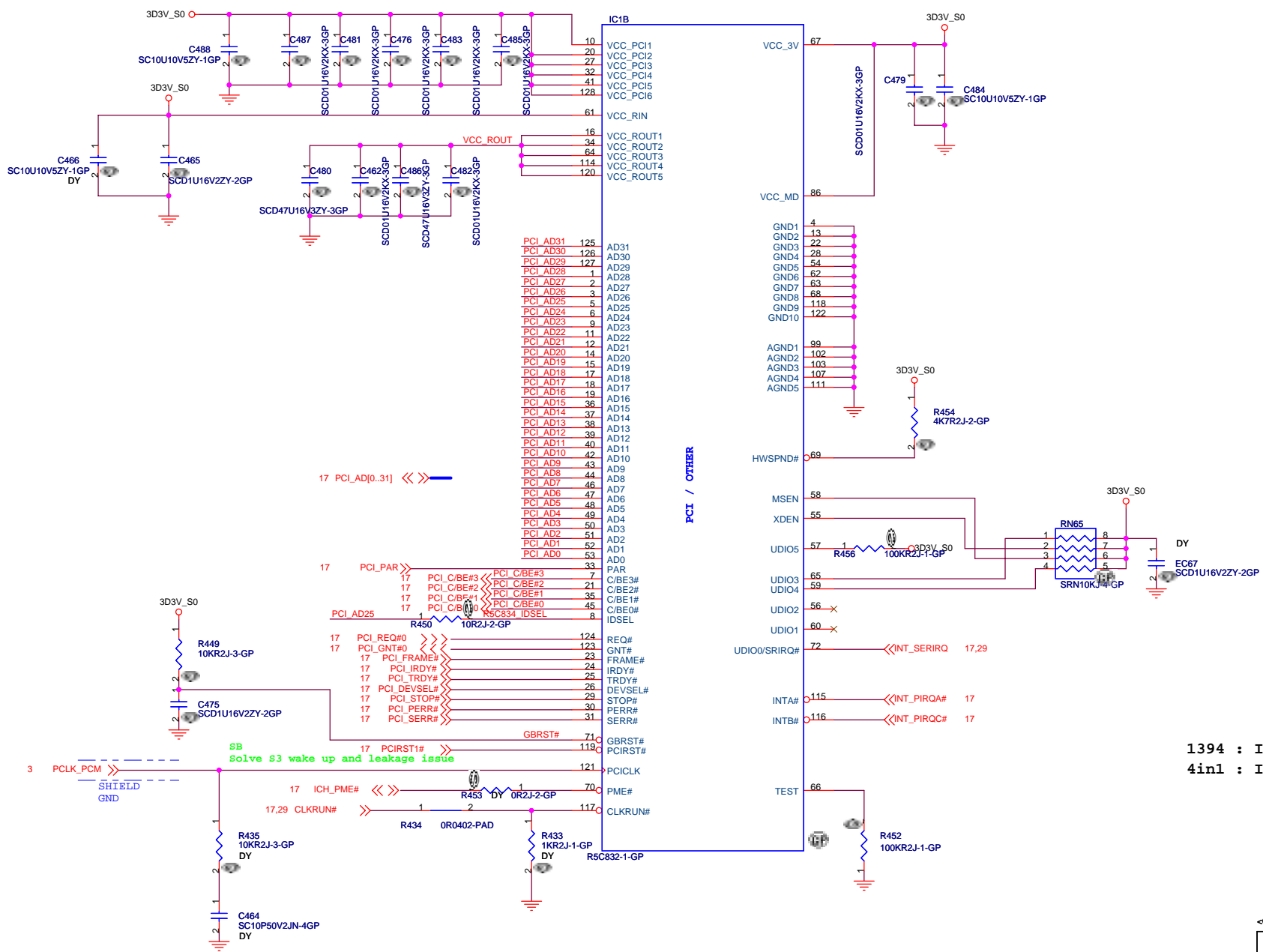
<b>緯創資通</b>		<b>Wistron Corporation</b>	
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<b>HD/CDROM</b>			
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D

C

B

A



1394 : INTA#  
4in1 : INTB#

<Core Design>

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<b>R5C832/PCI</b>		
Title		
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	<b>Akita</b>	<b>SD</b>
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D

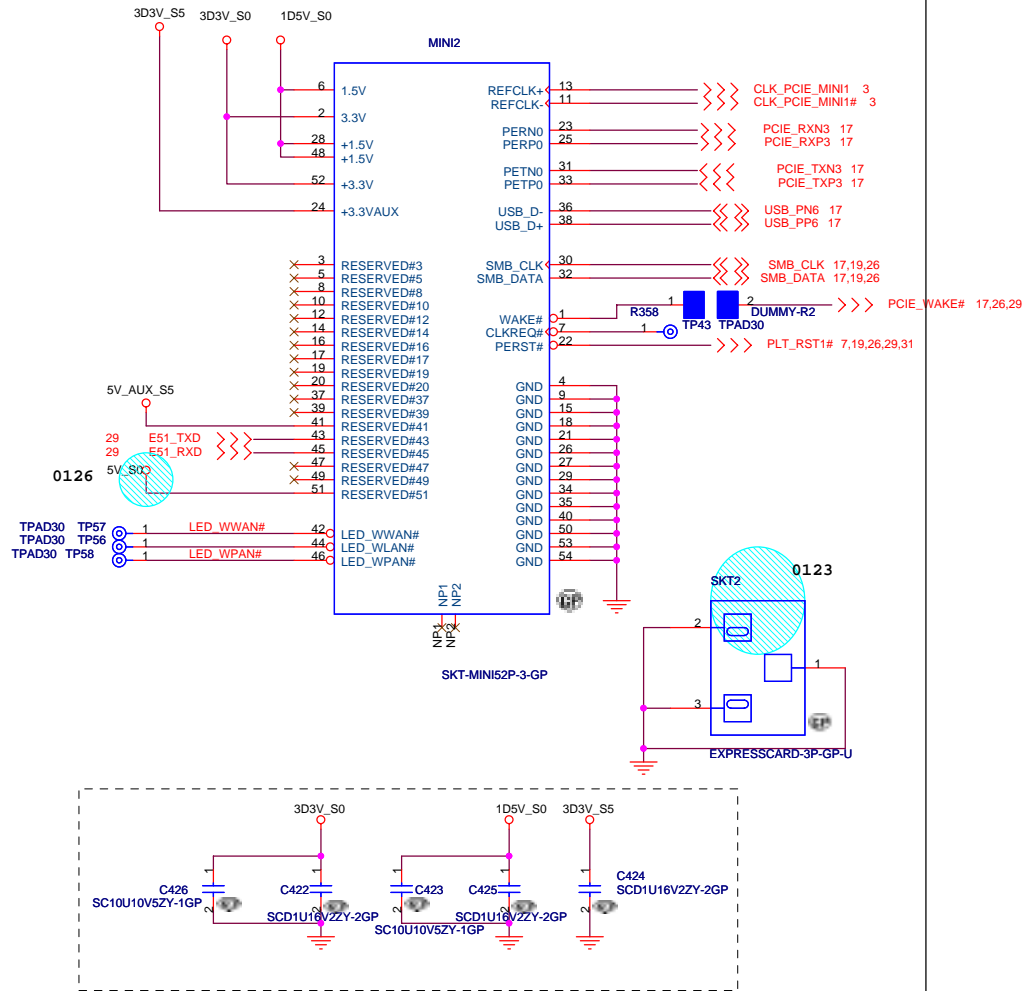
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B

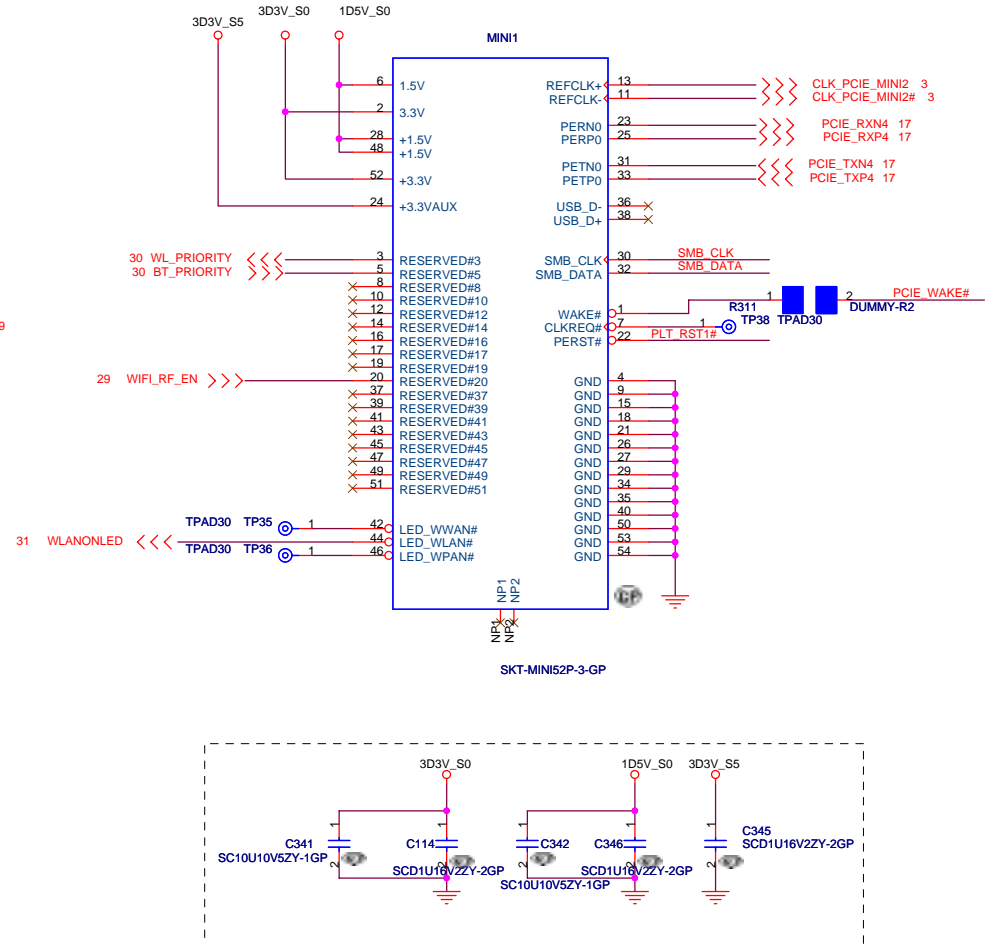
A



# Mini Card Connector



# Mini Card Connector 2



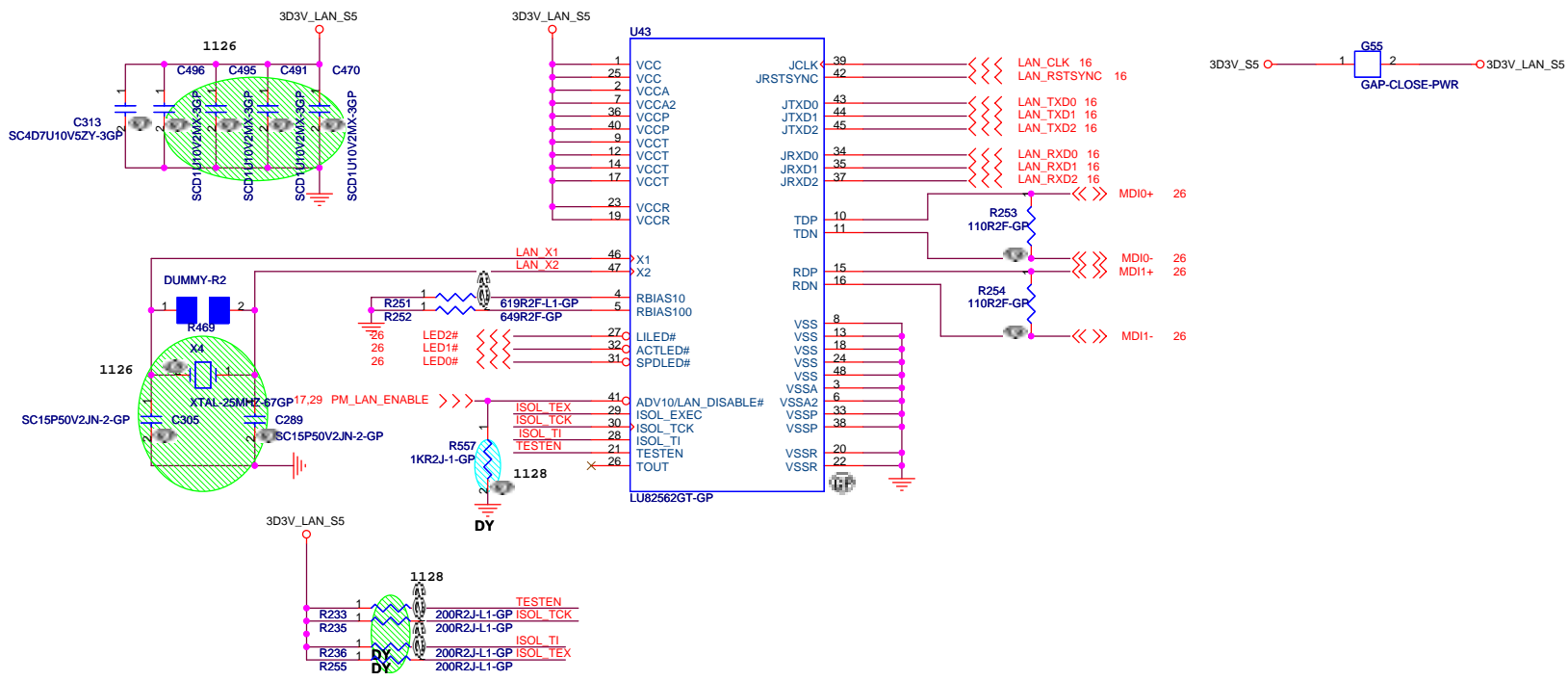
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Title: **MINI CARD CONN.**

Size A3 Document Number: **Akita** Rev: **SD**

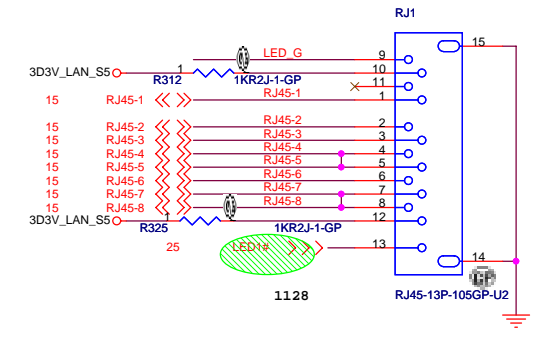
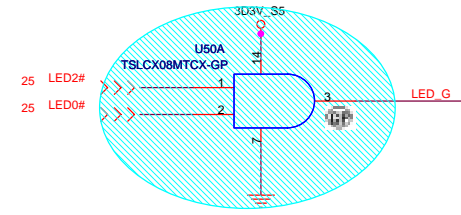
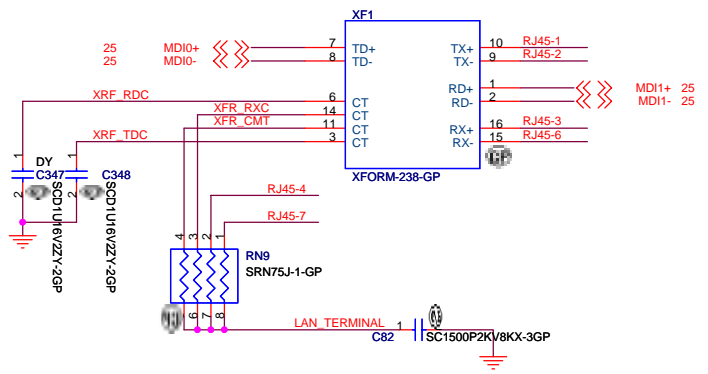
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Off : Link 10 Mbps  
 Green : Link 100 Mbps  
 Orange : Link 1000 Mbps

### 10/100M Lan Transformer

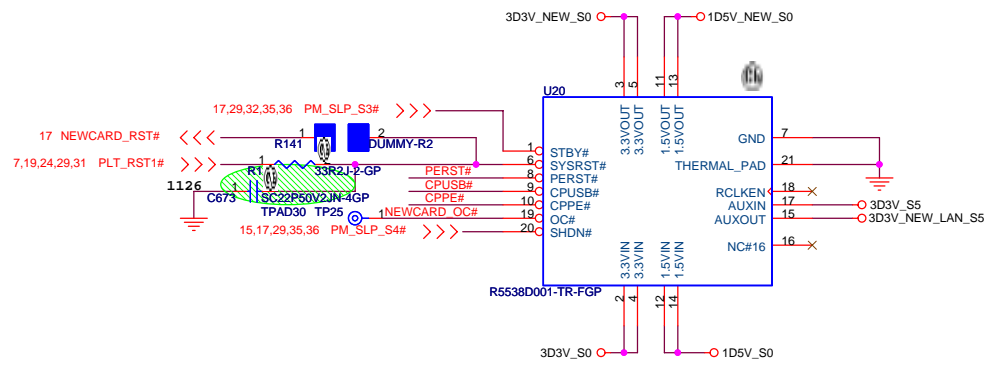
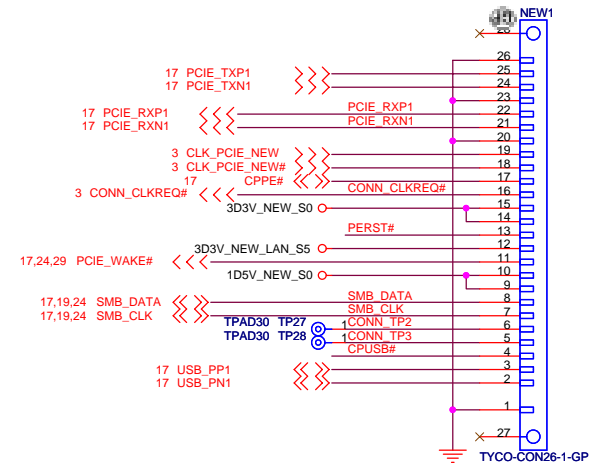
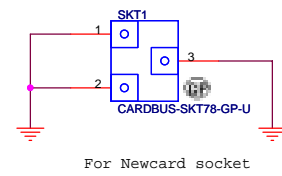
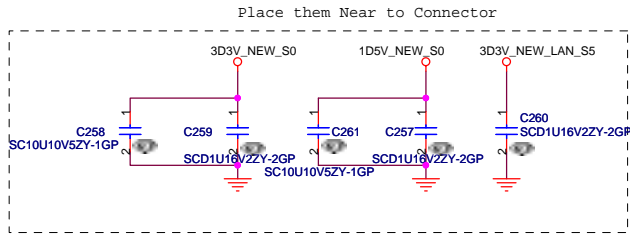
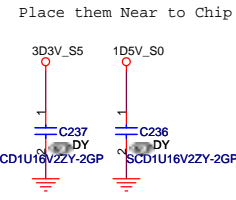
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



Green : Link up  
 Blinking : TX/RX activity

PIN09 : GREEN  
 PIN11 : ORANGE  
 PIN13 : YELLOW

### NEWCARD Connector



<Core Design>

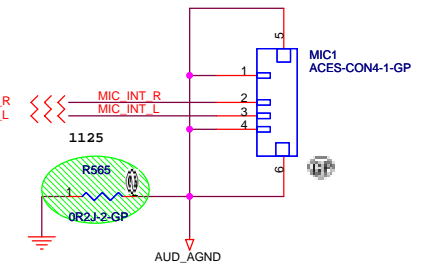
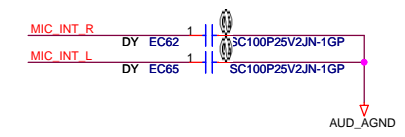
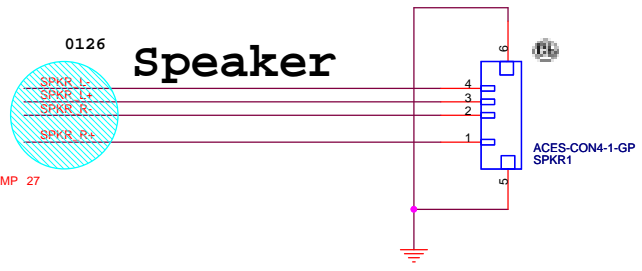
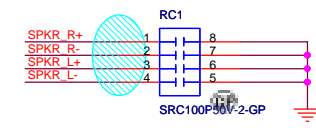
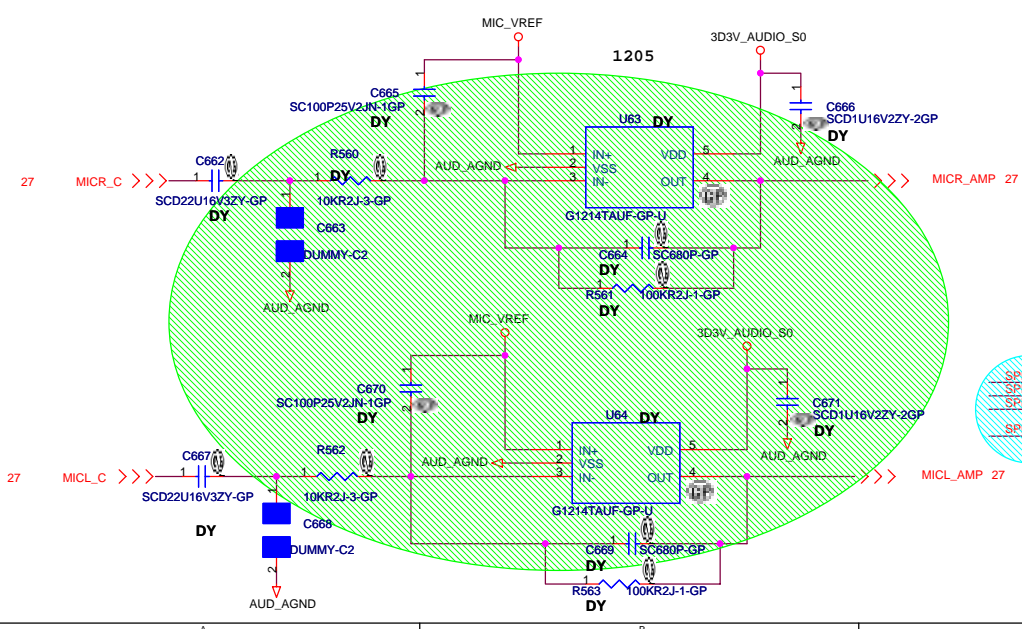
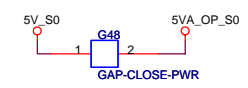
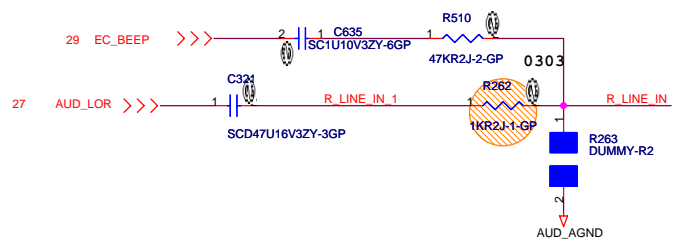
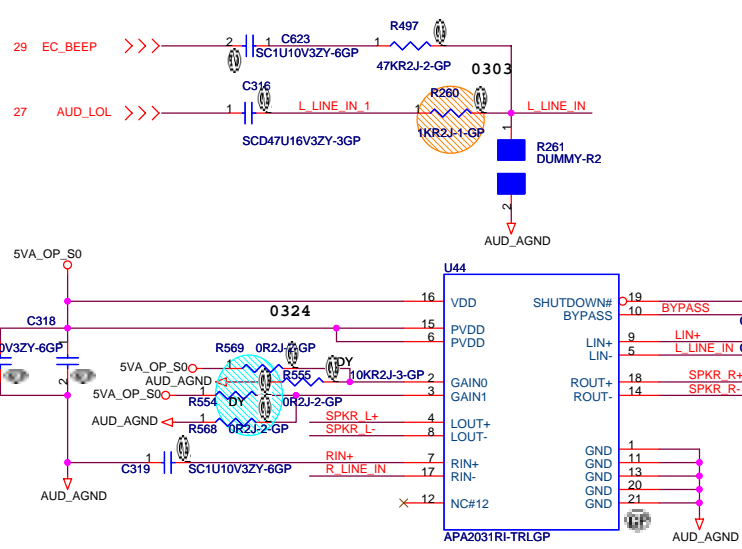
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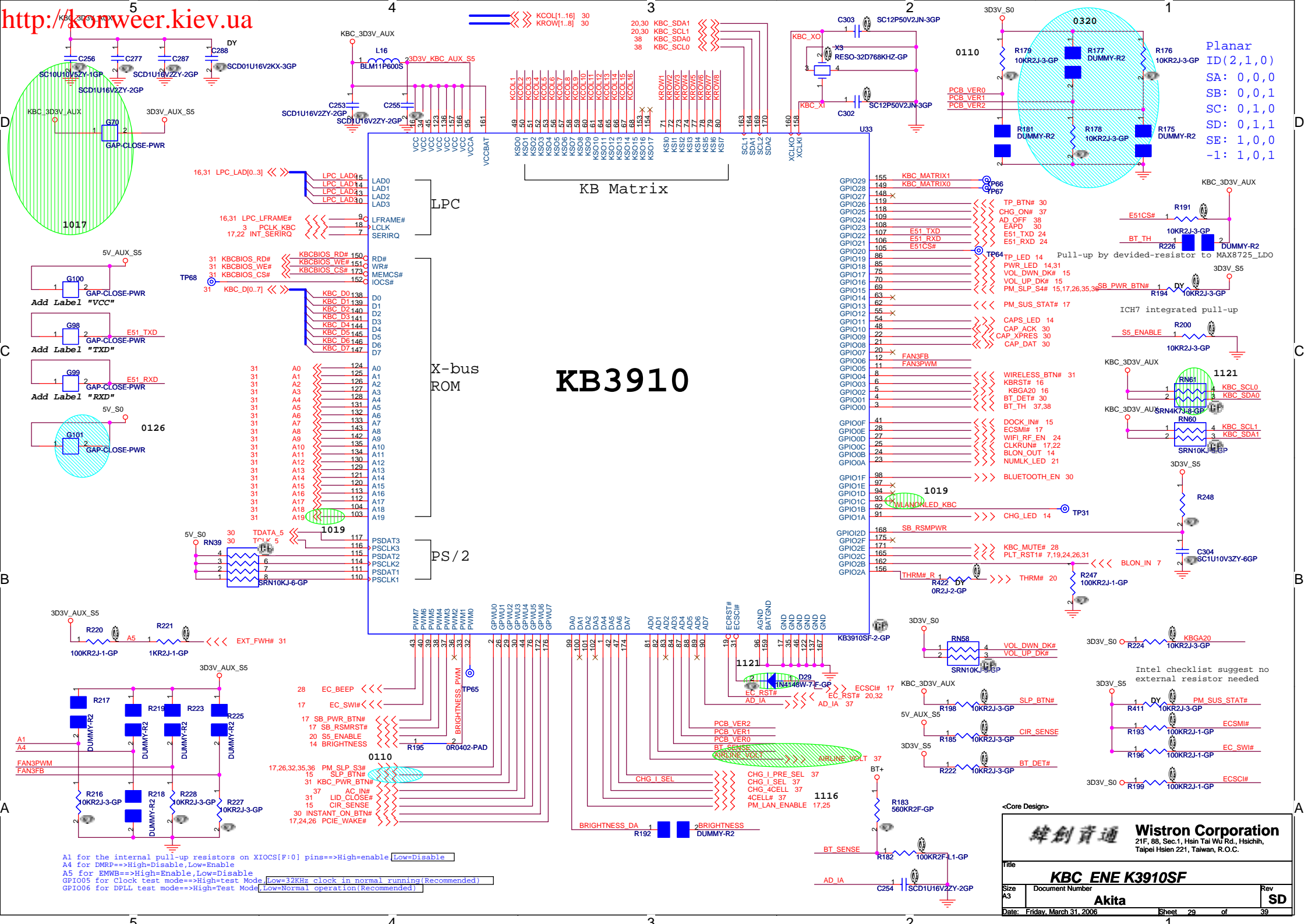
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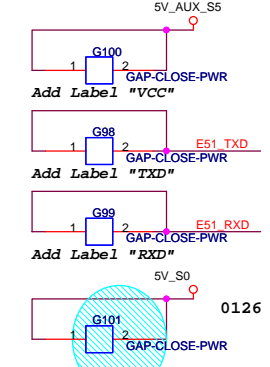






Planar ID(2,1,0)  
SA: 0,0,0  
SB: 0,0,1  
SC: 0,1,0  
SD: 0,1,1  
SE: 1,0,0  
-1: 1,0,1

# KB3910



A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable Low=Disable  
A4 for DMRP==>High=Disable, Low=Enable  
A5 for EMWB==>High=Enable, Low=Disable  
GPIO05 for Clock test mode==>High=Test Mode Low=32KHz clock in normal running(Recommended)  
GPIO06 for DPLL test mode==>High=Test Mode Low=Normal operation(Recommended)

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**KBC ENE K3910SF**

Size A3 Document Number Akita Rev SD

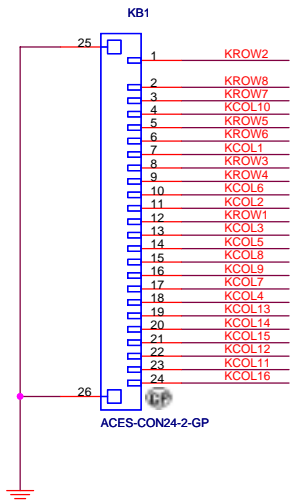
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### Internal Keyboard Connector

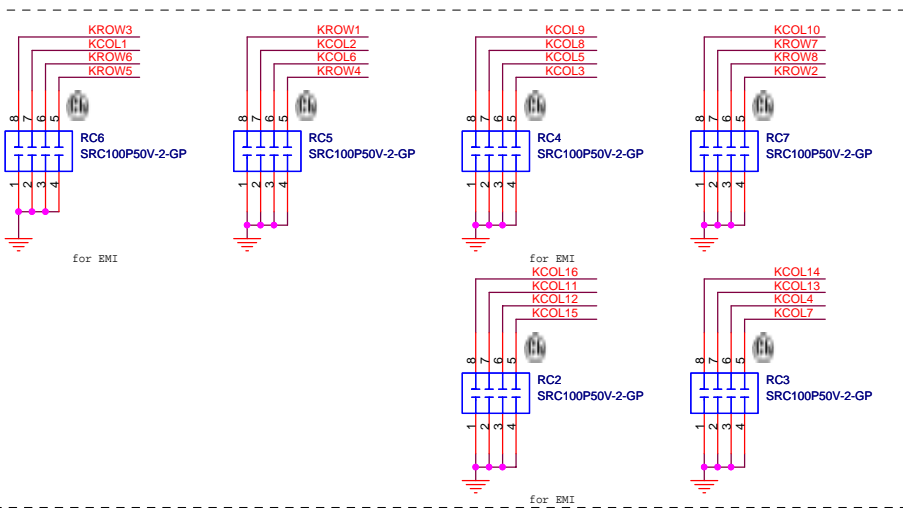
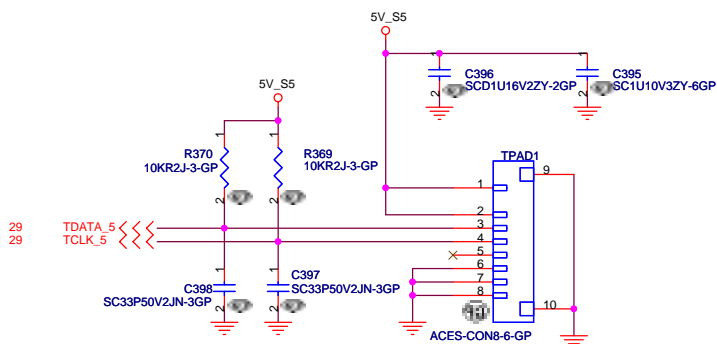
29 KROW[1..8] <<< <<<  
 29 KCOL[1..16] <<< <<<

Keyboard matrix ( from vendor )

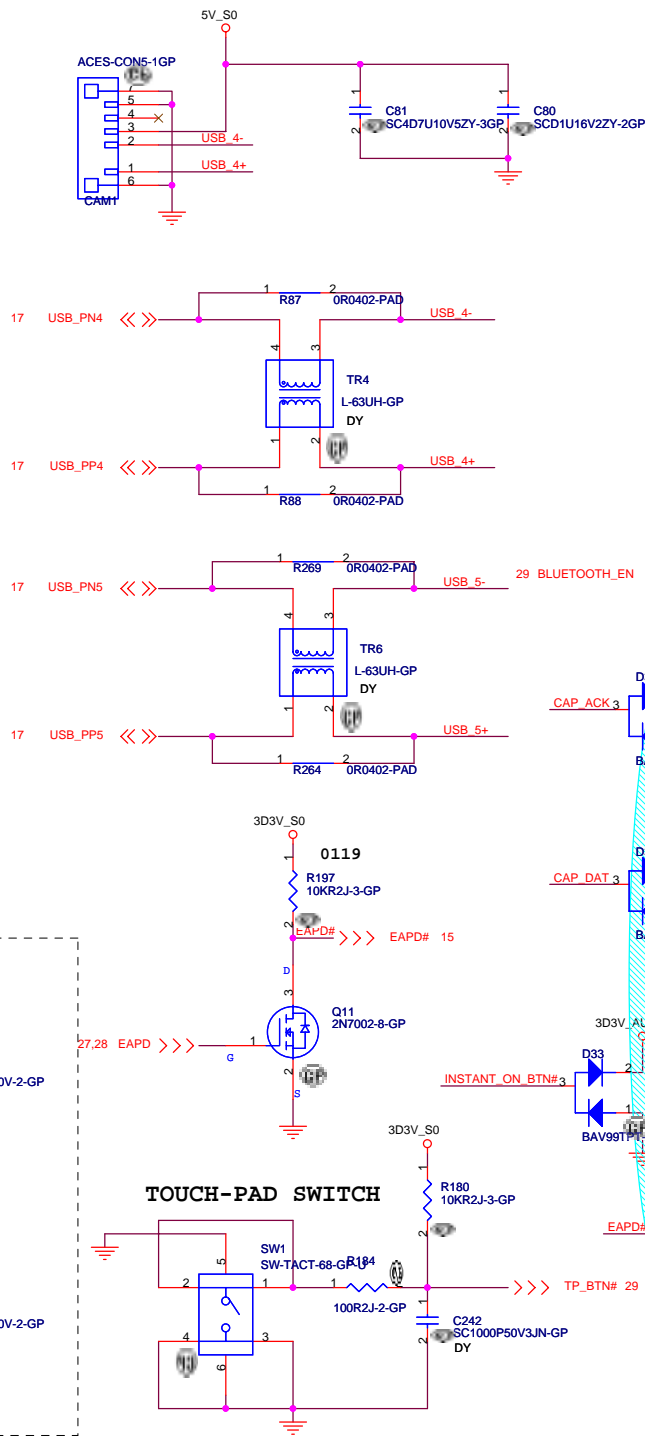
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



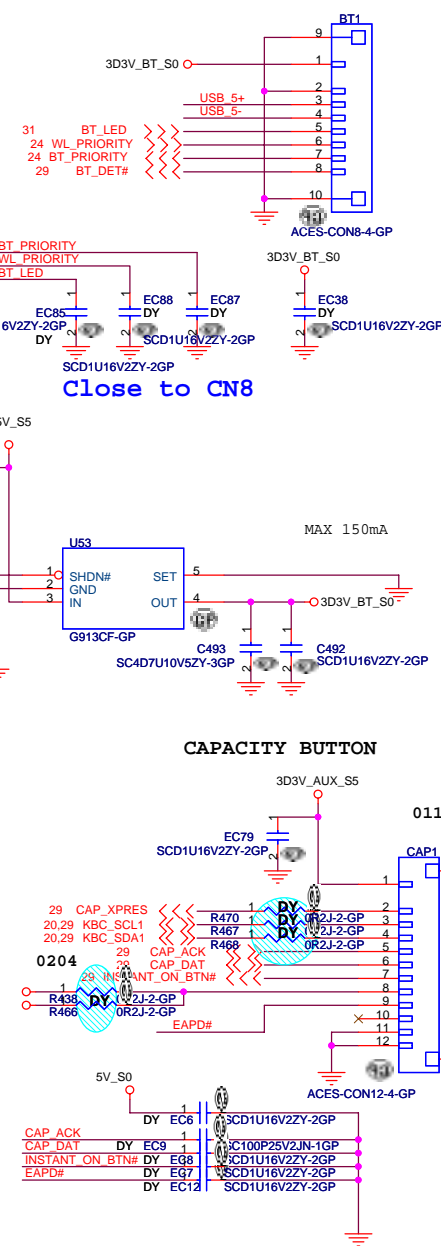
### TouchPad Connector



## CAMERA

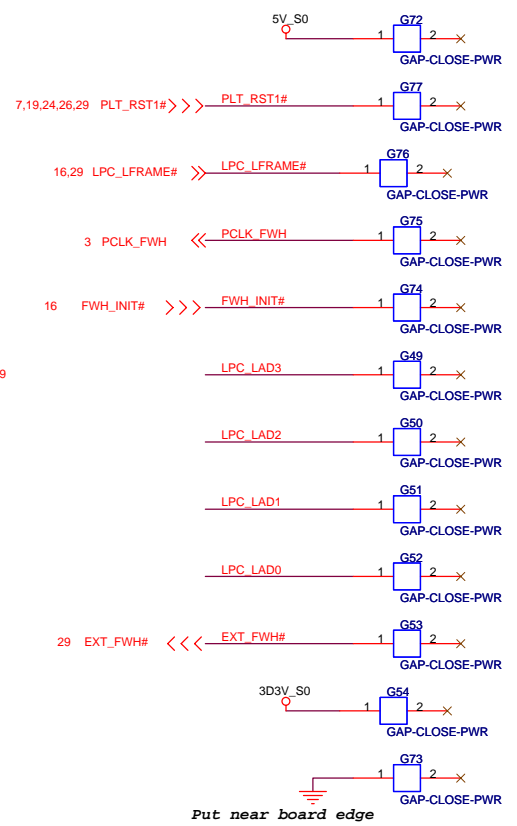
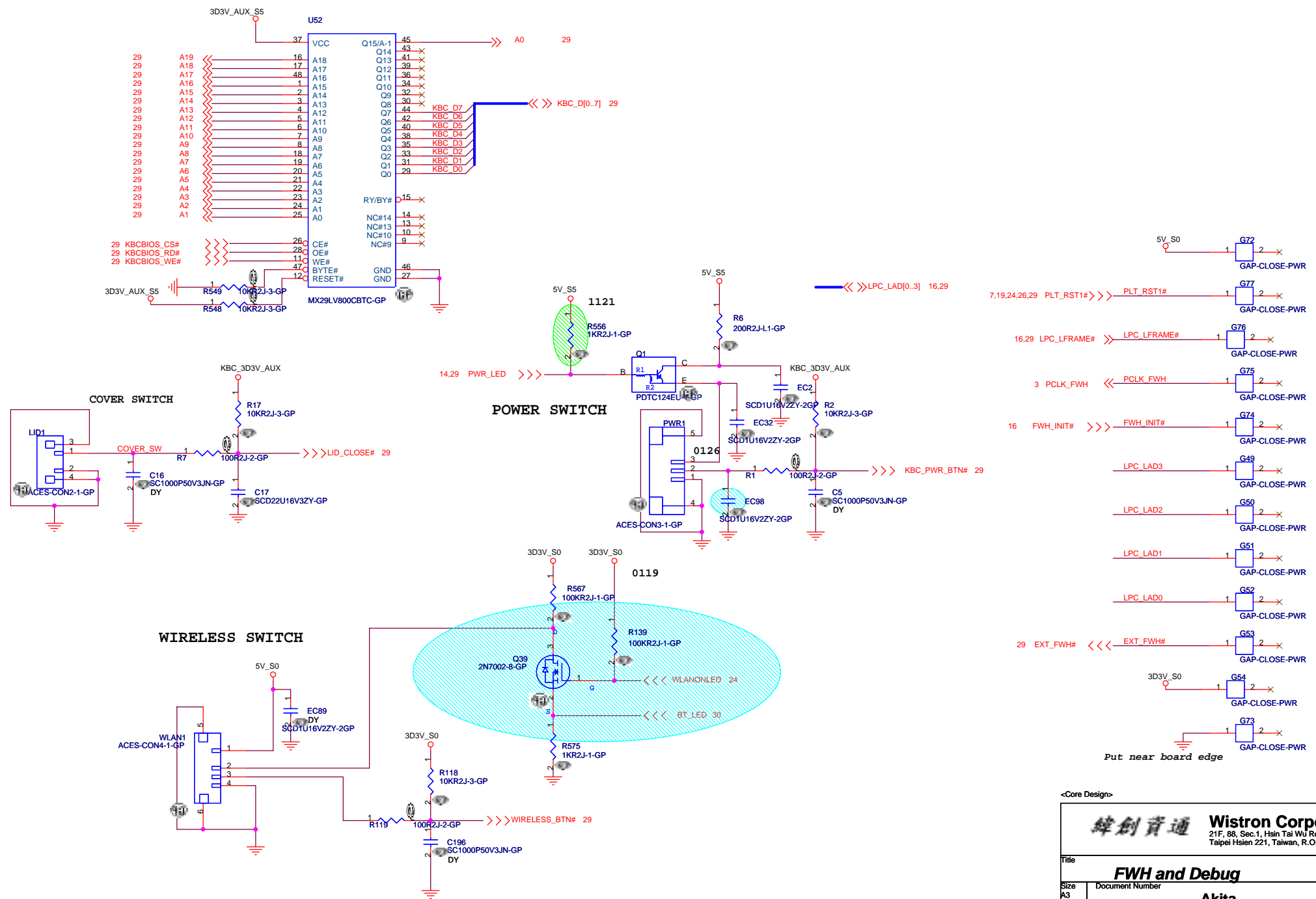


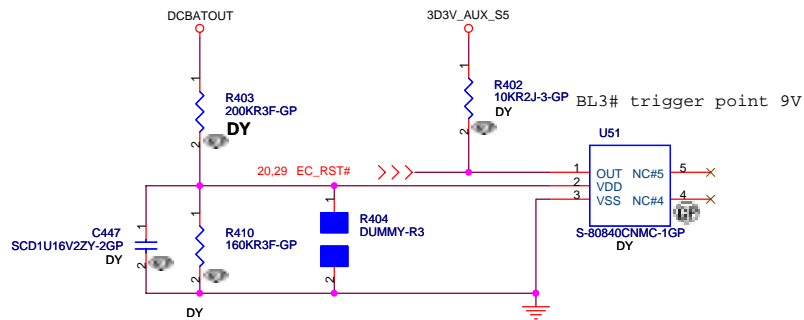
## Blue thumb



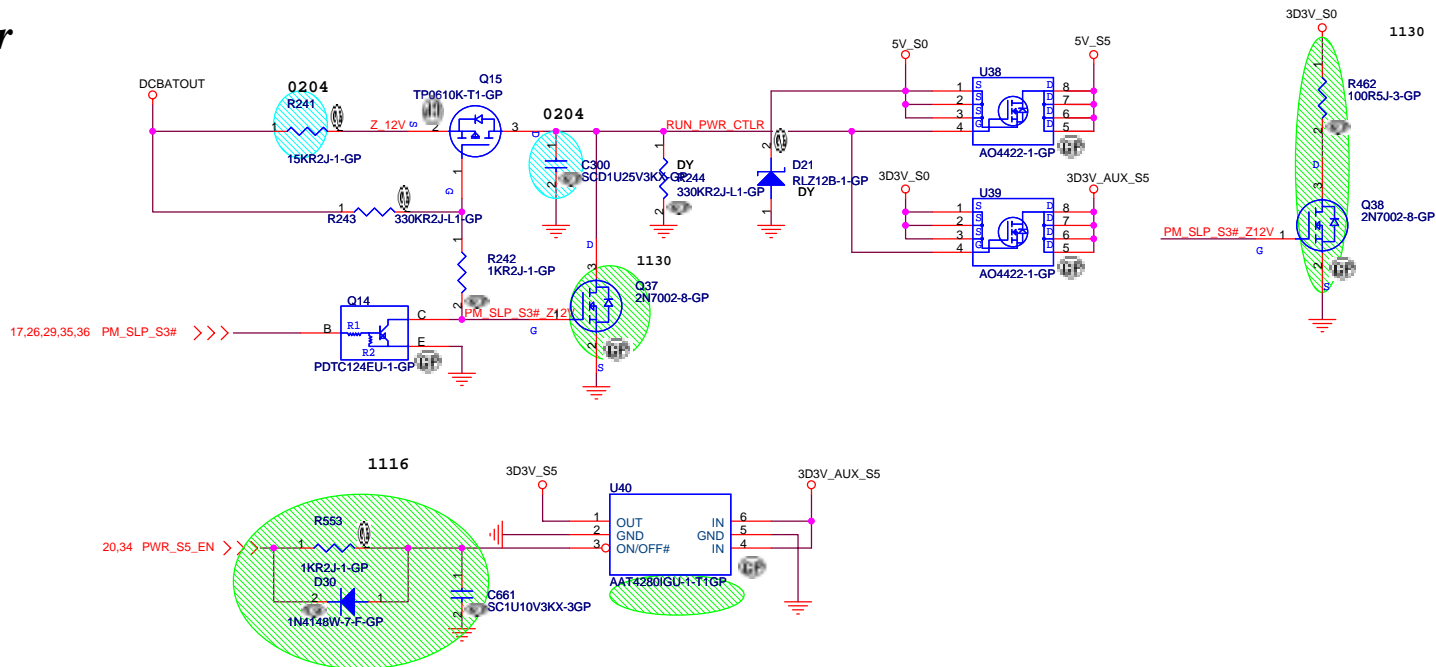
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<b>KeyBoard-CONN</b>			
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## Run Power





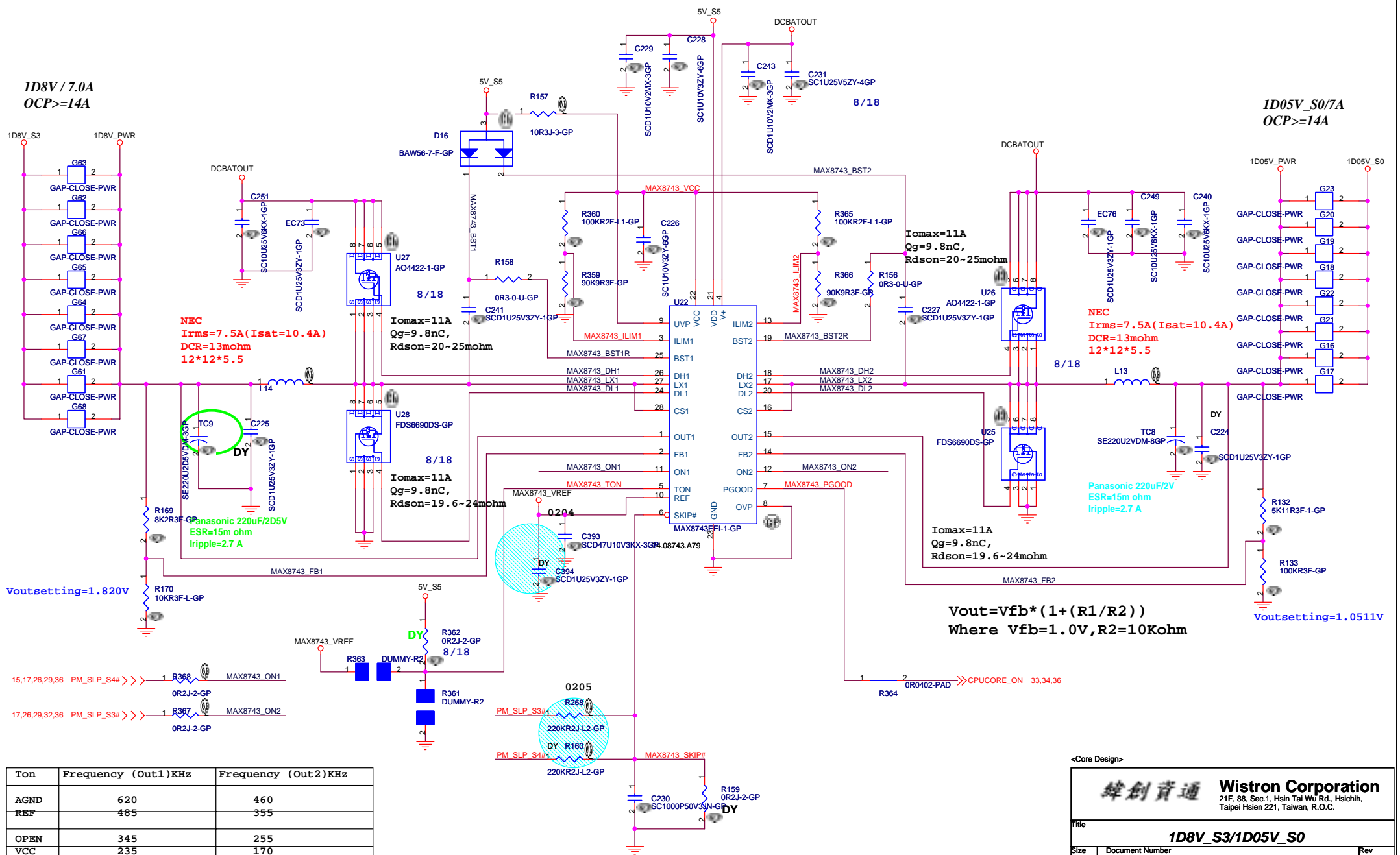


$I_{ocp}=7.0*2 = 14A$   
 $R_{ds,on}=17m\ ohm$   
 $V_{cs1}=I_{ocp}*R_{ds,on}=238mV$   
 $VILIM=V_{cs1}/0.1=2.38V$

$I_{ocp}=7.0*2 = 14A$   
 $R_{ds,on}=17m\ ohm$   
 $V_{cs1}=I_{ocp}*R_{ds,on}=238mV$   
 $VILIM=V_{cs1}/0.1=2.38V$

**ID8V / 7.0A**  
**OCp>=14A**

**ID05V\_S0/7A**  
**OCp>=14A**



**NEC**  
 $I_{rms}=7.5A (I_{sat}=10.4A)$   
 $DCR=1.3mohm$   
 $12*12*5.5$

**NEC**  
 $I_{rms}=7.5A (I_{sat}=10.4A)$   
 $DCR=1.3mohm$   
 $12*12*5.5$

$V_{out} = V_{fb} * (1 + (R1/R2))$   
 Where  $V_{fb}=1.0V, R2=10Kohm$

Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

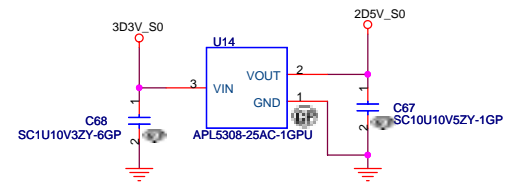
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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **1D8V\_S3/1D05V\_S0**

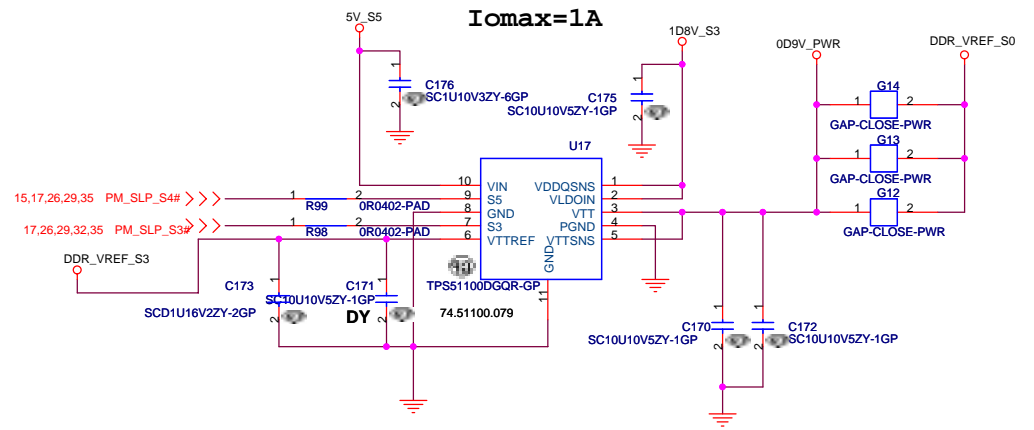
Size A3 Document Number **Akita** Rev **SD**

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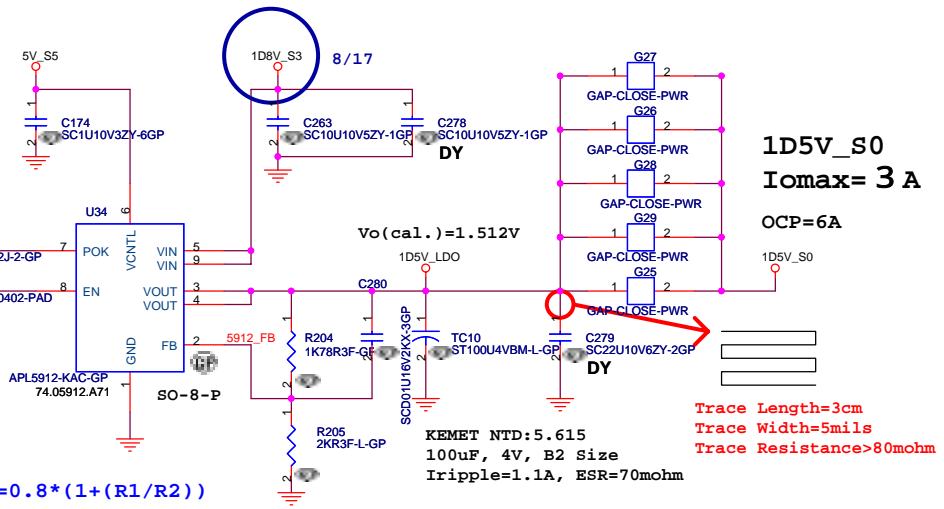
**2D5V\_S0**  
**Iomax=300mA**

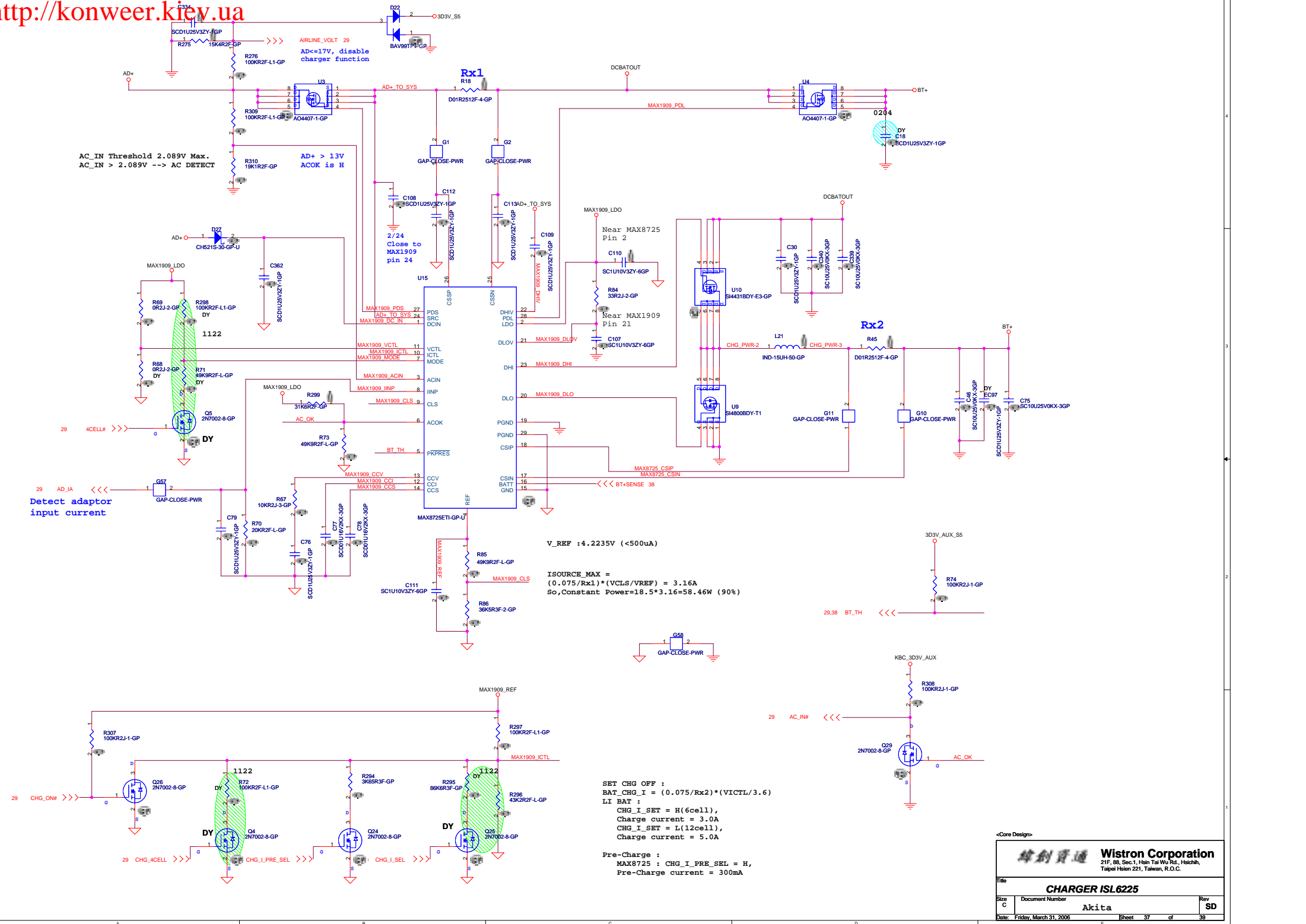


**0D9V**  
**Iomax=1A**



$V_o = 0.8 * (1 + (R1/R2))$





AC\_IN Threshold 2.089V Max.  
AC\_IN > 2.089V --> AC DETECT

AIRLINE\_VOLT 29  
AD<=17V, disable  
charger function

AD+ > 13V  
ACOK is H

Detect adaptor  
input current

V\_REF : 4.2235V (<500uA)

ISOURCE\_MAX =  
(0.075/Rx1)\*(VCLs/VREF) = 3.16A  
So, Constant Power=18.5\*3.16=58.46W (90%)

SET CHG OFF :  
BAT\_CHG\_I = (0.075/Rx2)\*(VICTL/3.6)  
LI BAT :  
CHG\_I\_SET = H(6cell),  
Charge current = 3.0A  
CHG\_I\_SET = L(12cell),  
Charge current = 5.0A

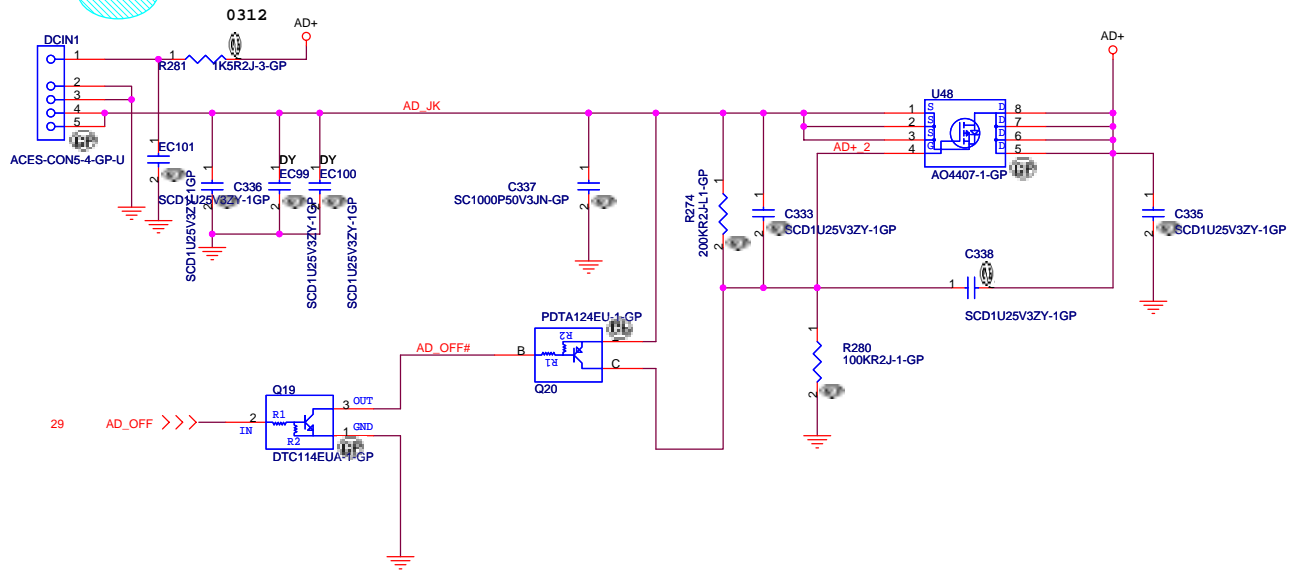
Pre-Charge :  
MAX8725 : CHG\_I\_PRE\_SEL = H,  
Pre-Charge current = 300mA

<Core Design>

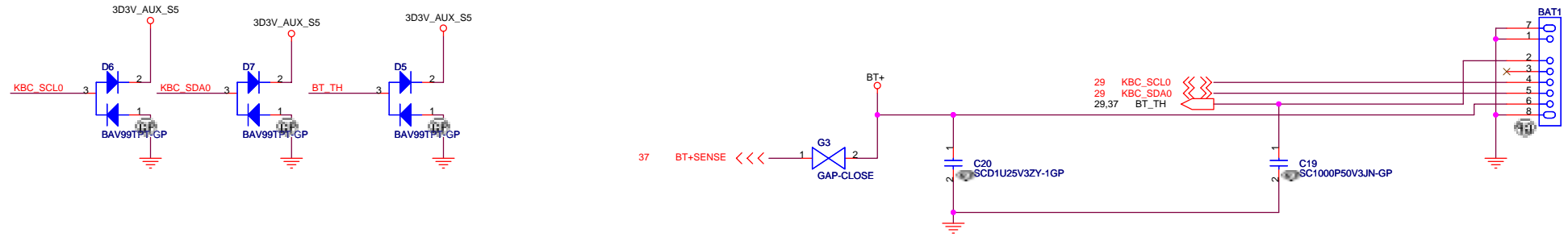
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Title	<b>CHARGER ISL6225</b>		Rev	SD
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Date:	Friday, March 31, 2006			

### Adaptor in to generate DCBATOUT



### BATTERY CONNECTOR

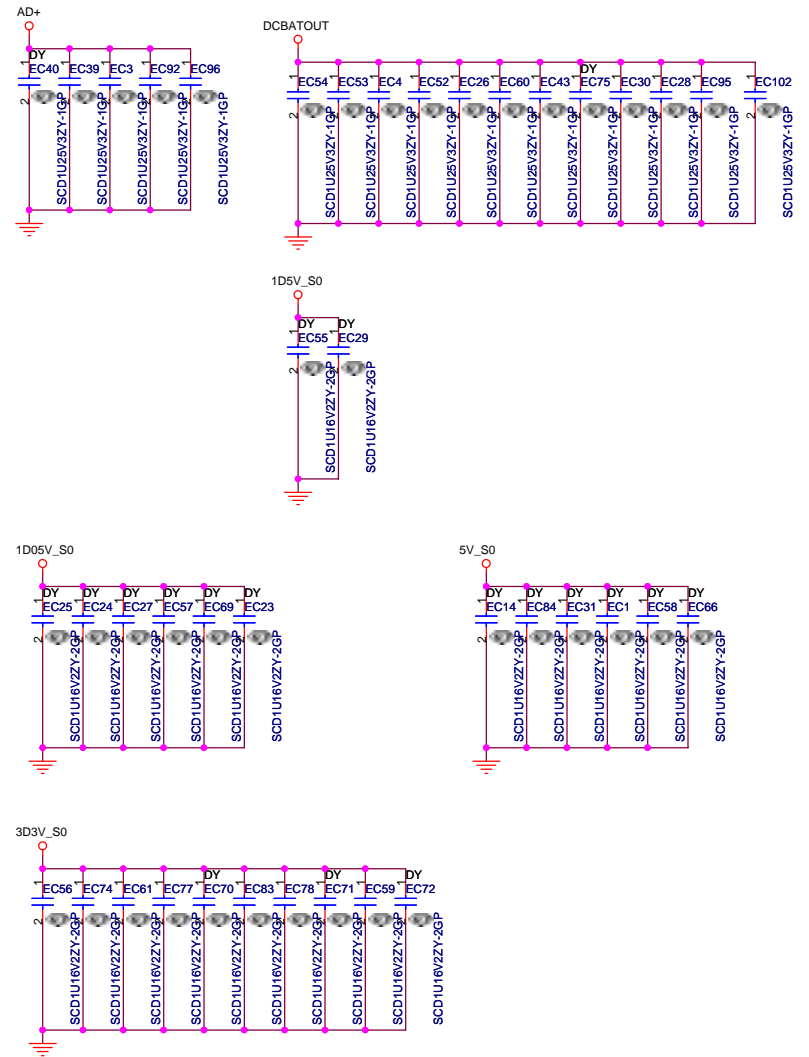
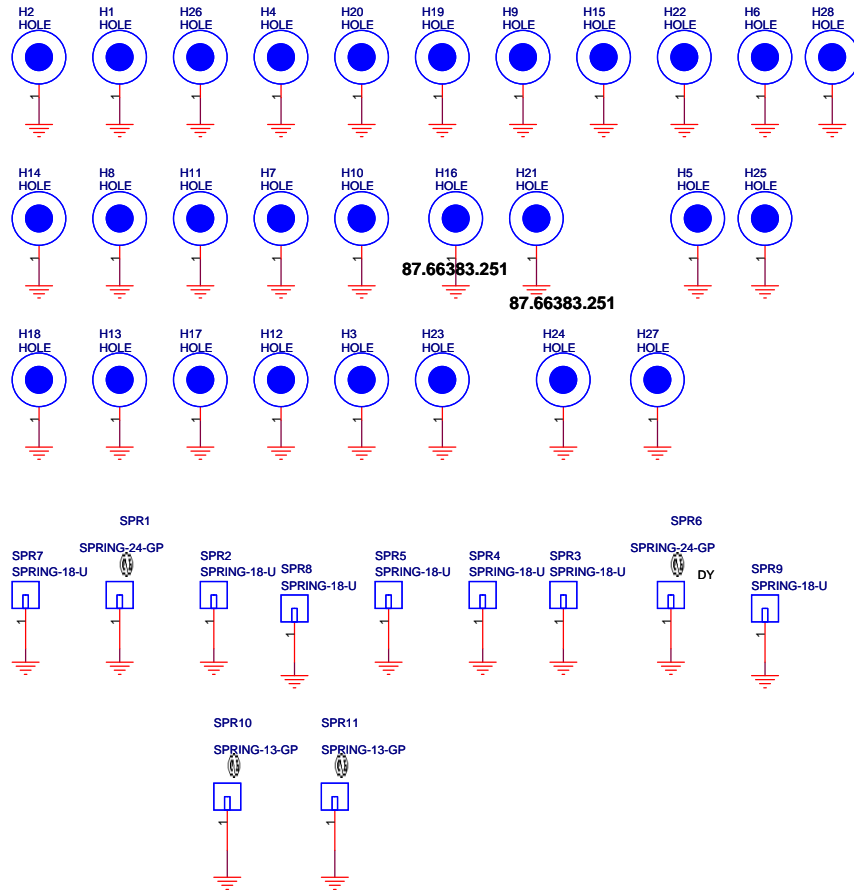


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緯創資通 **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **AD/BATT CONN**

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

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