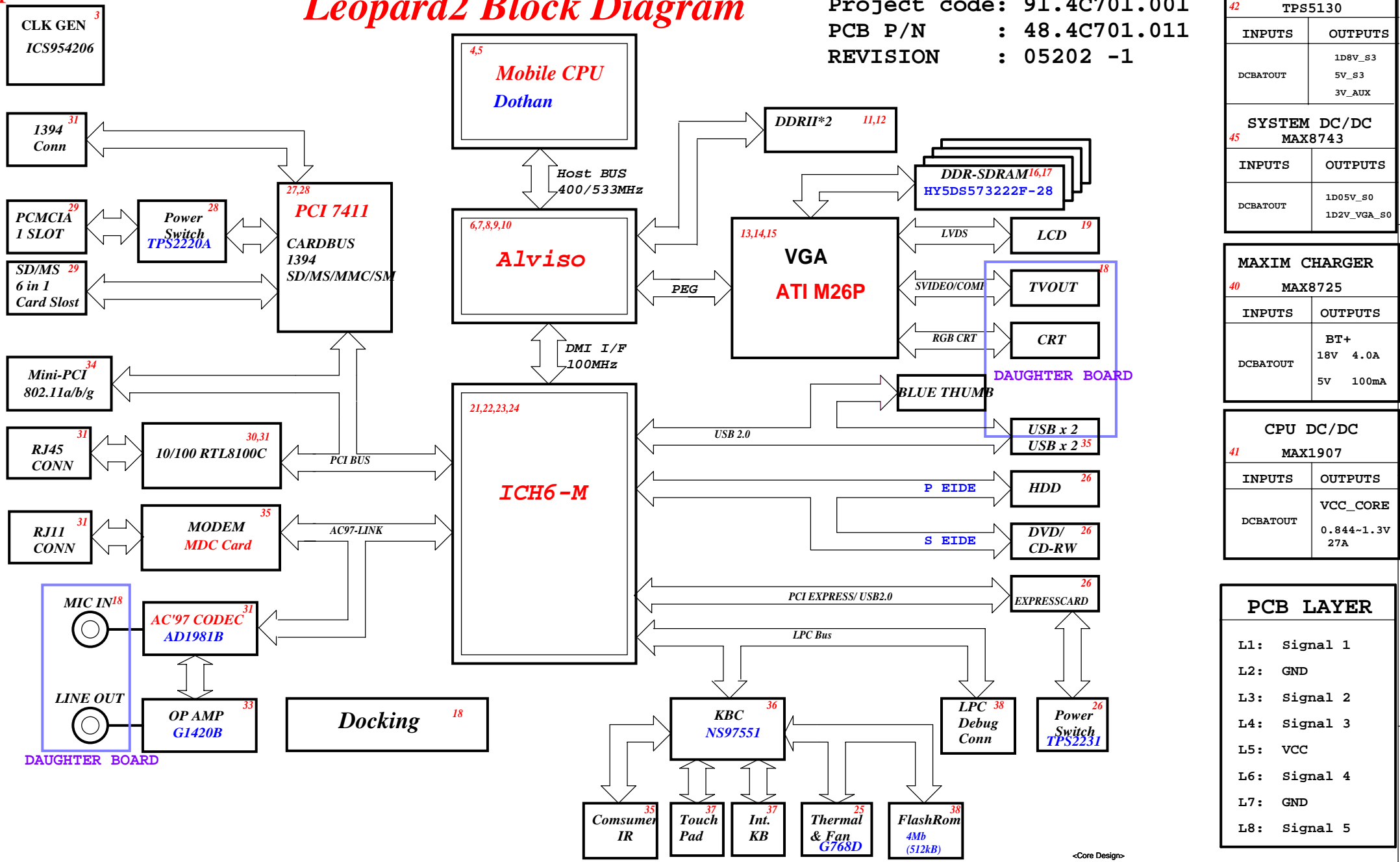


# Leopard2 Block Diagram

Project code: 91.4C701.001  
 PCB P/N : 48.4C701.011  
 REVISION : 05202 -1



SYSTEM DC/DC	
42 TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 5V_S3 3V_AUX

SYSTEM DC/DC	
45 MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_VGA_S0

MAXIM CHARGER	
40 MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC	
41 MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844-1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5

<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: A3 Document Number: **Leopard2** Rev: -1

Date: Monday, July 11, 2005 Sheet 1 of 47

**ICH6-M Integrated Pull-up and Pull-down Resistors**

ICH6-M EDS 14308 0.8v1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/PB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

**ICH6-M IDE Integrated Series Termination Resistors**

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

**Power name description**

5V\_S0= 5 Voltage power up on system work(S0 state)  
 5V\_S3= 5 Voltage suspend to RAM(S3 state)  
 5V\_S5= 5 Voltage soft off(S5 state)  
 3D3V\_S0= 3.3 Voltage power up on system work(S0 state)  
 3D3V\_S3= 3.3 Voltage suspend to RAM(S3 state)  
 3D3V\_S5= 3.3 Voltage soft off(S5 state)  
 LVDDR\_2D8V= 2.8 Voltage power up on system work(S0 state)  
 1D8V\_S3= 1.8 Voltage suspend to RAM(S3 state)  
 2D5V\_S0= 2.5 Voltage power up on system work(S0 state)

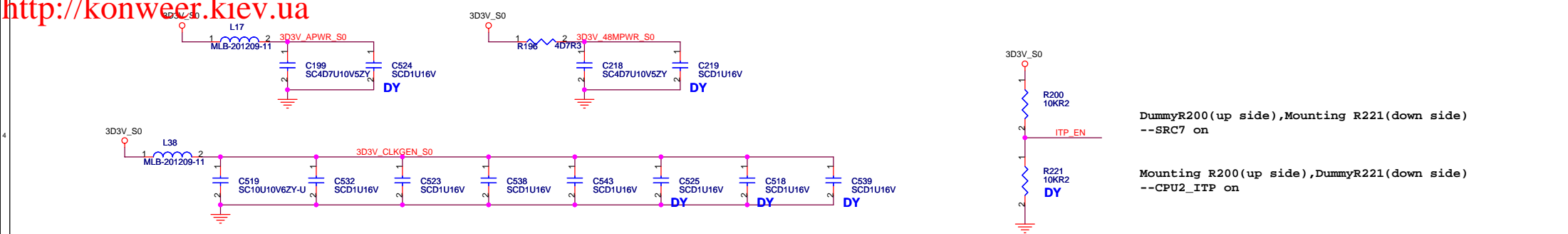
VCC\_CORE\_S0= CPU VID Voltage power up on system work(S0 state)  
 1D5V\_VCCA\_S0= 1.5 Voltage power up on system work(S0 state)  
 1D5V\_S0= 1.5 Voltage power up on system work(S0 state)  
 1D5V\_S5= 1.5 Voltage soft off(S5 state)  
 DDR\_VREF= 0.9 Voltage power up on system work(S0 state)  
 1D2V\_VGA\_S0= 1.2 Voltage power up on system work(S0 state) for VGA  
 VRAM\_VDDQ= 1.8 Voltage power up on system work(S0 state) for VRAM  
 1D05V\_S0= 1.05 Voltage power up on system work(S0 state)  
 CORE\_GMCH\_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power  
 VCCP\_GMCH\_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

**PCI RESOURCE TABLE**

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0# / GNT0#
Cardbus Controller TI7411	AD22	(CARBUS) P_INTG# (1394) P_INTF# (CARD READER) P_INTG#	REQ1# / GNT1#
LAN	AD23	P_INTE#	REQ2# / GNT2#
Blue Thumb	AD24		

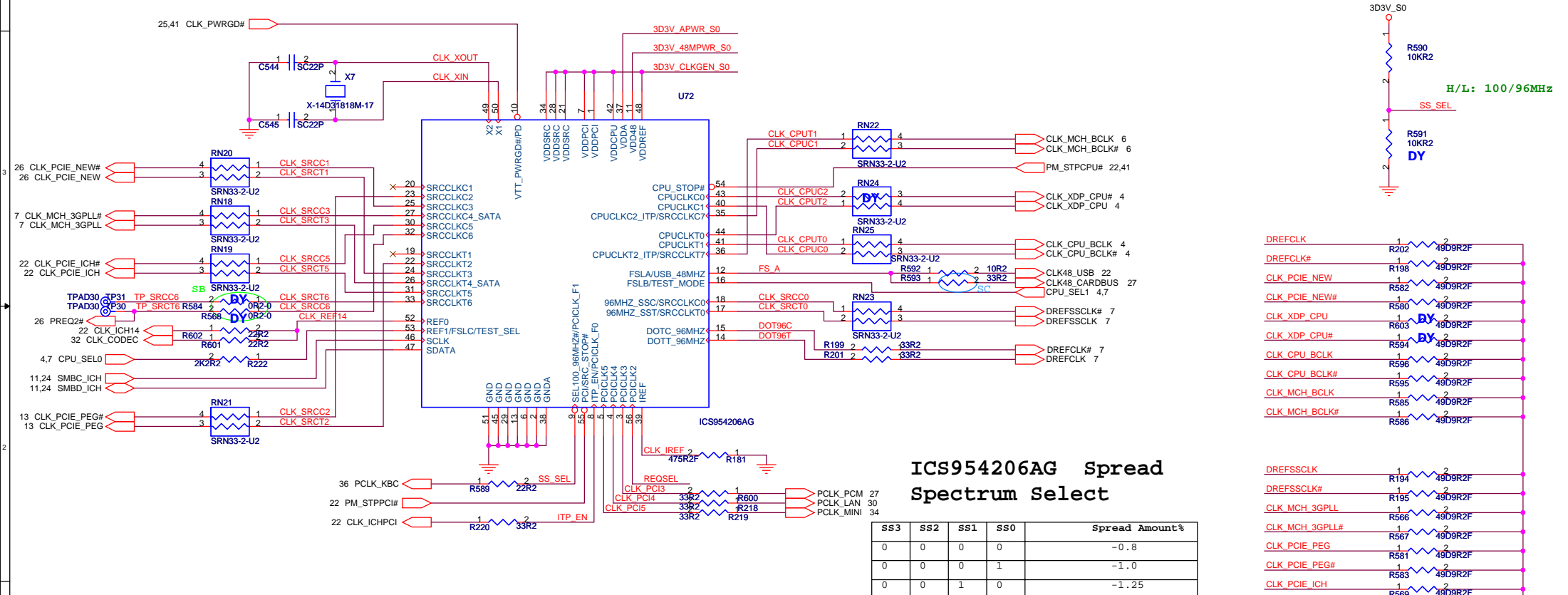
<Core Design>

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<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>			
Title		<b>ITP</b>	
Size A3	Document Number	<b>Leopard2</b>	
Date: Wednesday, July 06, 2005	Sheet 2 of 47	Rev	<b>-1</b>

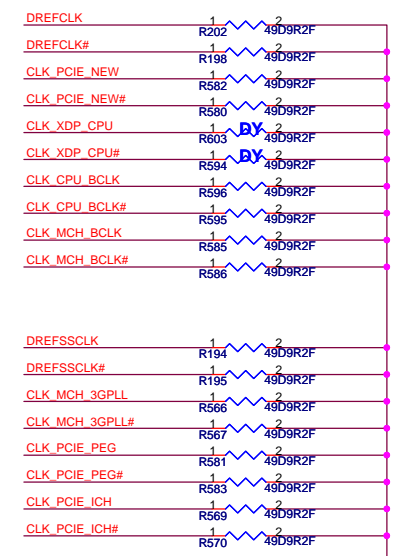


DummyR200(up side),Mounting R221(down side)  
--SRC7 on

Mounting R200(up side),DummyR221(down side)  
--CPU2\_ITP on



H/L: 100/96MHz



### ICS954206AG Spread Spectrum Select

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+0.3
1	0	0	1	+0.4
1	0	1	0	+0.5
1	0	1	1	+0.6
1	1	0	0	+0.8
1	1	0	1	+1.0
1	1	1	0	+1.25
1	1	1	1	+1.5

### NEAR CLKGEN

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

CLK\_CPU\_BCLK TP33  
CLK\_CPU\_BCLK# TPAD30  
close to CPU TP32  
TPAD30

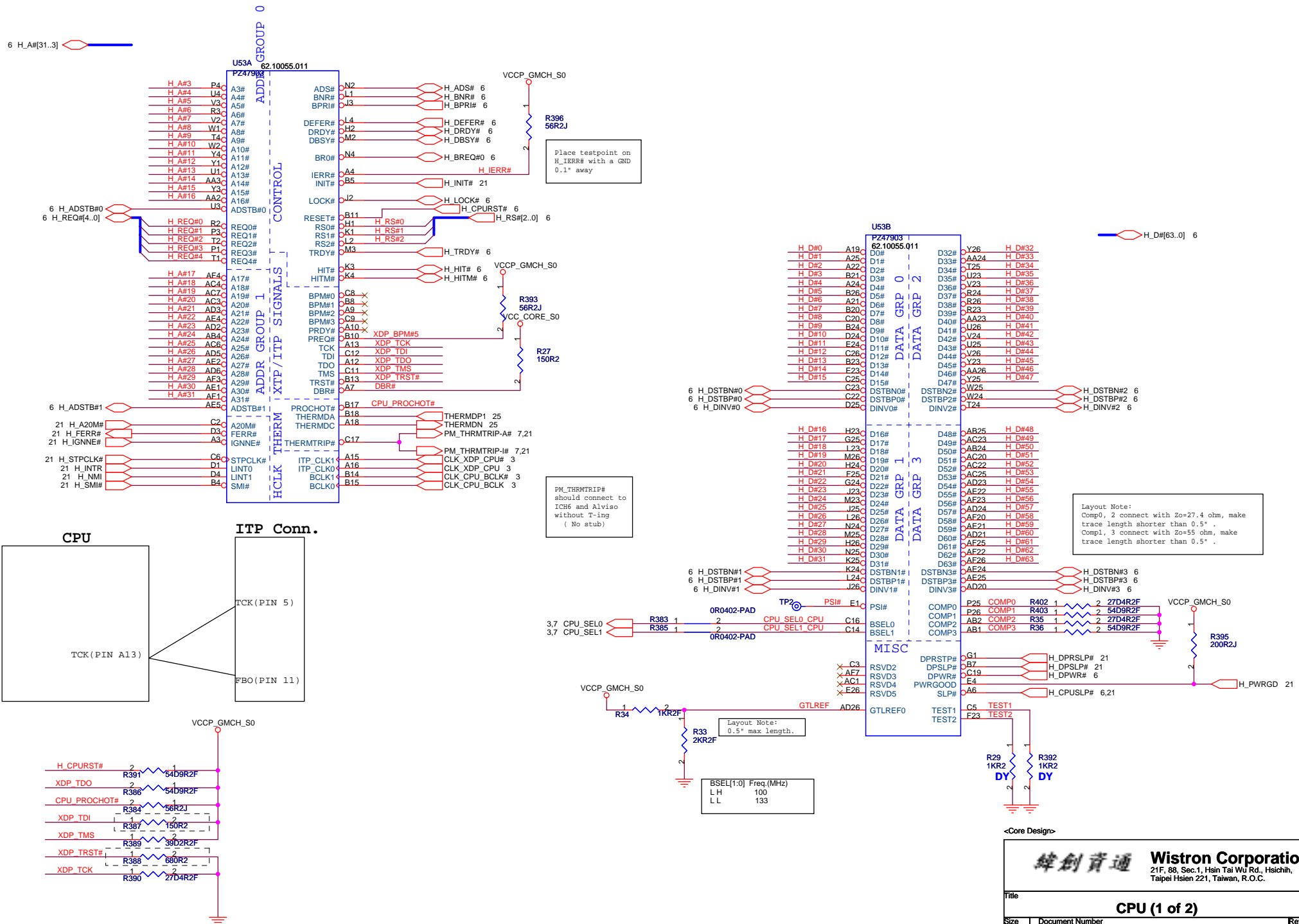
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Title: **Clock Generator (ICS954206AG)**

Size A3 Document Number **Leopard2** Rev -1

Date: Monday, July 11, 2005 Sheet 3 of 47



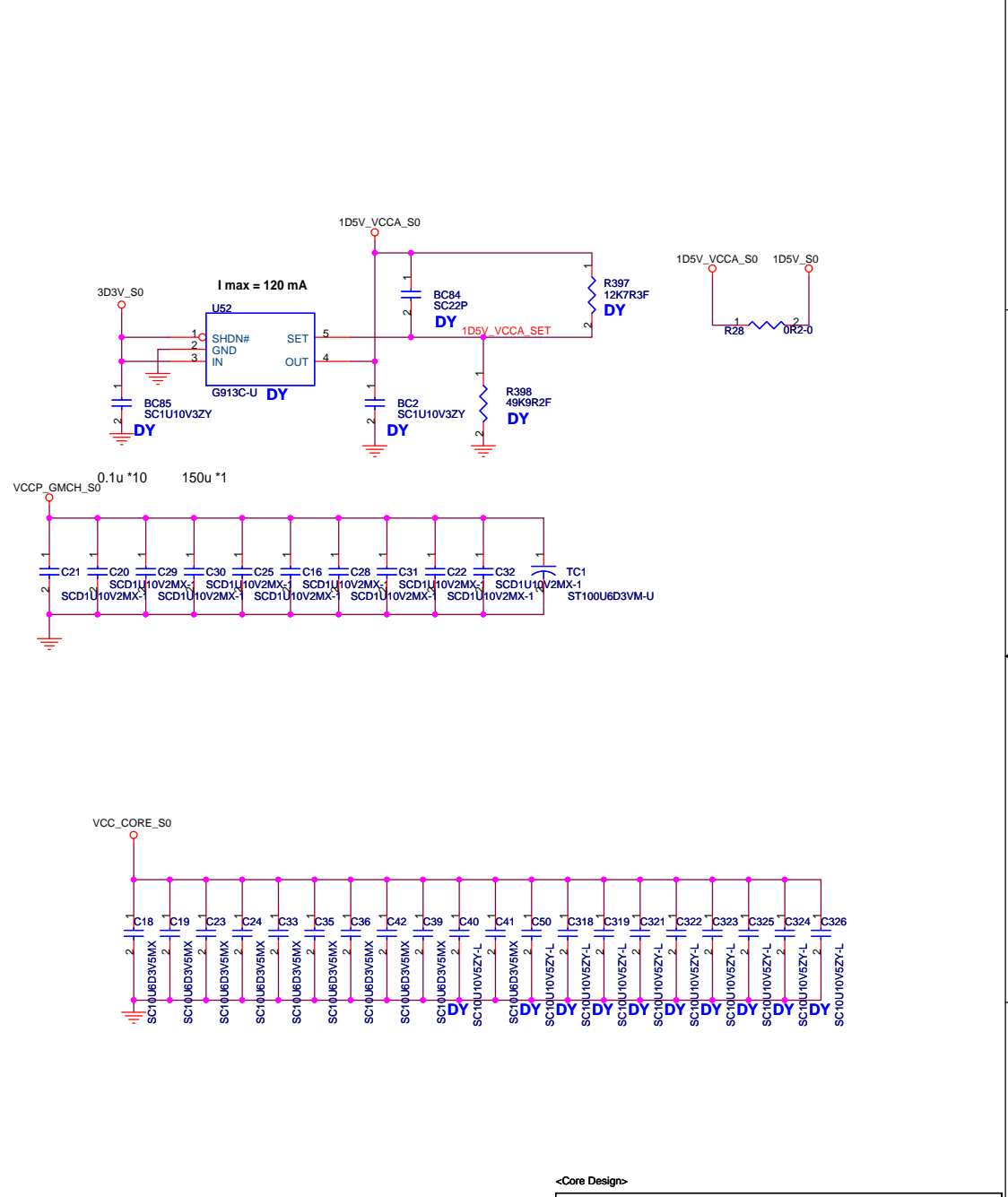
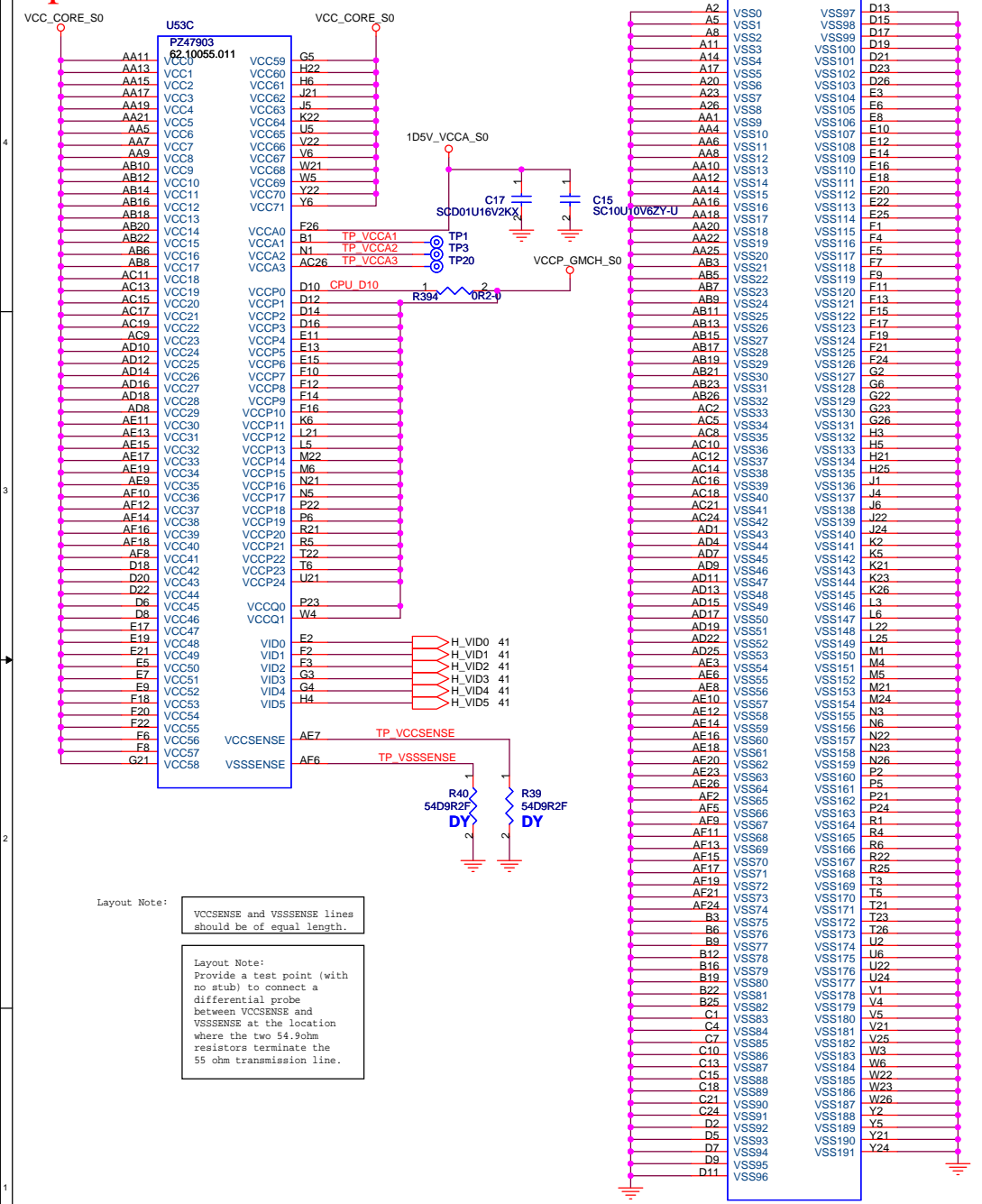
All place within 2" to CPU

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Title: **CPU (1 of 2)**

Size: A3 Document Number: **Leopard2** Rev: -1

Date: Monday, July 11, 2005 Sheet: 4 of 47



Layout Note:  
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:  
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

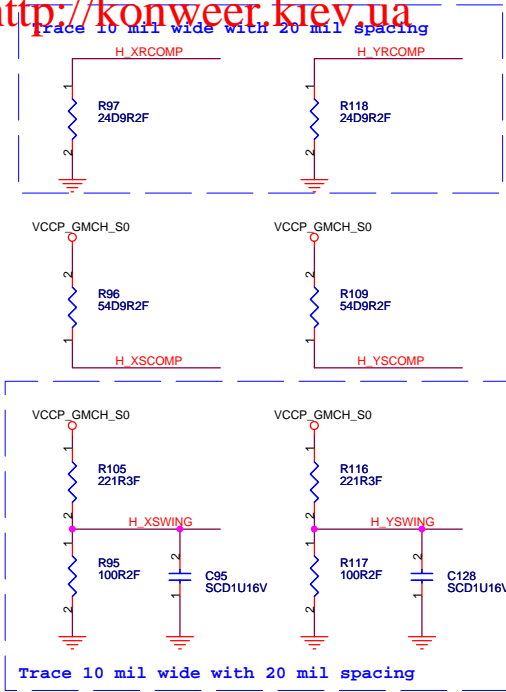
<Core Design>

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Title CPU (2 of 2)

Size A3 Document Number Leopard2 Rev SC

Date: Sunday, July 03, 2005 Sheet 5 of 47

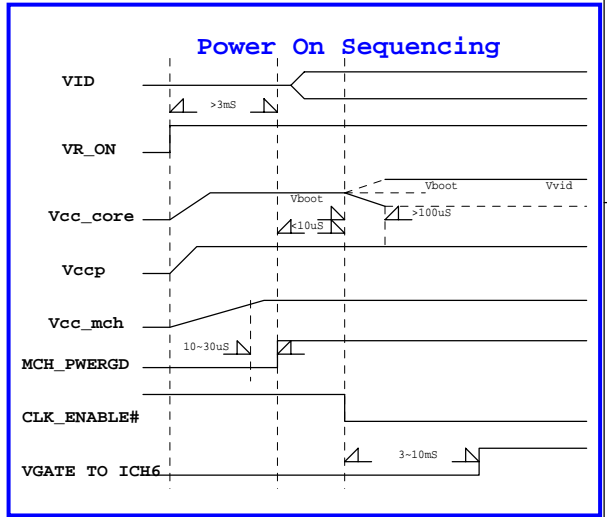
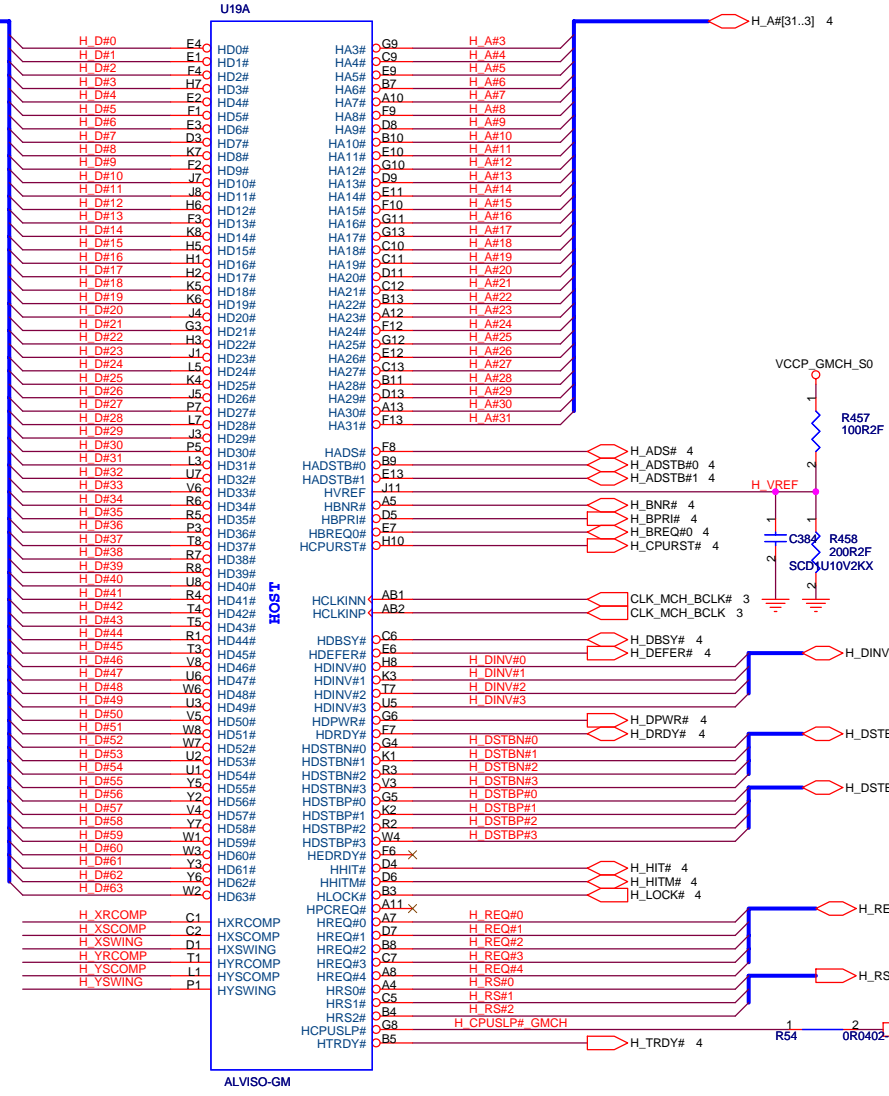


### Alviso Strapping Signals and Configuration

REV.NO. 1.0  
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 101 = FSB400 others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Dothan (Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes 1 = Normal (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reserved	
CFG18	GMCH core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reserved	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present(Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORX In signal.



ALVISO-GM: 71.0GMCH.08U  
ALVISO-PM: 71.0GMCH.0BU  
ALVISO-GML: 71.0GMCH.0JU

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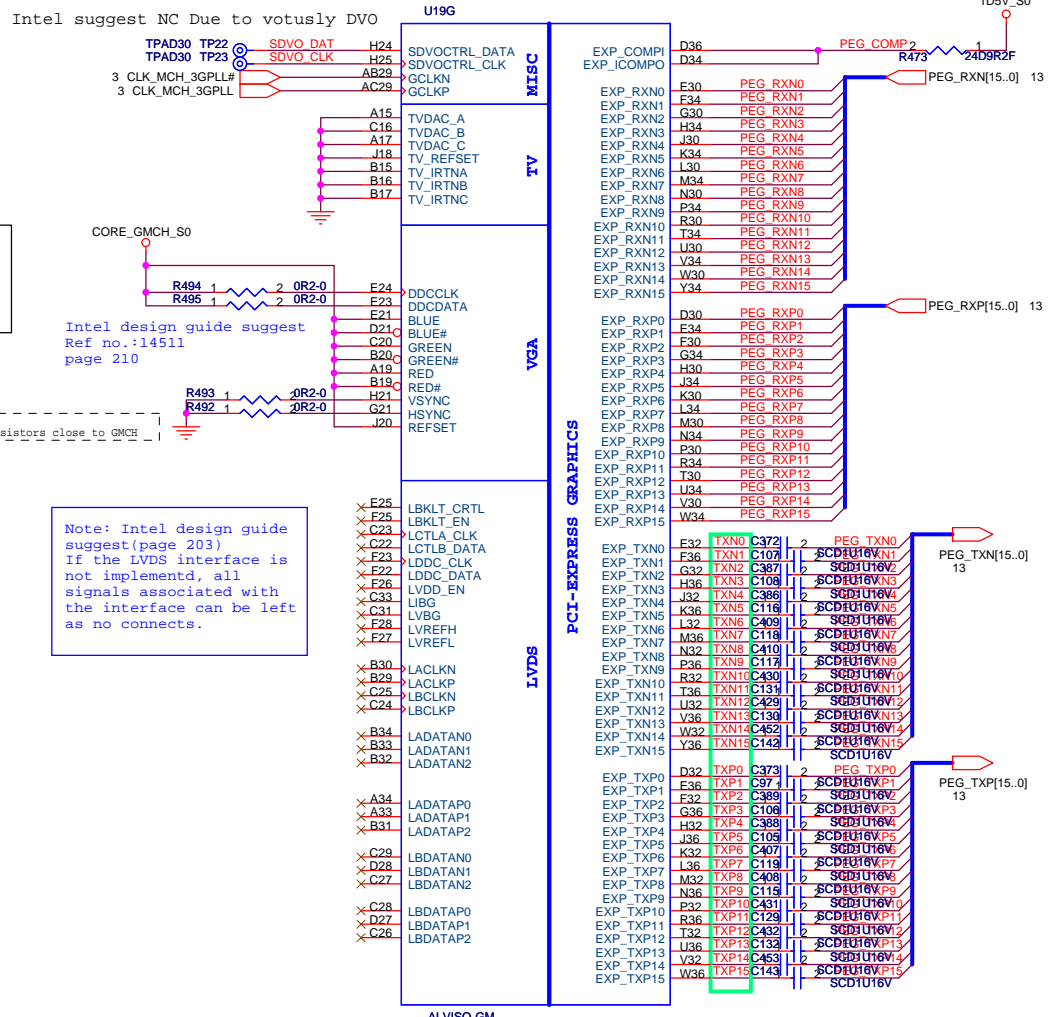
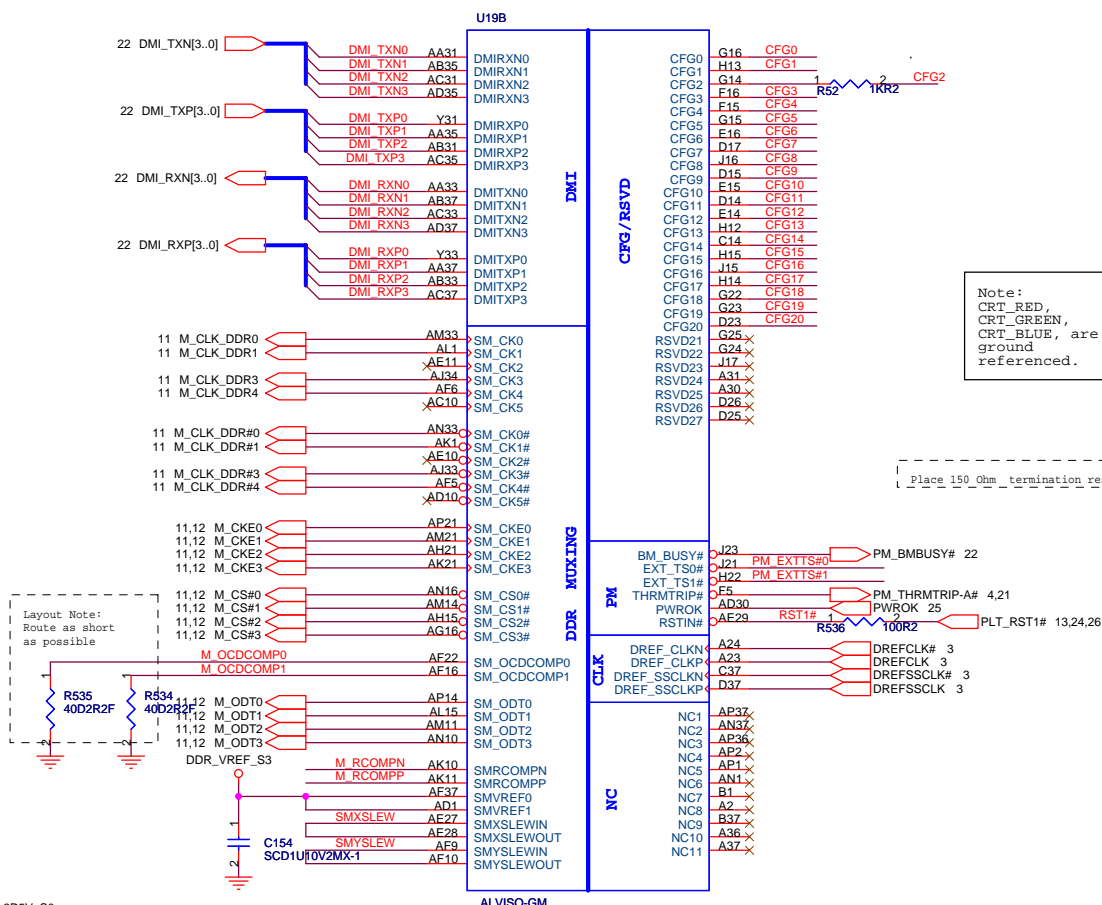
Title: **GMCH (1 of 5)**

Size A3 Document Number **Leopard2** Rev -1

Date: Monday, July 11, 2005 Sheet 6 of 47

Alviso will provide SDVO\_CTRLCLK and CTRLDATA pulldowns on-die

Intel suggest NC Due to votusly DVO

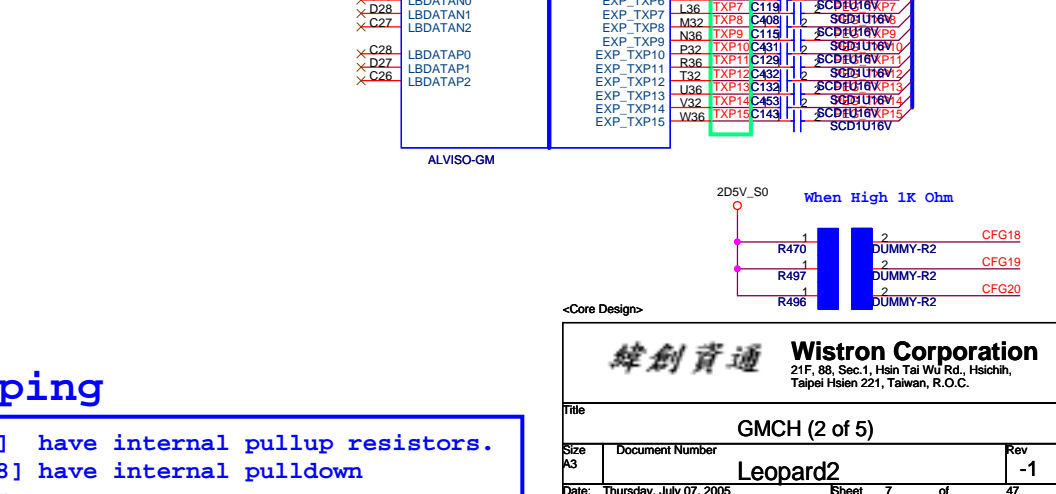
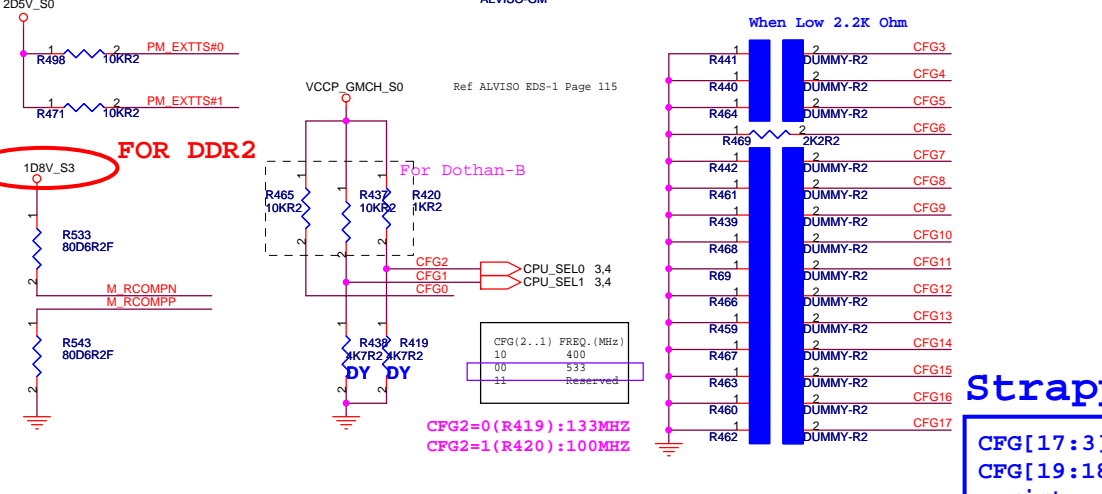


Note: CRT\_RED, CRT\_GREEN, CRT\_BLUE, are ground referenced.

Intel design guide suggest Ref no.:14511 page 210

Place 150 Ohm termination resistors close to GMCH

Note: Intel design guide suggest (page 203) If the LVDS interface is not implemented, all signals associated with the interface can be left as no connects.



### Strapping

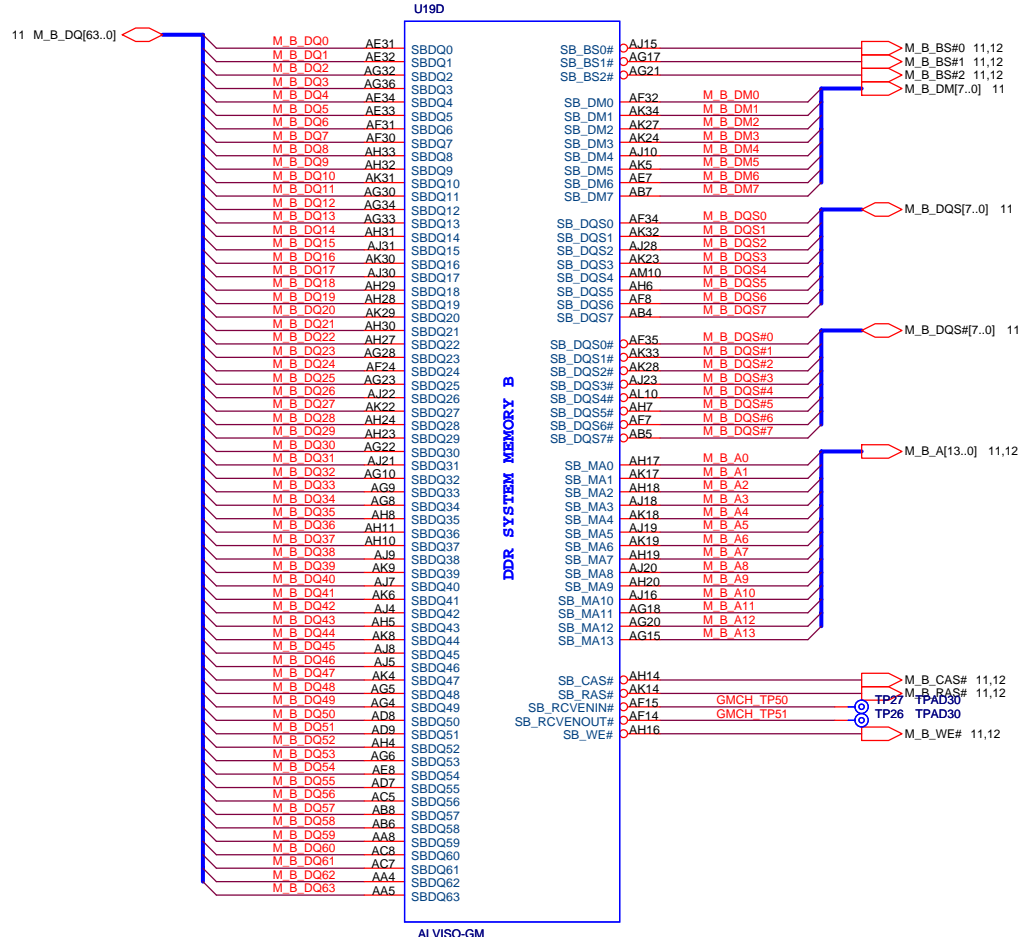
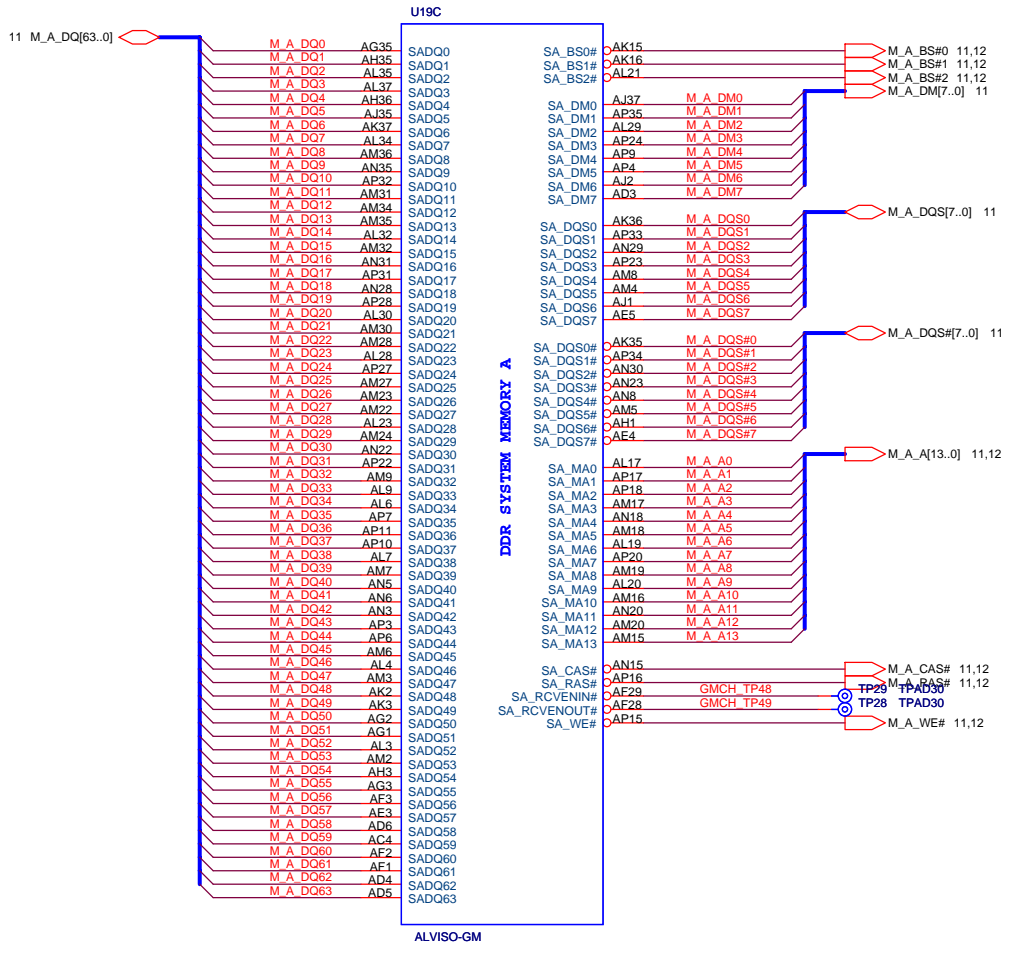
CFG[17:3] have internal pullup resistors.  
CFG[19:18] have internal pulldown resistors

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**GMCH (2 of 5)**

**Leopard2**

Date: Thursday, July 07, 2005 Sheet 7 of 47



<Core Design>

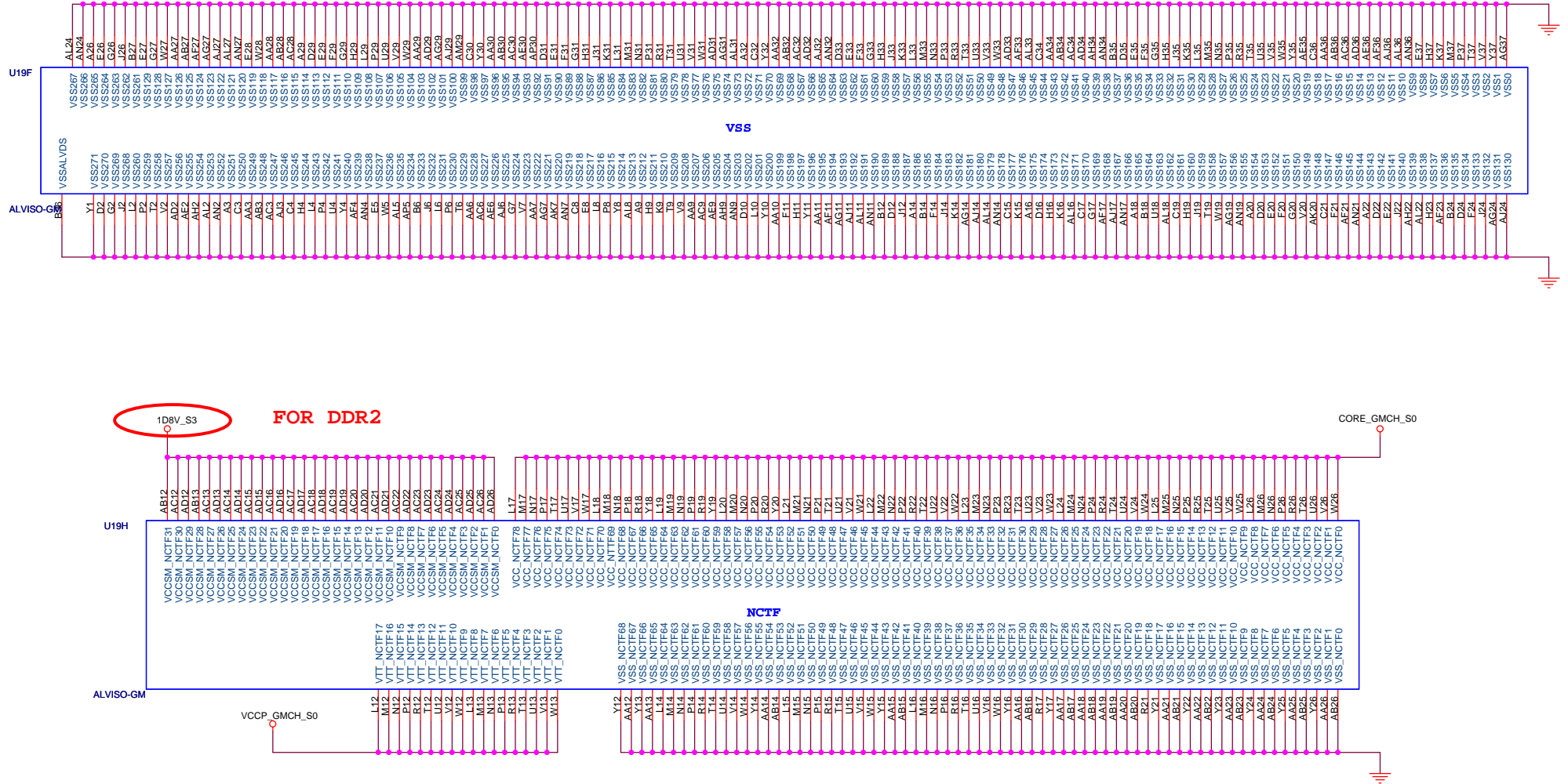
緯創資通 **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (3 of 5)**

Size: A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet: 8 of 47

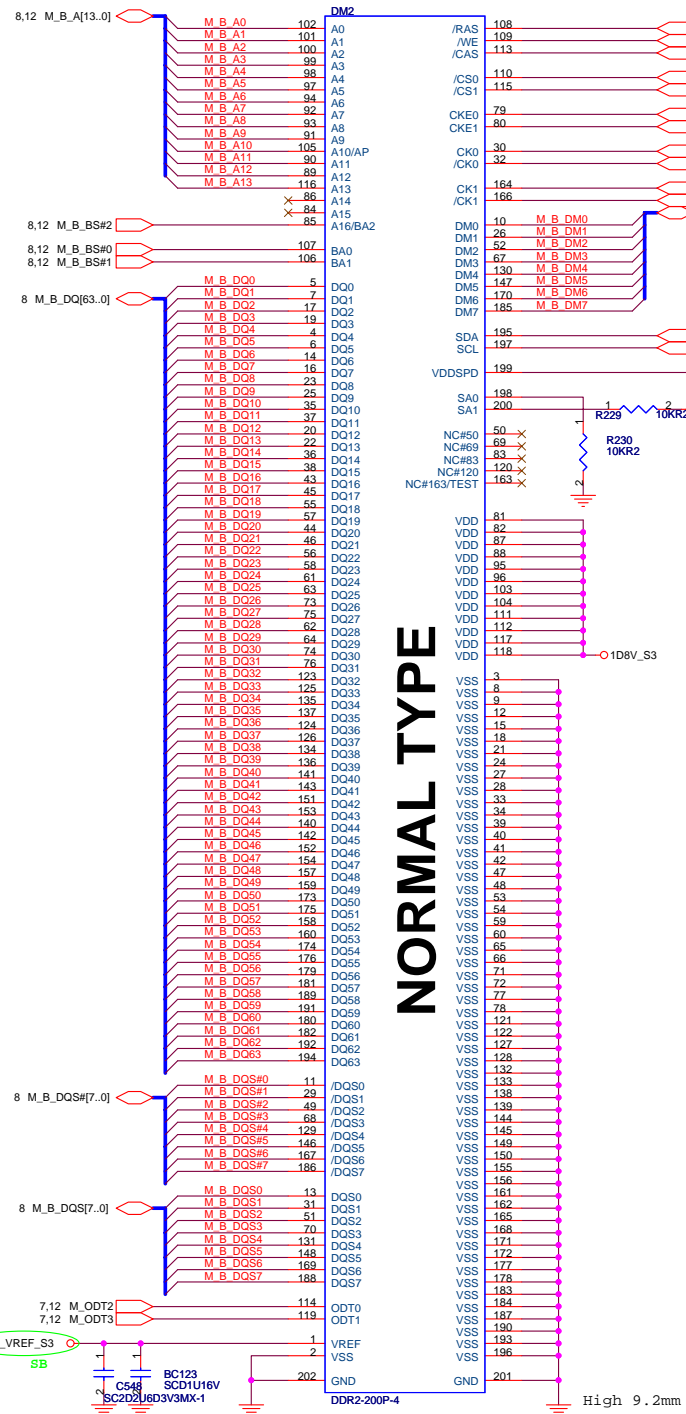




1D8V\_S3 FOR DDR2

VCCP\_GMCH\_S0

CORE\_GMCH\_S0



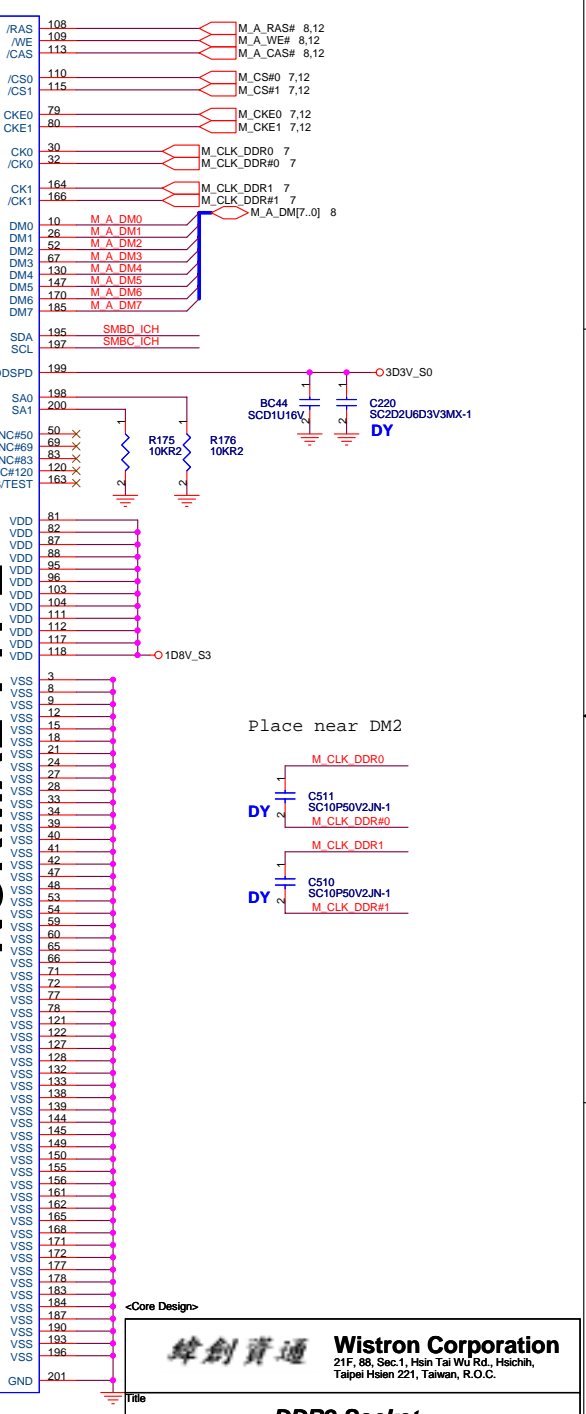
NORMAL TYPE

Hi 9.2 mm



NORMAL TYPE

Low 5.2 mm



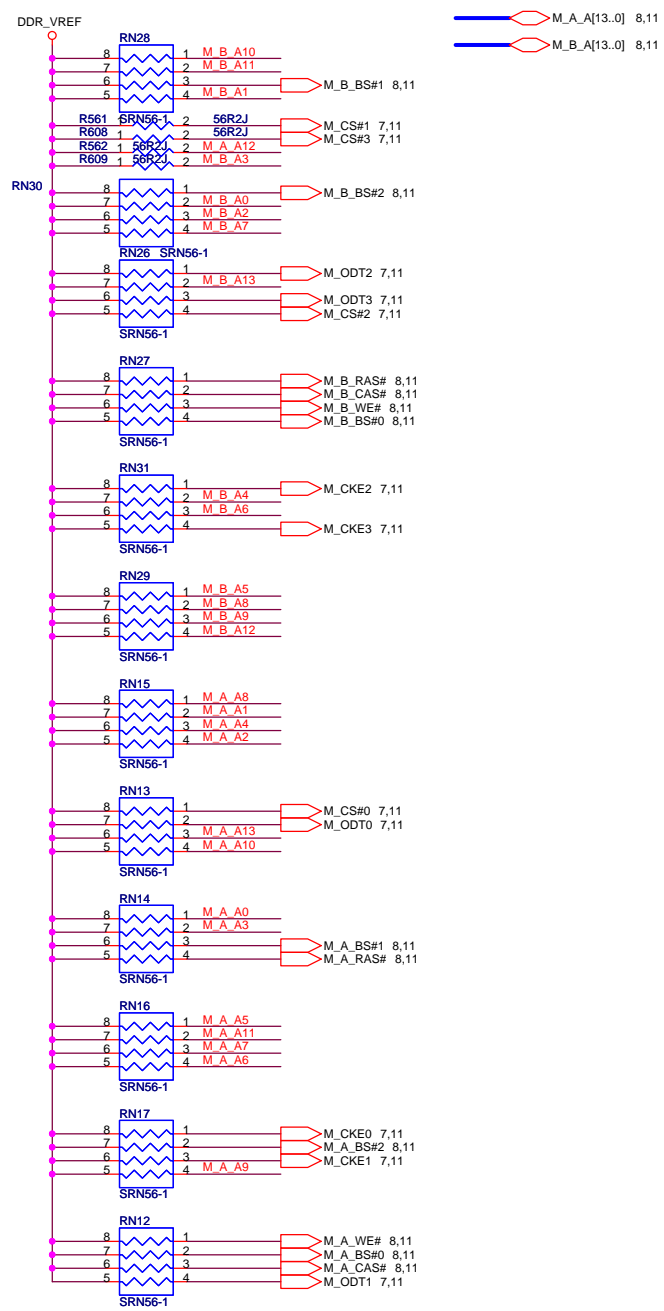
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**DDR2 Socket**

Title	Document Number	Rev
	Custom	-1
<b>Leopard 2</b>		
Date: Thursday, July 07, 2005	Sheet 11 of 47	

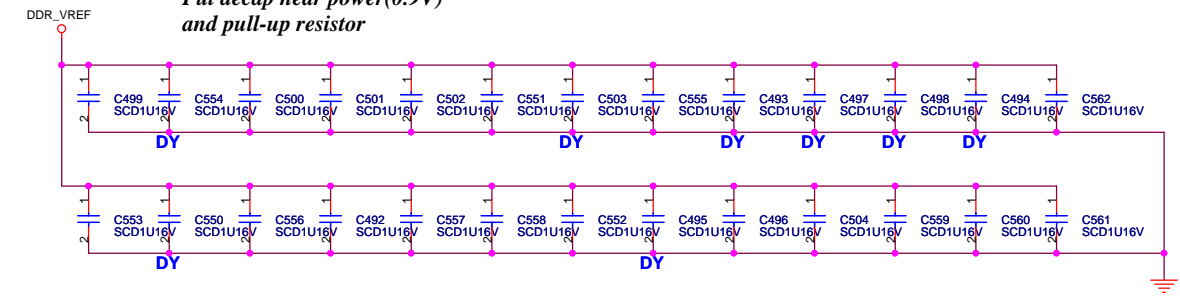
# PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

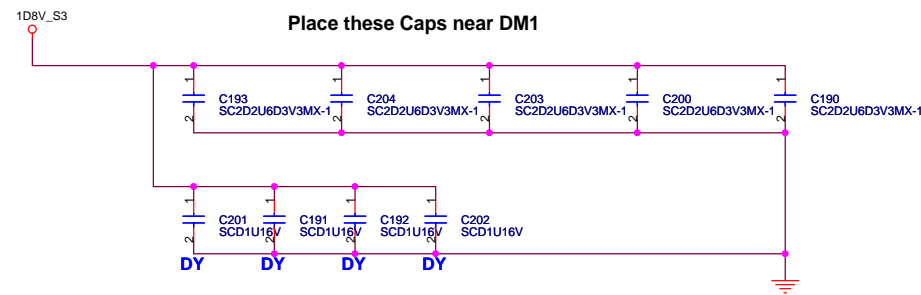


# Decoupling Capacitor

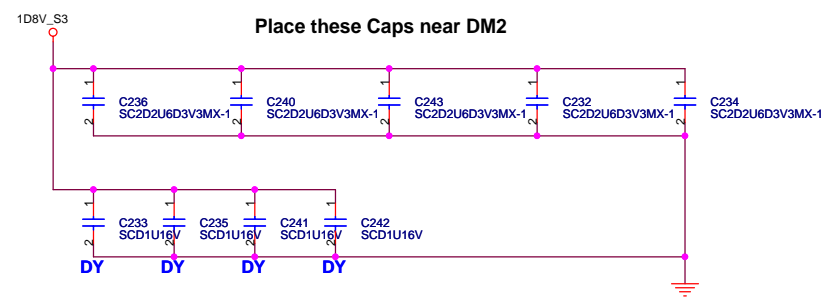
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2

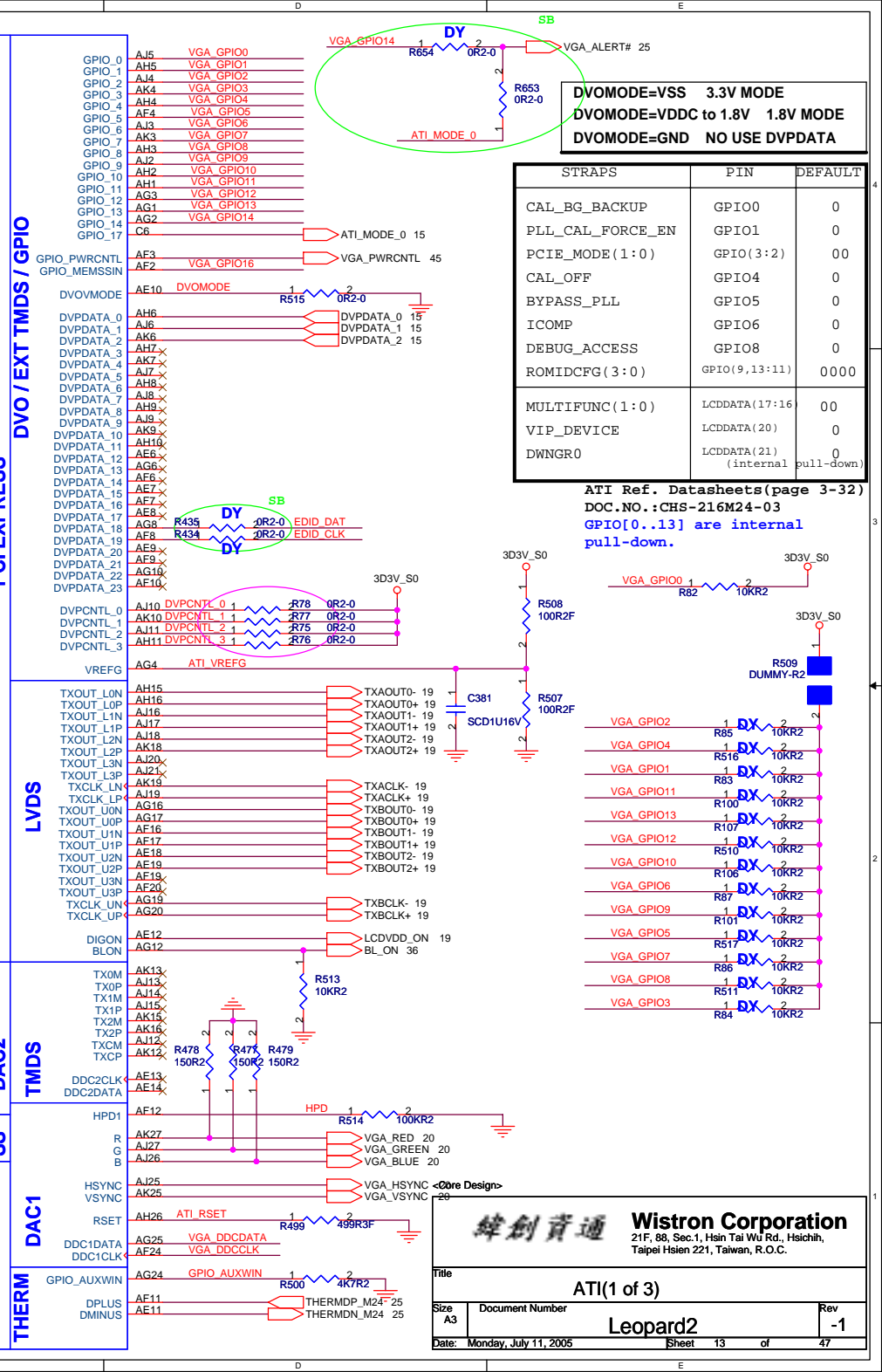
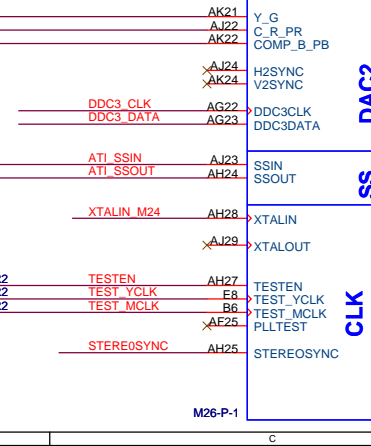
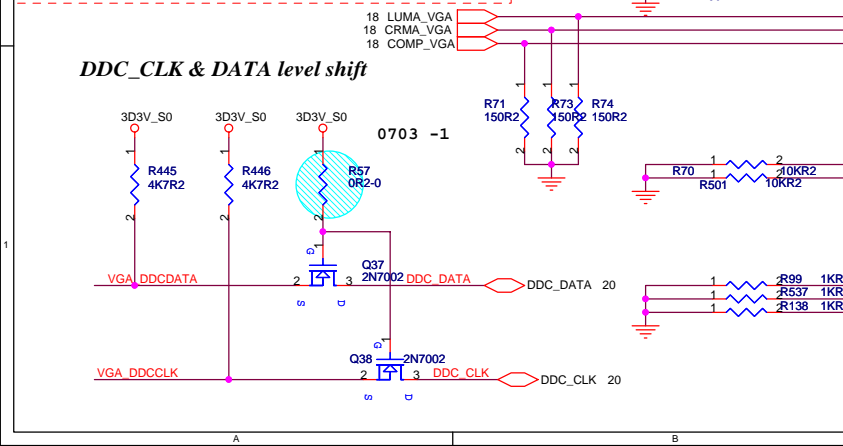
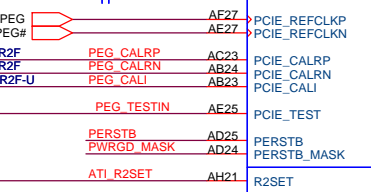
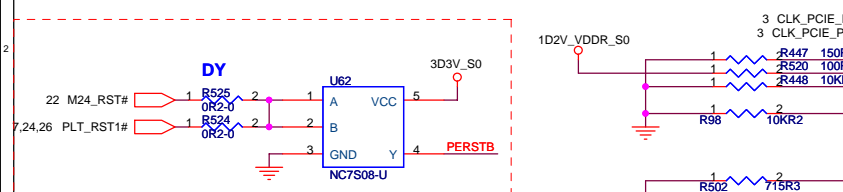
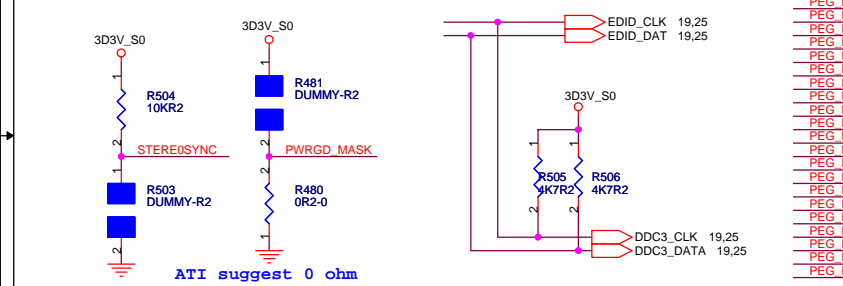
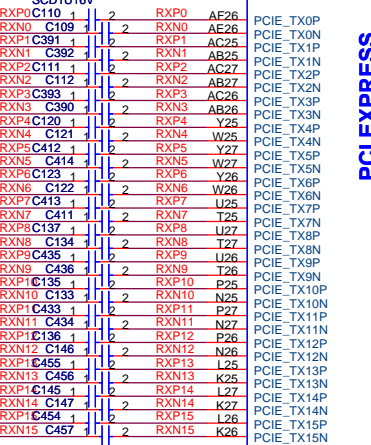
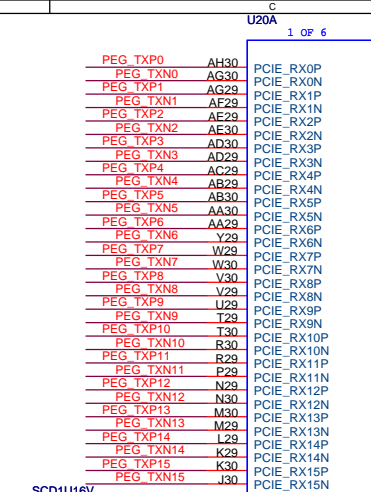
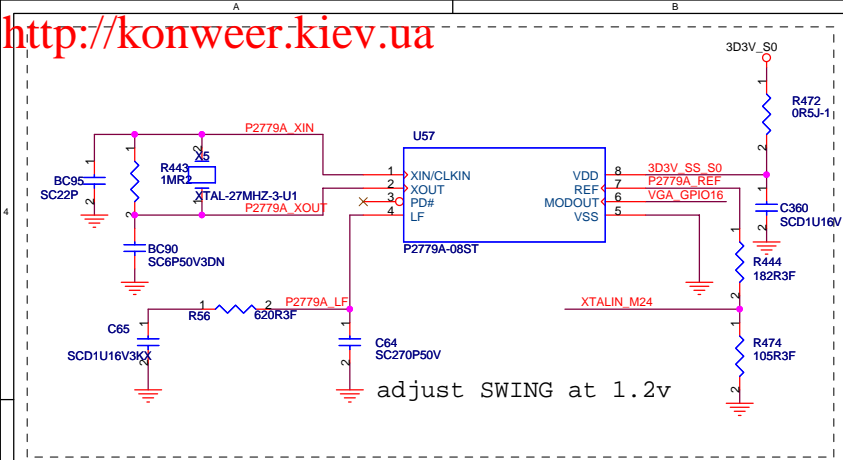


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Title: **DDR2 Termination Resistor**

Size: A3	Document Number: <b>Leopard2</b>	Rev: <b>-1</b>
Date: Thursday, July 07, 2005	Sheet: 12 of 47	

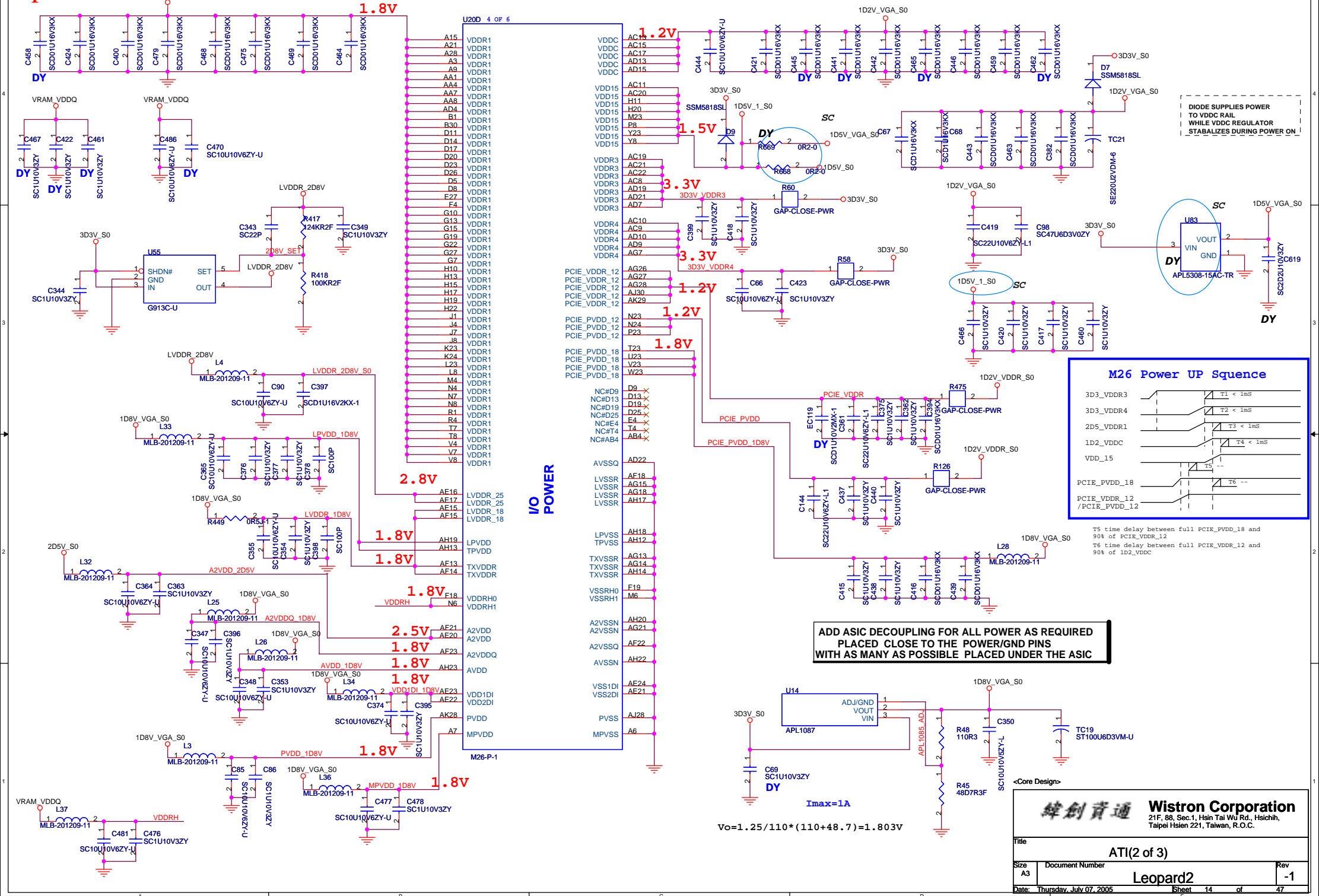


DVOMODE=VSS 3.3V MODE  
 DVOMODE=VDDC to 1.8V 1.8V MODE  
 DVOMODE=GND NO USE DVPPDATA

STRAPS	PIN	DEFAULT
CAL_BG_BACKUP	GPIO0	0
PLL_CAL_FORCE_EN	GPIO1	0
PCIE_MODE(1:0)	GPIO(3:2)	00
CAL_OFF	GPIO4	0
BYPASS_PLL	GPIO5	0
ICOMP	GPIO6	0
DEBUG_ACCESS	GPIO8	0
ROMIDCFG(3:0)	GPIO(9,13:11)	0000
MULTIFUNC(1:0)	LCDDATA(17:16)	00
VIP_DEVICE	LCDDATA(20)	0
DWNGR0	LCDDATA(21)	0 (internal pull-down)

ATI Ref. Datasheets (page 3-32)  
 DOC.NO.: CHS-216M24-03  
 GPIO[0..13] are internal pull-down.

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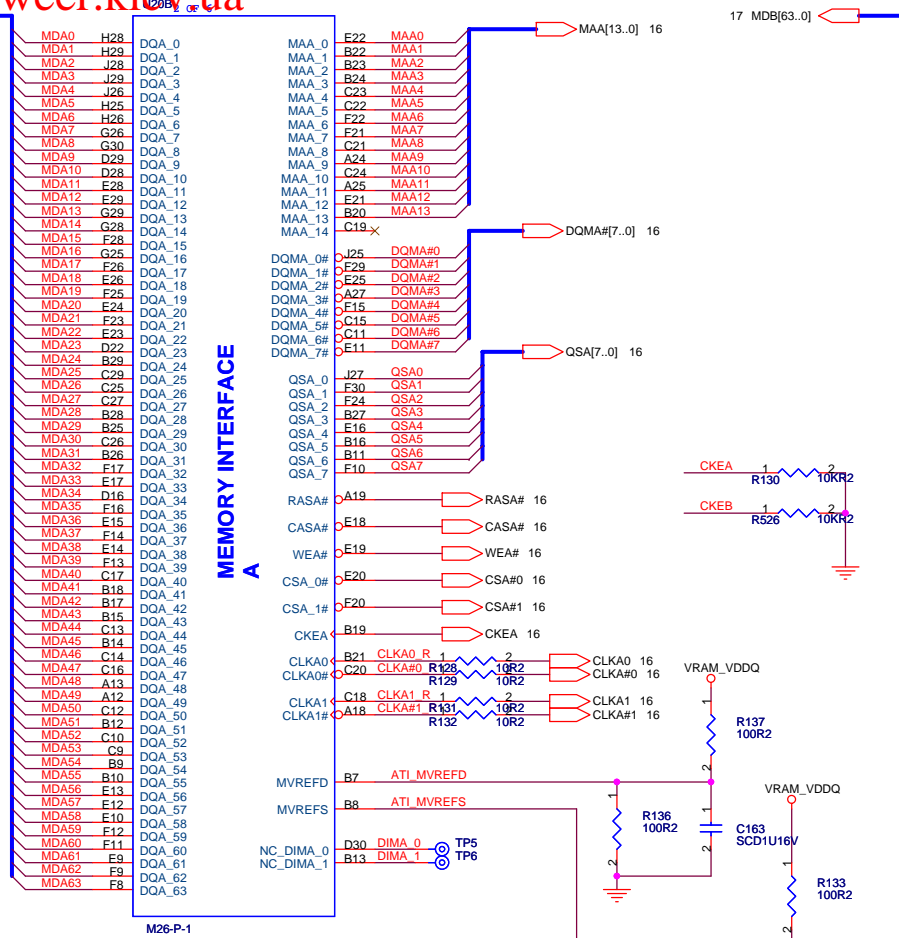


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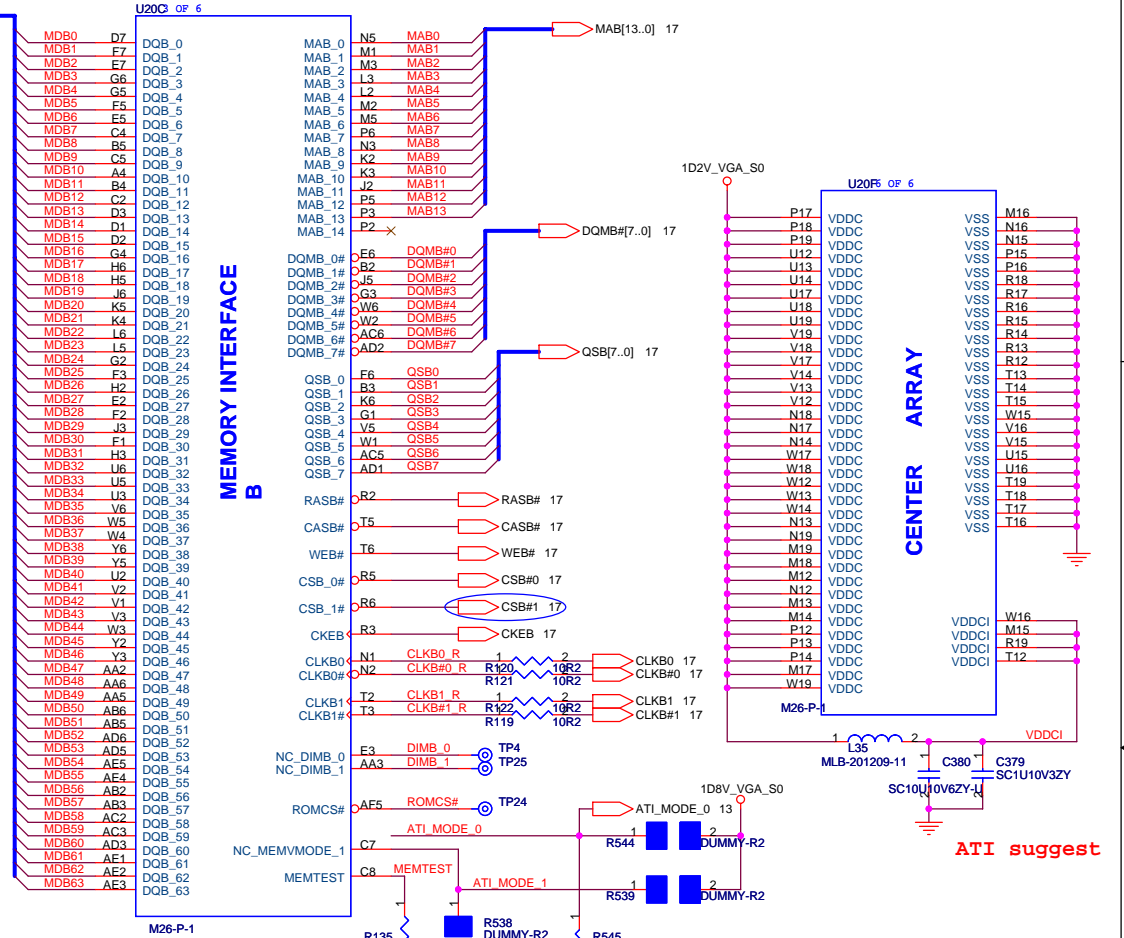
Title: **ATI(2 of 3)**

Size: A3 Document Number: **Leopard2** Rev: -1

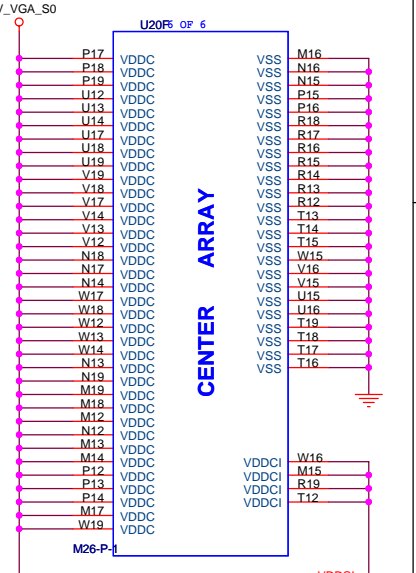
Date: Thursday, July 07, 2005 Sheet: 14 of 47



MEMORY CHANNEL A

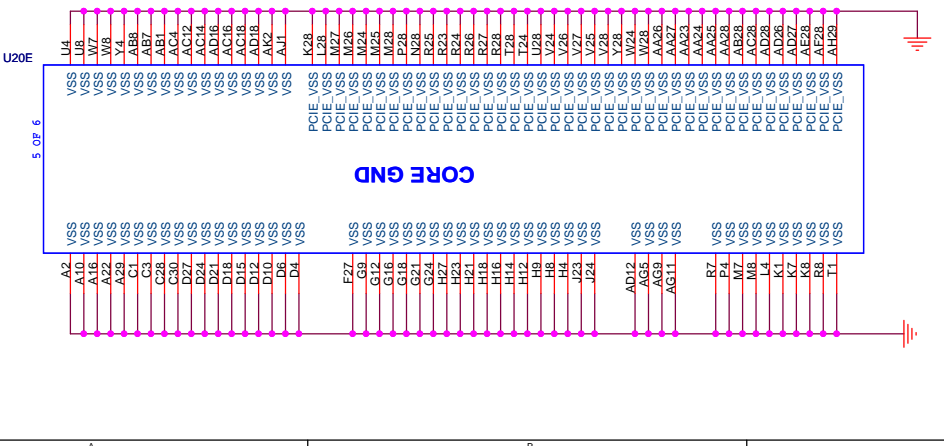


MEMORY CHANNEL B



ATI suggest

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

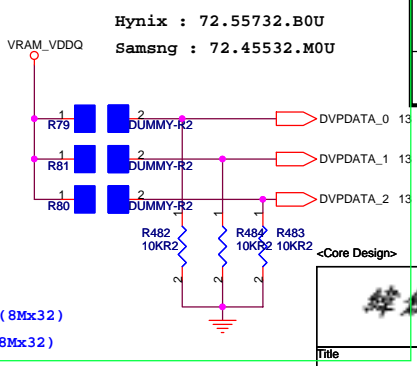


CORE GND

**VRAM Selection**

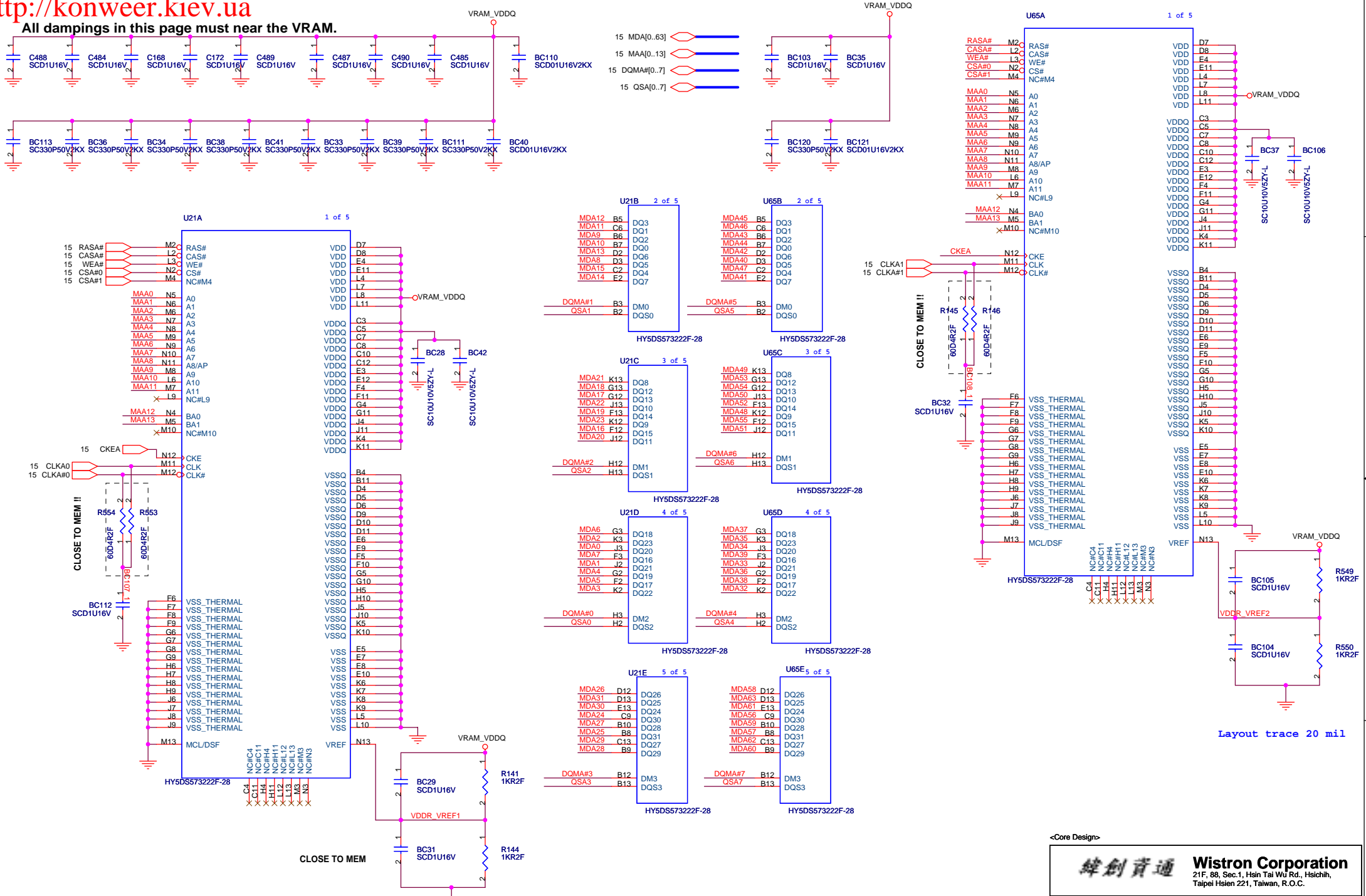
Vendor/Size	SETTING	DVPDATA_[2:0]
HYNIX/128M	000	
SAMSUNG/128M	001	
RESERVED	010	
RESERVED	011	
RESERVED	100	
RESERVED	101	
RESERVED	110	
RESERVED	111	

Hynix : HY5Ds73222F(P)-28 (8Mx32)  
 Samsung : K4D53235F-VC2A (8Mx32)



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All dampings in this page must near the VRAM.



Layout trace 20 mil

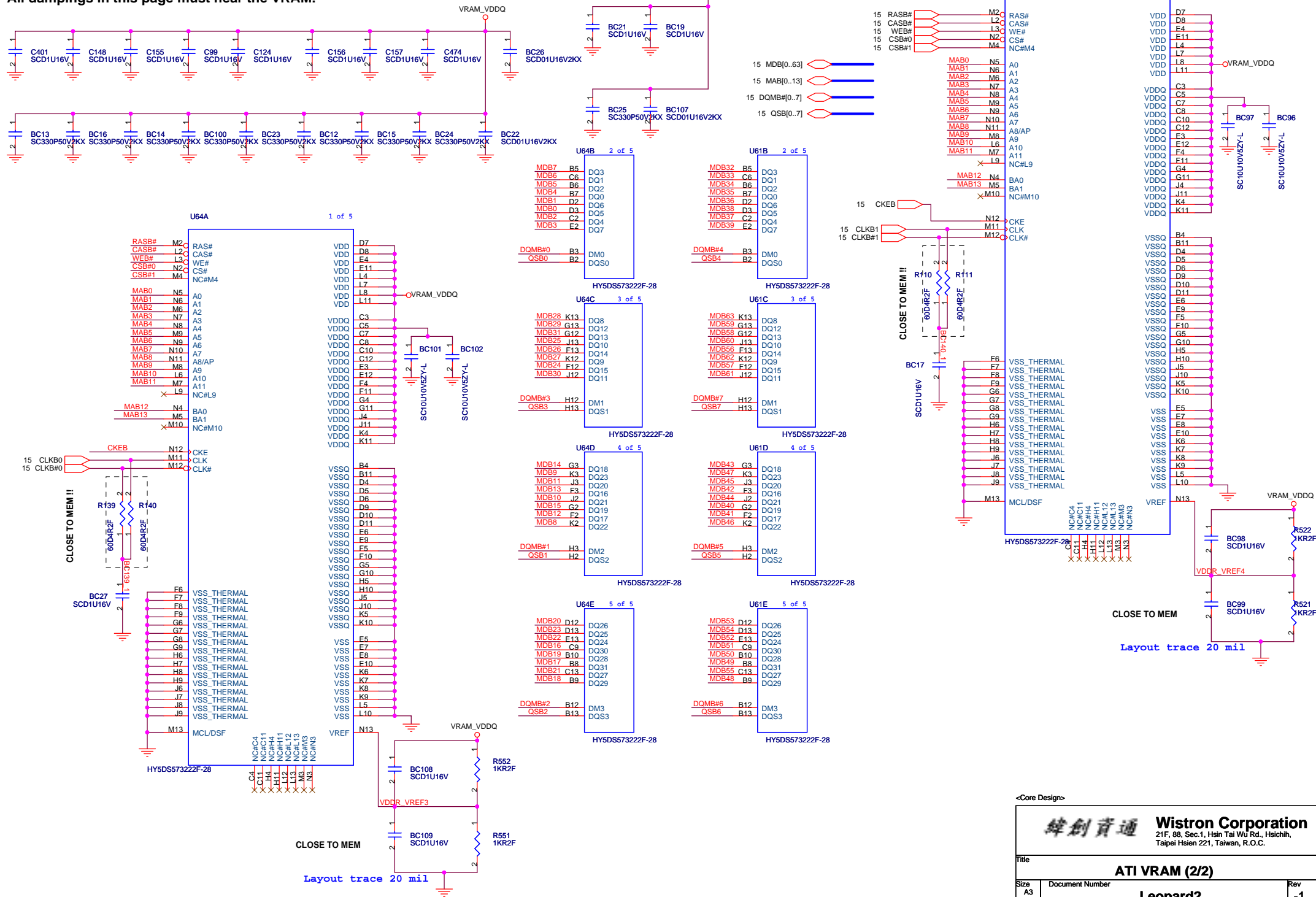
Layout trace 20 mil

<Core Design>

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Title	ATI VRAM (1/2)		Rev
Size	A3	Document Number	Leopard2
Date:	Thursday, July 07, 2005	Sheet	16 of 47

All dampings in this page must near the VRAM.

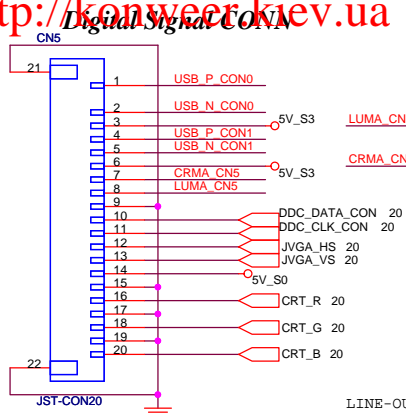


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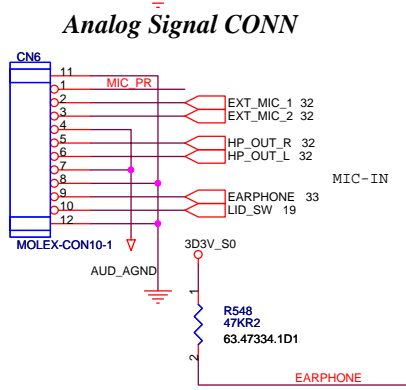
**緯創資通 Wistron Corporation**  
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**ATI VRAM (2/2)**

Title		
Size	Document Number	Rev
A3		-1
Date:	Thursday, July 07, 2005	Sheet 17 of 47

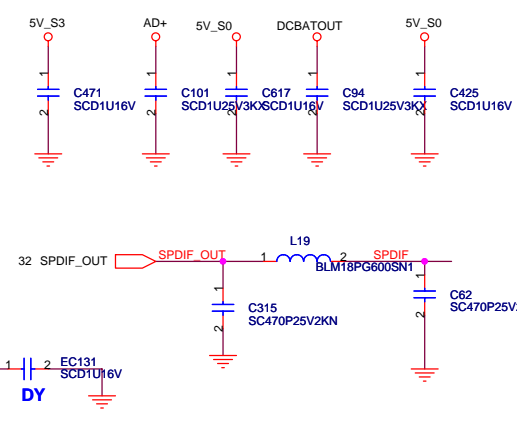
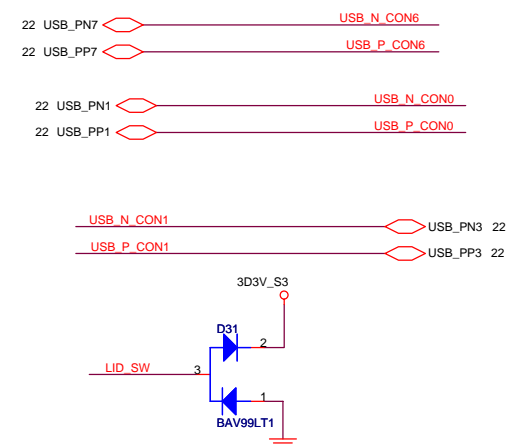
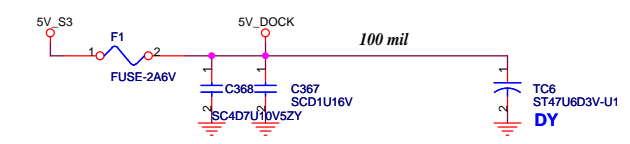
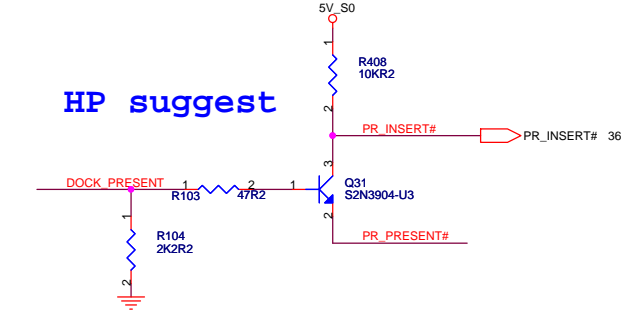


**Close to Docking CN**



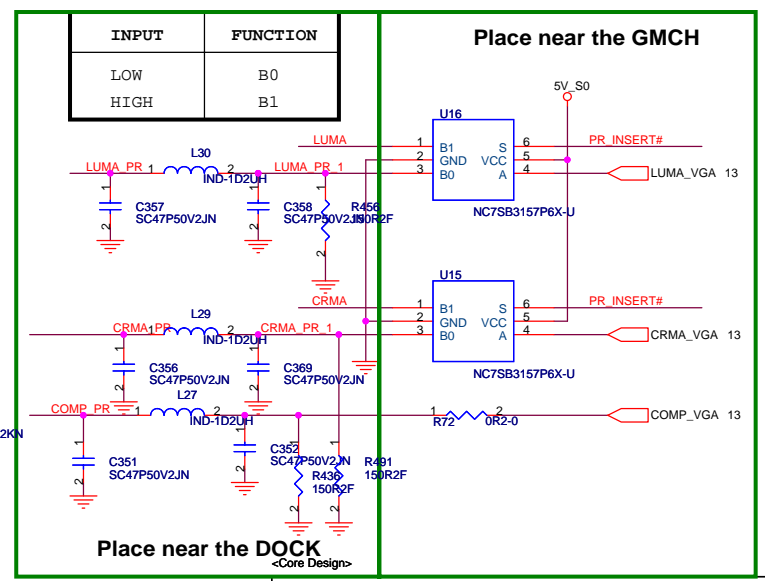
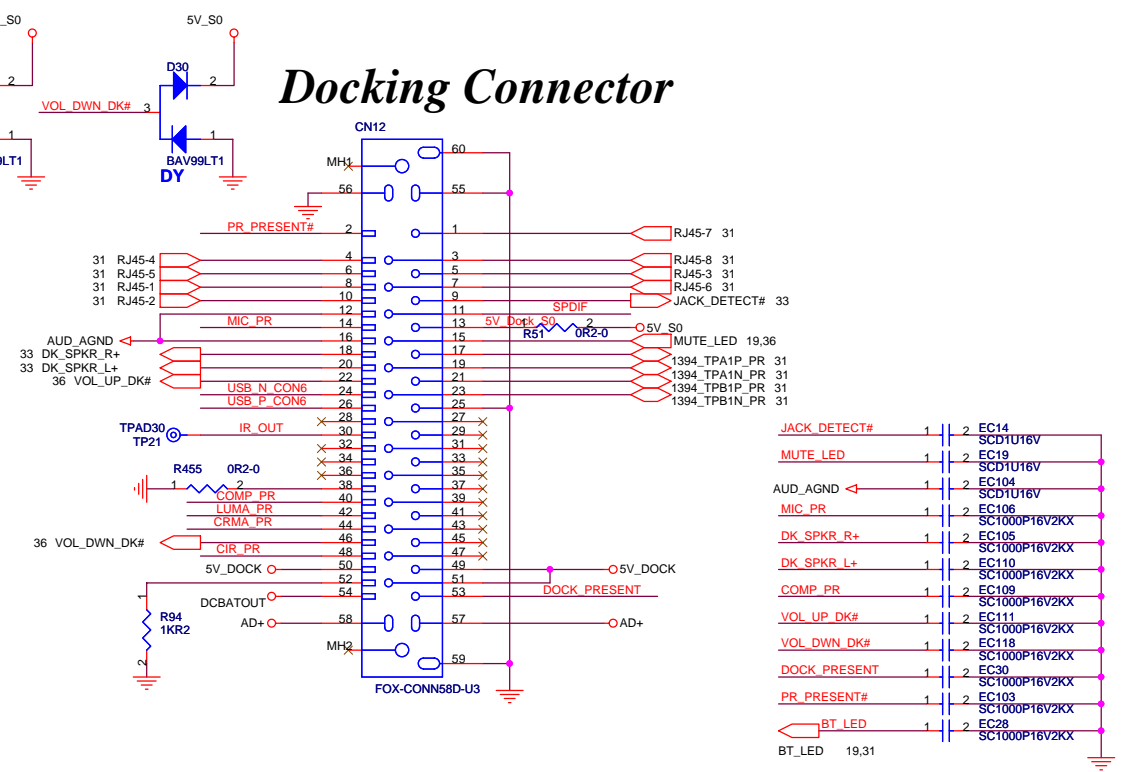
Please close to ICH6

HP suggest



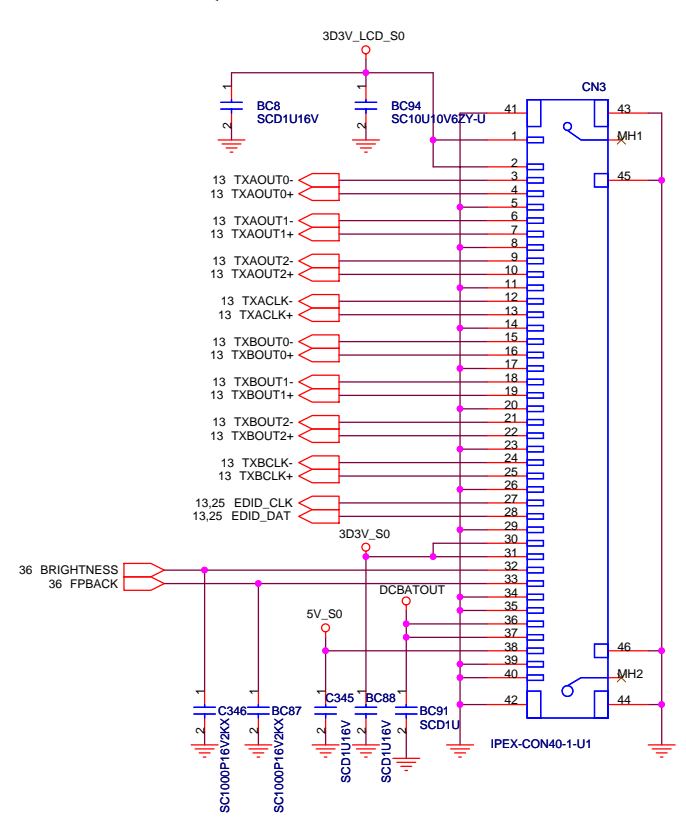
CIR, CIR\_PR, CIR\_KBC are connect together. default setting 12/12

**Docking Connector**

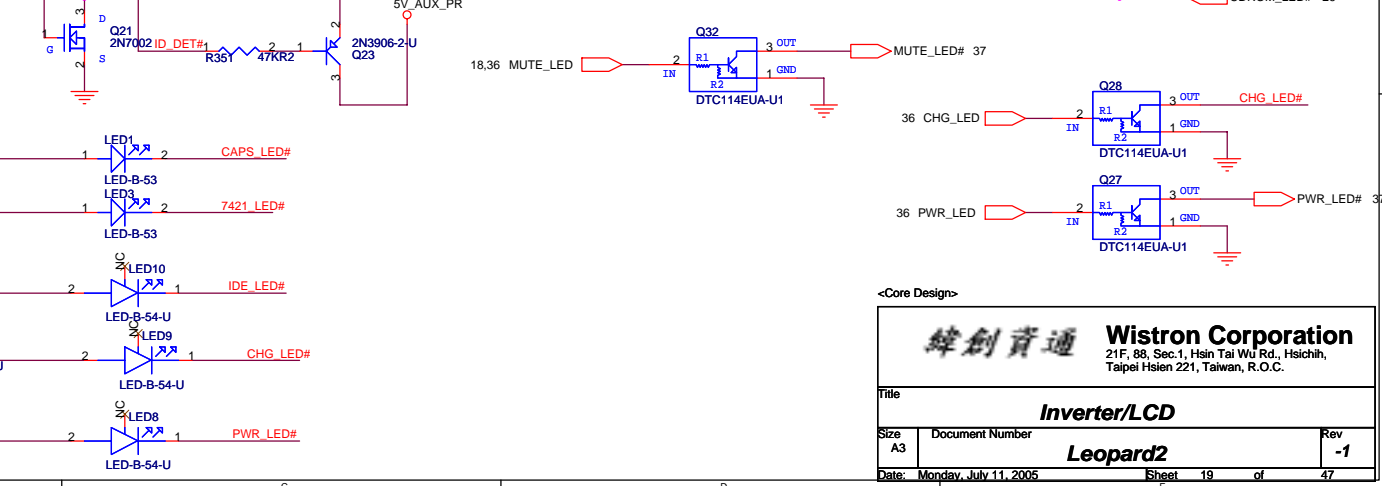
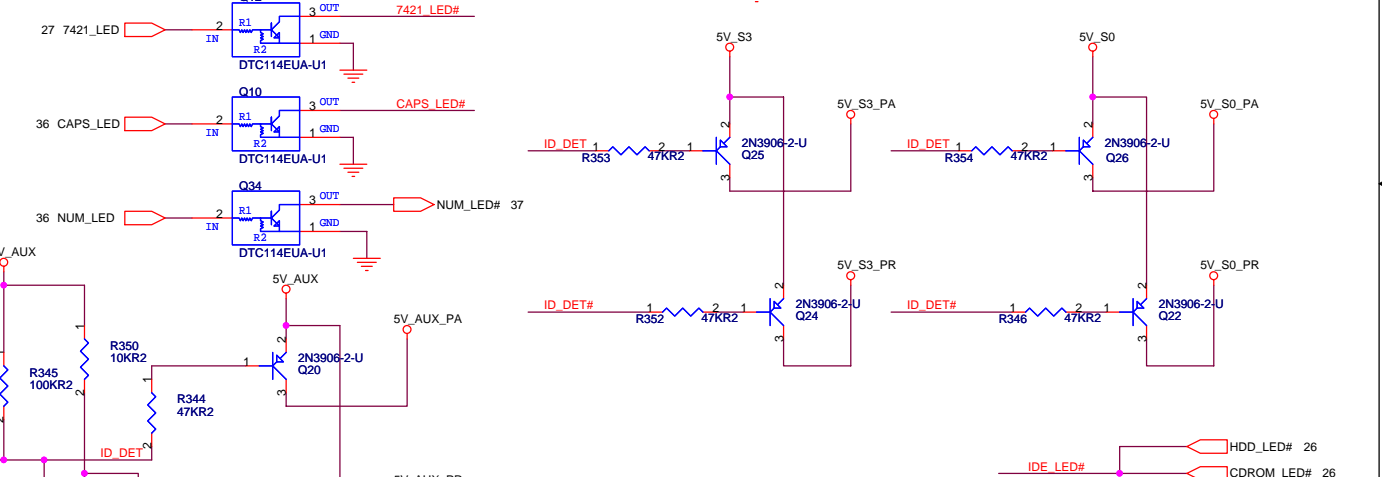
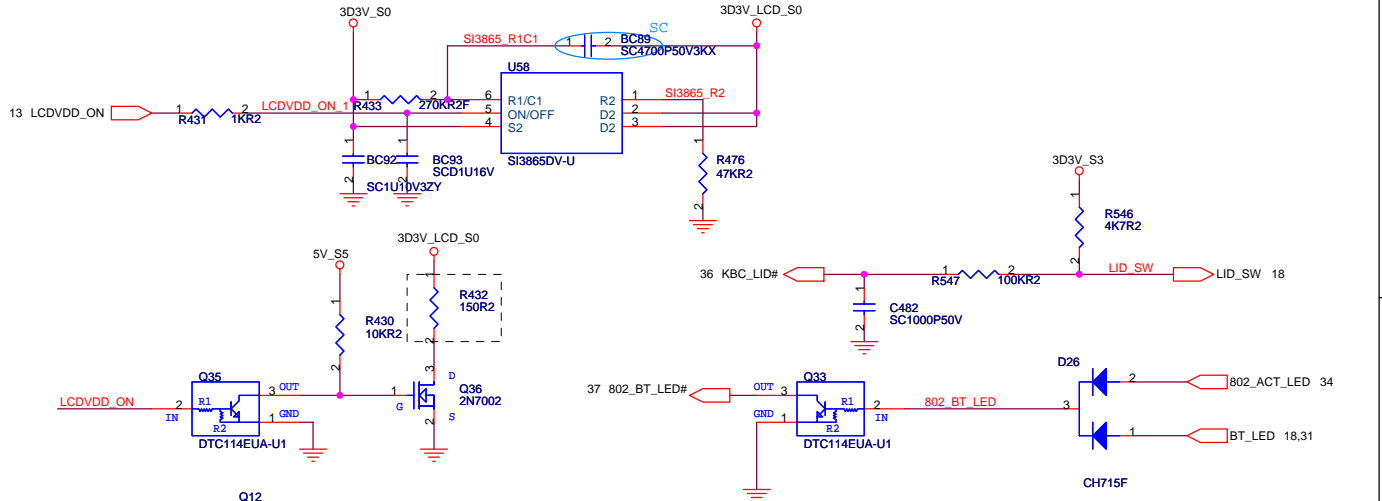
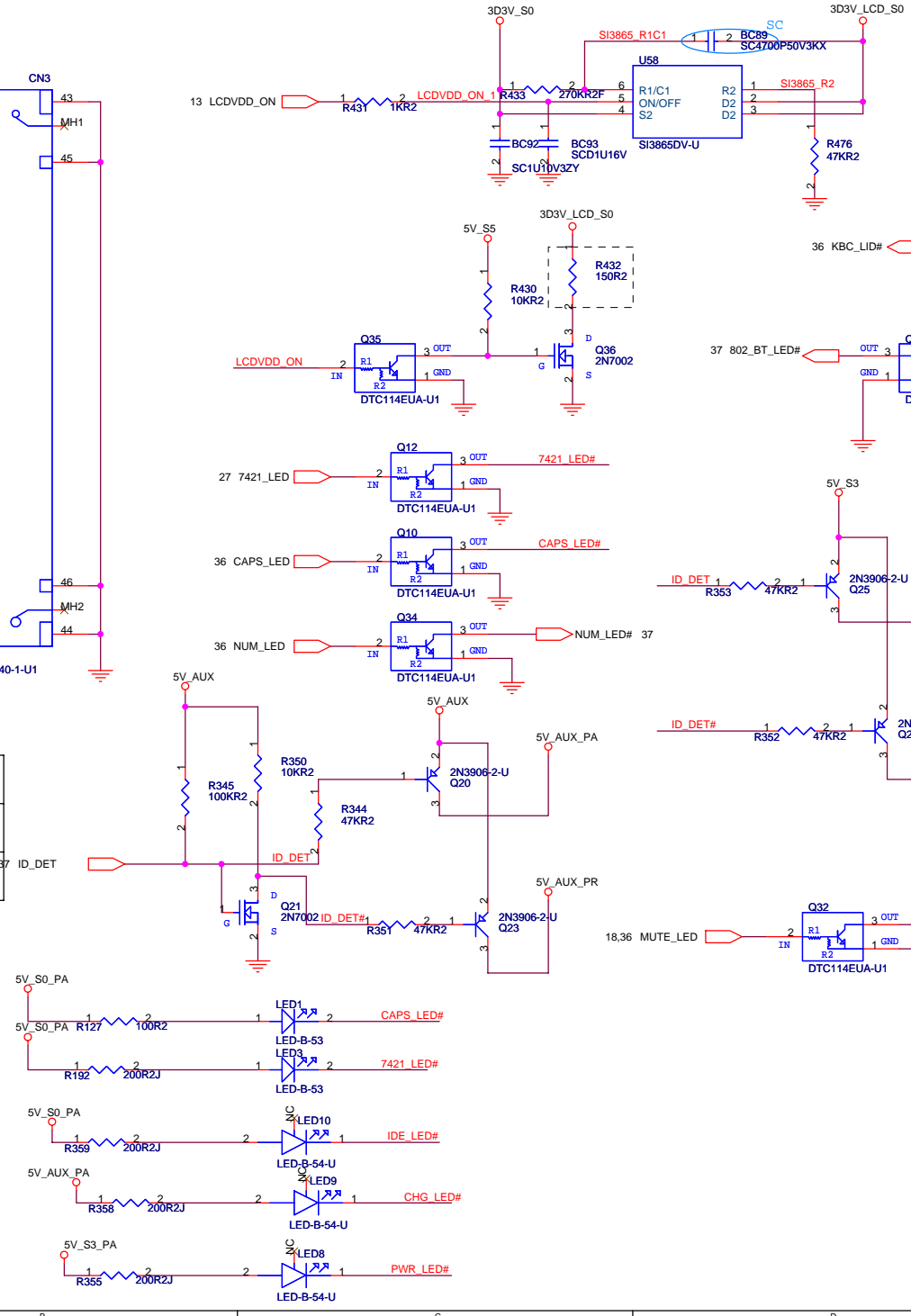
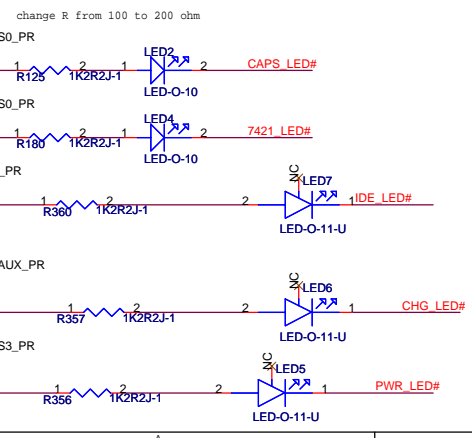


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# INVERTER / LCD



	PWR	CHR	HDD	IR	CAPS	7421
PR Botton	Amber LED4	Amber LED5	Amber LED6	U42	Amber LED1	Amber LED2
PA Top	Blue LED8	Blue LED7	Blue LED9	U64	Blue LED1	Blue LED2



<Core Design>

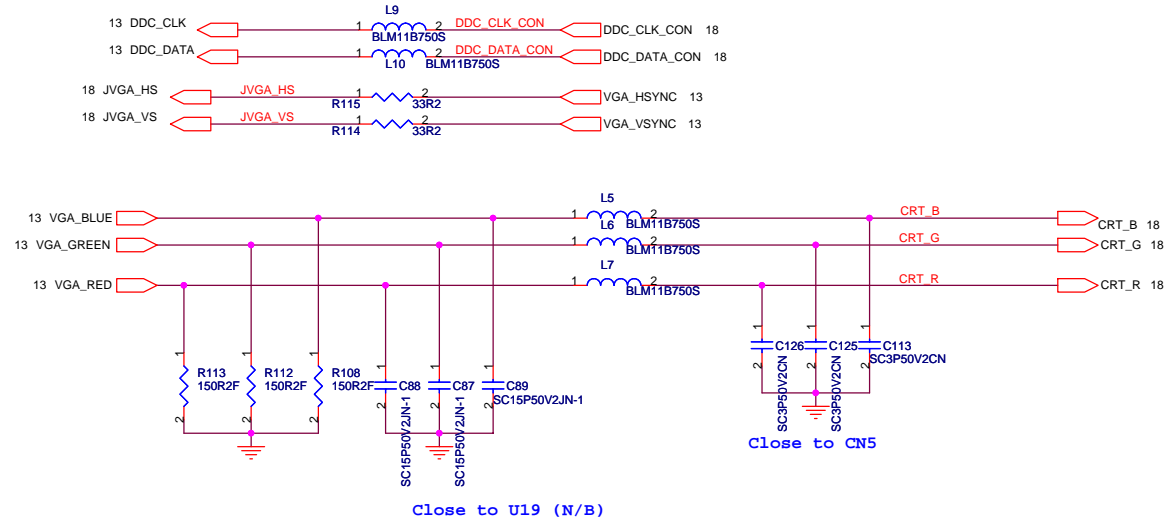
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Inverter/LCD**

Size: A3 Document Number: **Leopard2** Rev: **-1**

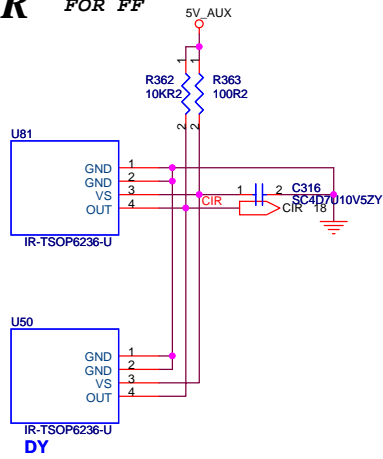
Date: Monday, July 11, 2005 Sheet: 19 of 47

# CRT

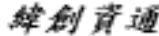


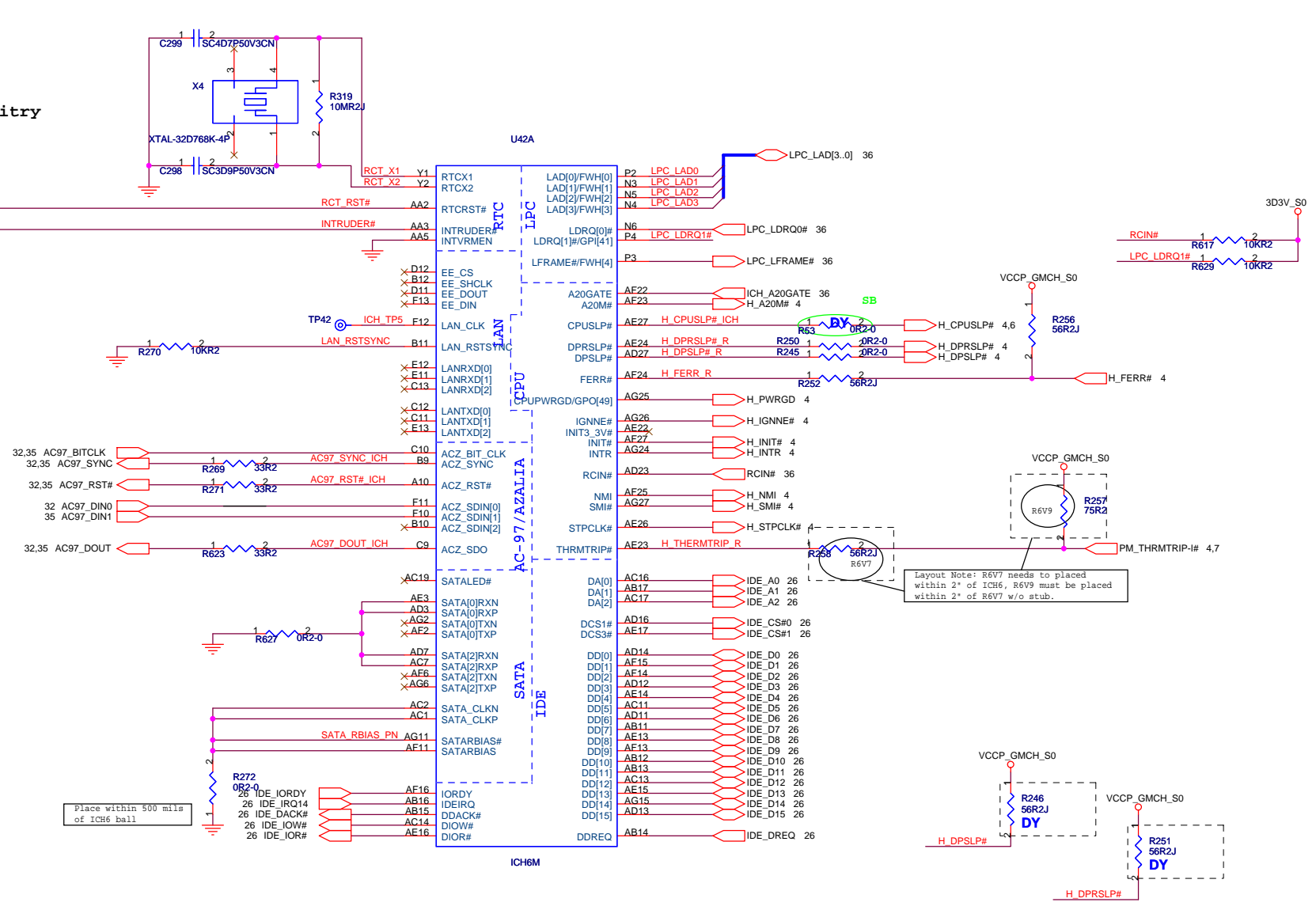
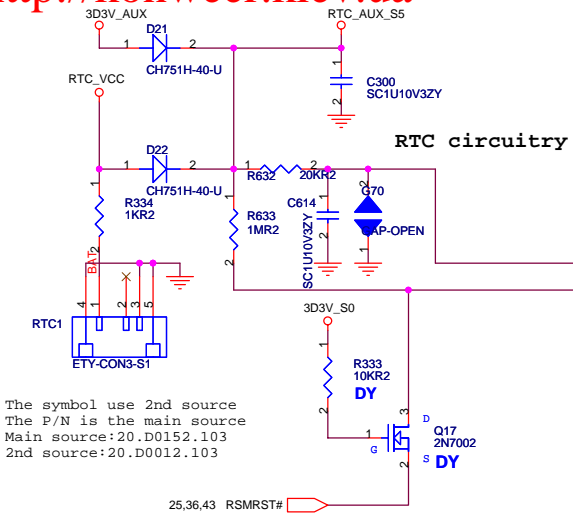
010804 Modified on Astro ID request

## CIR FOR FF



<Core Design>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> CRT/ CIR	
<b>Size</b> A3	<b>Document Number</b> Leopard2
<b>Date:</b> Thursday, July 07, 2005	<b>Rev</b> -1
Sheet 20 of 47	



Place within 500 mils of ICH6 ball

Layout Note: R6V7 needs to be placed within 2" of ICH6, R6V9 must be placed within 2" of R6V7 w/o stub.



Layout Note:  
Place above caps within  
100 mils of ICH near F27, P27, AB27

Layout Note:  
IDE decoupling

Layout Note:  
PCI decoupling

Place within 100  
mils of ICH  
near pin AG5

Place within 100  
mils of ICH  
near pin AG9

Place within 100  
mils of ICH  
near E26, E27

Place within 100  
mils of ICH  
pin AG10

Intel dummy  
Place within 100  
mils of ICH  
pin A13

Place within 100  
mils of ICH  
pin V7

Place within 100  
mils of ICH  
pin A17

Layout Note:  
Place near pin AA19

ALL NO\_STUFF Caps do  
not have layout  
requirements but if  
layout allows then place  
next to ICH6

Place within 100  
mils of ICH pin  
AG13, AG16

Layout Note:  
Distribute in PCI section  
near pin A2-A6 near D1-H1

Layout Note:  
Place near U7

Place both  
within 100 mils  
of ICH near D27

Place within 100  
mils of ICH  
C258  
SCD01U16V3KX

Place within 100  
mils of ICH

Place within 100  
mils of ICH  
pin G10

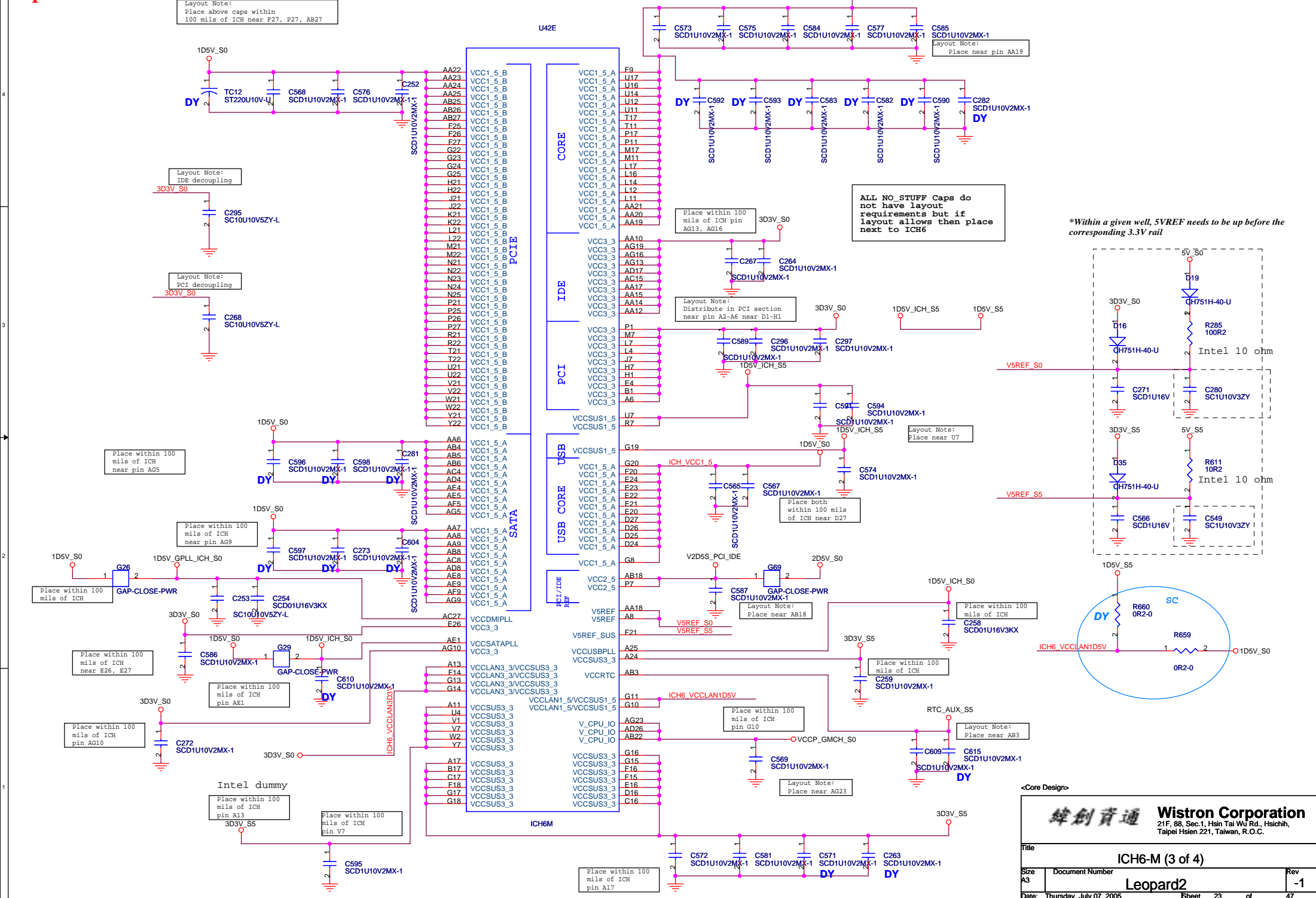
Layout Note:  
Place near AB3

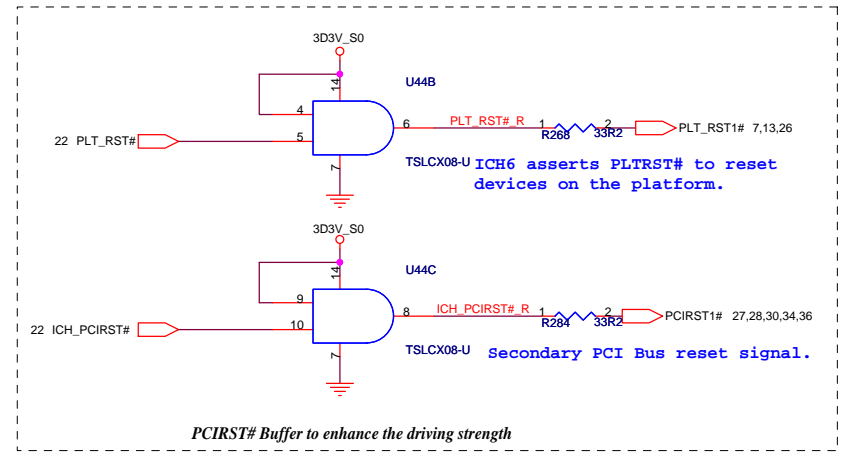
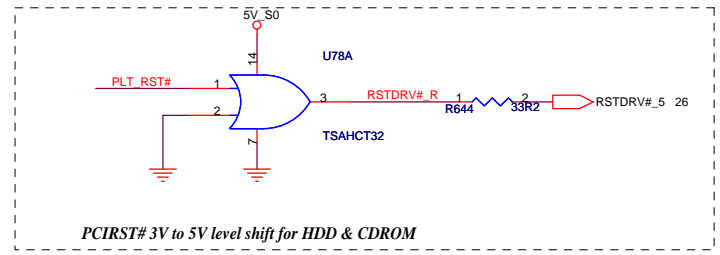
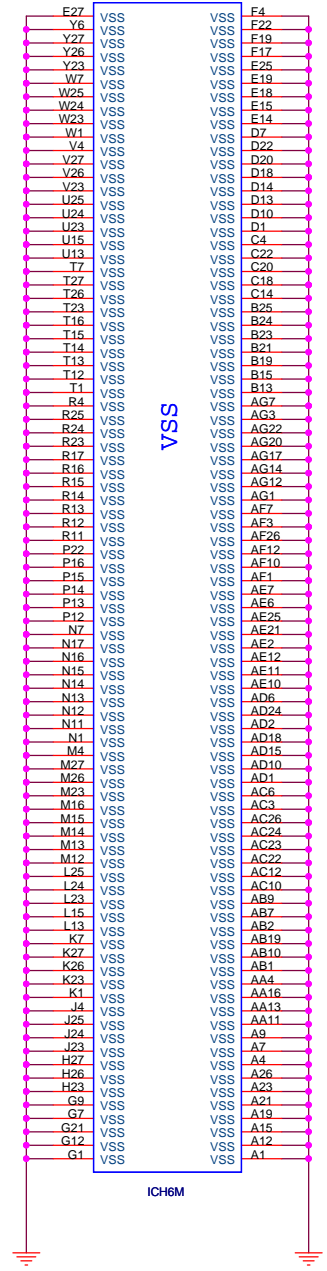
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH6-M (3 of 4)**

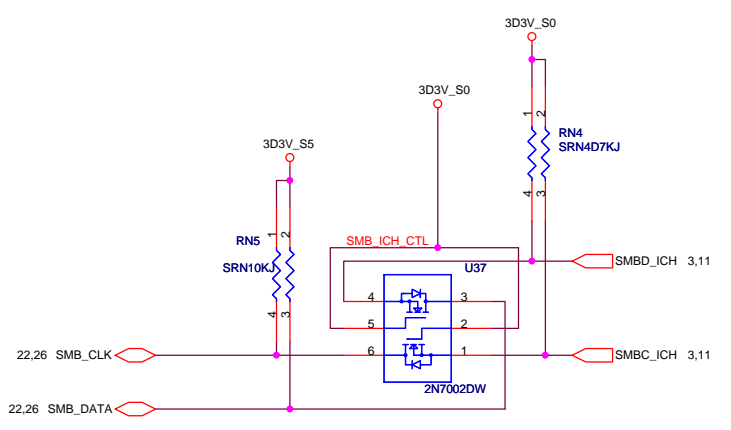
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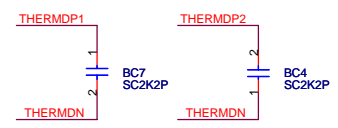
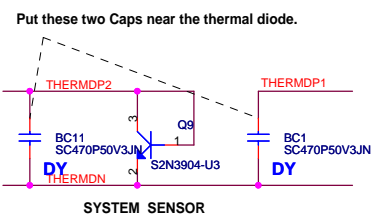
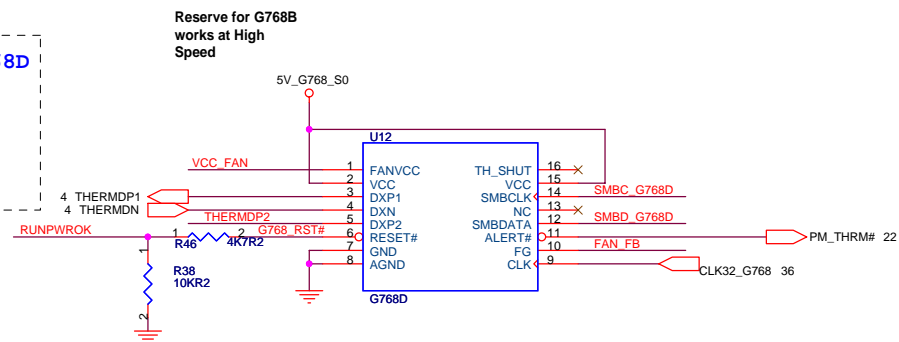
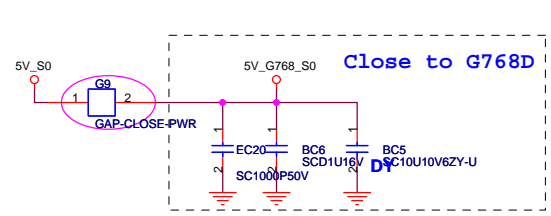
Date: Thursday, July 07, 2005 Sheet: 23 of 47





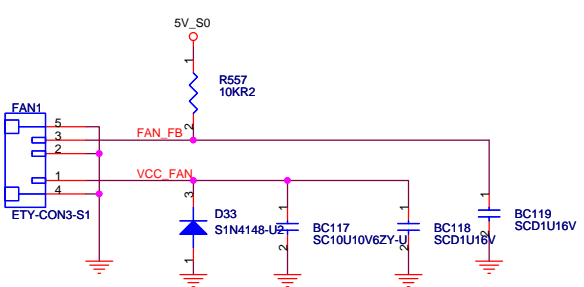
**SMBUS (ICH6 ---> SODIMM, CLKGEN)**



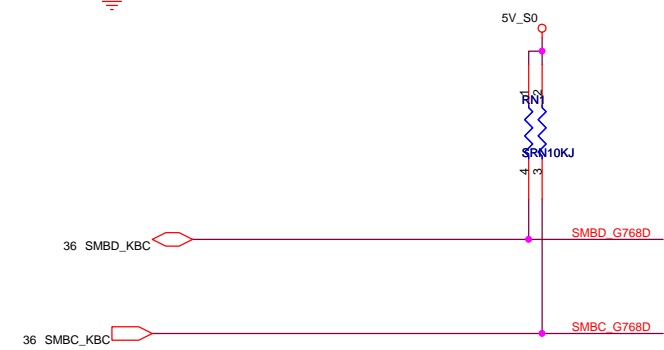
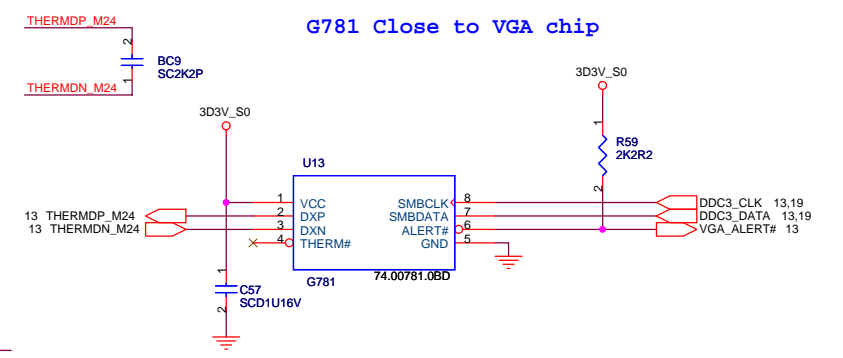
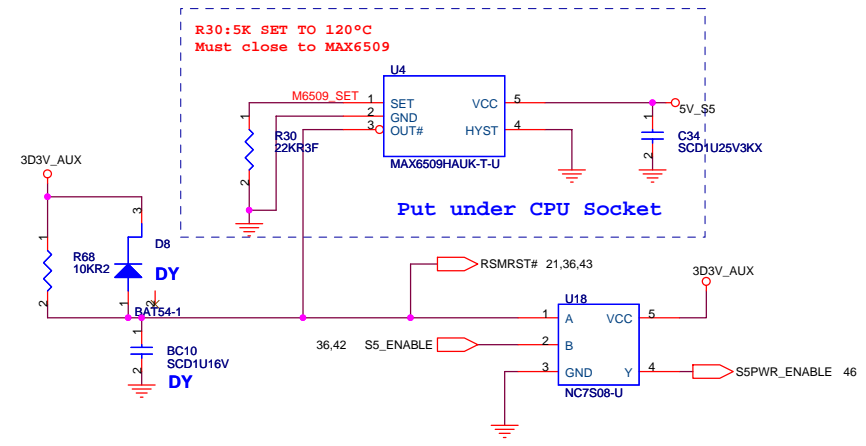
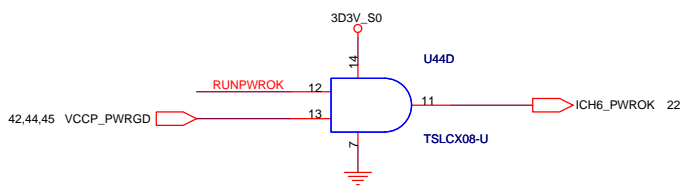
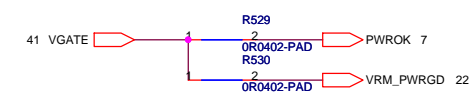
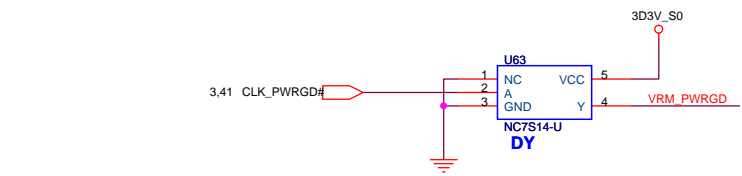


THERMDP1/DP2/THERMDN ON THE SAME LAYER  
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS  
CAPS CLOSE TO G768B

180 ms after VCC\_G768 > 4.38v, p2, 7



The symbol use 2nd source  
The P/N is the main source  
Main source:20.D0152.103  
2nd source:20.D0012.103



<Core Design>

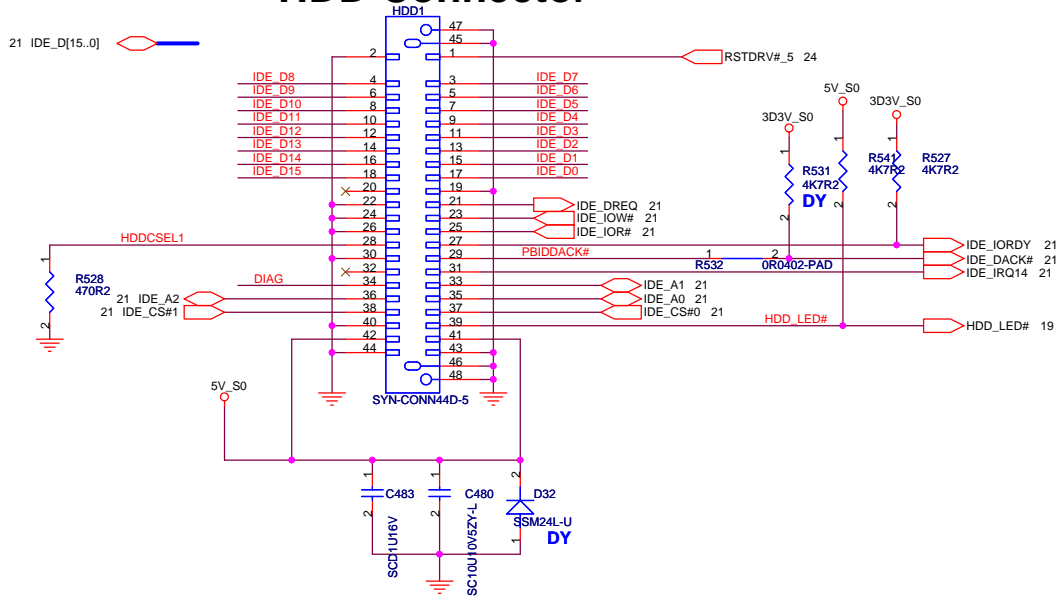
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **G768D**

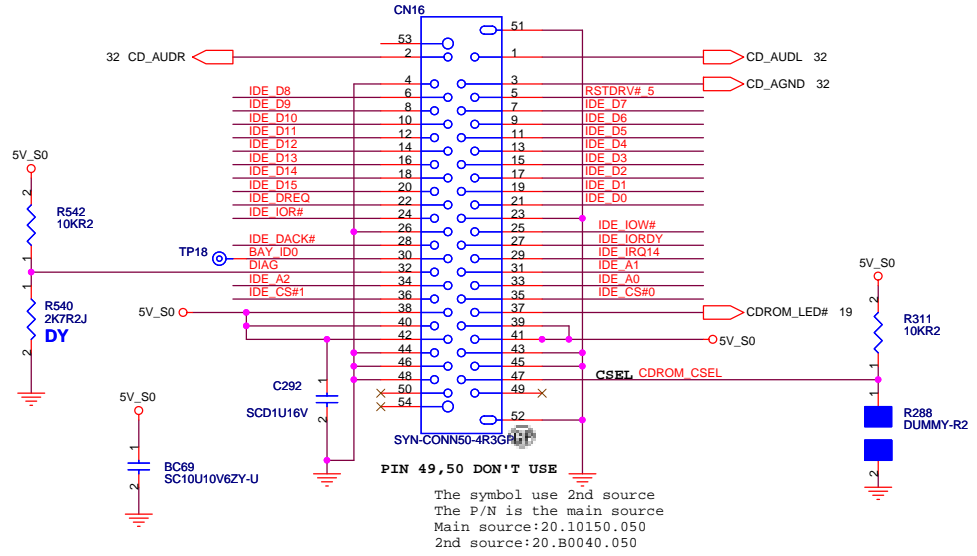
Size: A3 Document Number: **Leopard2** Rev: -1

Date: Monday, July 11, 2005 Sheet 25 of 47

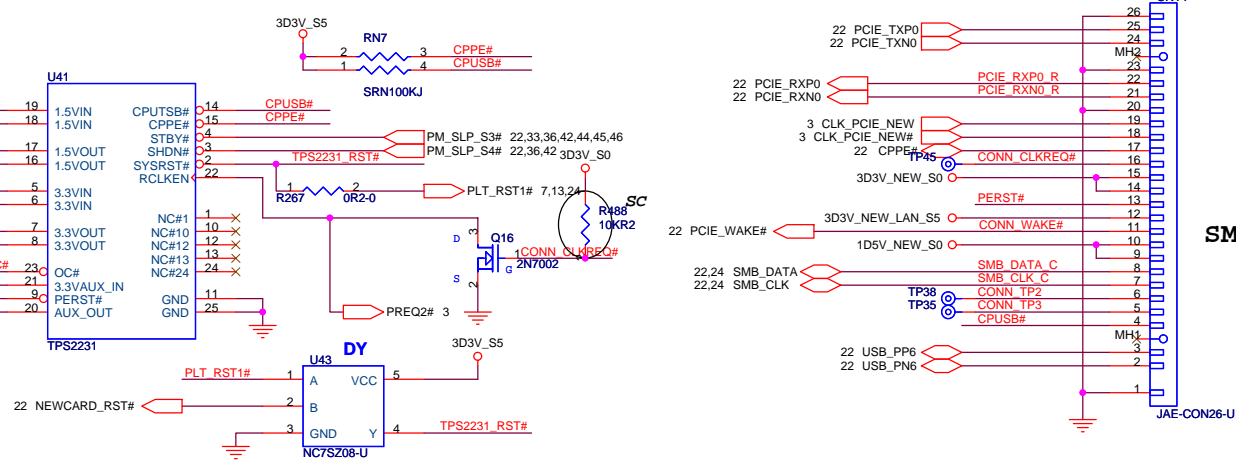
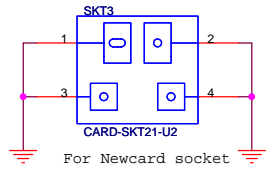
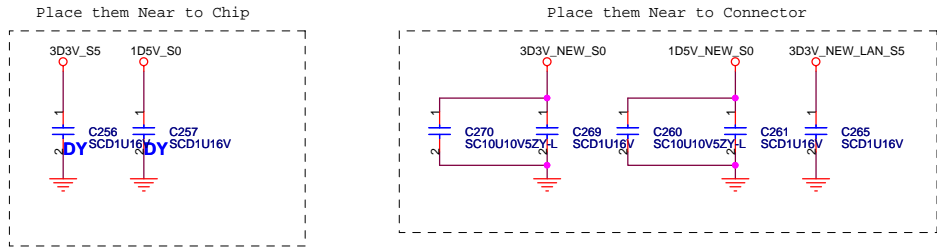
# HDD Connector



# CDROM



# NEWCARD Connector



<Core Design>

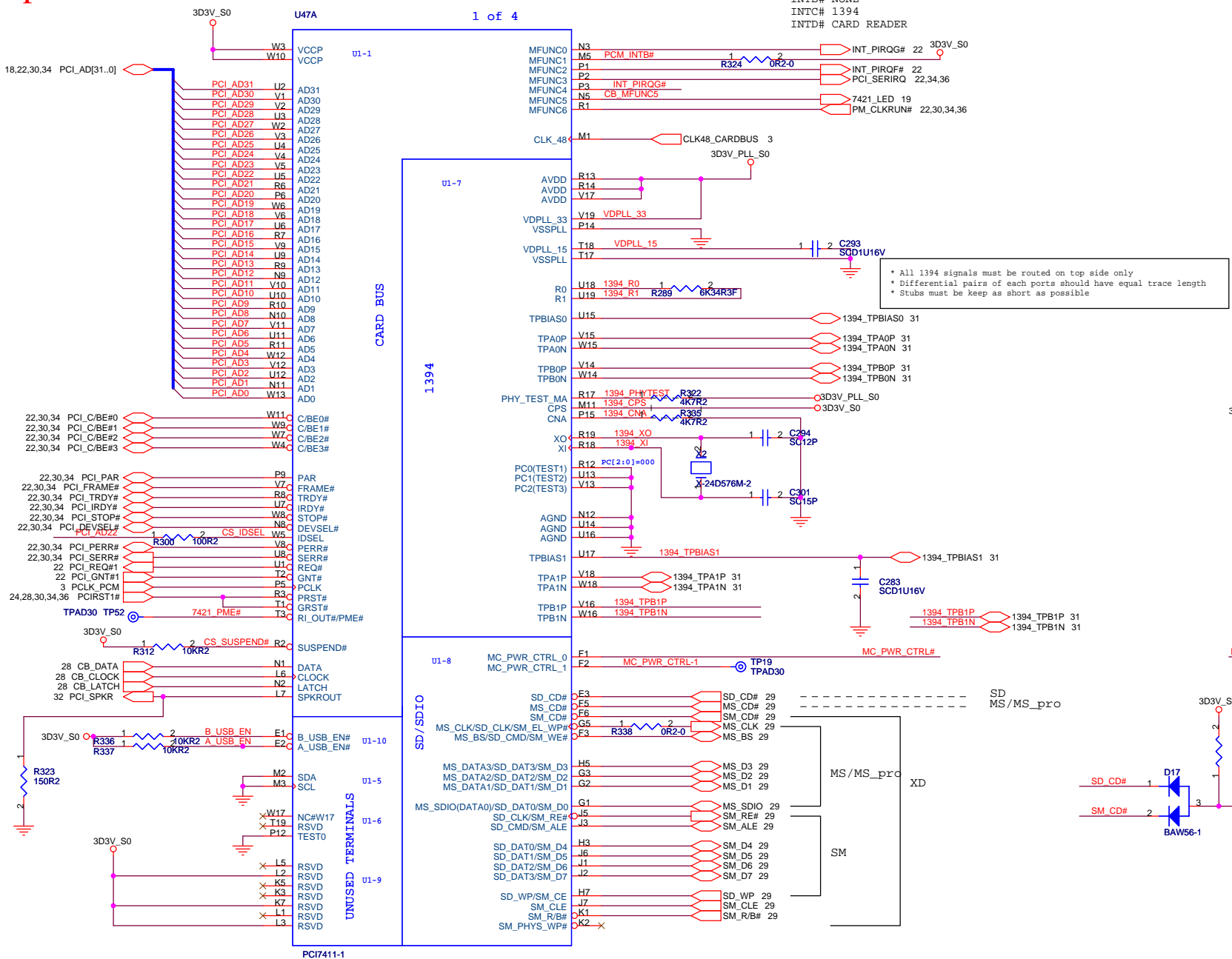
緯創資通 **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD / CDROM/NEWCARD**

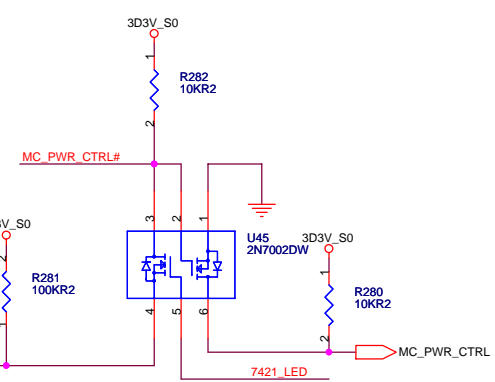
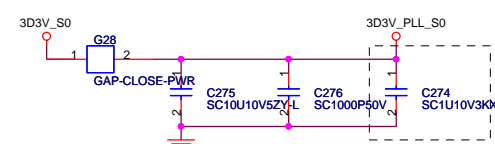
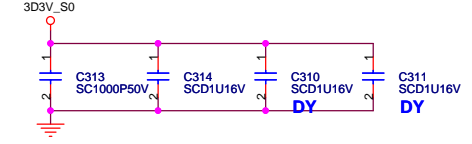
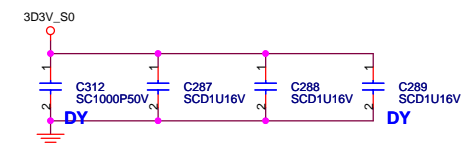
Size: A3 Document Number: **Leopard2** Rev: -1

Date: Monday, July 11, 2005 Sheet: 26 of 47

INTA# CARBUS 1  
INTB# NONE  
INTC# 1394  
INTD# CARD READER



Bypass/Decoupling Capacitors  
Should be places as close to  
PCI7421 as possible



\* All 1394 signals must be routed on top side only  
\* Differential pairs of each ports should have equal trace length  
\* Stubs must be keep as short as possible

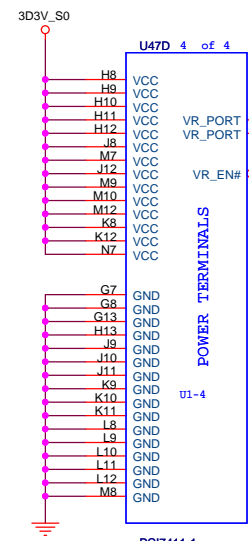
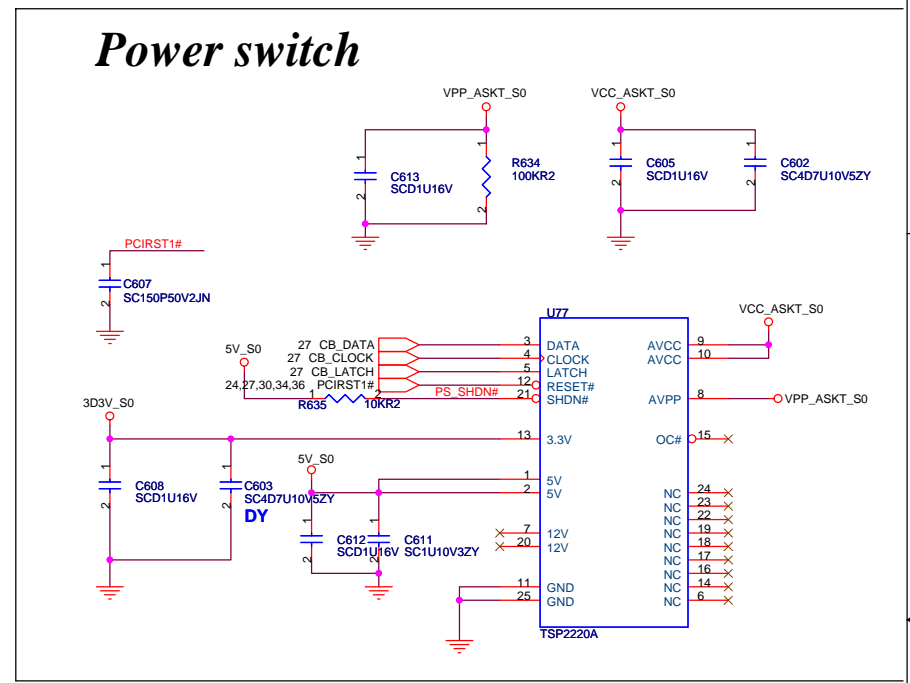
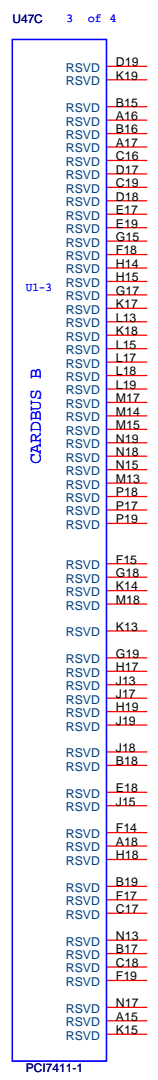
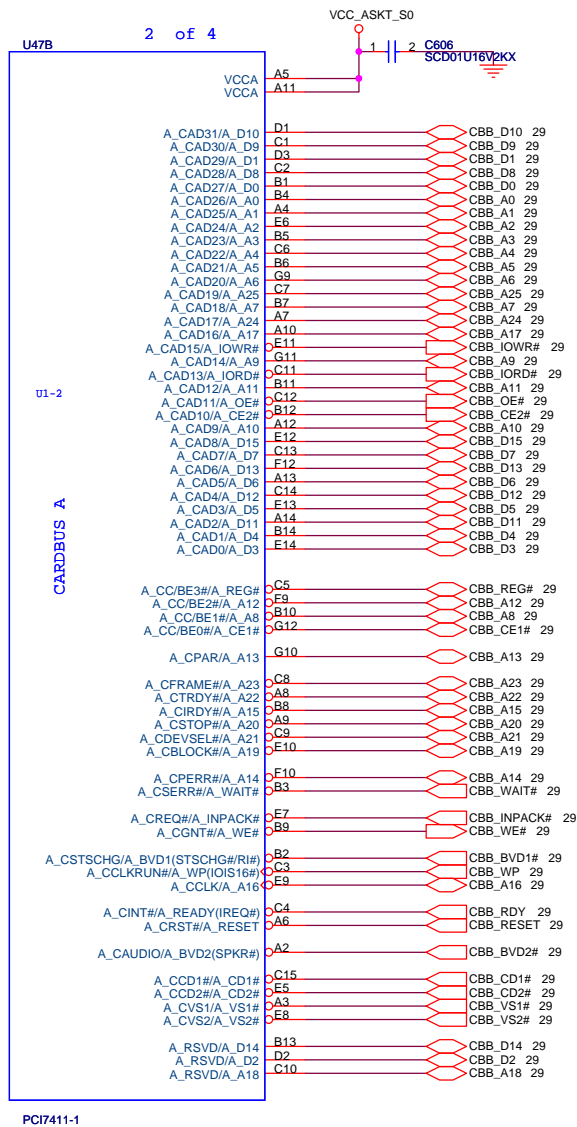
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緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: TI SNC1Q21 (1 of 2)

Size: A3 Document Number: Leopard2 Rev: -1

Date: Monday, July 11, 2005 Sheet: 27 of 47



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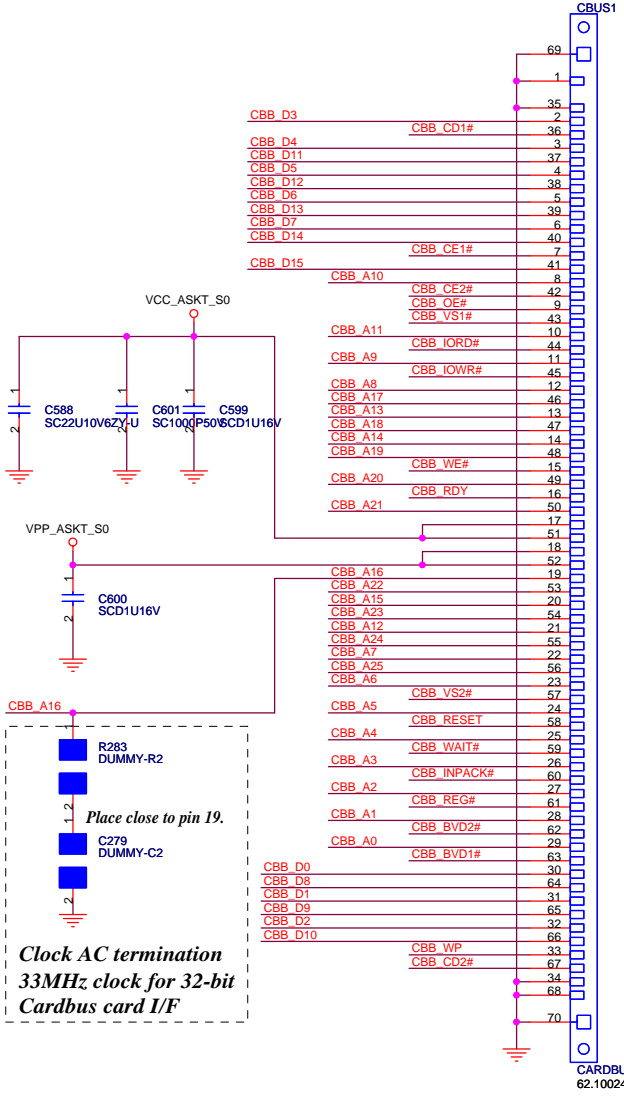
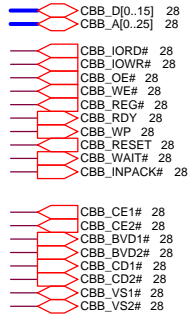
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TI PCI7411 GHK (2 of 2)

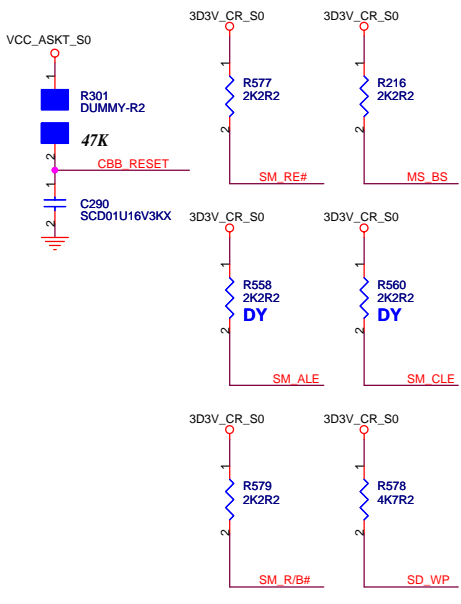
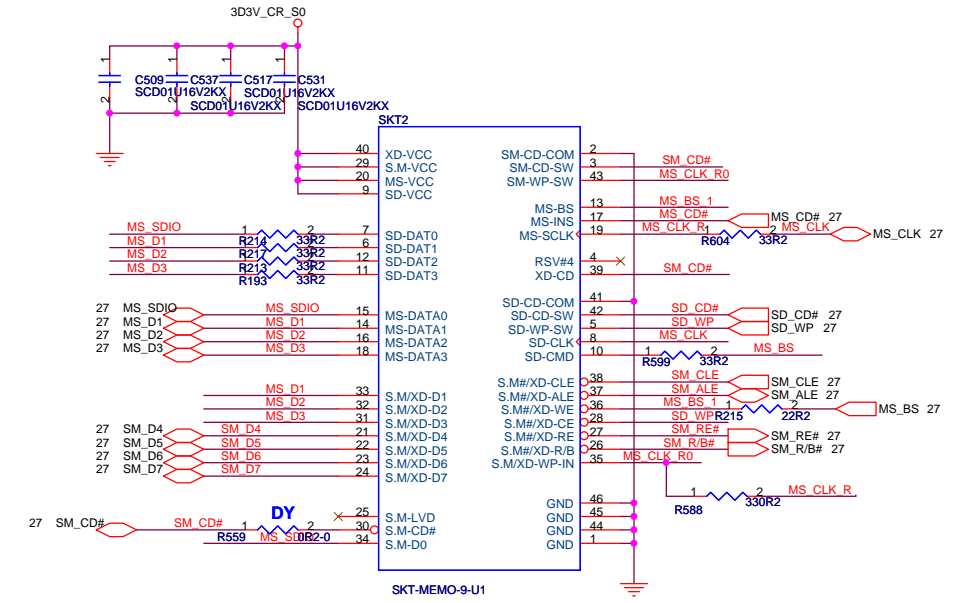
Size A3	Document Number	Rev -1
Date: Monday, July 11, 2005	Sheet 28 of 47	

# PCMCIA Socket

## Cardbus I/F



## 6 in 1 Connector



Clock AC termination  
33MHz clock for 32-bit  
Cardbus card I/F

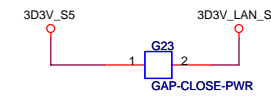
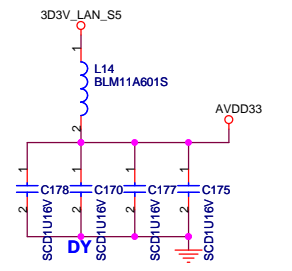
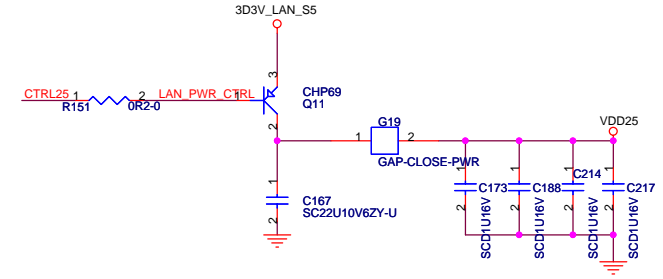
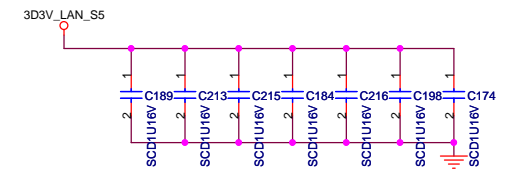
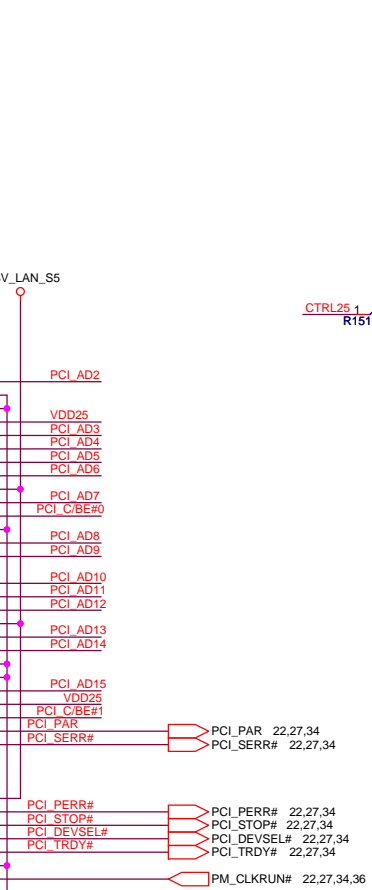
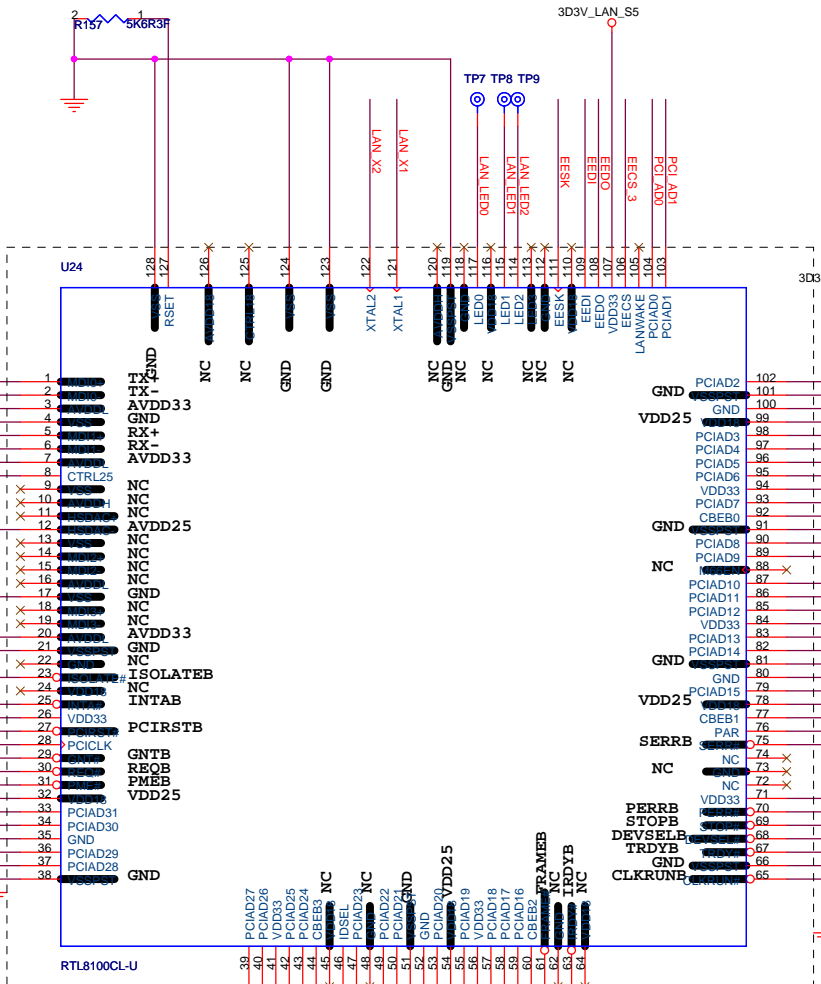
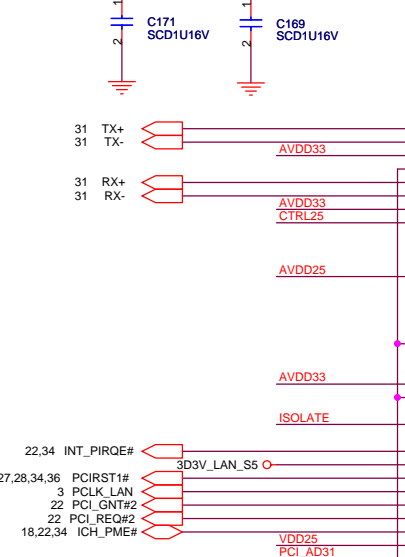
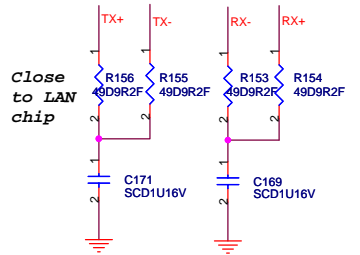
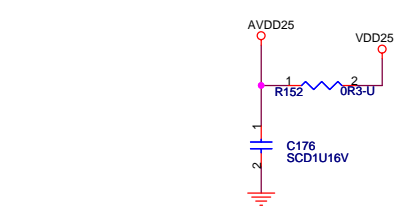
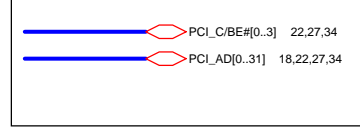
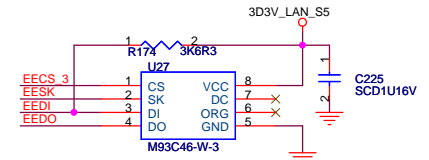
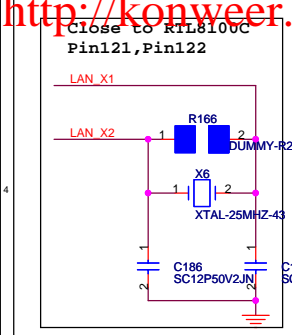
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**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCMCIA SLOT/ CARDBUS SKT**

Size: A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet: 29 of 47



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8100C

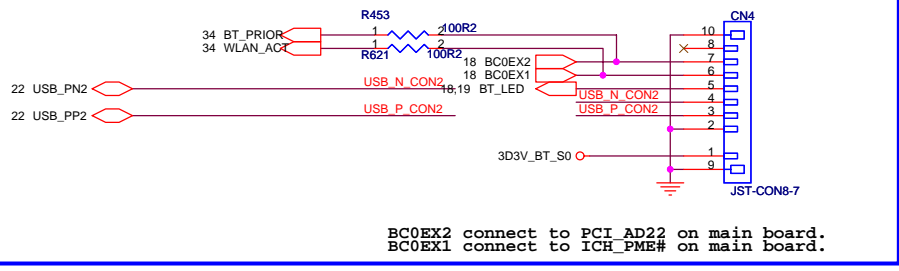
Size A3 Document Number: Leopard2 Rev -1

Date: Thursday, July 07, 2005 Sheet 30 of 47

# Blue thumb

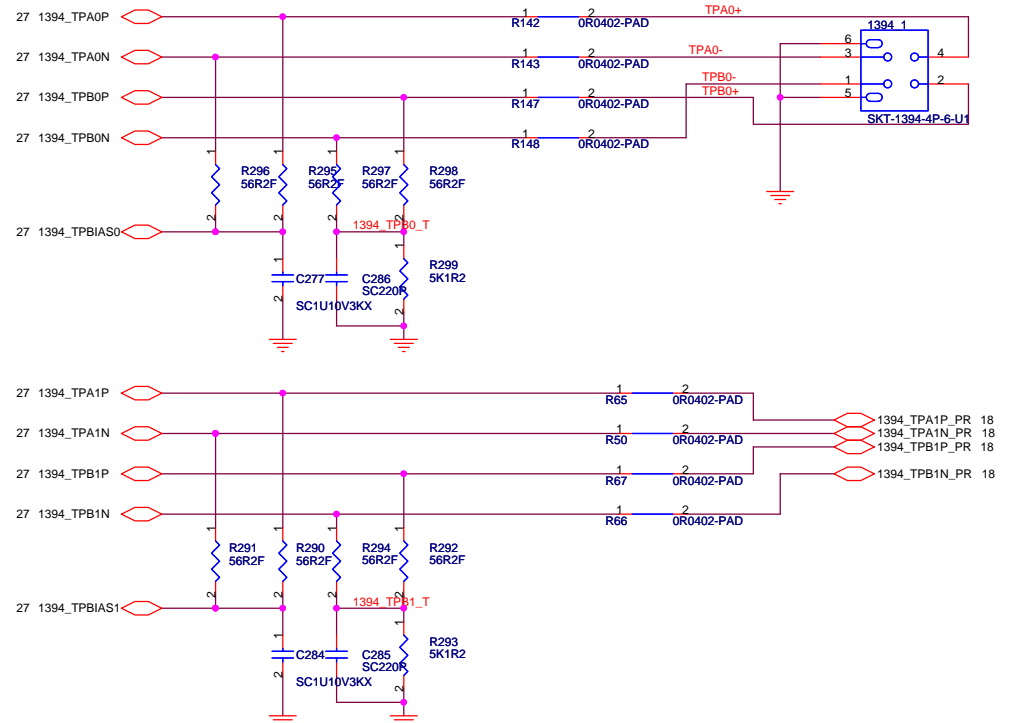
Place on bottom side

From NEW!  
1004-1



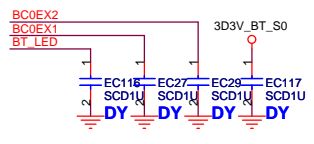
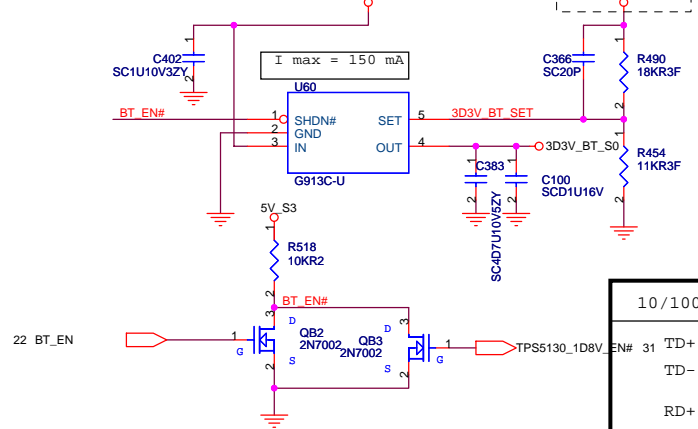
BC0EX2 connect to PCI\_AD22 on main board.  
BC0EX1 connect to ICH\_PMB# on main board.

# 1394 Connector



These components near to chip side.

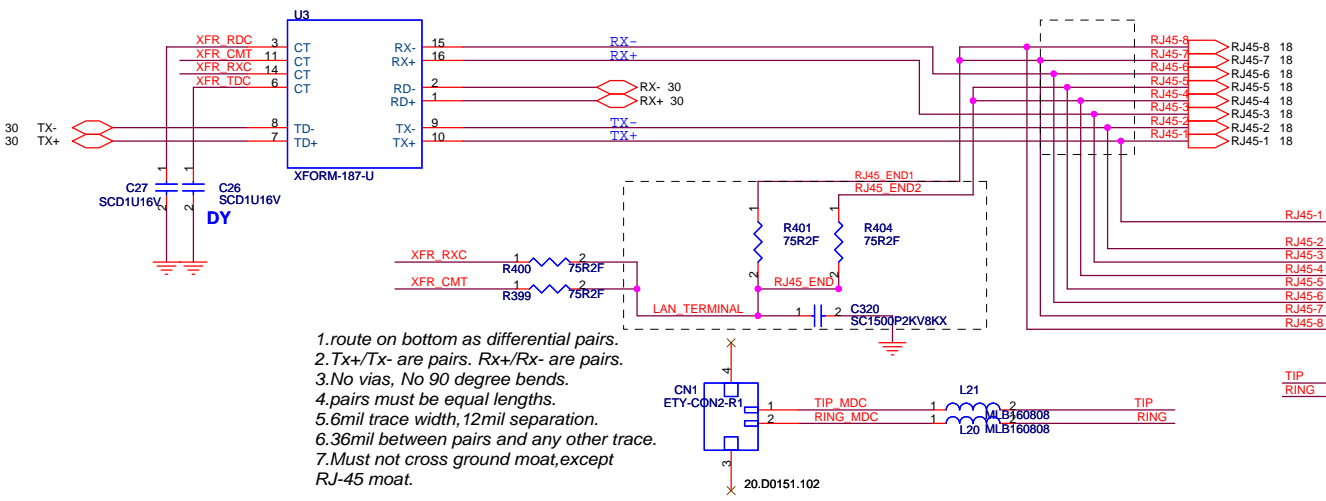
## POWER SWITCH



Close to CN20

10/100 LAN Transformer	RJ45 PIN
EN# 31 TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

## 10/100M Lan Transformer



1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

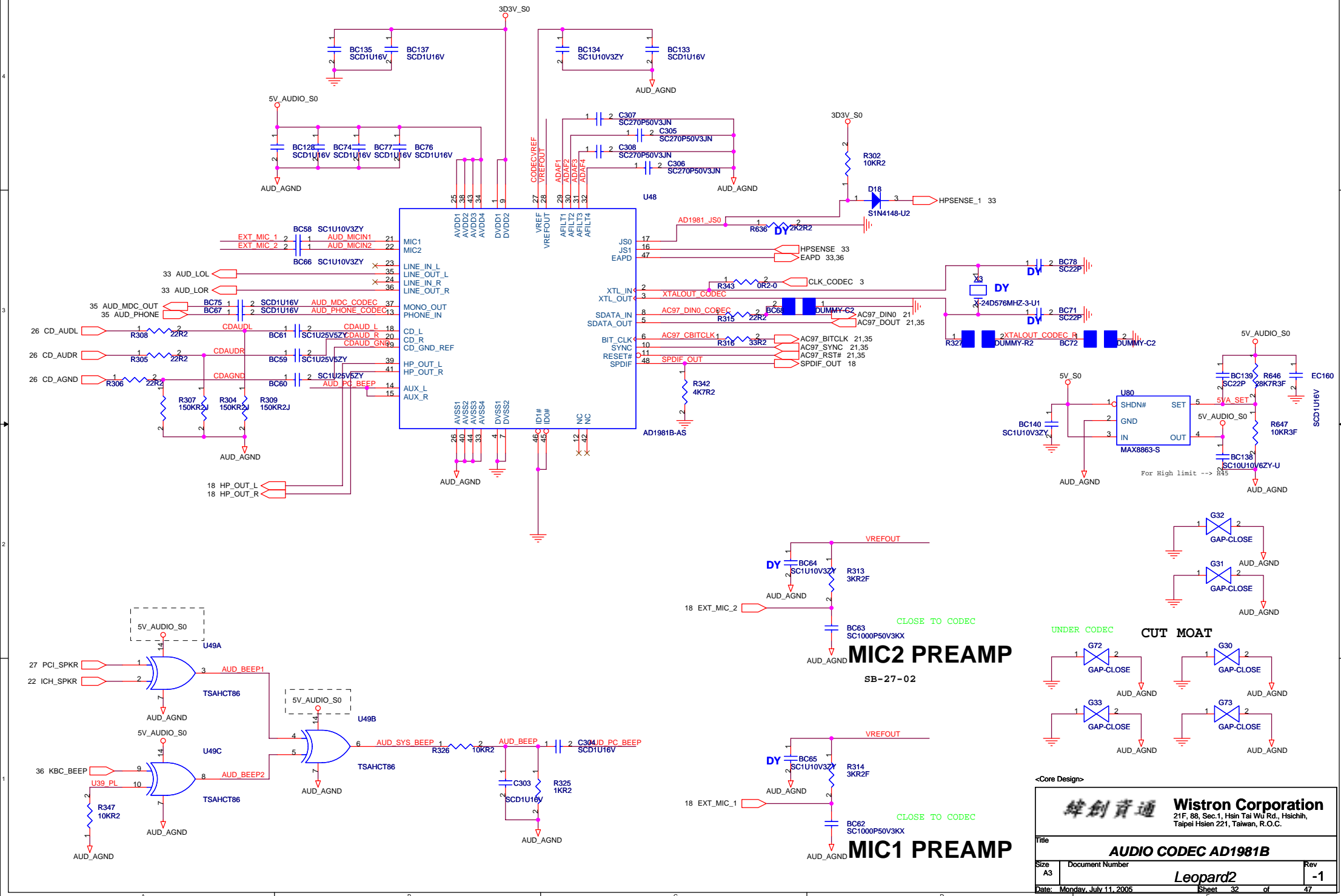
<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN / 1394 Connector**

Size A3 Document Number: **Leopard2** Rev: **-1**

Date: Monday, July 11, 2005 Sheet 31 of 47

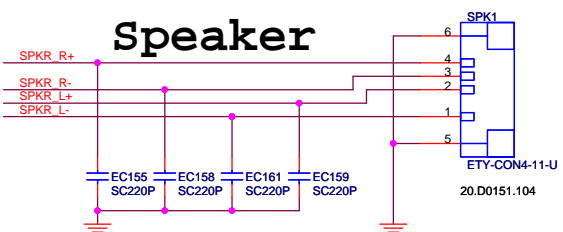
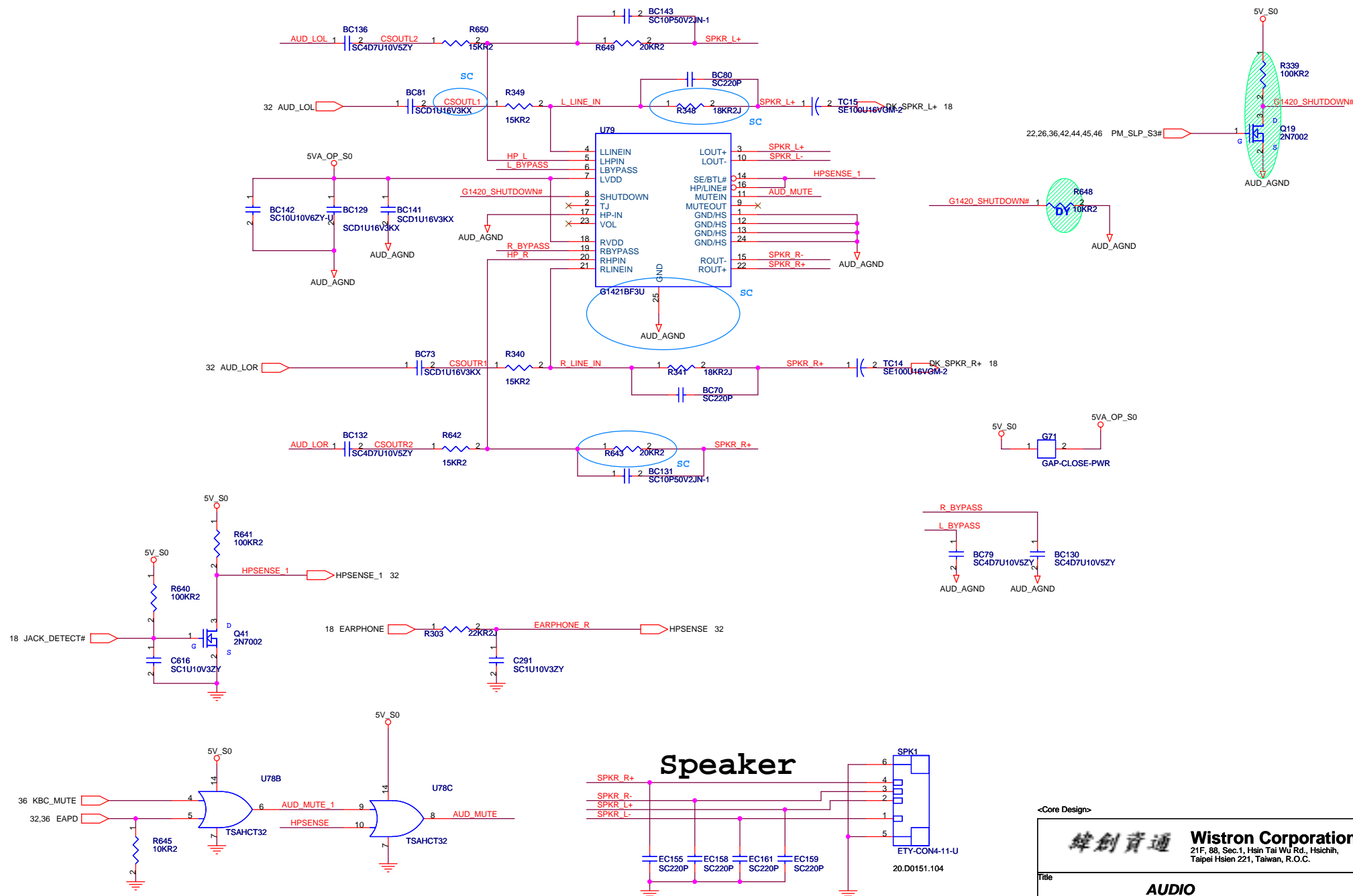


**<Core Design>**

緯創資通 **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsein 221, Taiwan, R.O.C.

Title: **AUDIO CODEC AD1981B**

Size A3	Document Number	Rev -1
Date: Monday, July 11, 2005	Sheet 32 of 47	



<Core Design>

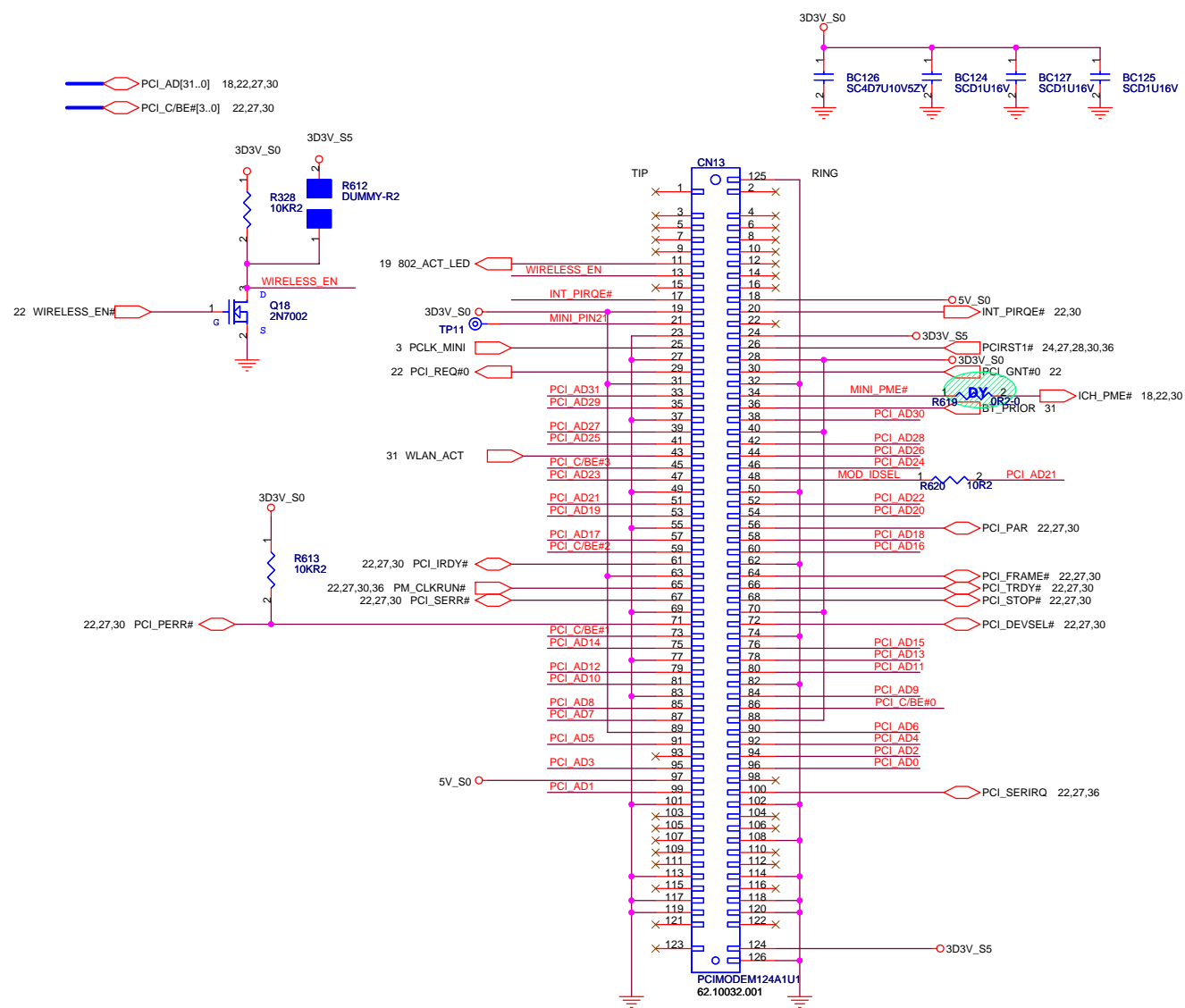
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO**

Size: A3 | Document Number: **Leopard2** | Rev: **-1**

Date: Thursday, July 07, 2005 | Sheet: 33 of 47

# MINI-PCI

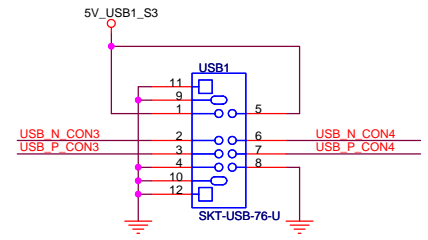
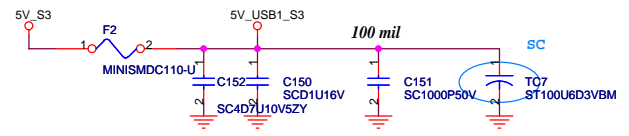


The symbol use 2nd source  
 The P/N is the main source  
 Main source:62.10032.001  
 2nd source:62.10032.031

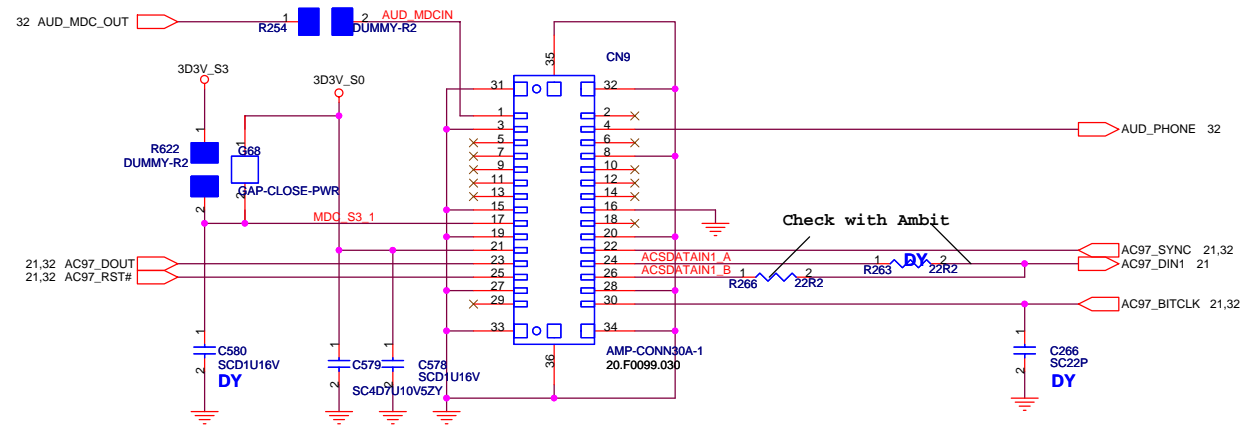
<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>MINI-PCI</b>			
Title			
Size A3	Document Number	Rev	
	<b>Leopard2</b>	<b>-1</b>	
Date: Thursday, July 07, 2005	Sheet 34	of 47	

### USB POWER



### MDC Connector



<Core Design>

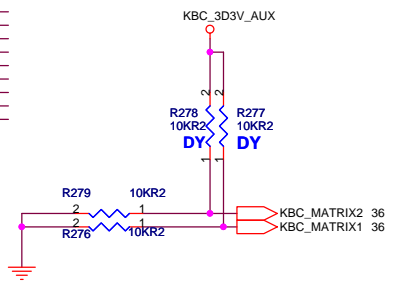
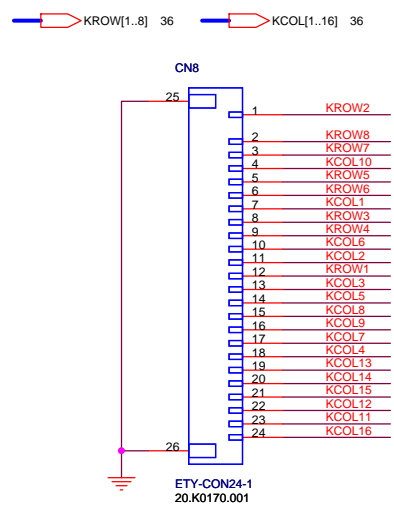
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB / MDC CONN.**

Size: A3	Document Number: <b>Leopard2</b>	Rev: <b>-1</b>
Date: Thursday, July 07, 2005	Sheet: 35	of 47



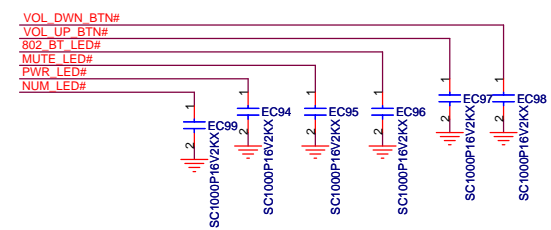
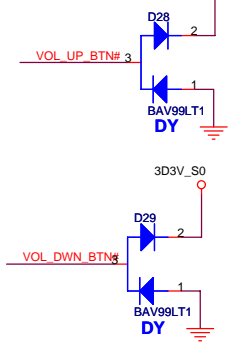
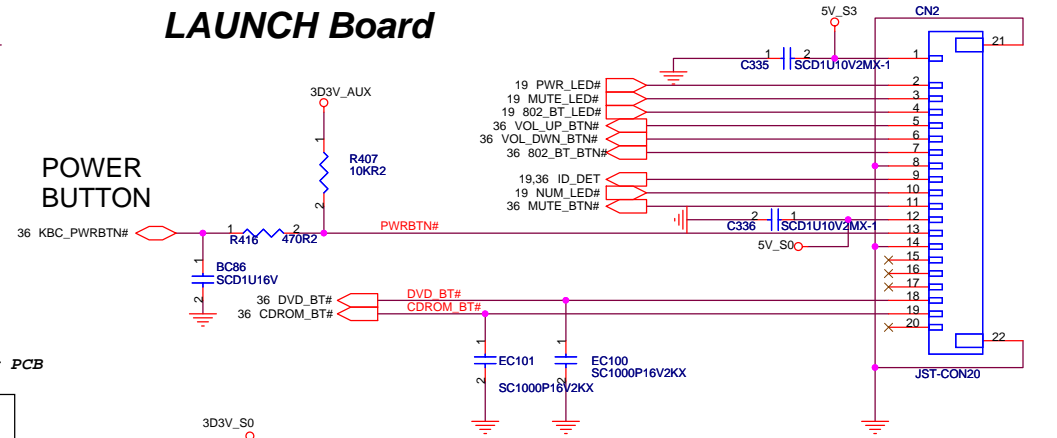
### INTERNAL KEYBOARD CONNECTOR



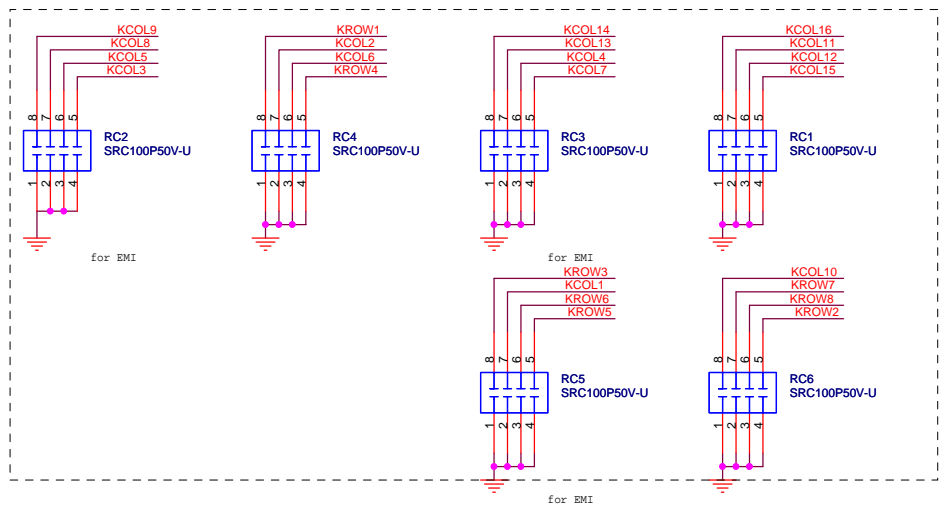
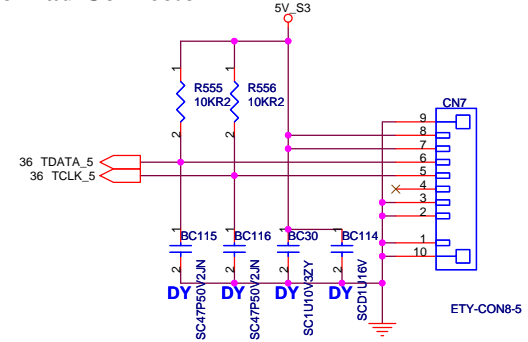
the matrix table for PCB

	PA	PR
Discrete	00	01
UMA	10	11

### LAUNCH Board



### TouchPad Connector



<Core Design>

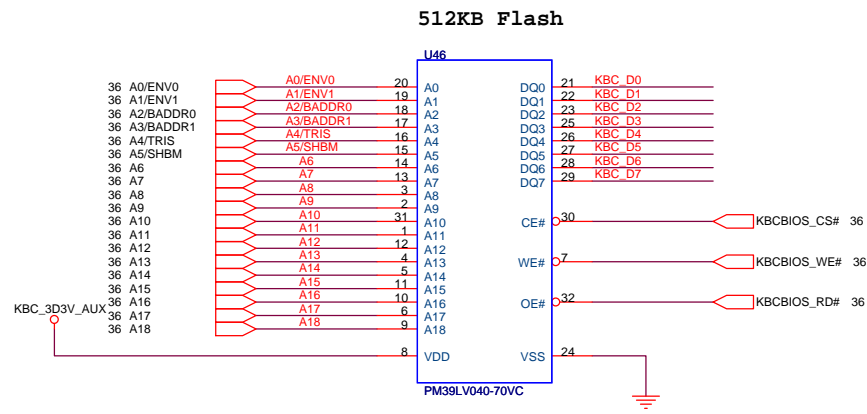
緯創資通 Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KEYBOARD/TOUCH PAD/Launch key**

Size: A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet: 37 of 47

# FLASH ROM



KBC\_D[0..7] 36

<Core Design>

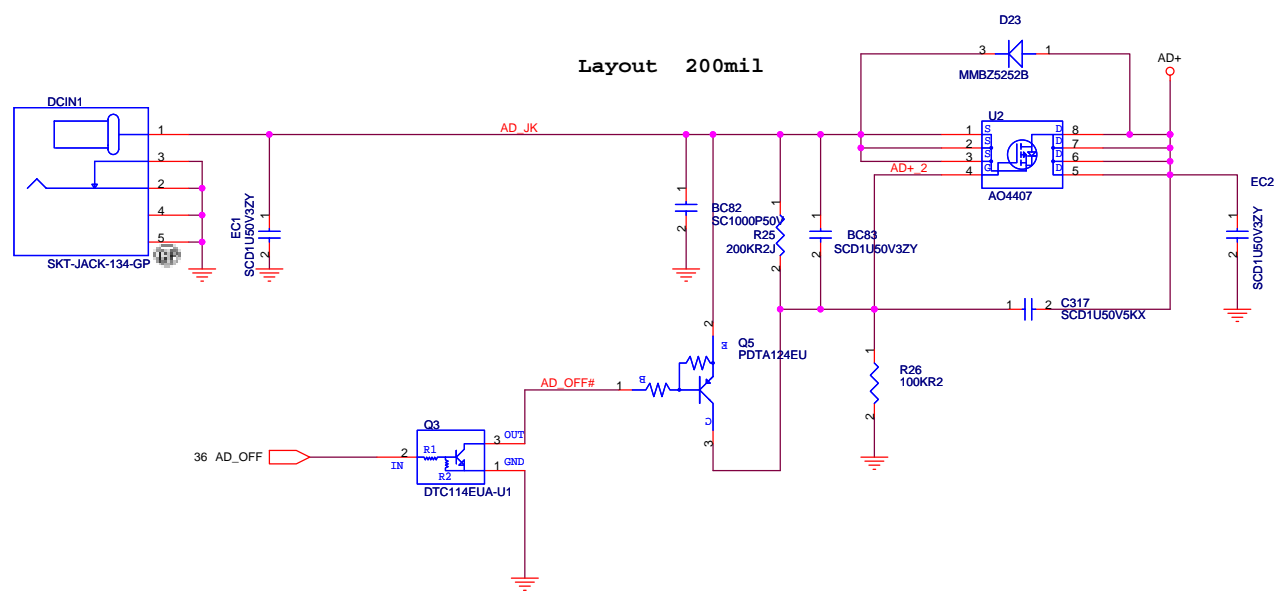
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS/GF**

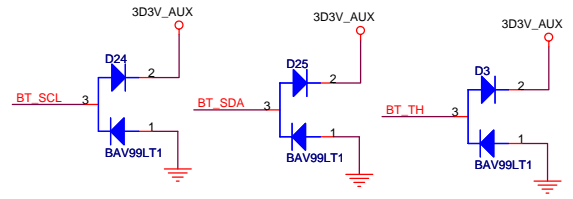
Size: A3	Document Number: <b>Leopard2</b>	Rev: <b>-1</b>
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Date: Thursday, July 07, 2005 Sheet 38 of 47

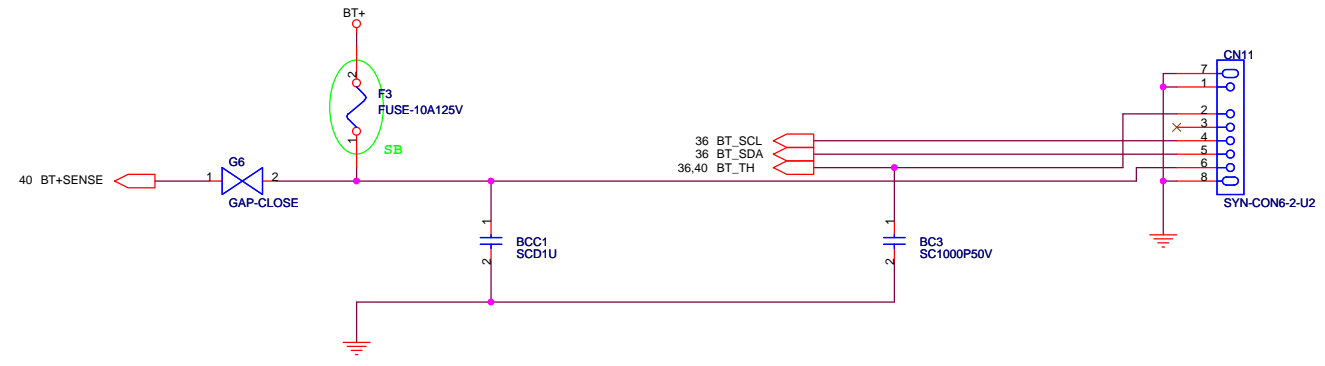
### Adaptor in to generate DCBATOUT



Layout 200mil



### BATTERY CONNECTOR



<Core Design>

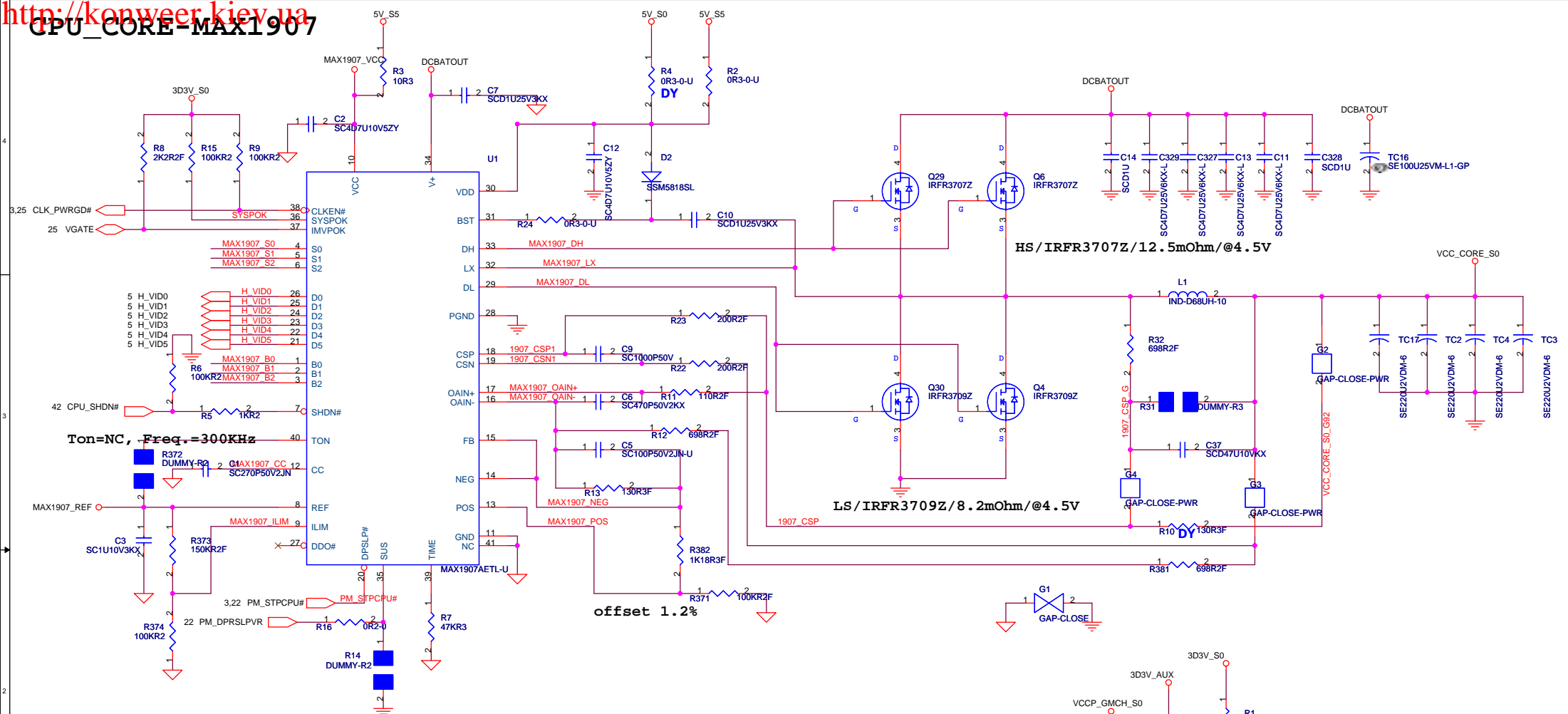
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Adaptor/ Battery conn.**

Size: A3 Document Number: **Leopard2** Rev: **-1**

Date: Thursday, July 07, 2005 Sheet 39 of 47

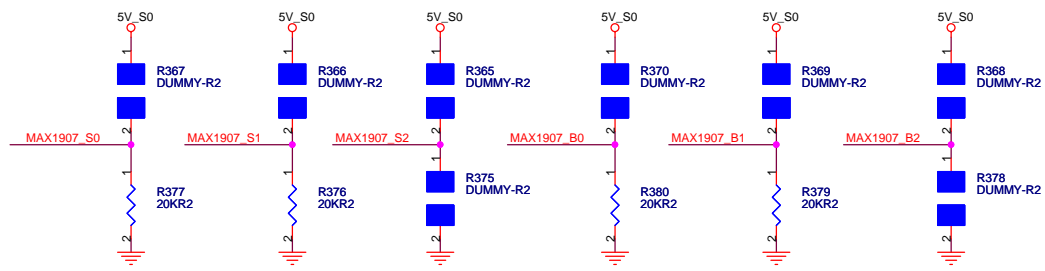




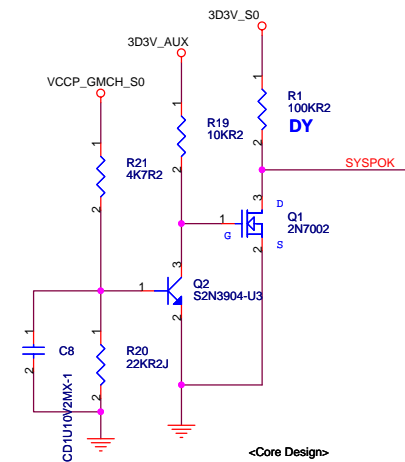
OCP=30A, Vally current = 27.5A,  
Vilim=550mV(55mVp-p\*10)

Deeper Sleep Voltage : 0.748V  
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V  
, B0=L, B1=L, B2=Open



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	v
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940



<Core Design>

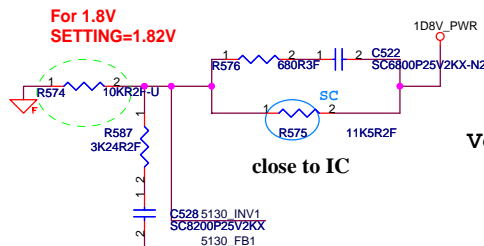
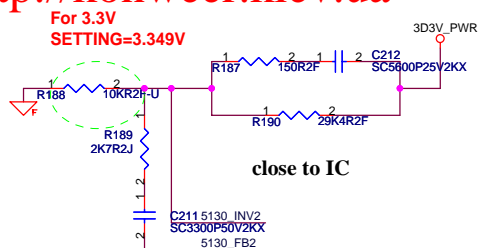
緯創資通 **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **IMVP IV-CPU POWER-MAX1907**

Size: A3 Document Number: **Leopard2** Rev: **-1**

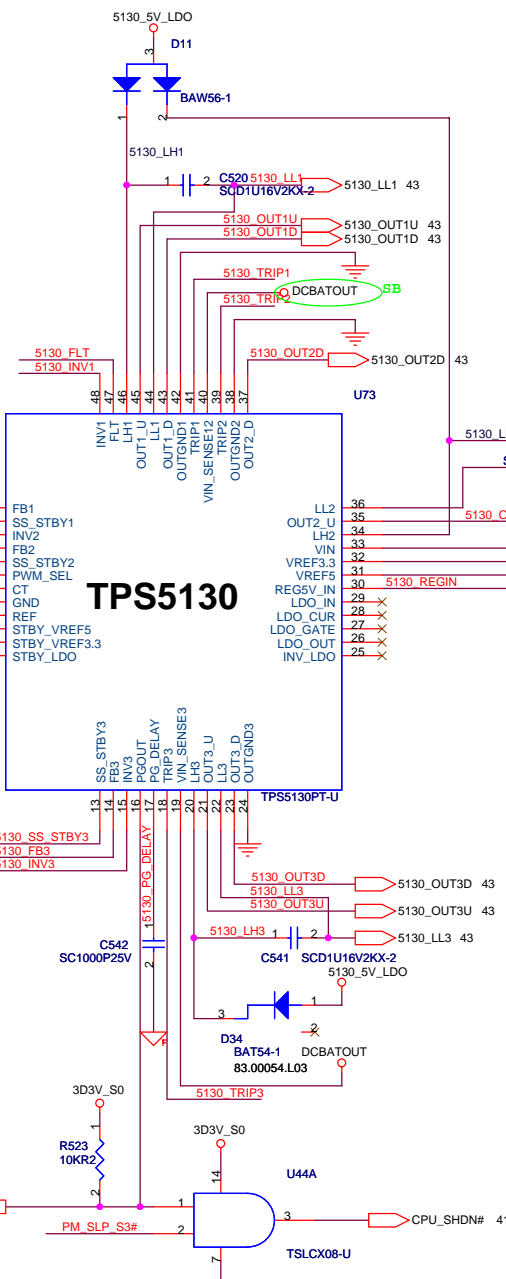
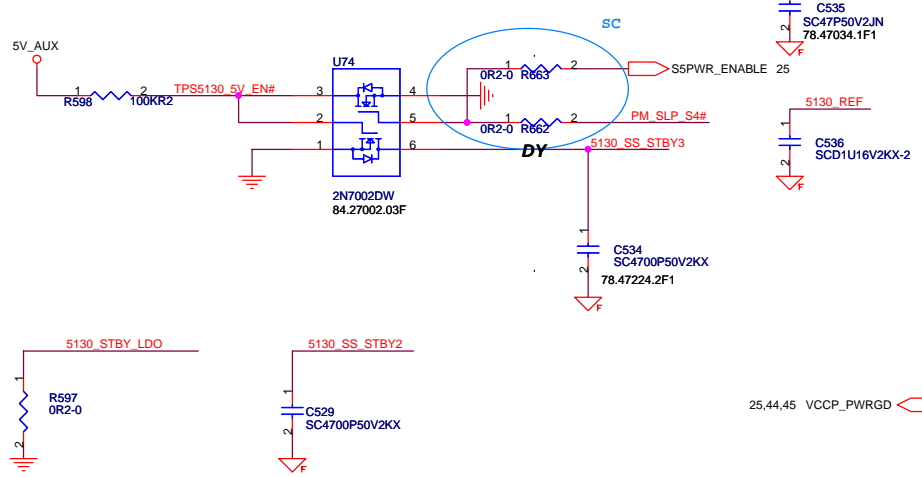
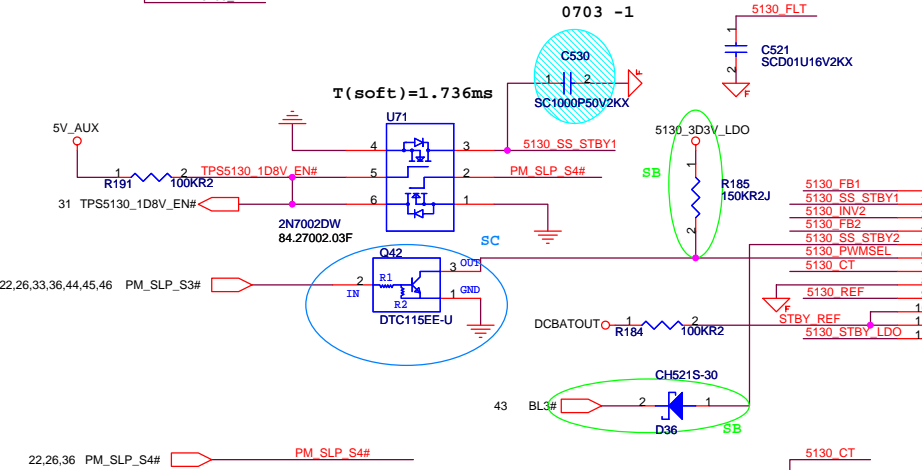
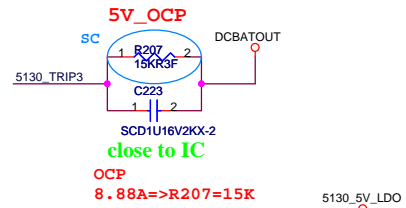
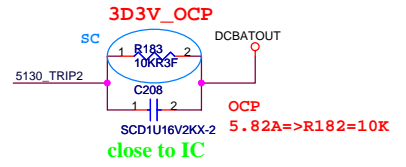
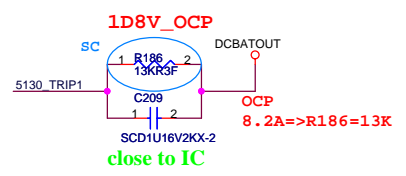
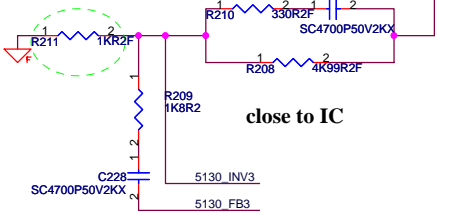
Date: Monday, July 11, 2005 Sheet: 41 of 47

# TI TPS5130 for 1D8V, 3D3V, 5V



$$V_o = (R1 * 0.85) / R2 + 0.85$$

(1D8V=>CH1 , 3D3V=>CH2 , 5V =>CH3)  
For 5V  
SETTING=5.0915V



	Condition	Voltage
PWM_SEL	H : Auto PWM/SKIP	2.2V(Min)~
	L : PWM fixed (300KHz)	~0.3V(Max)

<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

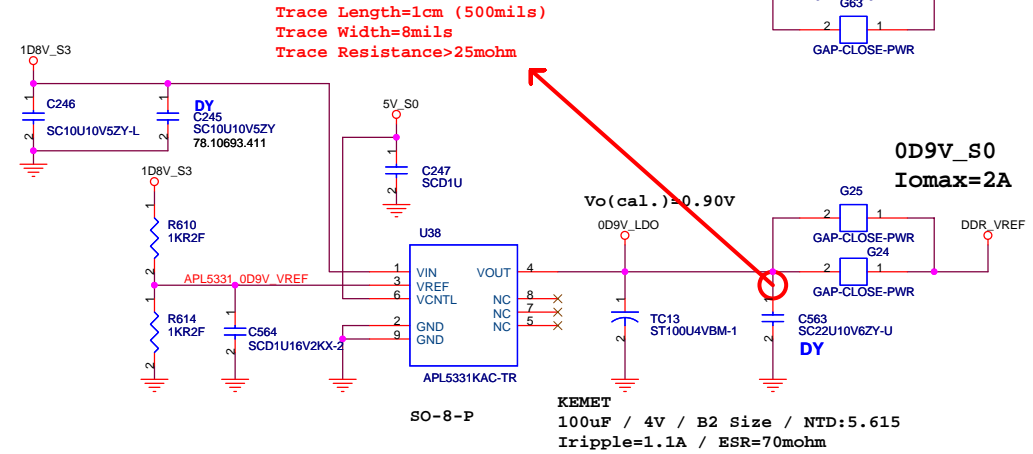
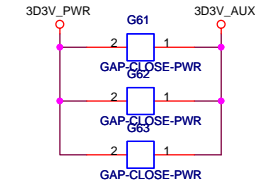
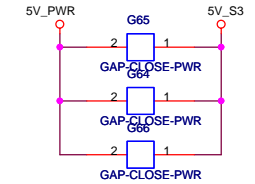
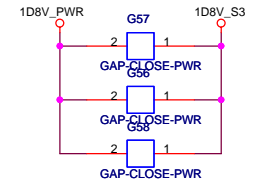
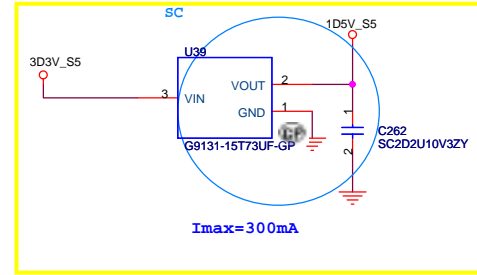
Title: **TPS5130 (3D3V/5V/1D8V)**

Size: A3 Document Number: **Leopard2** Rev: -1

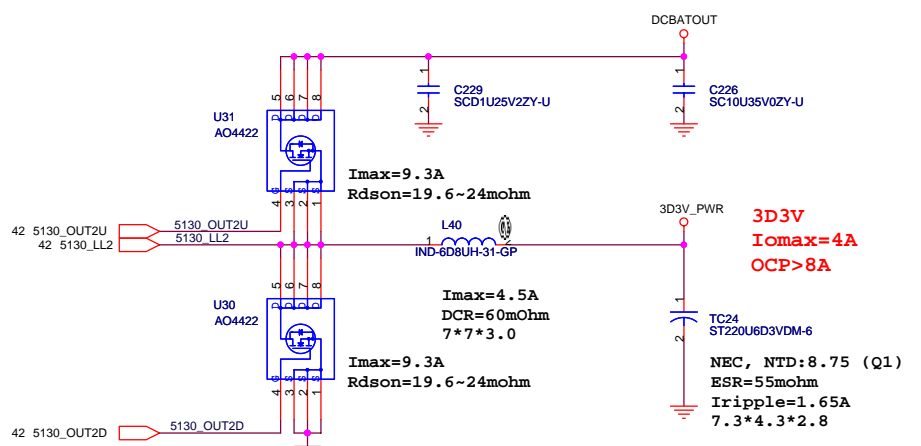
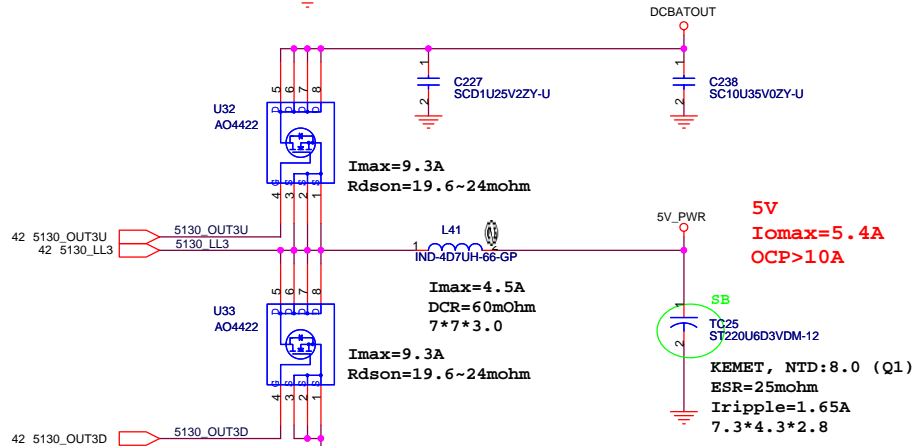
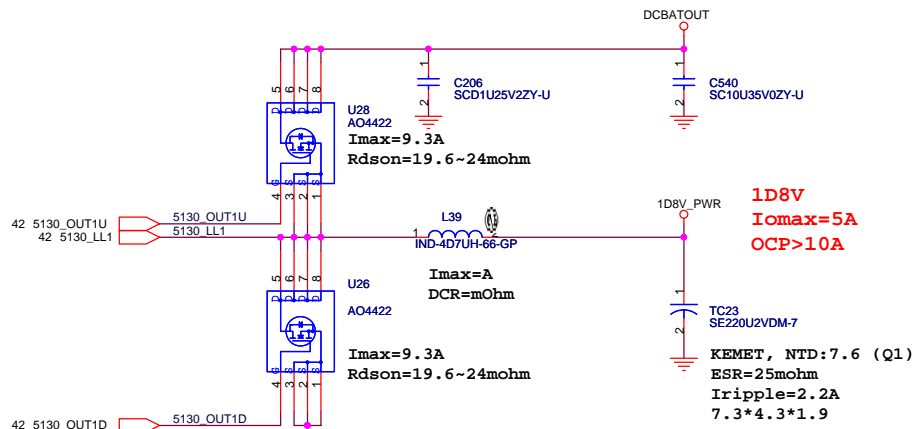
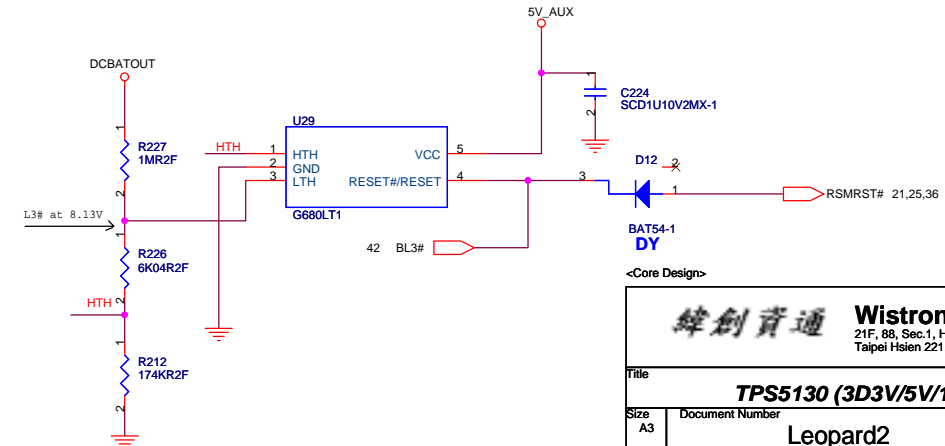
Date: Thursday, July 07, 2005 Sheet: 42 of 47

HW Thermal Throttling

**1.5V\_S5 (For ICH6)**

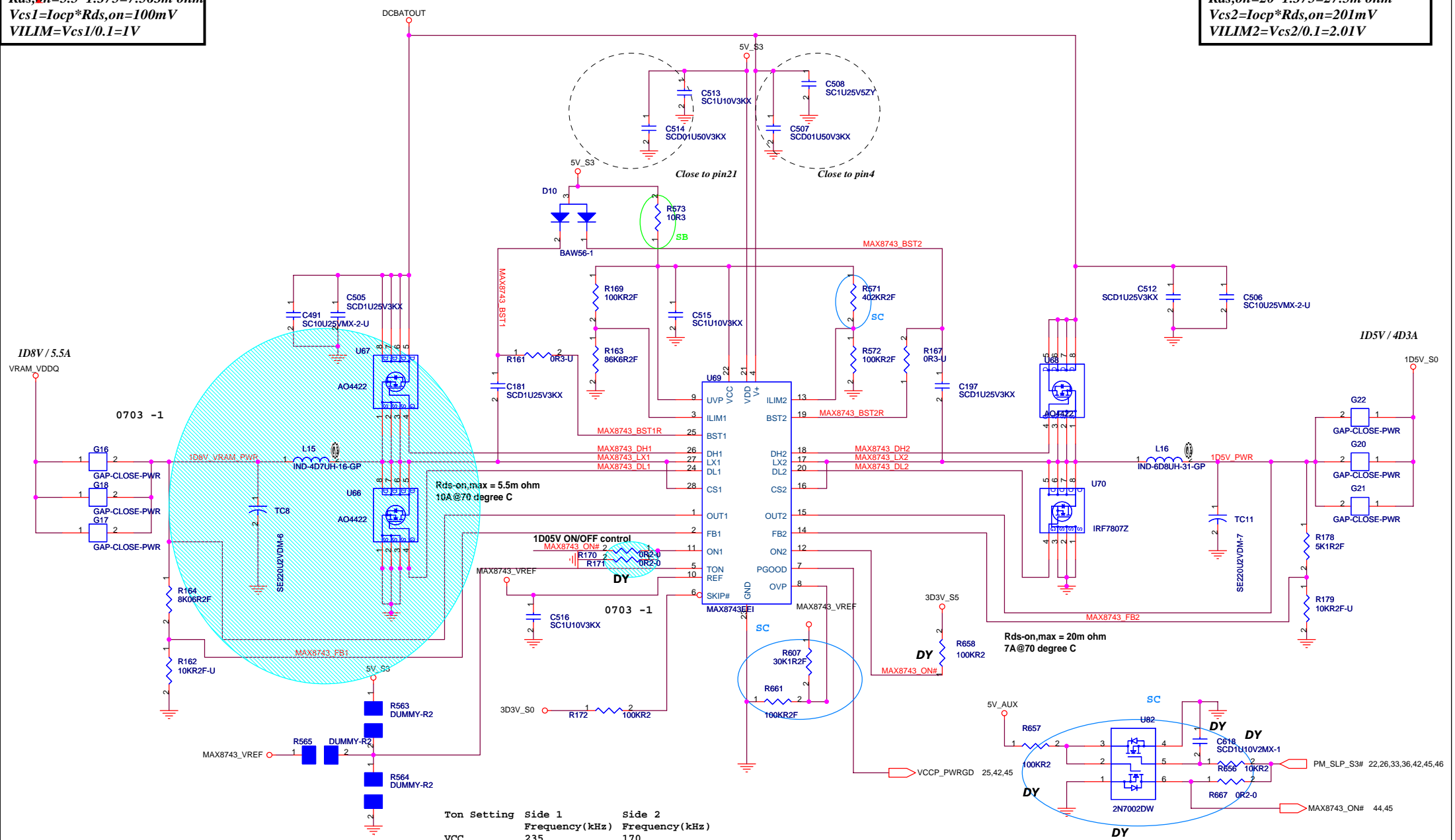


**L3# circuit**

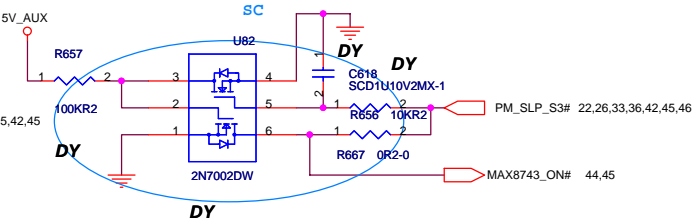


$I_{ocp} = 7.8 * 1.7 = 13.3A$   
 $R_{ds,on} = 5.5 * 1.375 = 7.563m\ ohm$   
 $V_{cs1} = I_{ocp} * R_{ds,on} = 100mV$   
 $V_{ILIM} = V_{cs1} / 0.1 = 1V$

$I_{ocp} = 4.3 * 1.7 = 7.3A$   
 $R_{ds,on} = 20 * 1.375 = 27.5m\ ohm$   
 $V_{cs2} = I_{ocp} * R_{ds,on} = 201mV$   
 $V_{ILIM2} = V_{cs2} / 0.1 = 2.01V$



Ton Setting	Side 1	Side 2
Frequency (kHz)	235	170
VCC	235	170
Float	345	255
VREF	485	355
AGND	620	460



<Core Design>

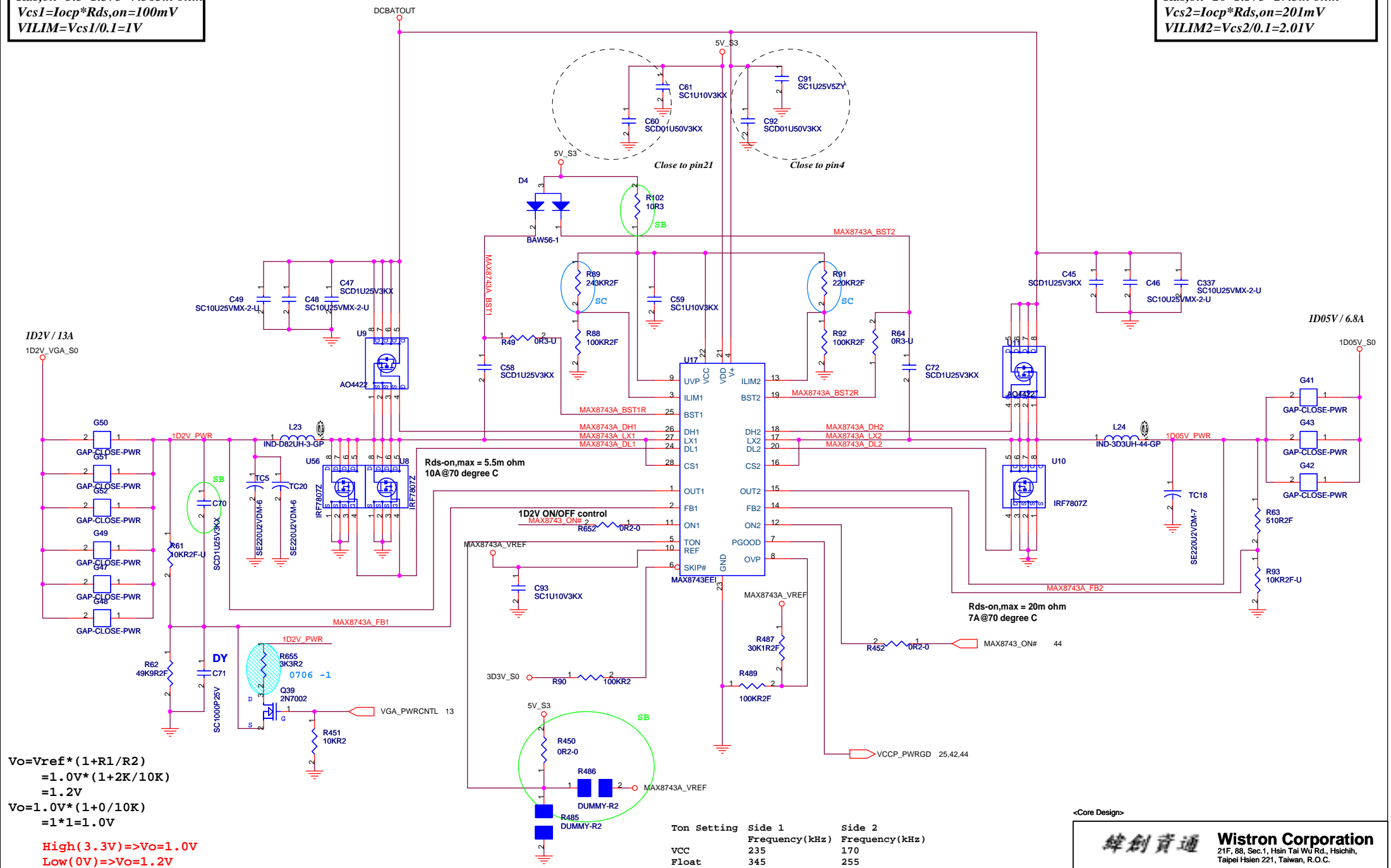
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

**MAX8743 (1D8V\_S0/1D5V\_S0)**

File	MAX8743 (1D8V_S0/1D5V_S0)	
Size	Document Number	Rev
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$I_{ocp} = 4.3 * 1.7 = 7.3A$   
 $R_{ds,on} = 20 * 1.375 = 27.5m\ \Omega$   
 $V_{cs1} = I_{ocp} * R_{ds,on} = 100mV$   
 $VILIM = V_{cs1} / 0.1 = 1V$

$I_{ocp} = 7.8 * 1.7 = 13.3A$   
 $R_{ds,on} = 5.5 * 1.375 = 7.563m\ \Omega$   
 $V_{cs1} = I_{ocp} * R_{ds,on} = 100mV$   
 $VILIM = V_{cs1} / 0.1 = 1V$



$V_o = V_{ref} * (1 + R1/R2)$   
 $= 1.0V * (1 + 2K/10K)$   
 $= 1.2V$   
 $V_o = 1.0V * (1 + 0/10K)$   
 $= 1 * 1 = 1.0V$   
**High (3.3V) =>  $V_o = 1.0V$**   
**Low (0V) =>  $V_o = 1.2V$**

M24/M26 POWER PLAY (VGA\_PWRCNTL)  
 high (3.3V) = set lower core voltage (VDDC = 1.0V)  
 low (0V) = set higher core voltage (VDDC = 1.2V)

Ton Setting	Side 1 Frequency (kHz)	Side 2 Frequency (kHz)
VCC	235	170
Float	345	255
VREF	485	355
AGND	620	460

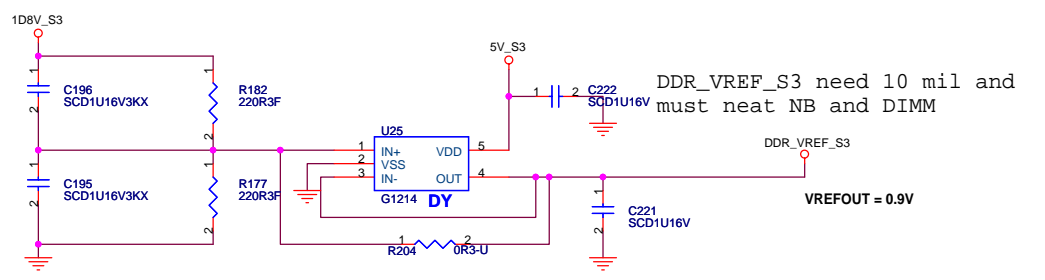
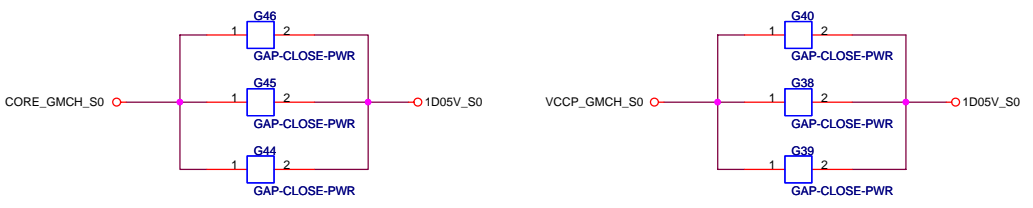
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**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **MAX8743 (1D2V\_VGA\_S0/1D05V)**

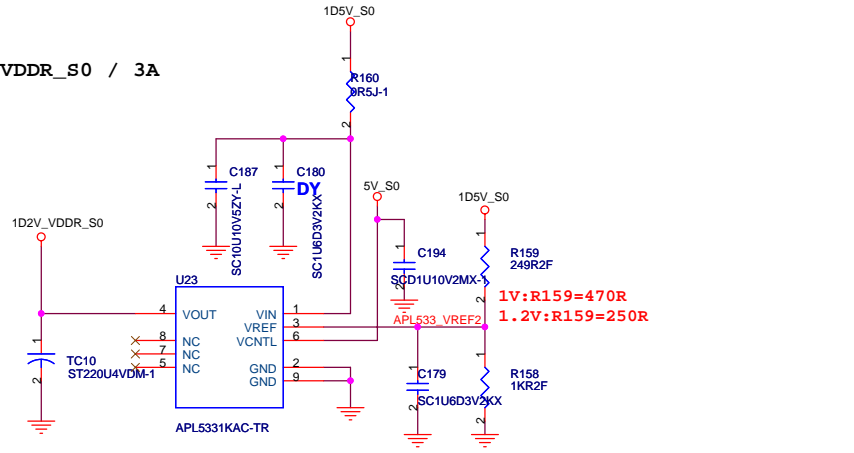
Size A3	Document Number	Rev
	<b>Leopard2</b>	-1

Date: Thursday, July 07, 2005 Sheet 45 of 47

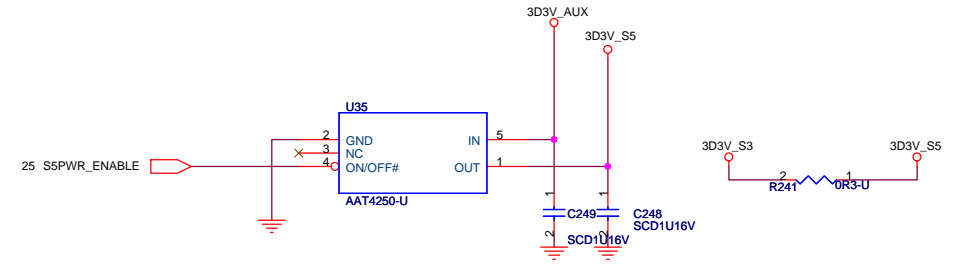


**FOR DDR2 Power**

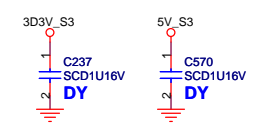
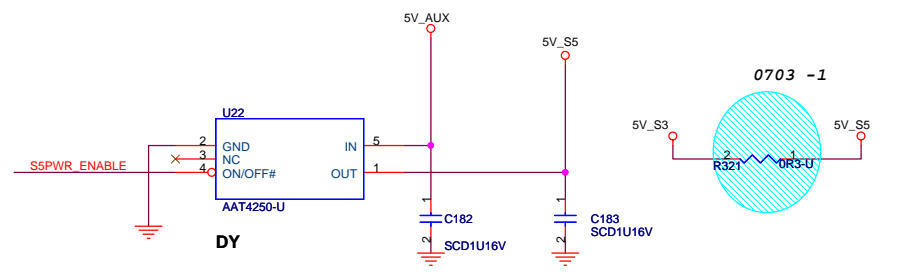
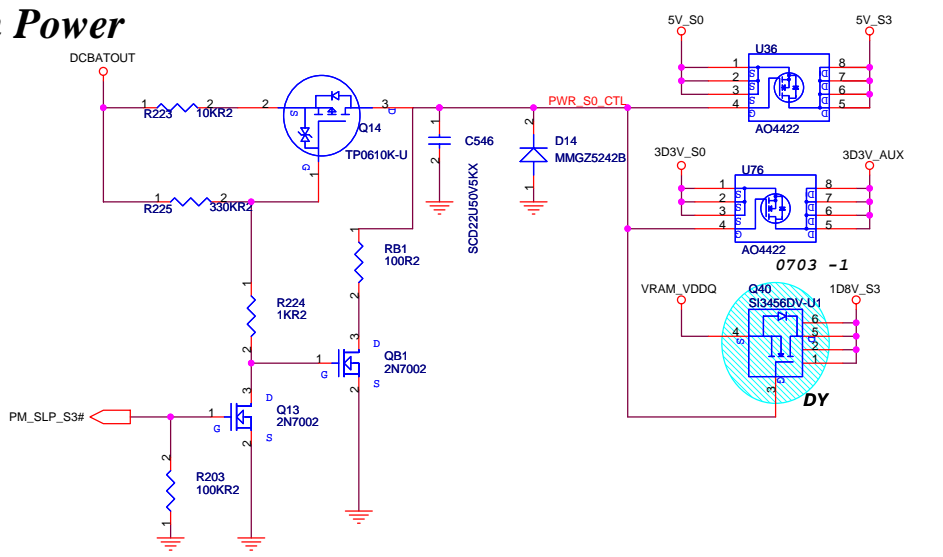
**1D2V\_VDDR\_S0 / 3A**



**Suspend Power**



**Run Power**



<Core Design>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWRPLANE&RESETLOGIC**

Size A3 Document Number: **Leopard2** Rev: **-1**

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