

# Compal confidential

## Schematics Document

Mobile Penryn uFCPGA with Intel  
Cantiga\_PM+ICH9-M core logic

2008-02-25

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				Rev: 0.4
				Sheet 1 of 53



**Voltage Rails**      O MEANS ON      X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS +NVVDD +PCIE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

**Symbol Note :**

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build  
DEBUG@ : means just reserve for debug.

**USB assignment:**

- USB-0 Right side
- USB-1 Right side
- USB-2 Left side(with ESATA)
- USB-3 Dock
- USB-4 Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Finger Printer
- USB-8 MiniCard(WWAN/TV)
- USB-9 Express card
- USB-10 X
- USB-11 X

**PCIe assignment:**

- PCIe-1 TV tuner/WWAN/Robeson
- PCIe-2 X
- PCIe-3 WLAN
- PCIe-4 GLAN (Marvell)
- PCIe-5 Card reader
- PCIe-6 New Card

**SMBUS Control Table**

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIF	MINI CARD	Sensor board	NB9M Thermal Sensor	NB9M	G-sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	V	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V	V	X
ICH_SMBCLK ICH_SMBDATA	ICH9	X	X	X	X	V	V	V	X	X	X	V

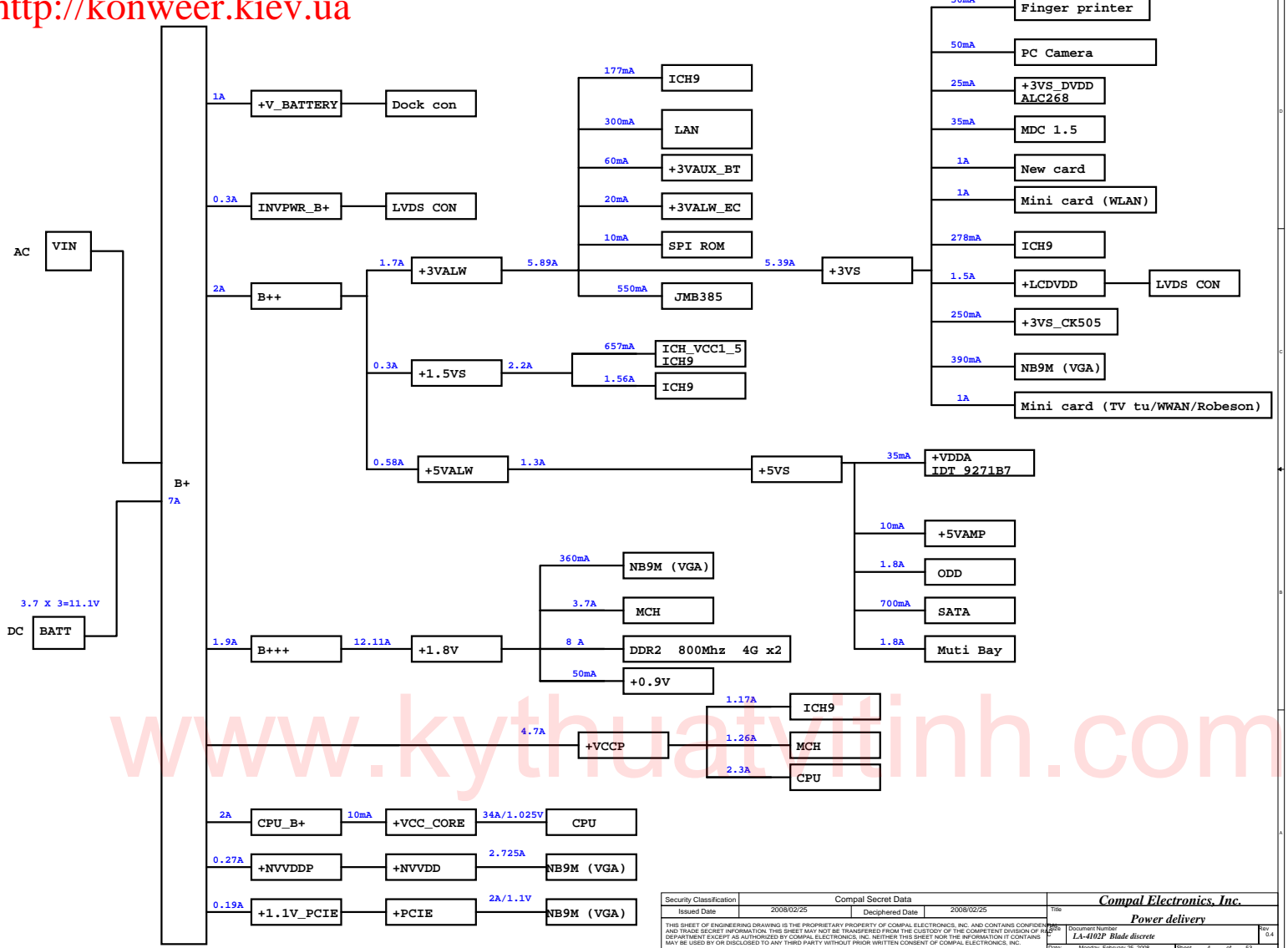
**NB9M SMBUS Control Table**

	SOURCE	LVDS	CRT	HDMI
DDC2_DATA DDC2_CLK	NB9M	V	X	X
3VDDCDA 3VDDCCL	NB9M	X	V	X
HDMIDAT_VGA HDMICLK_VGA	NB9M	X	X	V

**I2C / SMBUS ADDRESSING**

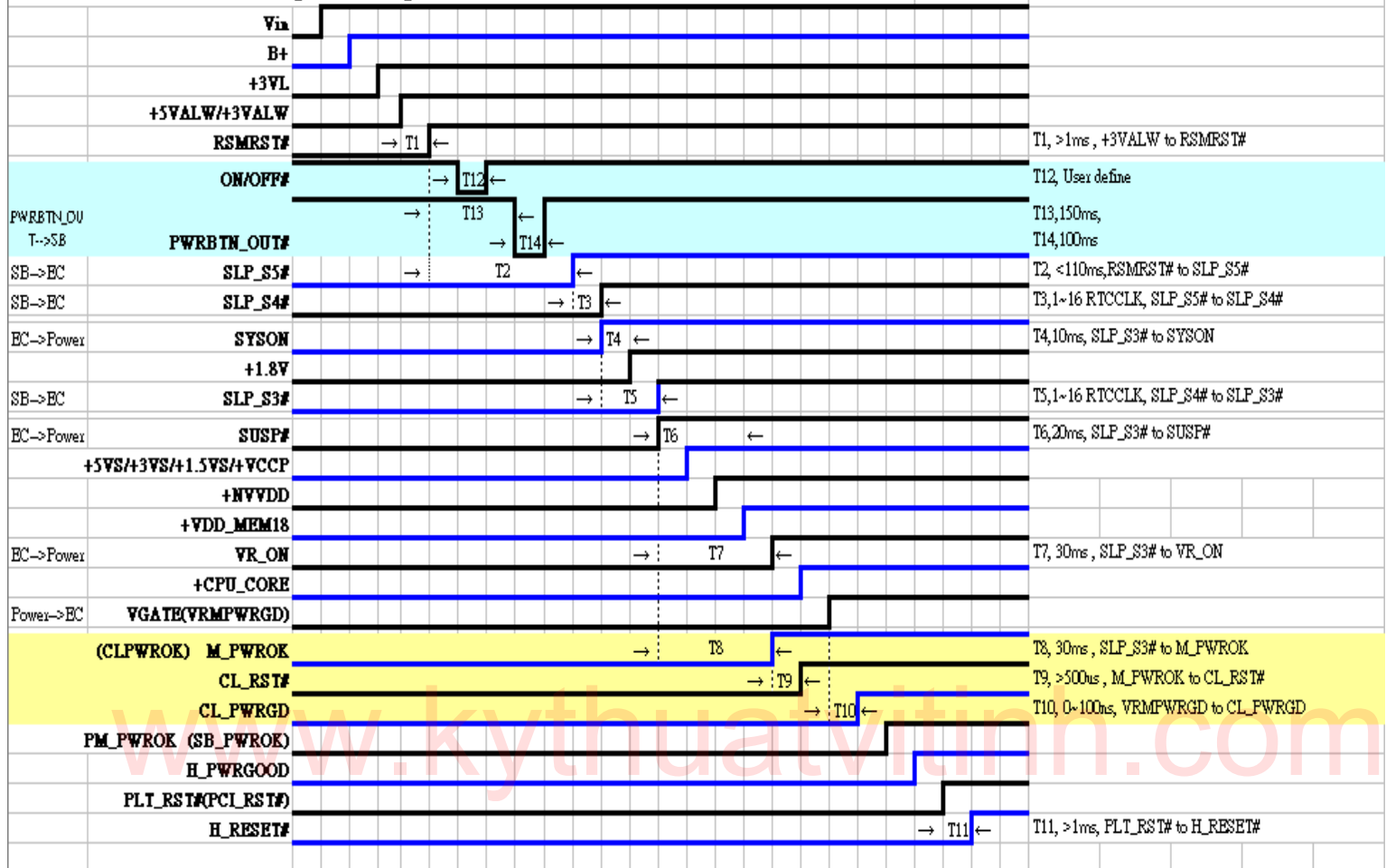
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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			Date	Monday, February 25, 2008	Sheet 3 of 63



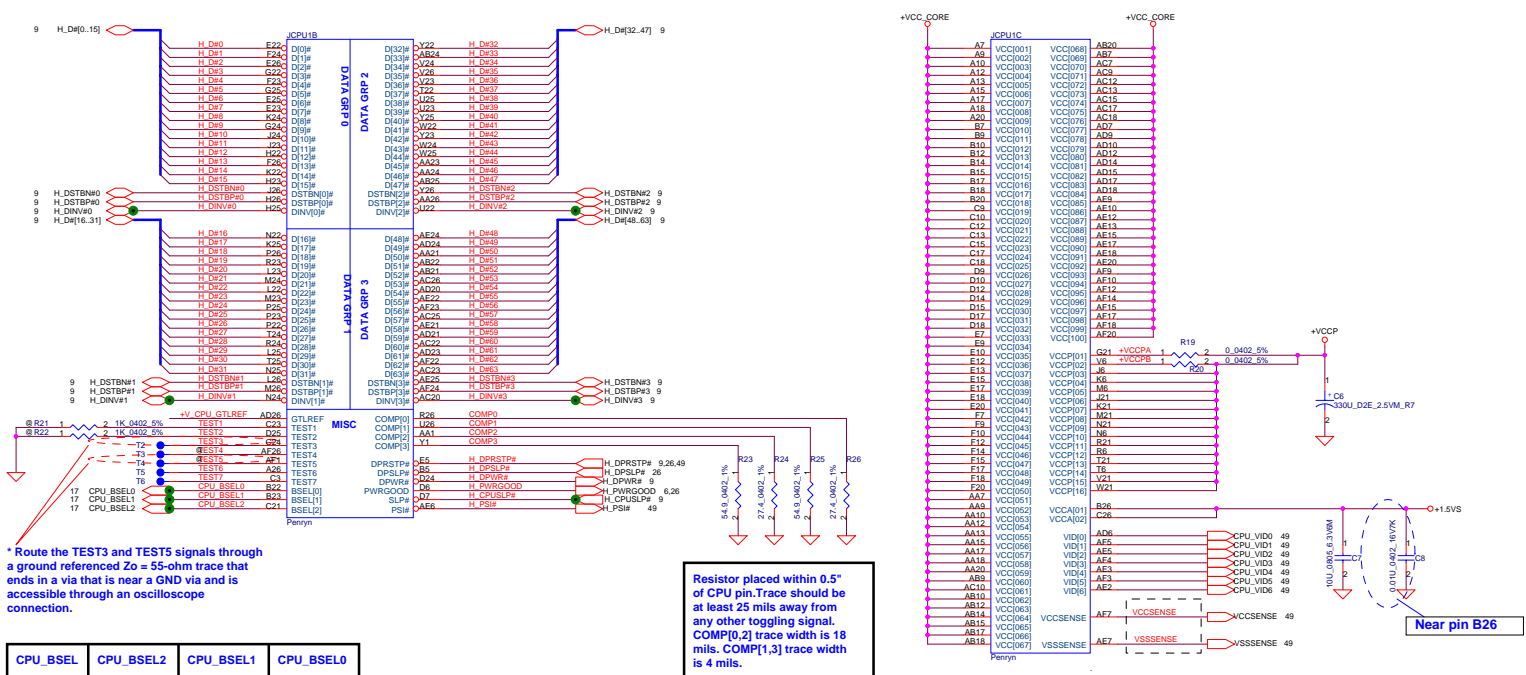
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				Power delivery
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### JAL50 Discrete power sequence AC mode



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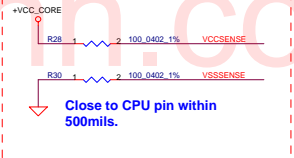
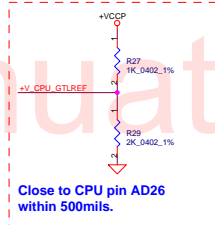


\* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor pin trace should be 0.5" of CPU pin. Trace width at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

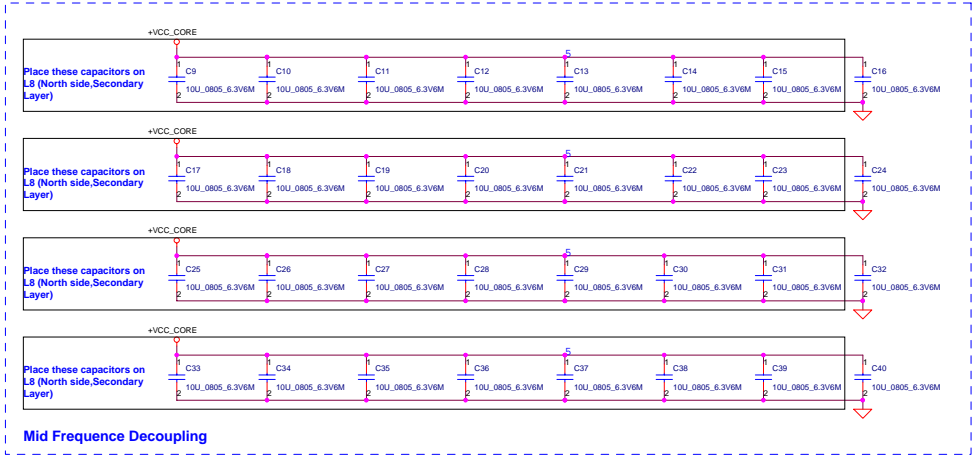
Length match within 25 mils. The trace width/space/other is 20/7/25.



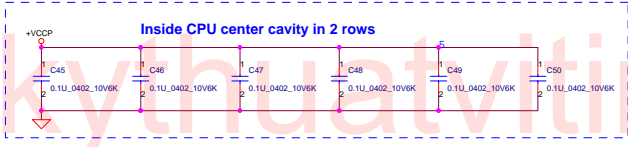
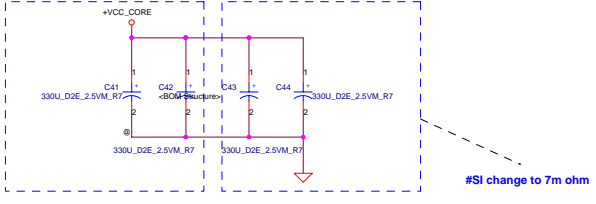
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Size	Document Number	Customer	LA-4102P Blade discrete	Rev	0.4
Date	Monday, February 25, 2008	Sheet	7	of	53

ICPUID	VSSID	Part
A4	VSS001	P6
A4	VSS002	P21
A11	VSS003	P24
A14	VSS004	R2
A16	VSS005	R5
A18	VSS006	R22
A21	VSS007	R22
AF2	VSS008	T1
BB	VSS009	T23
BB	VSS010	T23
B11	VSS011	T26
B13	VSS012	T3
B16	VSS013	U8
B21	VSS014	U24
B24	VSS015	U24
CC	VSS016	V5
CC	VSS017	V2
C11	VSS018	V22
C11	VSS019	V22
C14	VSS020	W1
C16	VSS021	W4
C18	VSS022	W2
C2	VSS023	Y3
C22	VSS024	Y3
CA5	VSS025	Y21
D11	VSS026	Y21
D4	VSS027	Y24
D8	VSS028	Y42
D11	VSS029	Y45
D18	VSS030	Y45
D18	VSS031	AA11
D23	VSS032	AA18
D23	VSS033	AA16
D26	VSS034	AA15
E4	VSS035	AA2
E6	VSS036	AA22
E11	VSS037	AB1
E14	VSS038	AB8
E16	VSS039	AB11
E18	VSS040	AB11
E21	VSS041	AB12
E24	VSS042	AB13
E24	VSS043	AB13
F2	VSS044	AB23
F8	VSS045	AB26
F11	VSS046	AC6
F18	VSS047	AC6
F19	VSS048	AC11
F2	VSS049	AC11
F22	VSS050	AC14
F22	VSS051	AC14
F25	VSS052	AC19
G1	VSS053	AC24
G2	VSS054	AC24
G26	VSS055	AD5
H3	VSS056	AD5
H8	VSS057	AD8
H21	VSS058	AD13
H24	VSS059	AD16
J2	VSS060	AD19
J2	VSS061	AD22
J22	VSS062	AD25
K2	VSS063	AE1
K4	VSS064	AE1
K4	VSS065	AE4
K4	VSS066	AE8
K23	VSS067	AE11
K26	VSS068	AE14
L3	VSS069	AE15
L6	VSS070	AE18
L21	VSS071	AE22
L24	VSS072	AE28
M2	VSS073	AF3
M2	VSS074	AF6
M22	VSS075	AF8
M22	VSS076	AF11
N1	VSS077	AF13
N4	VSS078	AF16
N23	VSS079	AF19
N23	VSS080	AF22
P8	VSS081	AF25

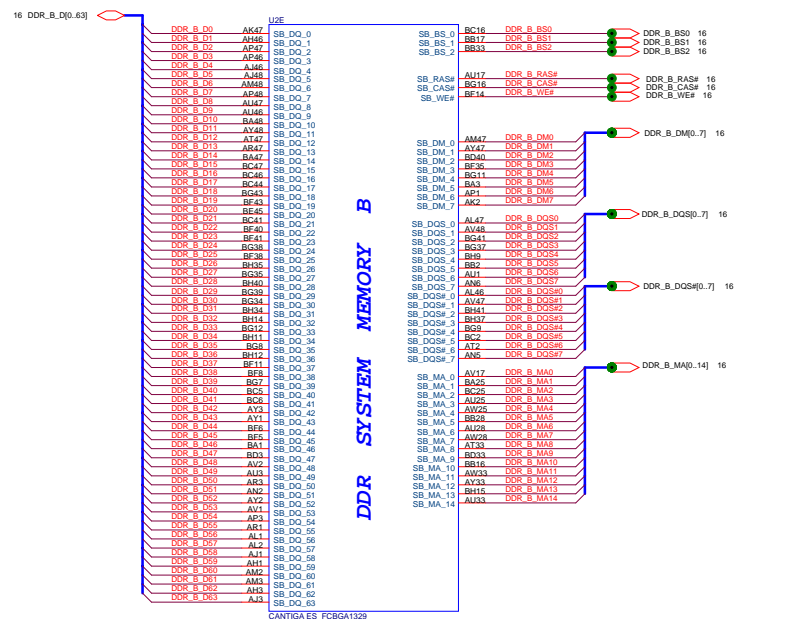
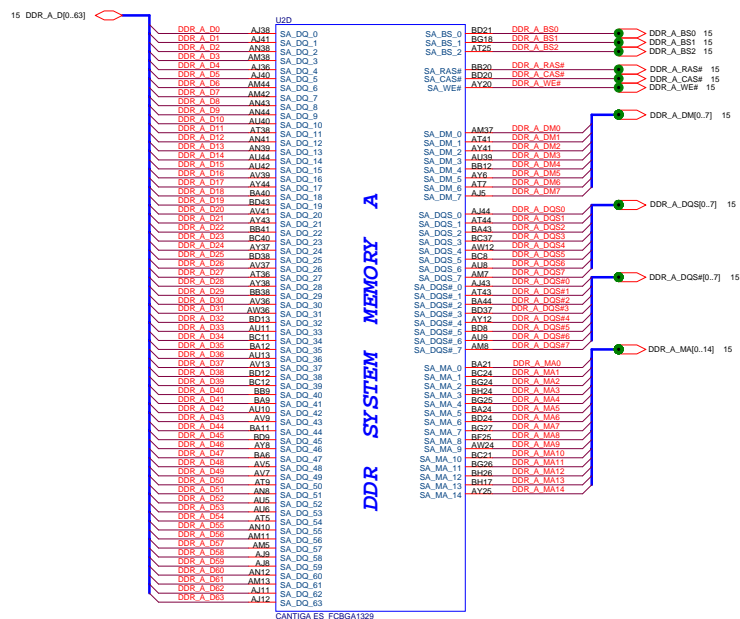


**Near CPU CORE regulator** ESR <= 1.5m ohm Capacitor > 1980uF



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Custom	LA-4102P Blade discrete	0.4			
Date	Monday, February 25, 2008	Sheet	8	of 53	





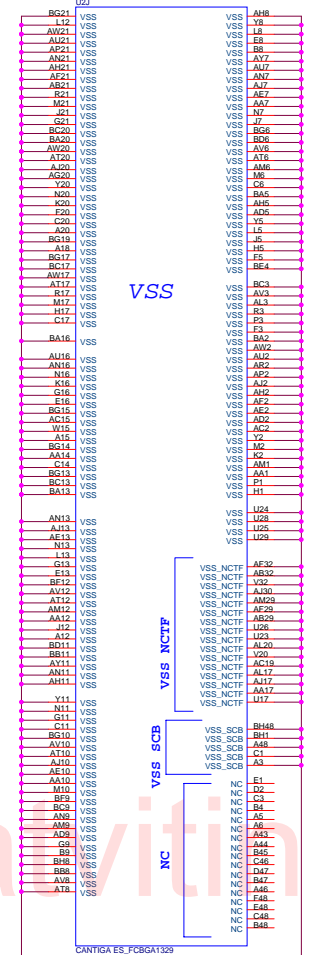
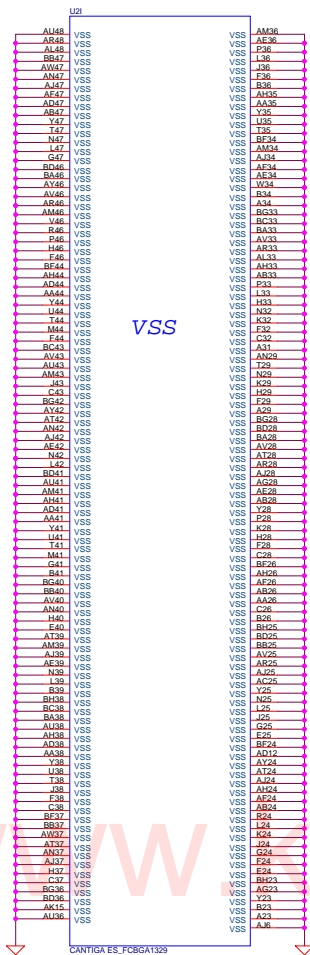
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LA-4102P Blade discrete				Rev. 0.4
Date:	Monday, February 25, 2008	Sheet	19	of 53







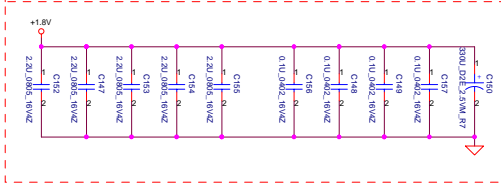


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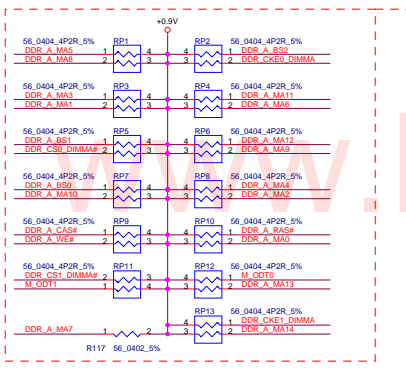
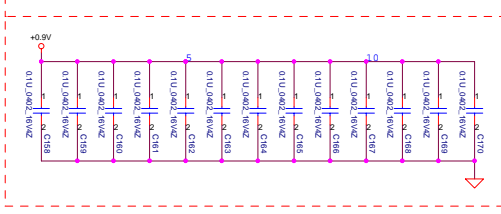
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				Custom	LA-4102P Blade discrete
				Date	Monday, February 25, 2008
				Sheet	14 of 53



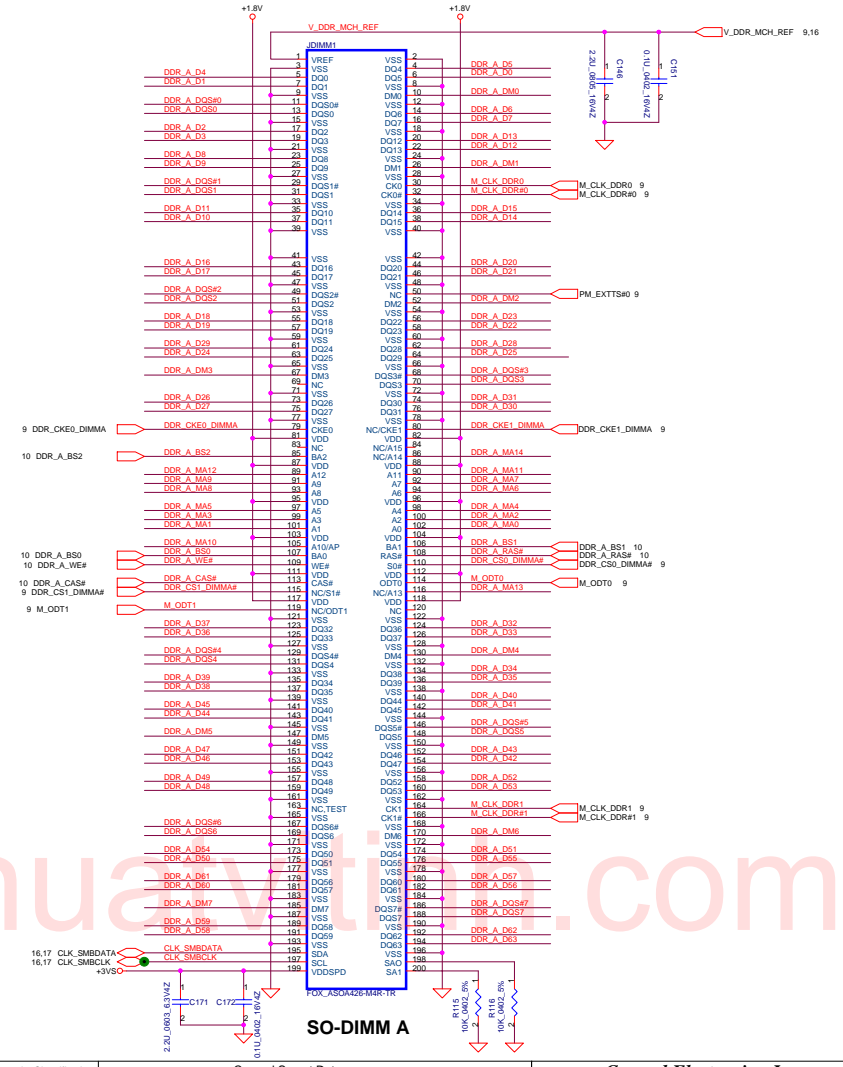
Layout Note:  
Place near JP2



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:  
Place these resistor closely JP3, all trace length Max=1.5"

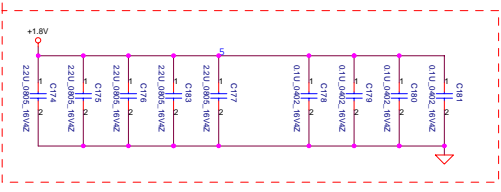


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				DDR1-SODIMM SLOT1	
				Size	Document Number
				Custom	LA-102P Blade discrete
				Date	Monday, February 25, 2008
				Sheet	16 of 53

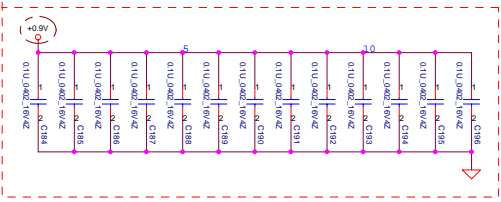
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- 10 DDR\_B\_DS0[0..7]
- 10 DDR\_B\_DM[0..7]
- 10 DDR\_B\_DQS[0..7]
- 10 DDR\_B\_MA[0..14]

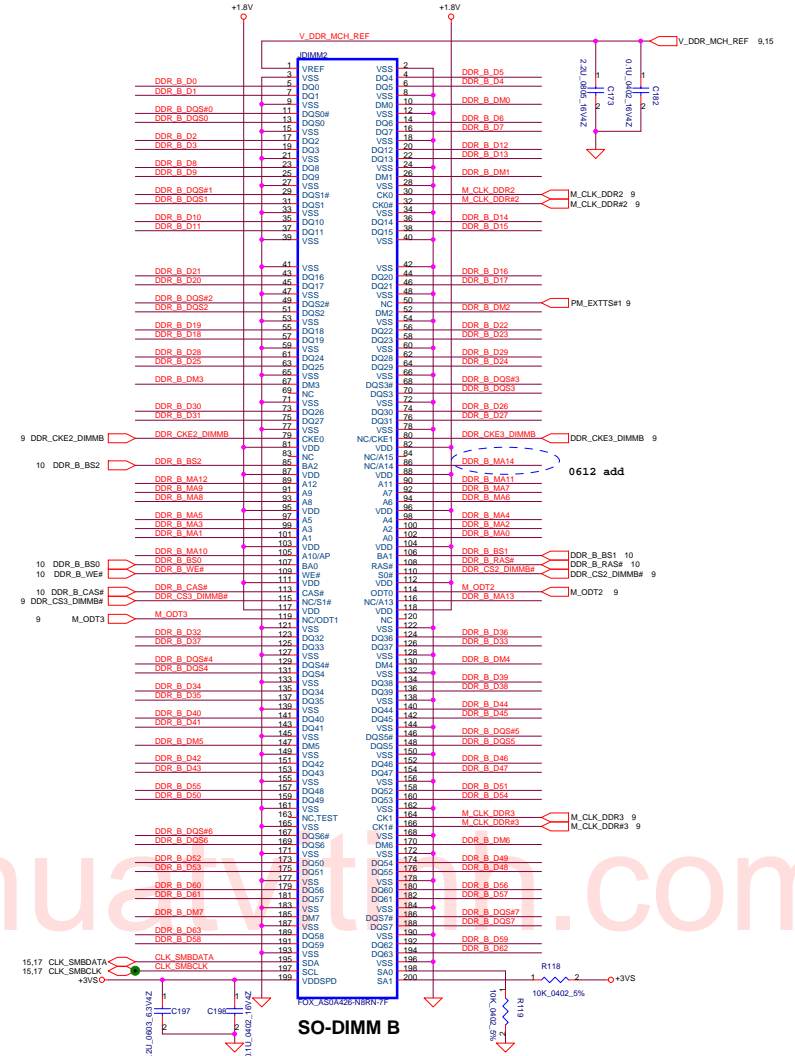
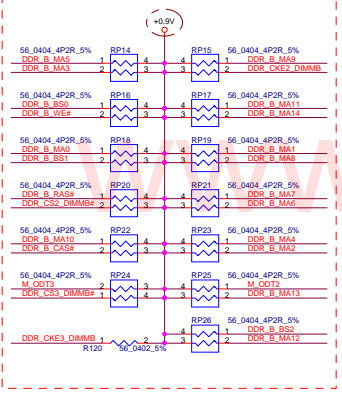
Layout Note:  
Place near JP10



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



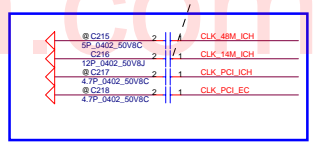
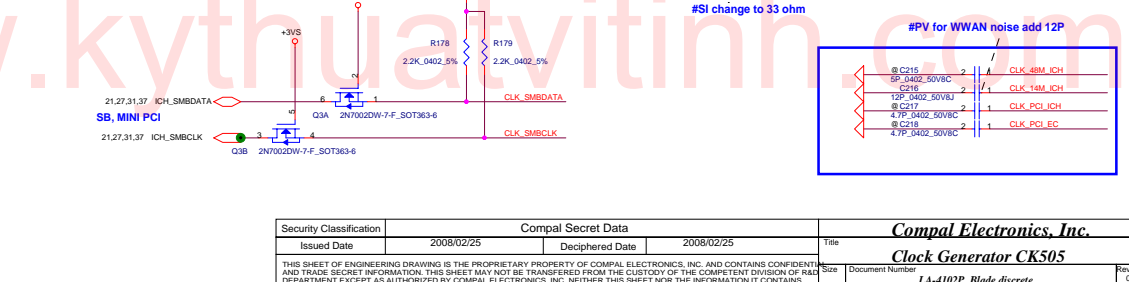
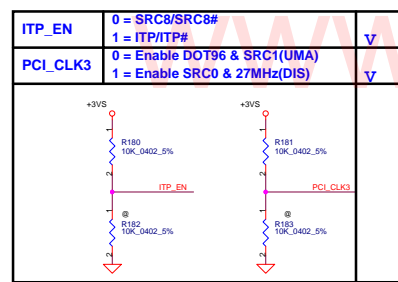
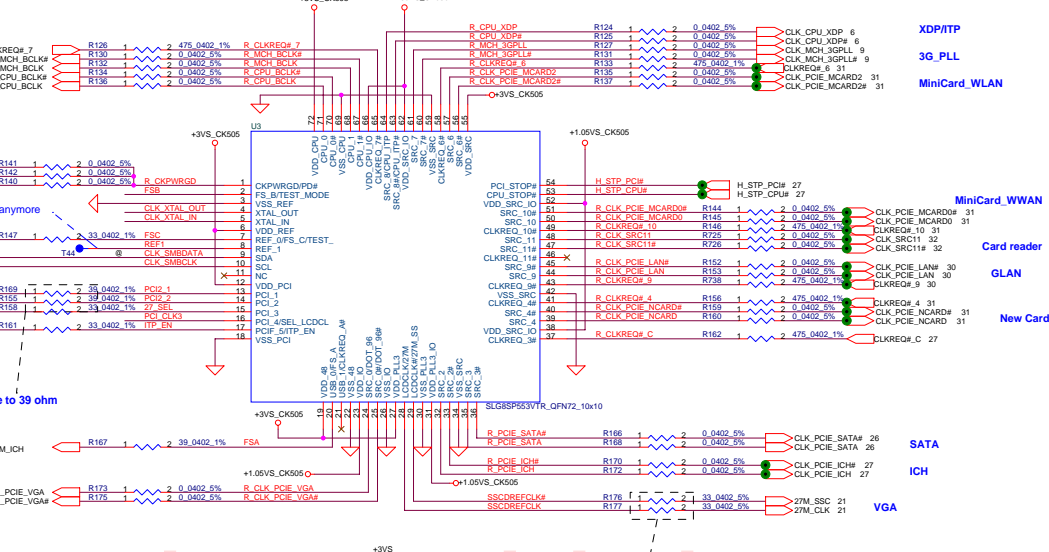
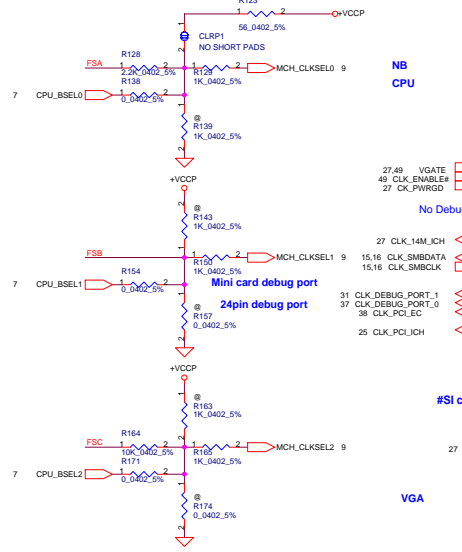
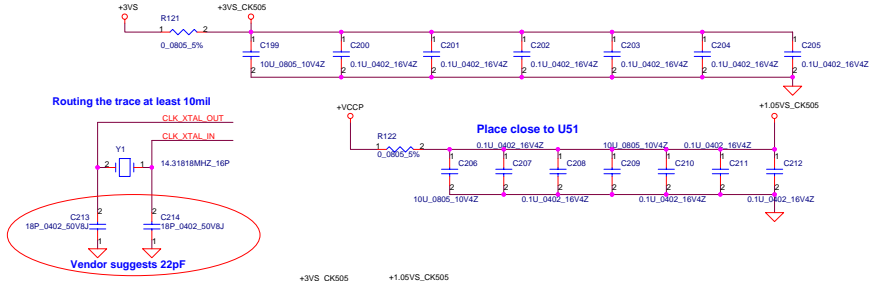
Layout Note:  
Place these resistor closely JP3, all trace length Max=1.5"



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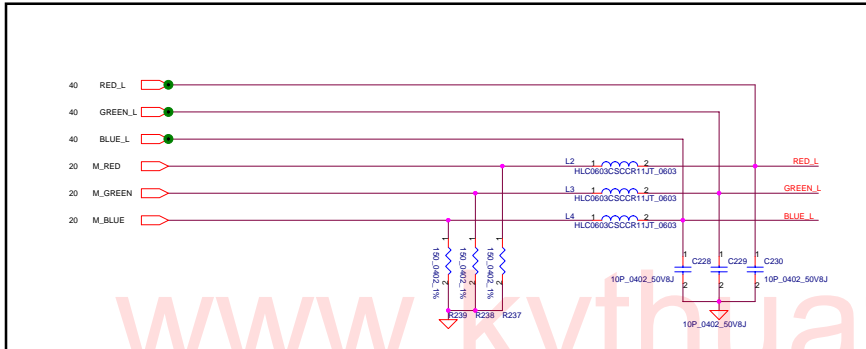
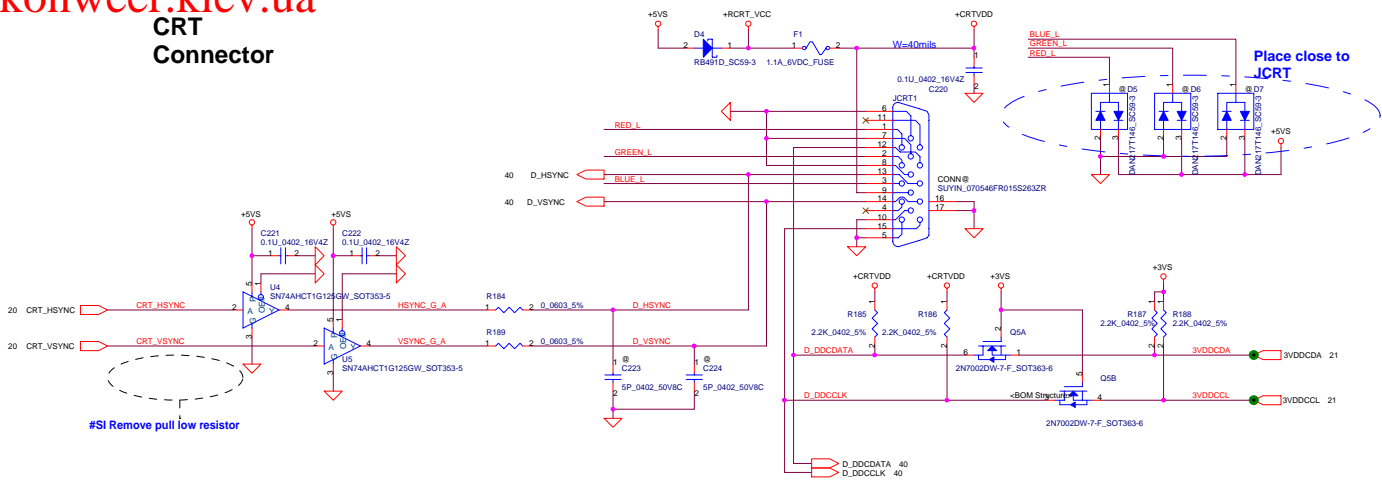
CLKS#	FSB#	CLKSEL#	FSB#	CLKSEL#	PC#	FSB#	CLKSEL#	USB
MHz	MHz	MHz	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						

**Reserved**



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Date	Monday, February 25, 2008	Sheet	17 of 53

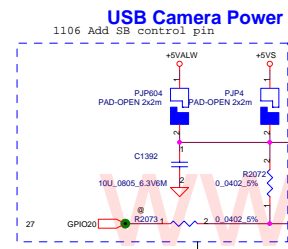
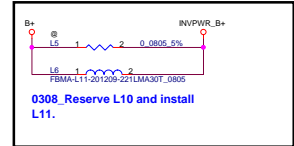
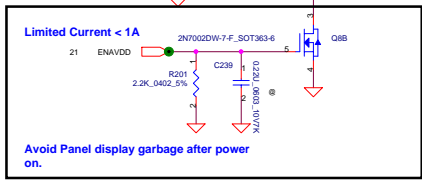
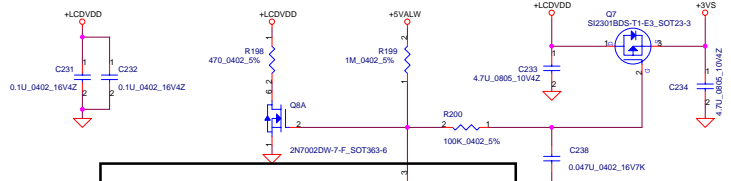
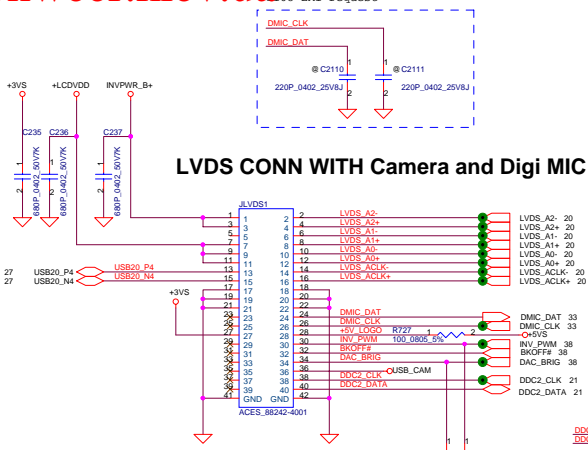
# CRT Connector



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	LA-4102P Blade discrete	0.4	Date	Manday, February 25, 2008	Sheet 18 of 53

108 EMI request

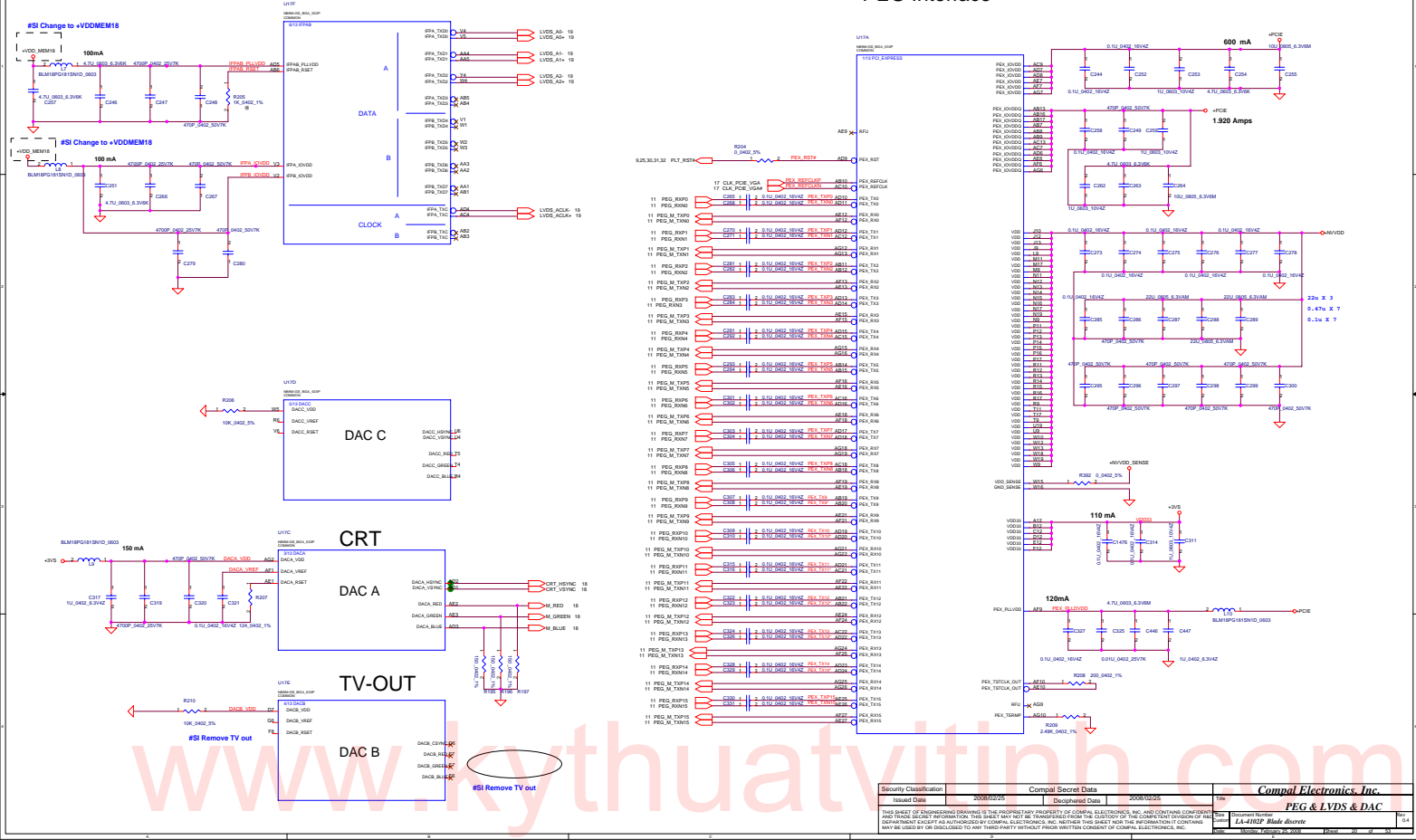


USB\_VCCA is +3.9V  
 USB\_VCCA = 1.25X(1+R1091/R1093)

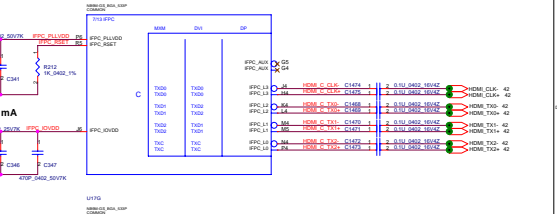
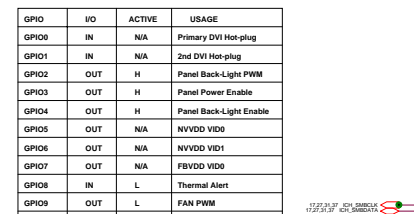
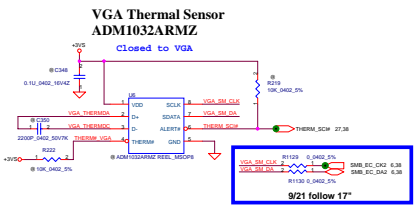
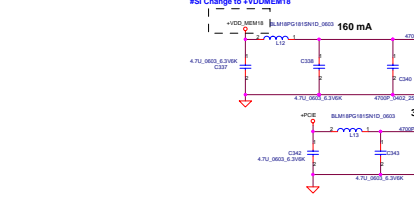
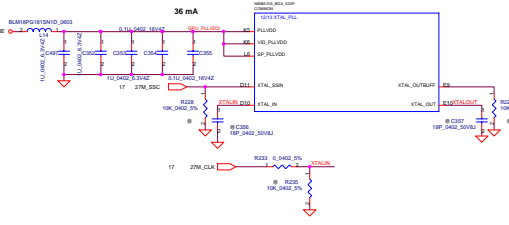
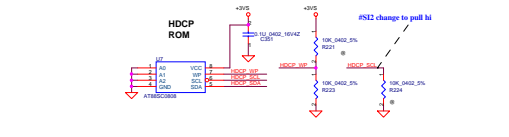
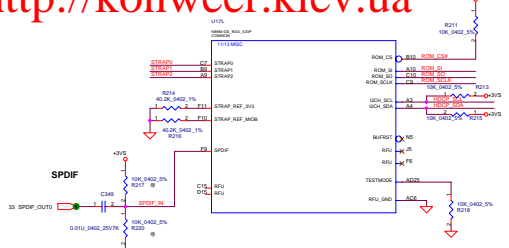
#SI Add GPIO20 control and reserve +5VS

#SI change lib  
 #PV reserve pull low 10K  
 #512 for EMI

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				Document Number
				LA-4102P Blade discrete
				Rev
				0.4
				Date
				Monday, February 25, 2008
				Sheet
				19 of 53



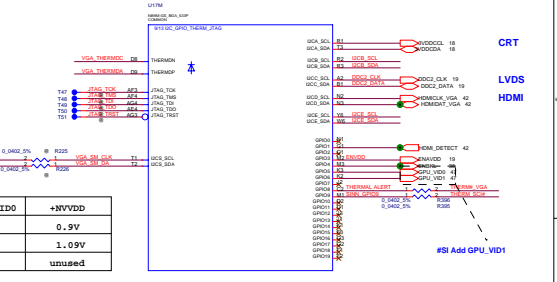
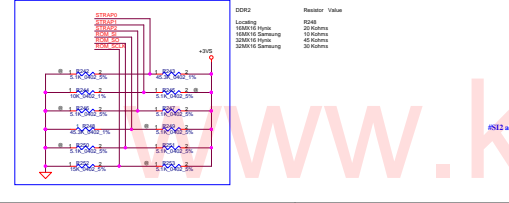
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GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	FAN Thermal
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNC0
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control

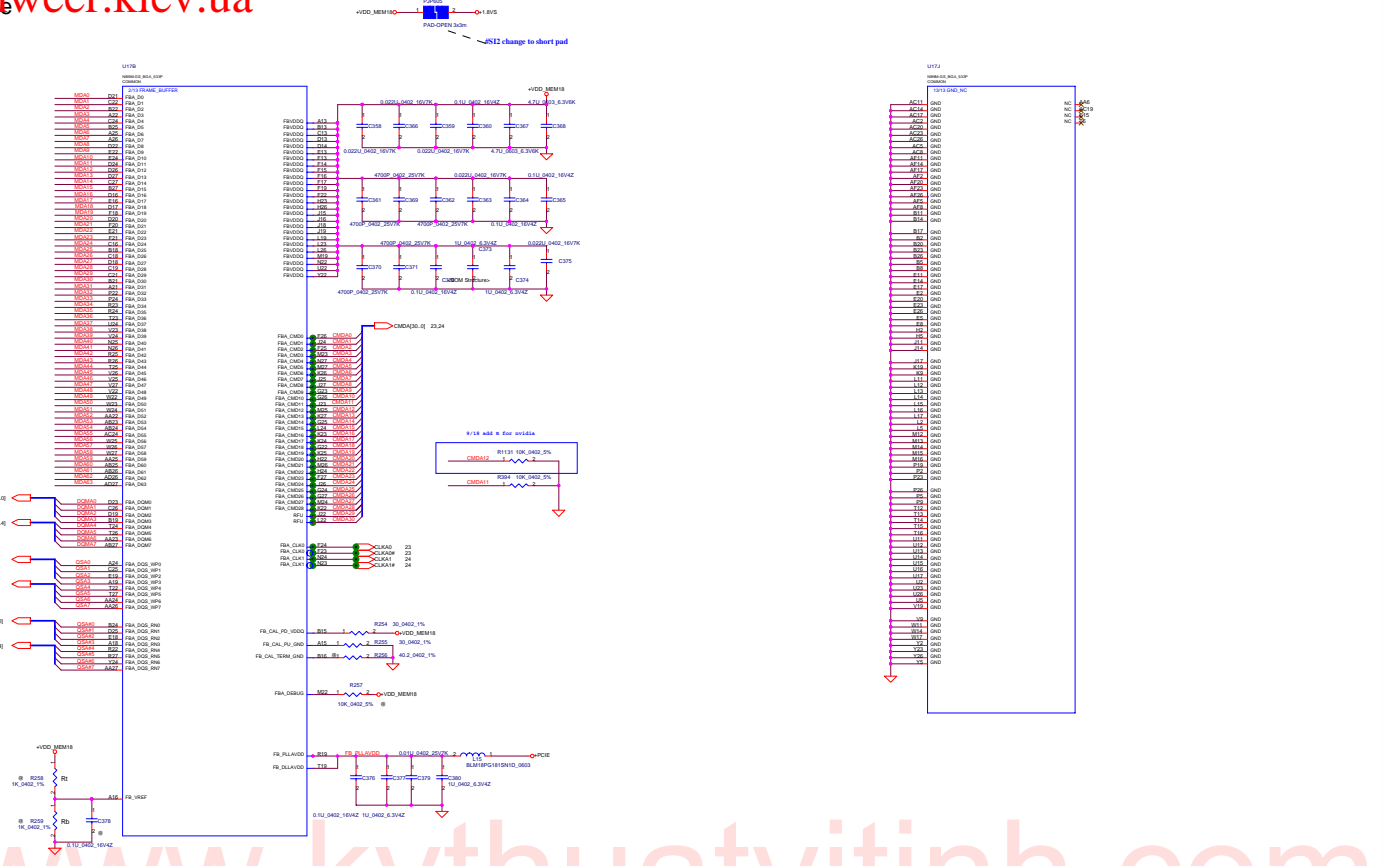
GPU_VID1	GPU_VID0	+NVVDD
0	0	0.5V
0	1	1.09V
1	0	unused

Straps  
MULTI LEVEL STRAPS



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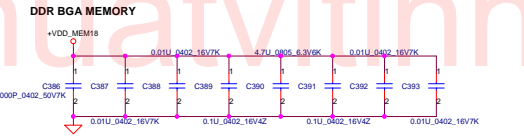
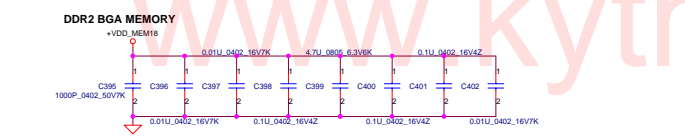
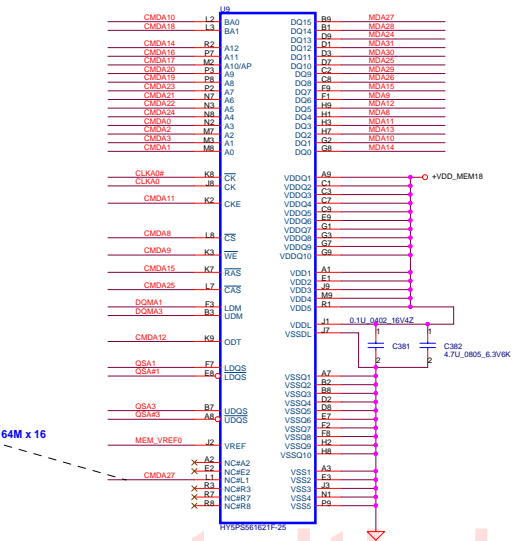
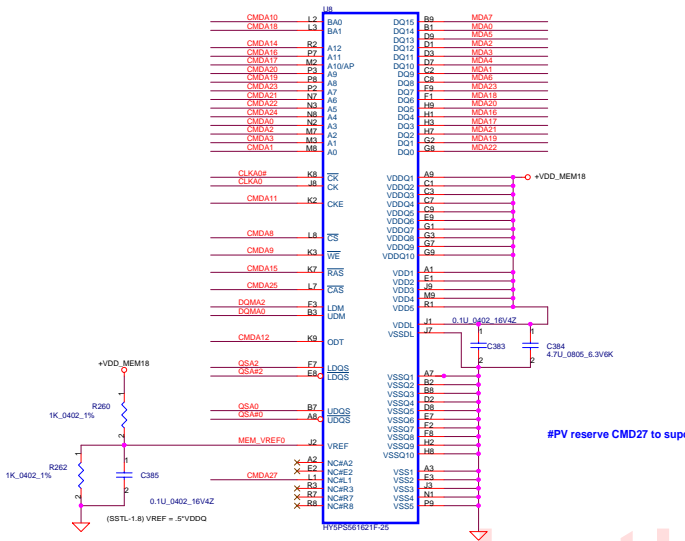
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- 23 MD4V15\_101 - MD4V15\_101
- 24 MD4V17\_321 - MD4V17\_321
- 24 MD4V15\_401 - MD4V15\_401



32Mx16 DDR2 400MHz \*4==>256MB  
64Mx16 DDR2 400MHz\*4==>512MB

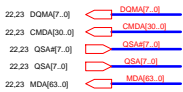
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- 22.24 GSA[7..0] QSA17..0
- 22.24 DQMA[7..0] DQMA17..0
- 22.24 MDA[63..0] MDA63..0
- 22.24 CMDA[30..0] CMDA30..0

	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

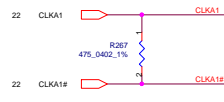
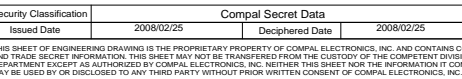
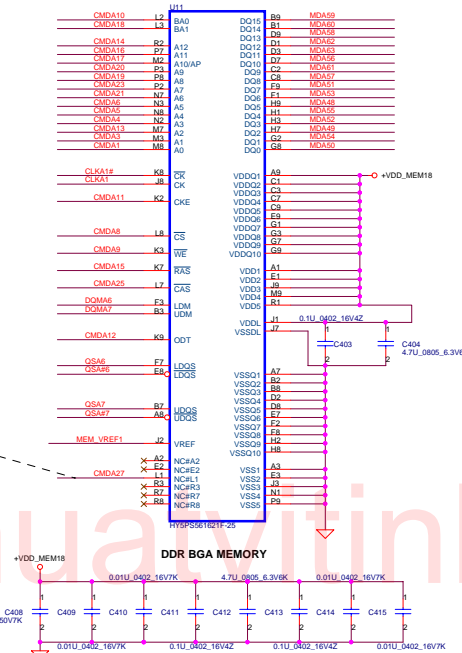
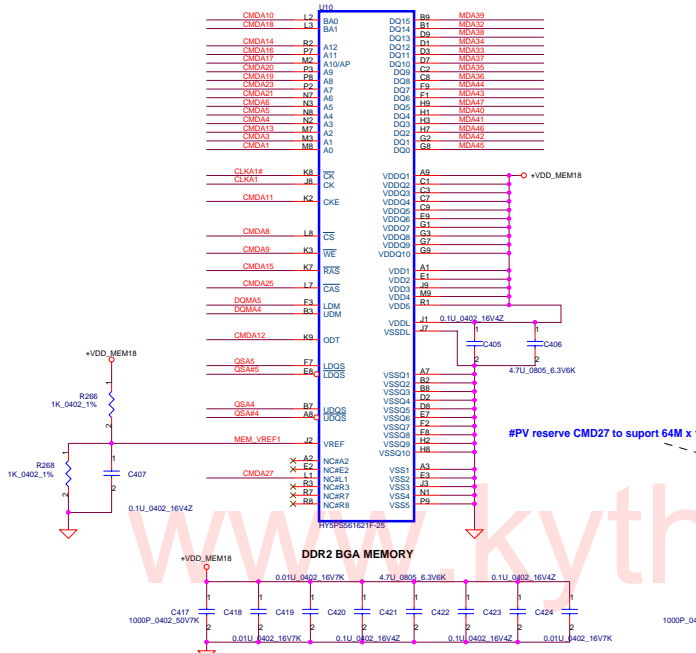


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			Document Number	CHANNEL A EXT. 256M_1
Date	Monday, February 25, 2008	Sheet	7	of 16

32Mx16 DDR2 400MHz \*4==>256MB  
 64Mx16 DDR2 400MHz\*4==>512MB



Address	DATA	Bus
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4	A3	
CMD5	A4	
CMD6	A5	
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

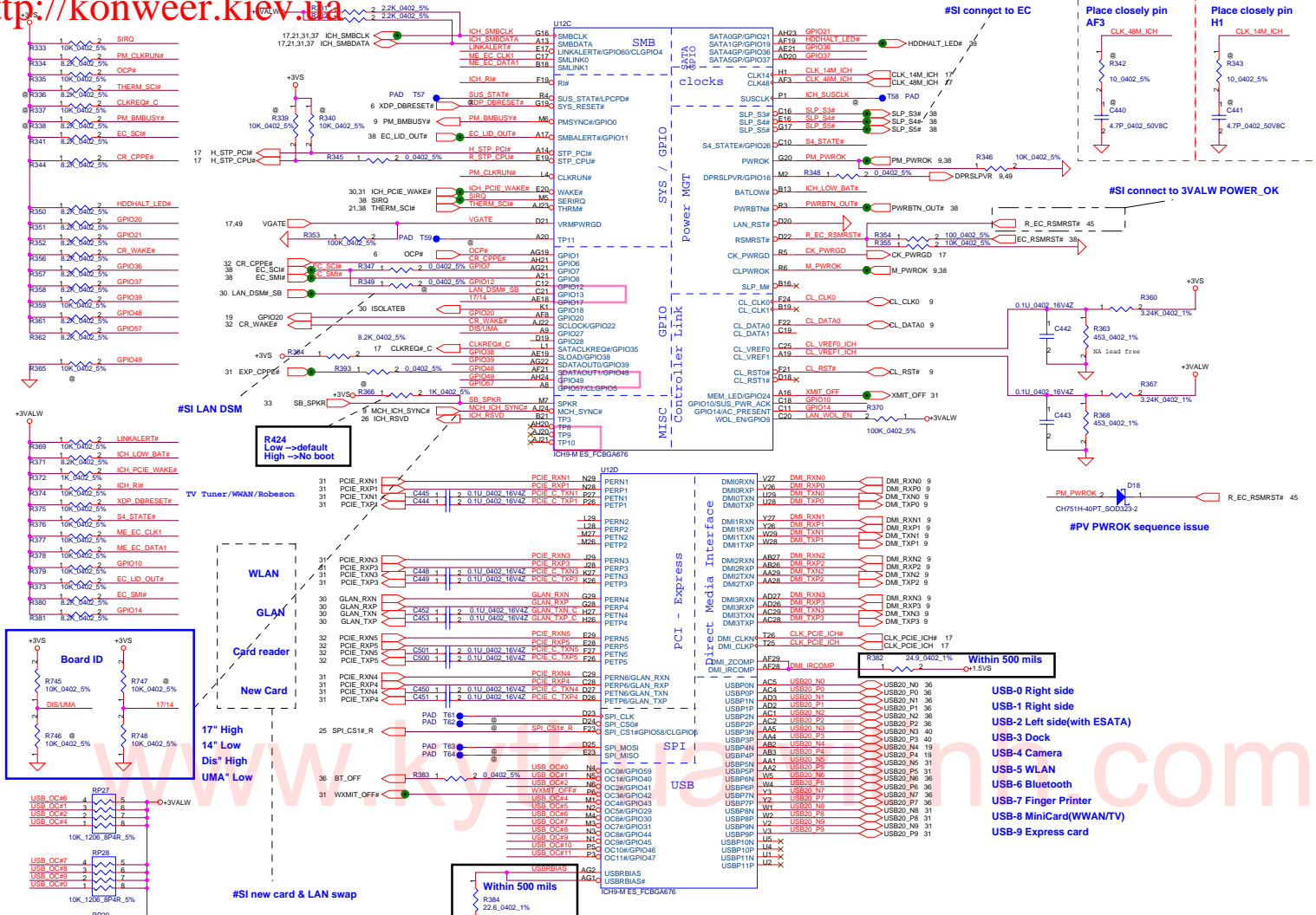


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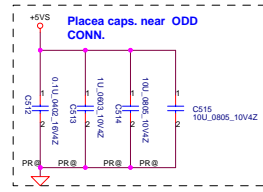
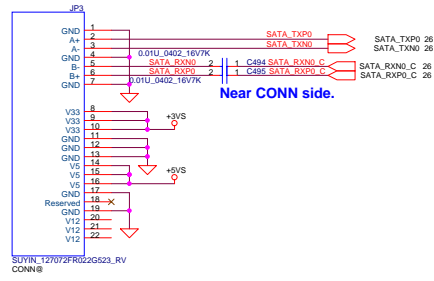
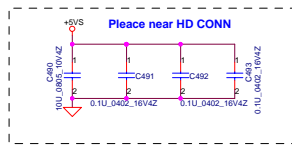
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Custom	LA-4102P Blade discrete	Date	Monday, February 25, 2008	
Sheet	27	of	53	

- USB-0 Right side
- USB-1 Right side
- USB-2 Left side(with ESATA)
- USB-3 Dock
- USB-4 Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Finger Printer
- USB-8 MiniCard(WAN/TV)
- USB-9 Express card

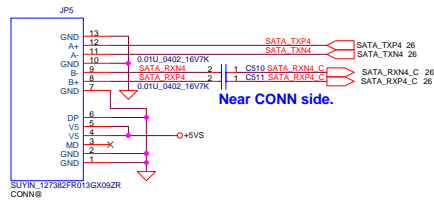
Compal Electronics, Inc.  
 ICH9(3/4) DMI,USB,GPIO,PCIE  
 LA-4102P Blade discrete



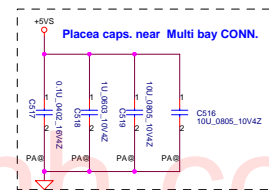
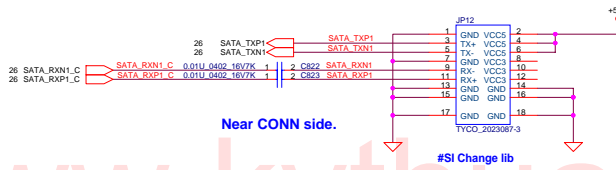
### HDD Connector



### CD-ROM Connector



### Multi Bay Connector

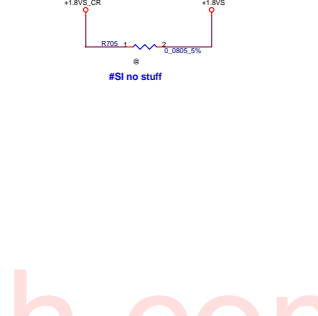
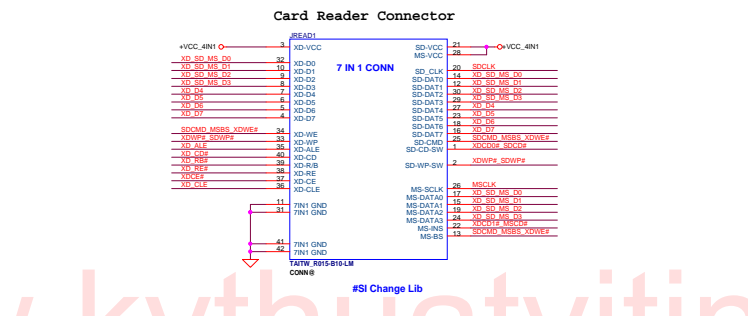
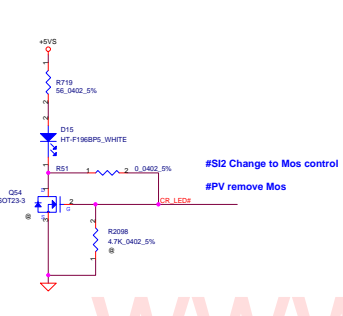
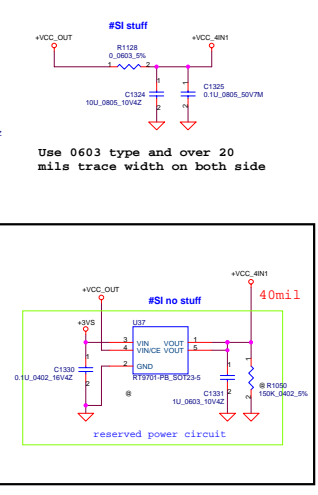
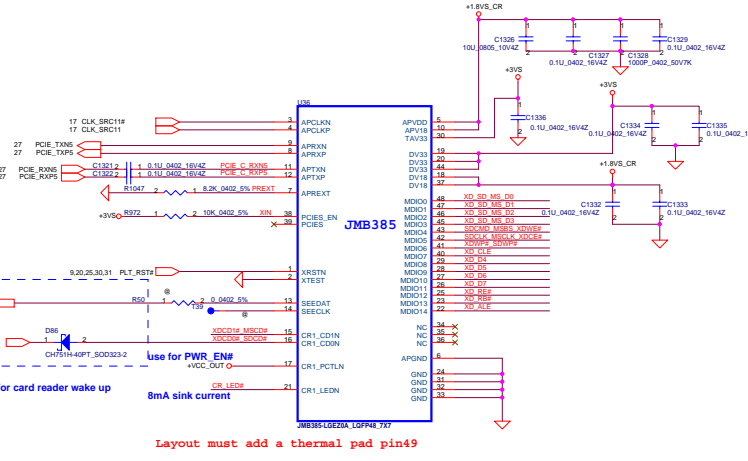
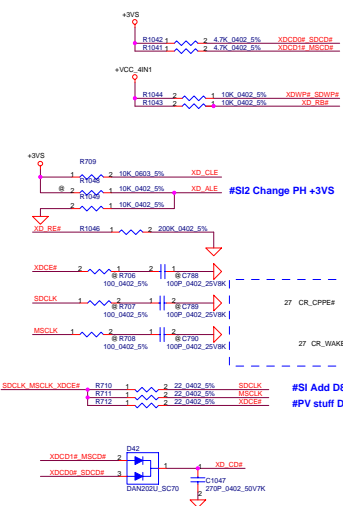


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Size	Document Number	Customer	LA-4102P Blade discrete	Date
			Monday, February 25, 2008	Sheet 28 of 53



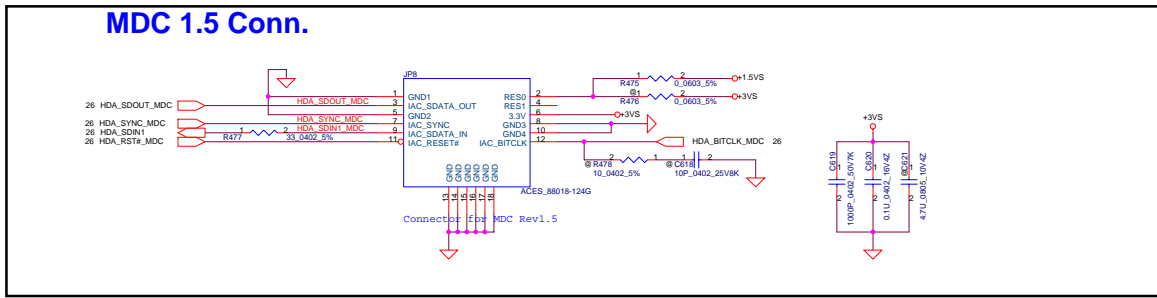




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Compal Electronics, Inc. USB CardReader&CONN LA-1102P Blade discrete				04
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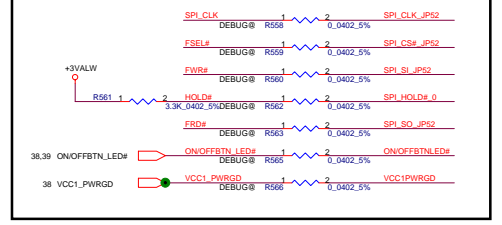
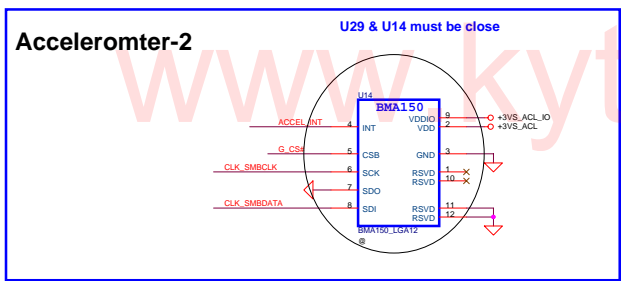
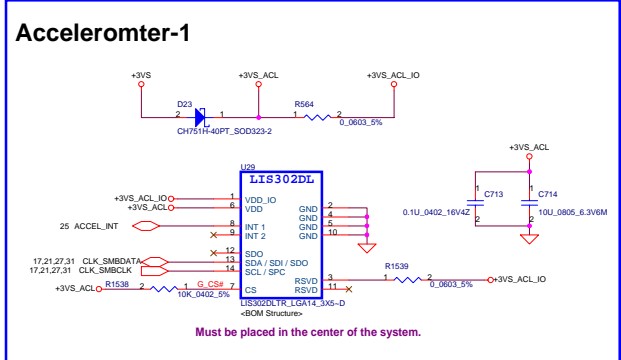
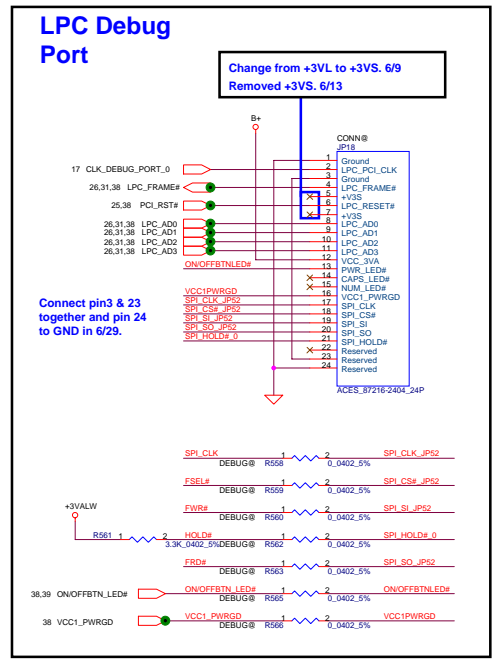
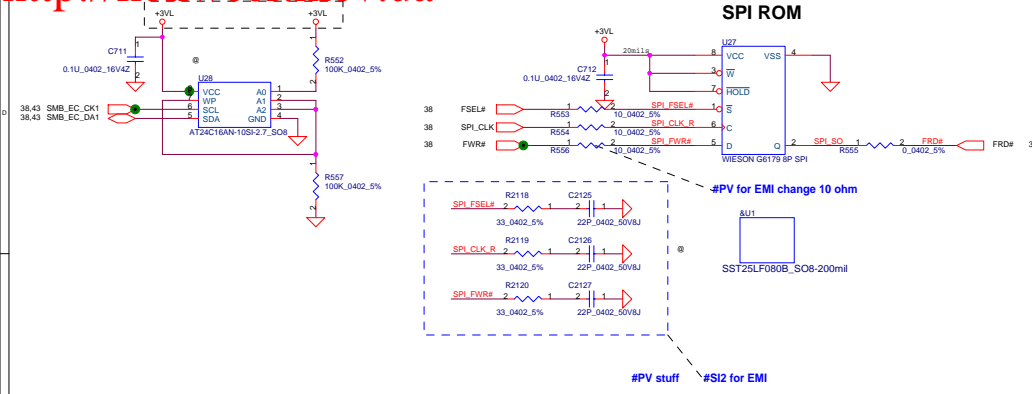


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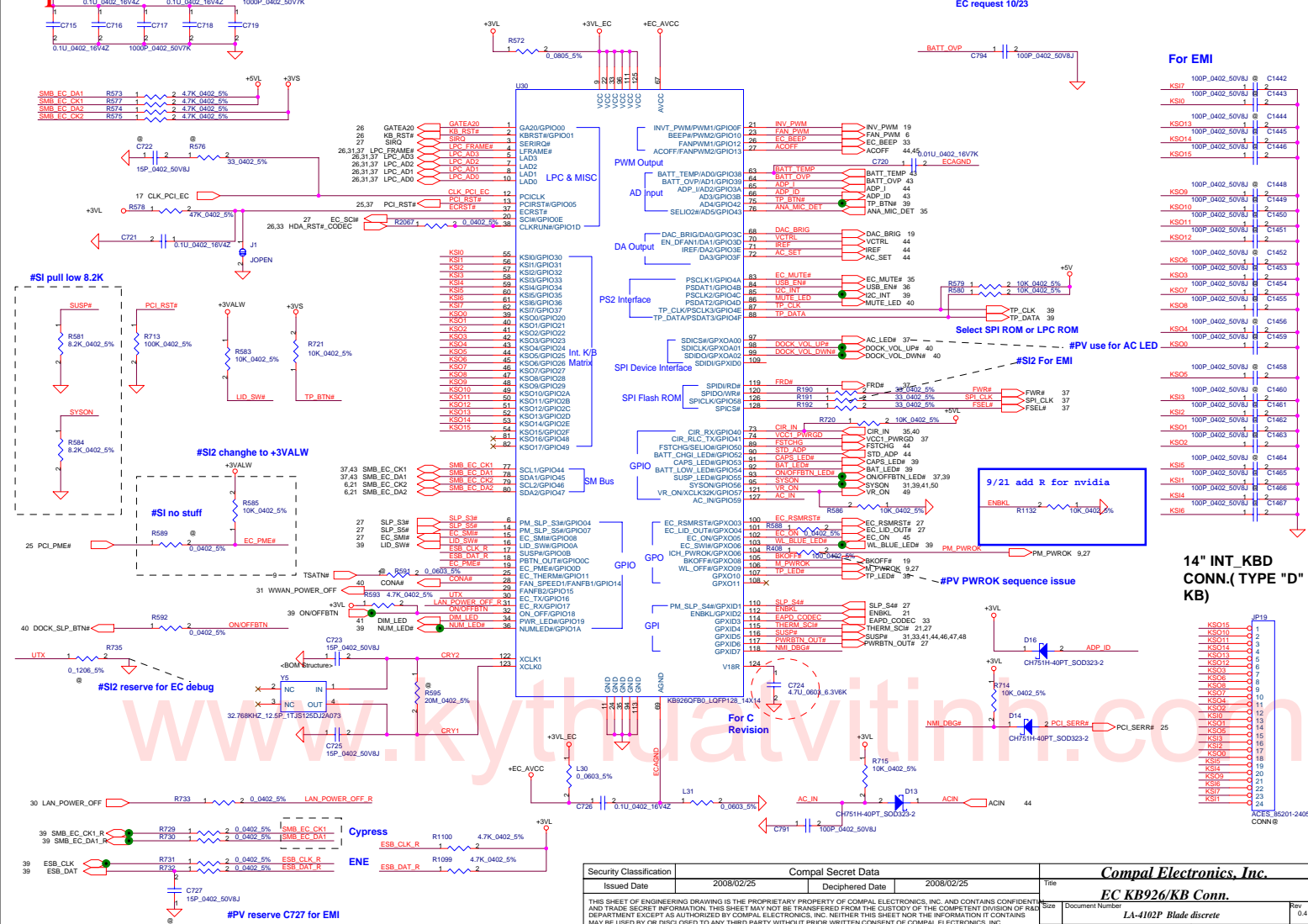
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				<b>LA-4102P Blade discrete</b>	
				Rev 0.4	
				Date: Monday, February 25, 2008	
				Sheet 31 of 53	



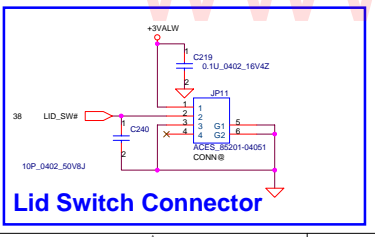
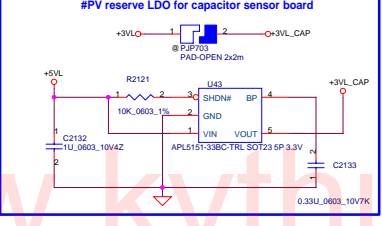
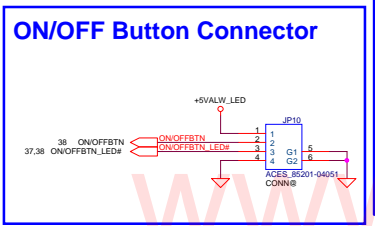
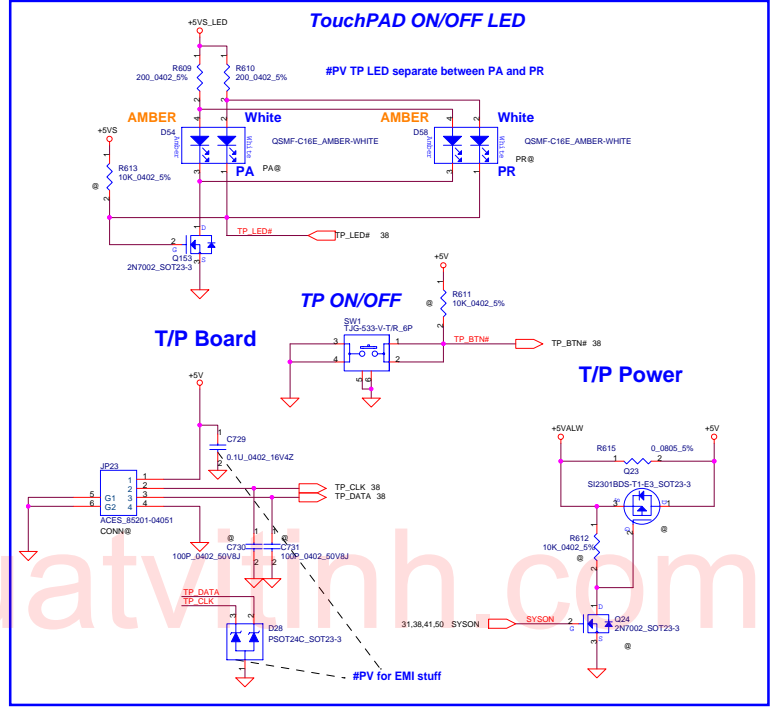
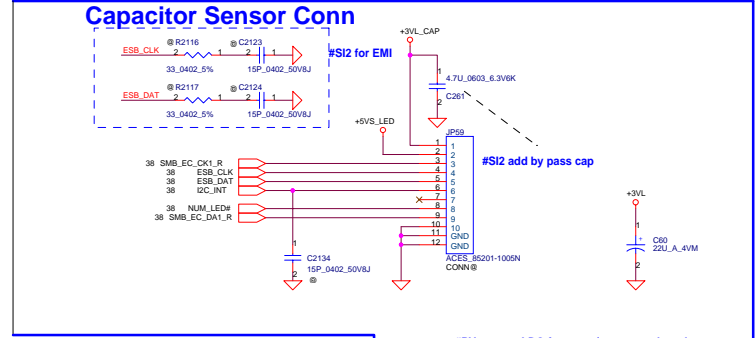
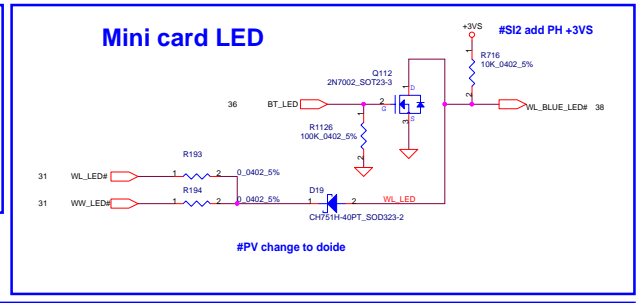
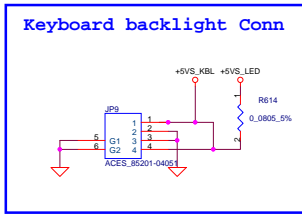
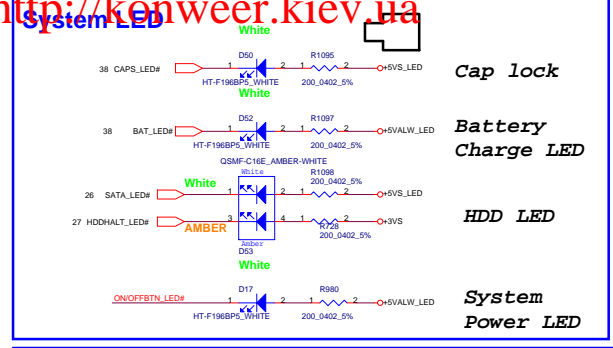




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				LA-4102P Blade discrete	0.4
Date	Monday, February 25, 2008	Sheet	37	of 53	



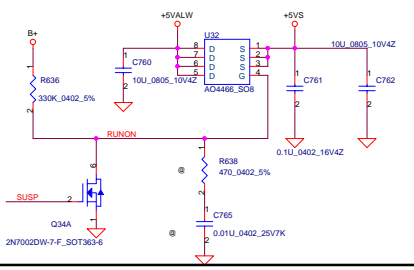
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EC KB926/KB Conn.			LA-4102P Blade discrete	0.4
Date	Monday, February 25, 2008	Sheet	38	of 53



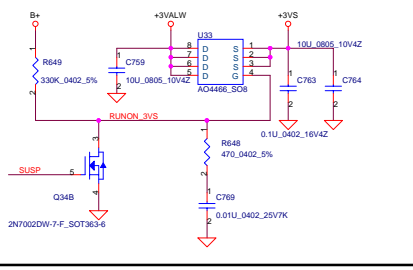
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			Size Document Number <b>LA-4102P Blade discrete</b>
			Rev 0.4
			Date Monday, February 25, 2008
			Sheet 38 of 53



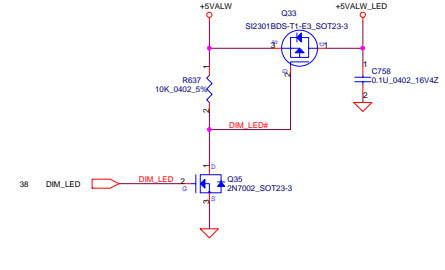
**+5VALW to +5VS Transfer**



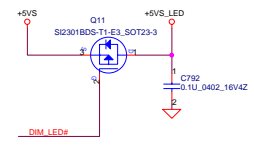
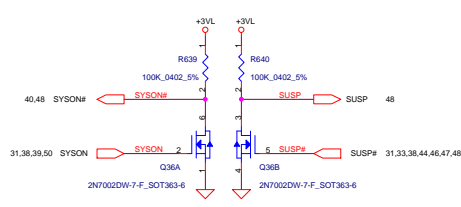
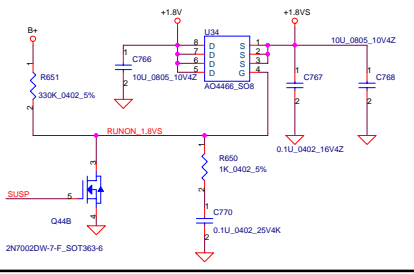
**+3VALW to +3VS Transfer**



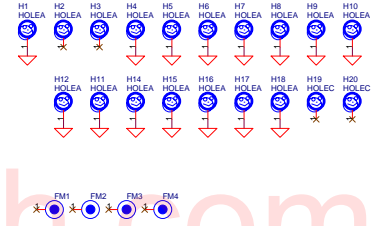
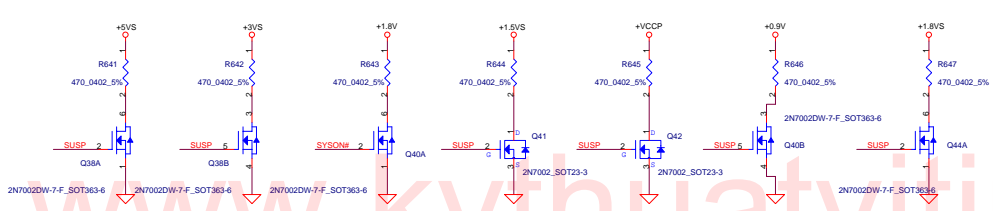
**DIM LED**



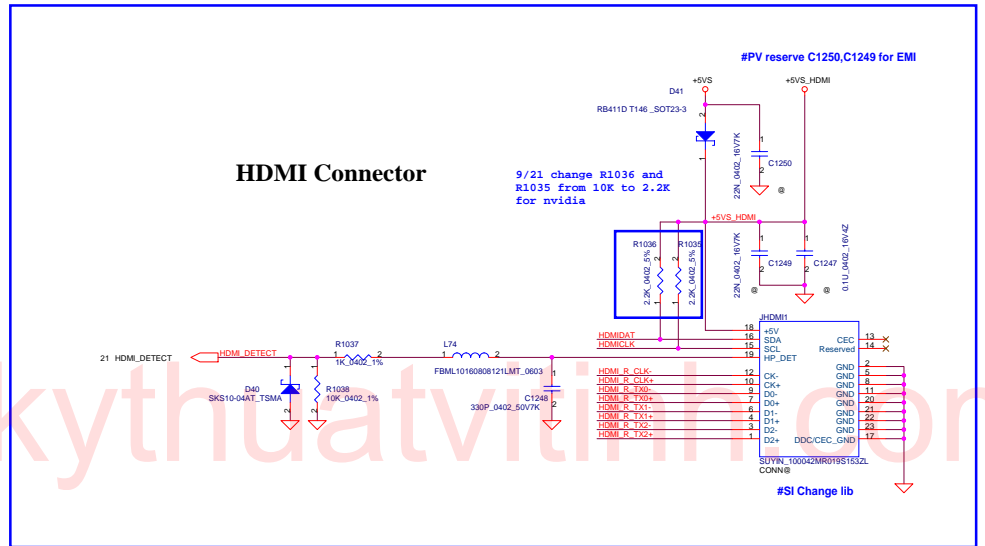
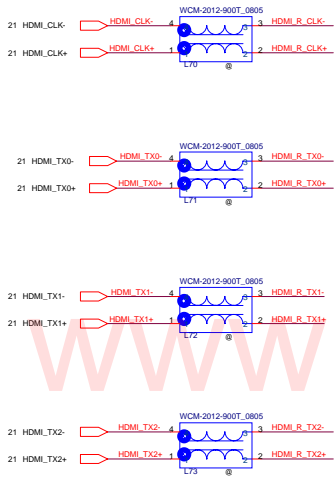
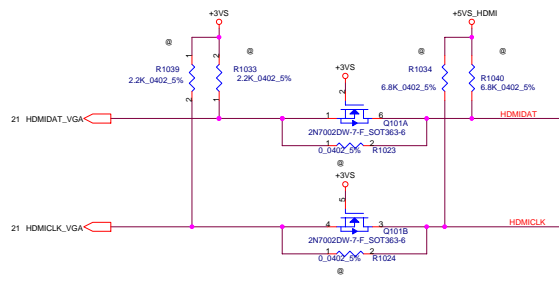
**+1.8V to +1.8VS Transfer**



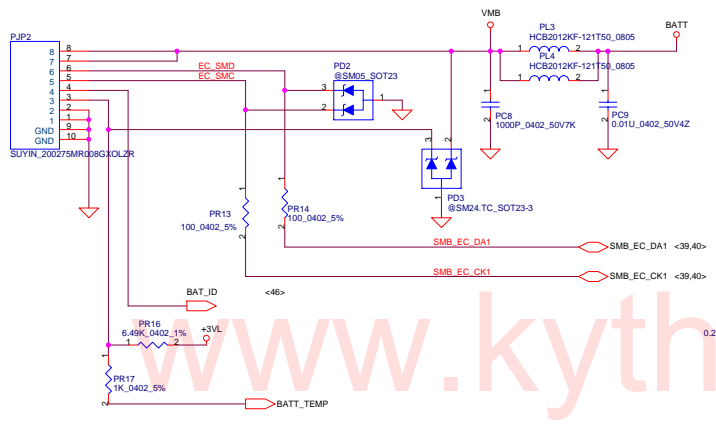
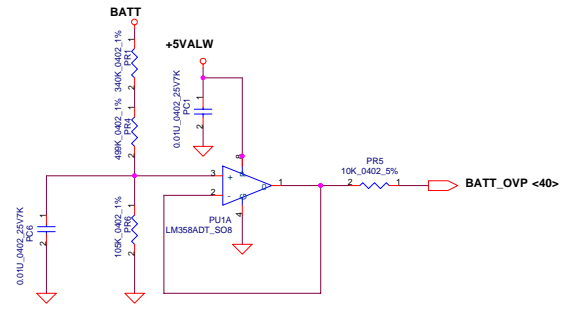
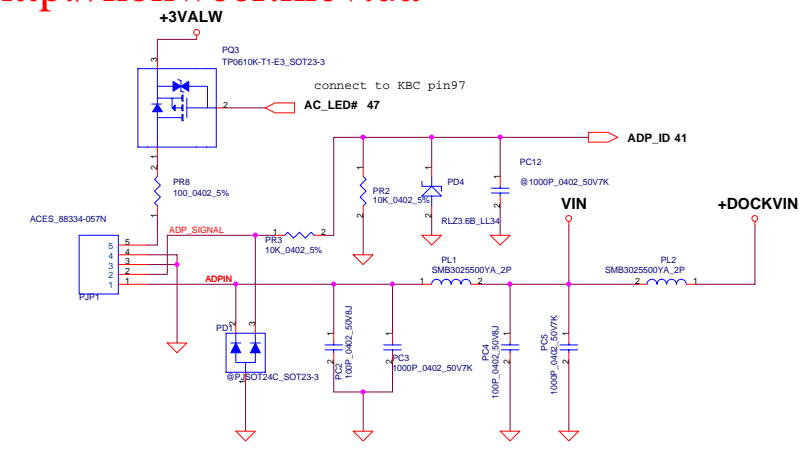
**Discharge circuit**



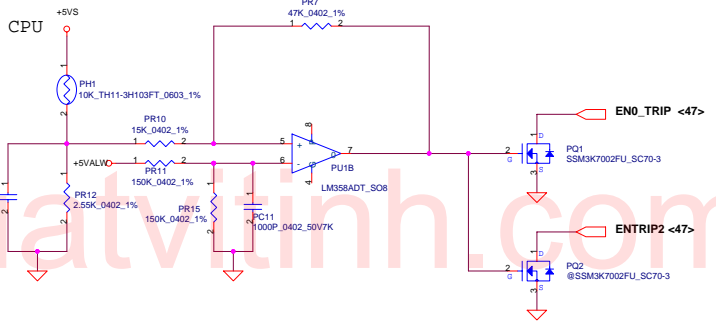
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Issued Date	2008/02/25	Deciphered Date	2009/02/25	DC/DC Interface
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Date	Monday, February 25, 2008	Sheet	41	of 53



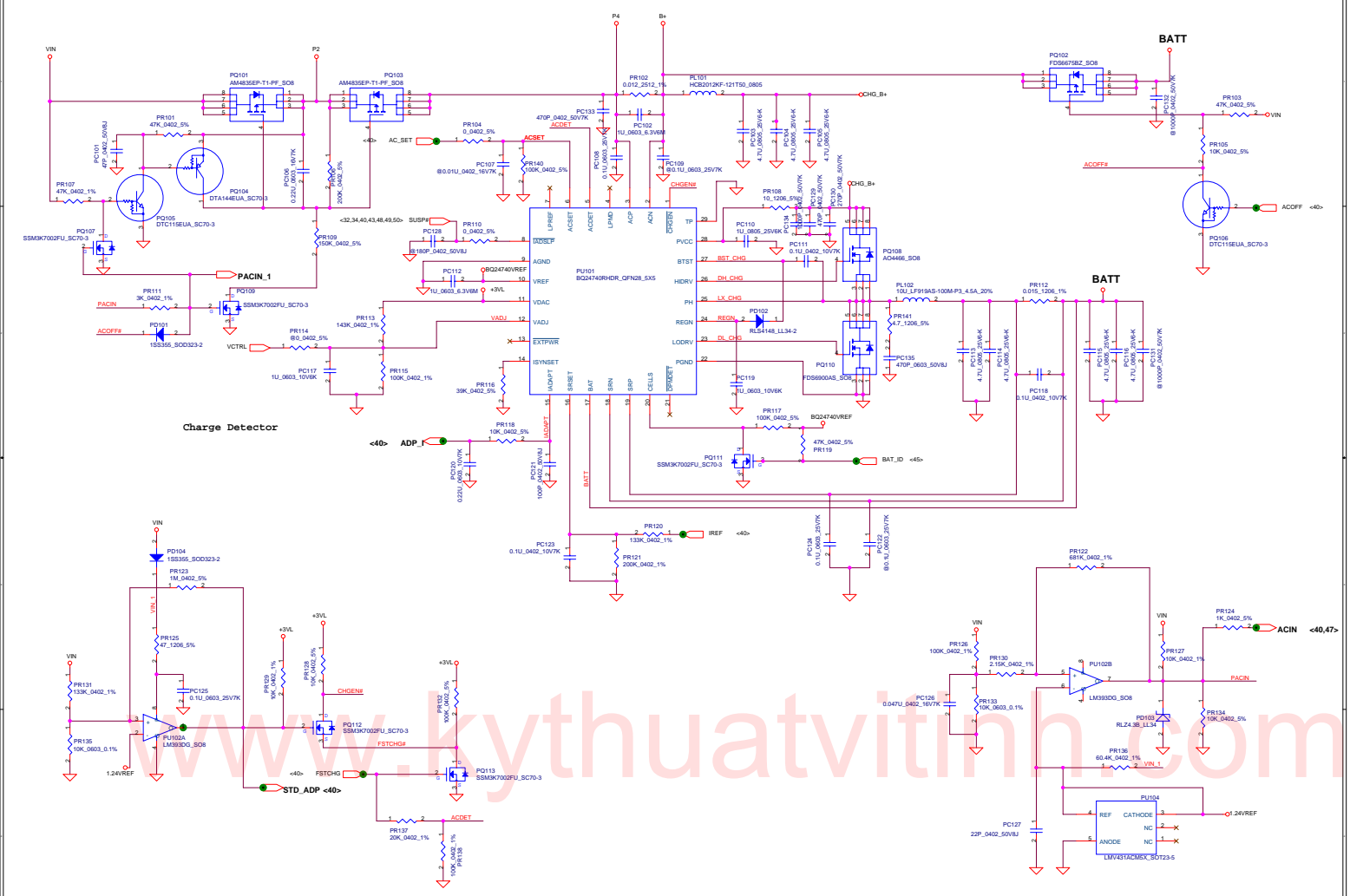
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Issued Date	2008/02/25	Deciphered Date	2008/02/25	<b>Compal Electronics, Inc.</b>
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				Document Number
				LA-4102P Blade discrete
				Rev
				0.4
				Date
				Monday, February 25, 2008
				Sheet
				42 of 53



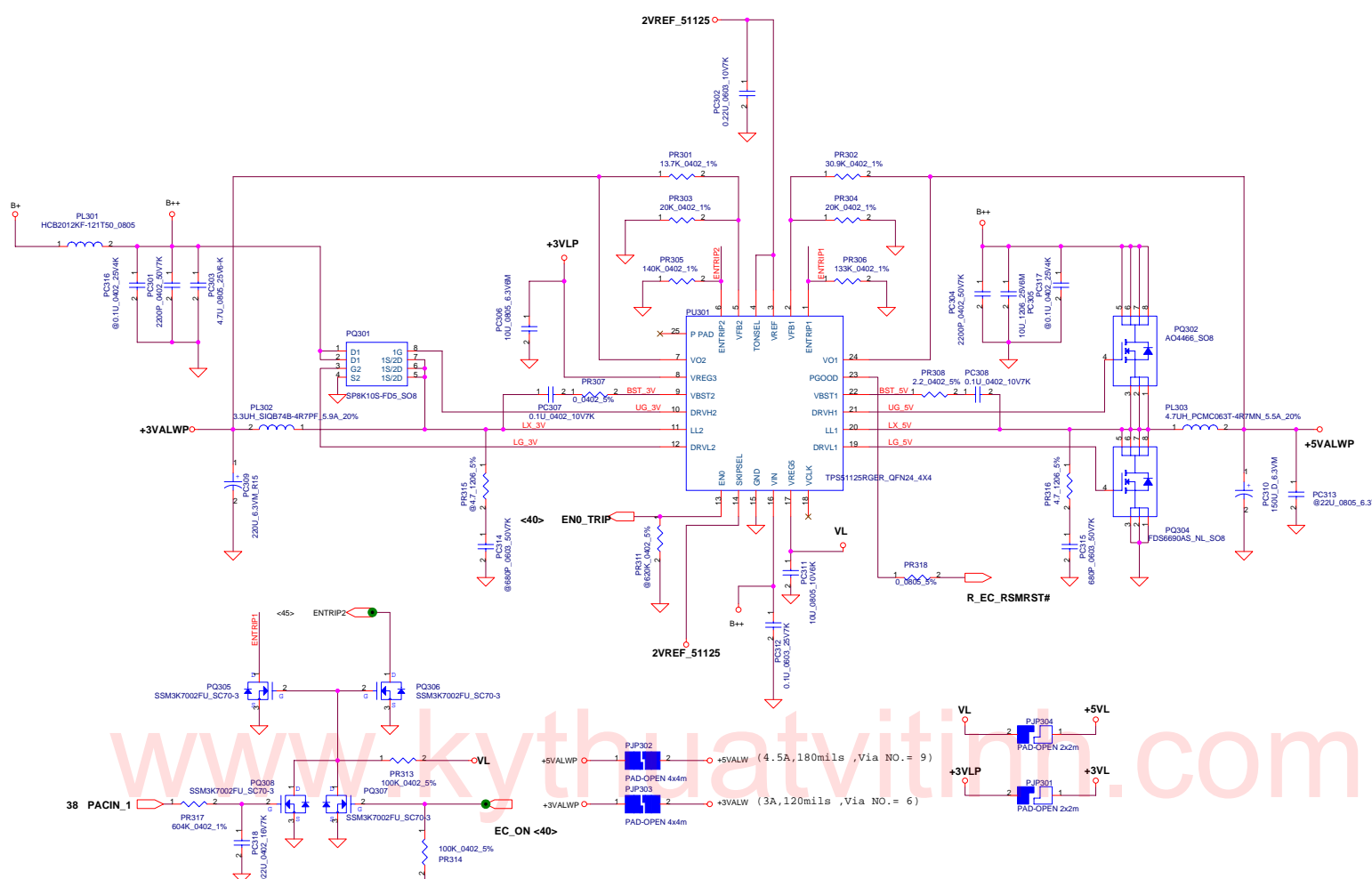
PH1 under CPU bottom side :  
 CPU thermal protection at 90 +/-3 degree C  
 Recovery at 47 +/-3 degree C



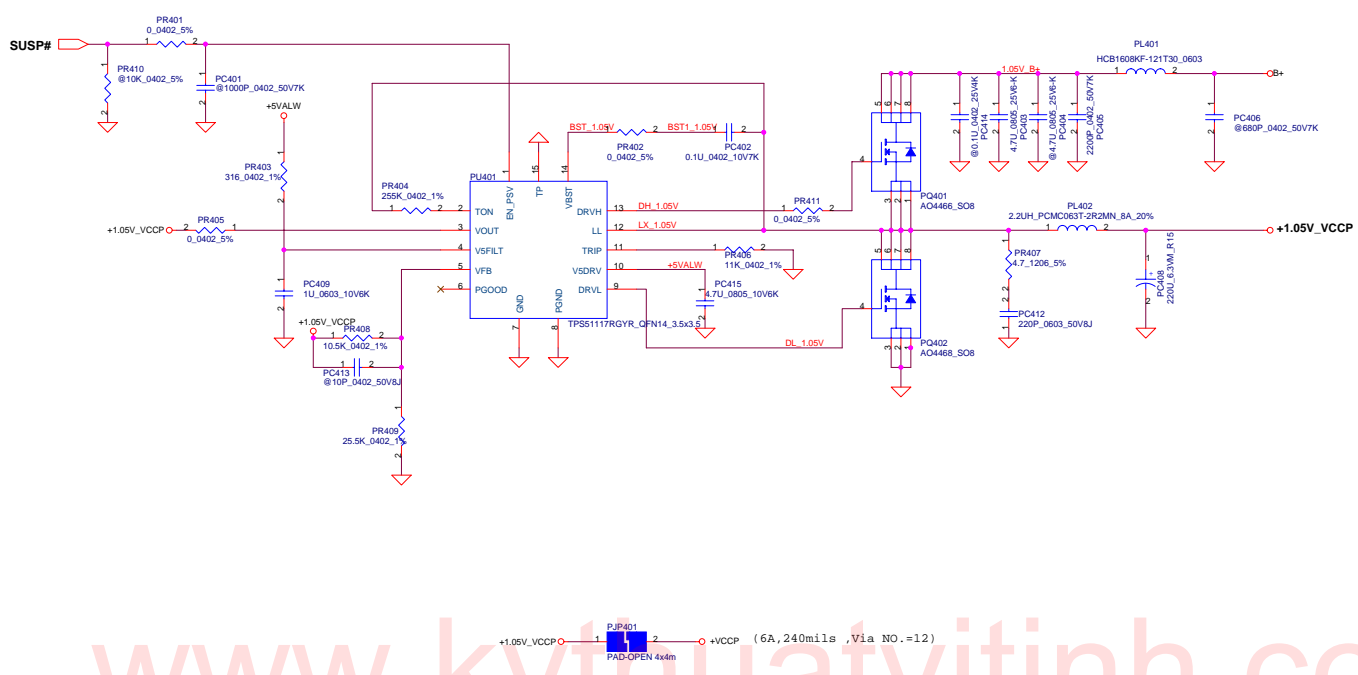
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Issued Date	2008/02/25	Deciphered Date	2008/02/25	DC Connector/CPU_OTP	
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Date	Monday, February 25, 2008	Sheet	43	of	52



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Account No.	Project No.		Rev.
	LA-1102P		0.4
Doc No.	Revision	Page	
ME2505	February 25, 2008	24	28

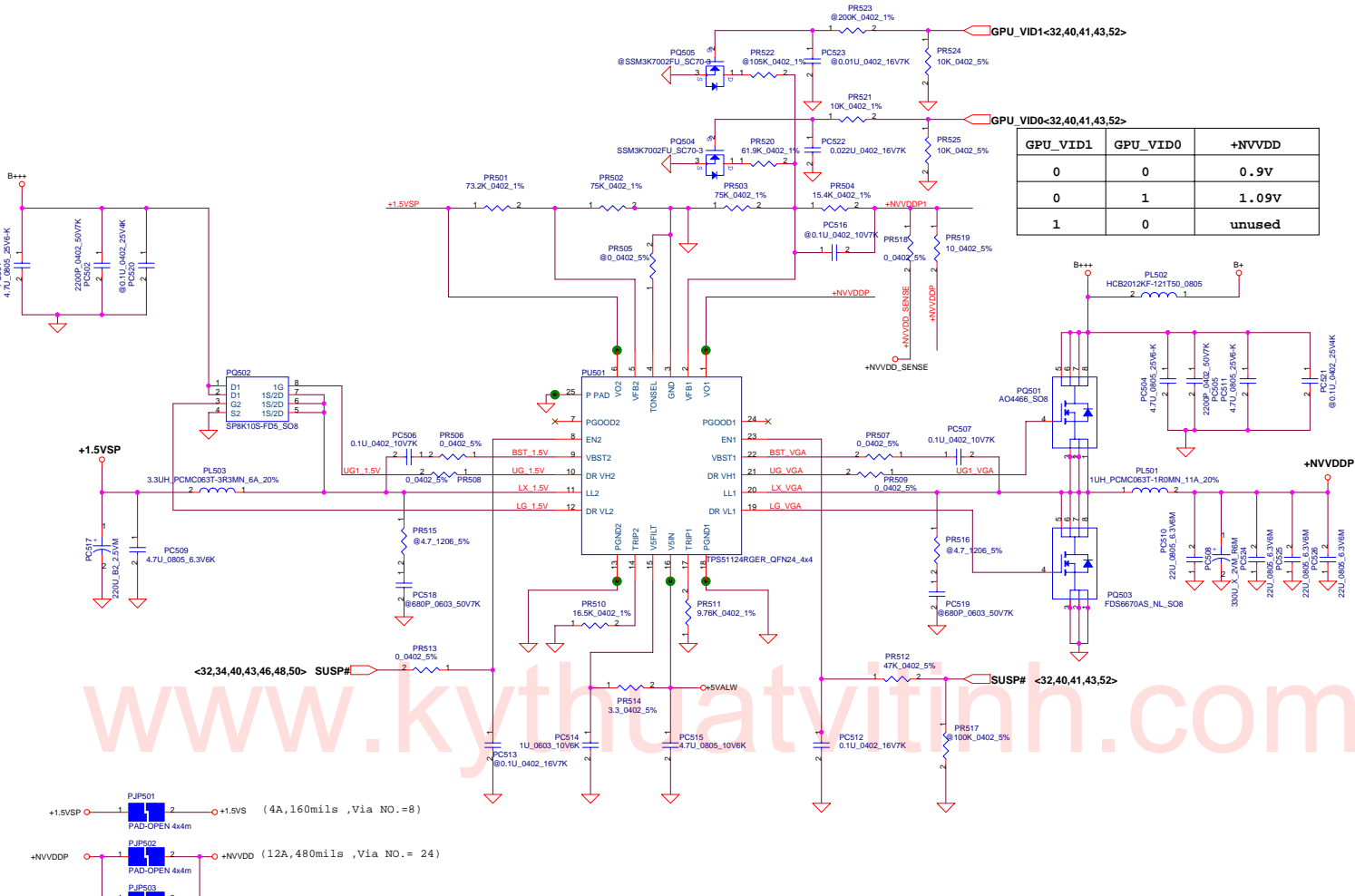


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Issued Date	2008/02/25	Deciphered Date	2008/02/25	3.3VALWP/5VALWP	
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			Date	Monday, February 25, 2008	Sheet 46 of 52



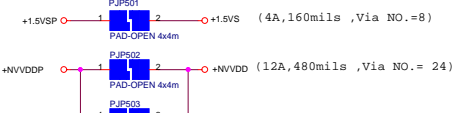
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Date: Monday, February 25, 2008				Sheet 46 of 52

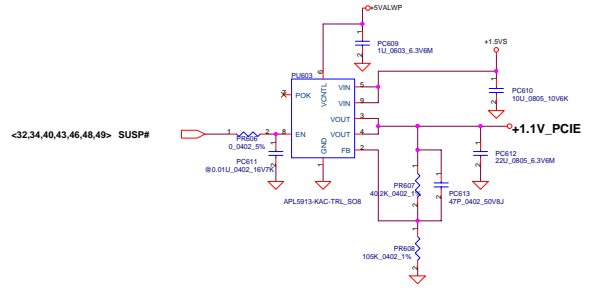
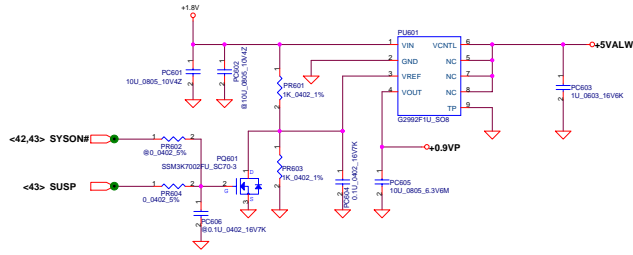


GPU_VID1	GPU_VID0	+NVVDD
0	0	0.9V
0	1	1.09V
1	0	unused

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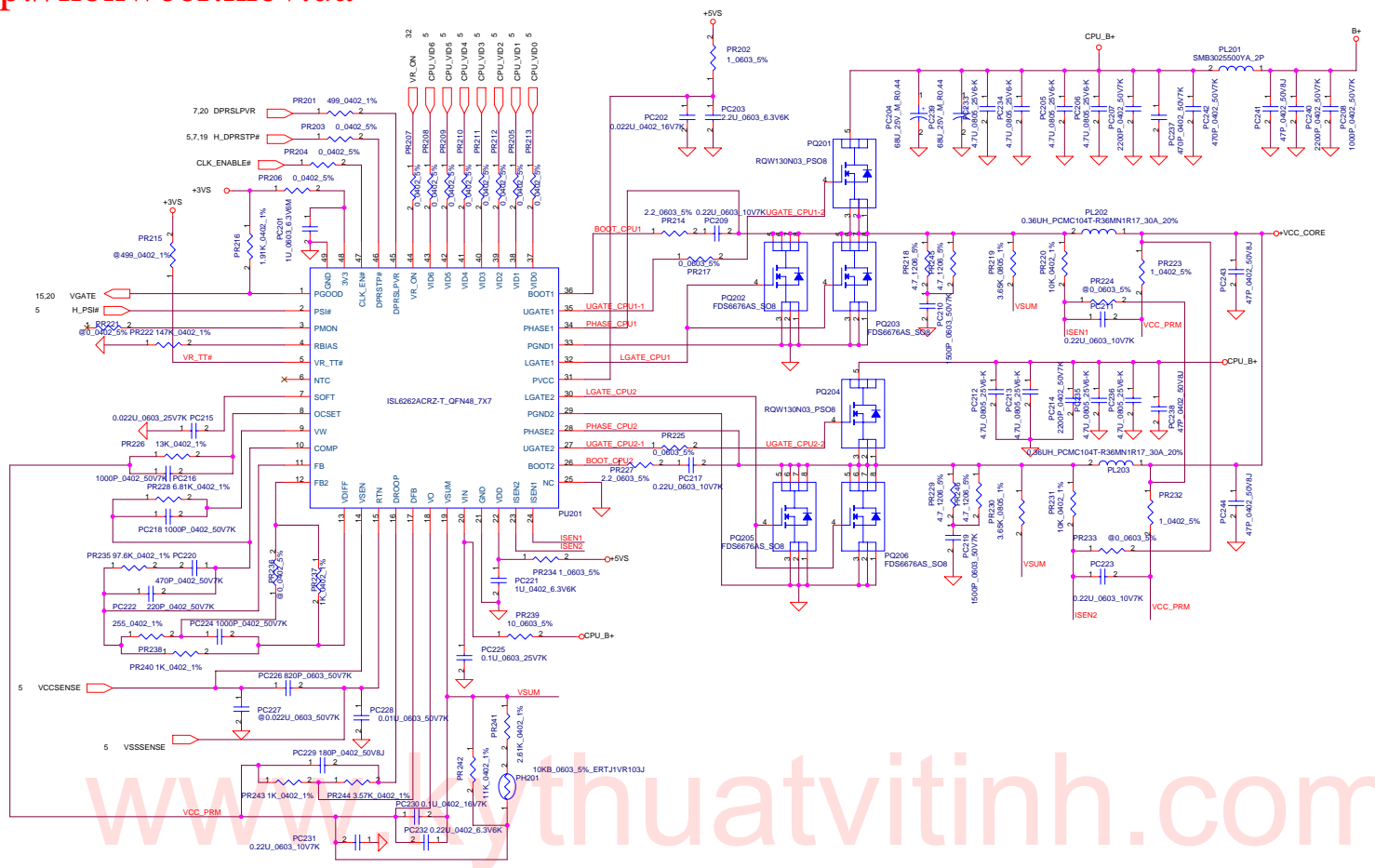


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Date	Monday, February 25, 2008	Sheet	47	of	52



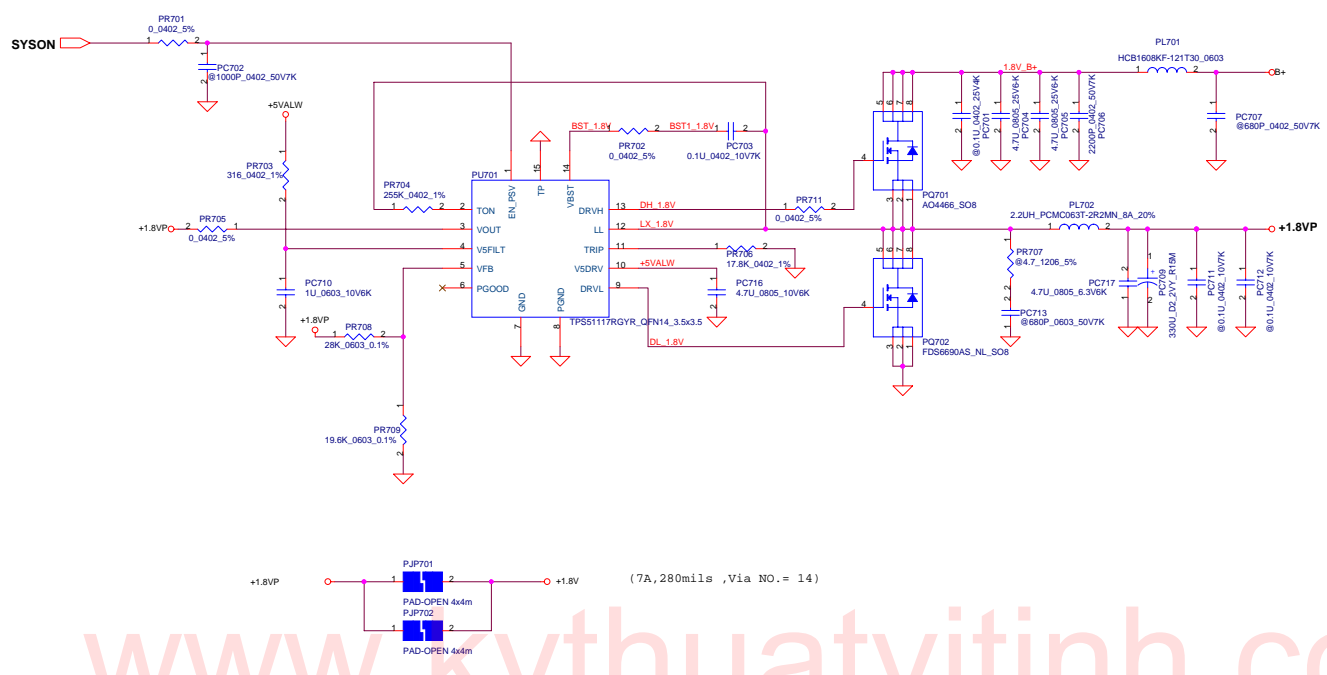
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				Document Number
				Rev
				04
				Date
				Monday, February 25, 2008
				Sheet
				48 of 59



<b>Compal Electronics, Inc.</b>	
File:	<b>+CPU_CORE</b>
Project Number:	
Revision:	Rev 0.4
Date:	Monday, February 25, 2008
Sheet:	49 of 52

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					LA-4102P Blade discrete
				Date	Monday, February 25, 2008
				Sheet	50 of 52
				Rev	0.4

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	43	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12	
2	45	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301, cancel PQ303.	
3	44	Charger	11/06	Compal	EMI solution	Add PC128	
4	49	CPU_CORE	11/06	Compal	EMI solution	Add PC240	
5	47	1.5VSP/VGA_CORE	11/06	Compal	for VGA voltage steps	Add PQ505, PR523, PR524, PR525	
6	45	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
7	44	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133	
8	49	+CPU_CORE	12/31	Compal	EMI solution	Add PC242	
9	47	+1.5VSP/VGA COREP	01/02	Compal	HW request	Change PR513 to 0_ohm	
10	44	Charger	01/02	Compal	EMI solution	Add PC135 and PR141	
11	49	+CPU_CORE	02/15	Compal	Change high-side MOS for WWAN	Change PQ201 and PQ204 to powerpak	
12	43	DC Connector /CPU_OTP	02/15	Compal	AC LED change to KBC control	ACLEd# connect to EC pin 97	
13	43	DC Connector /CPU_OTP	02/19	Compal	WWAM issue	add PC241 47pF	
14	49	+CPU_CORE	02/19	Compal	WWAM issue	add PC243 PC244 47pF	

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				Document Number	0.4
				Custom	
				LA-4102P Blade discrete	
				Date	Monday, February 25, 2008
				Sheet	51 of 52

Item	Fix Files / (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41, C42, C43, C44 Change ESR=7m ohm	11/21	DB
2	Disable TV out function from Docking	20	TV signal unconnected,DACB_VDD pull low 10K (R948).	11/07	DB
3	Update Connetor Library		CRT(JCRT1), HDMI(JHDMI1), ESATA(JP53), Finger print(JJP24), FAN(JP2), Speaker(JP60), Multi bay(JP12), Dual LED(D53, D54	11/17	DB
4	Delete LVDS B channel	19,20	Schematic Delete	11/17	DB
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K , R1093=100K,Add GPIO 20 to turn off power	11/07	DB
6	Reserve Card reader D3E function	27,32	GPIO6= CR_CPPE# , GPIO22=CR_WAKE#	11/17	DB
7	Swap PCIE LAN and New card	27	Swap PCIE4 and PICE6	11/17	DB
8	Change GPU 1.8VS power	20, 21	Change 1.8VS to +VDD_MEM18	11/17	DB
9	Change G sensor control from SB, LED drive by +5VS	27, 39	Change G sensor control from SB	11/17	DB
10	Avoid Battery mode can't boot issue	38, 45	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	DB
11	Add G sensor ST and Bosch	37	Add G sensor ST and Bosch	11/17	DB
12	Change LAN solution (Marvell to Realtek)	30	Change LAN solution (Marvell to Realtek)	11/17	DB
13	LAN transformer interfere	30	U19 Change to correct transformer type	11/17	DB
14	Cardreader schematic review,add D3E function	32	R709-->10K, R1047-->8.2K, R1128-->Stuff, R705-->@, U37-->@, Cardreader LED-->+5VS, add D3E function	11/17	DB
15	Jack can't detect normal	33	R1059 change from 39.2 to 39.2K	11/17	DB
16	Docking can not power on	40	Add power on circuit D57,Q13R751,R752,R753	11/17	DB
17	HP audio team recommend	33, 35	C1480-C1487, C1352, C1354 change to 0.022U, Amp output setup to 15.6 dB, Reserve C747, C748 for GNDA and GND	11/17	DB
18	Audio jack can't detect normal	35	Add Pull up resistor R750 to +3VALW	11/17	DB
19	Docking HP audio test fail	35	Add C795, C796 to avoid DC level, and add R968, R969 to reduce HP out level	11/17	DB
20	Leakage problem	38	Correct direction prectek leakage	11/07	DB
21	EC pin define update	38	Delete EC_PME#, SYSON PU, SUSP# PU, LID_SW# change to +3VALW, Delete CLKRUN#, R582->@ for C0 chip, CIR PU+5VL, add 100P to BATT_OVP(EC recommend)	11/07	DB
22	Can't Hibernation(SLP_S4#)	38	Connect SLP_S4# to SB	11/17	DB
23	EC can't receive docking present	40	CONA# change +3VL	11/12	DB
24	Reserve capacitor on digital MIC for EMI request	19	Add C496,C498	11/07	DB
25	Add 2N7002 to GND on HDMI to avoid leakage.	21	Add Q74	01/04	SI
26	+VDD_MEM18 to +1.8VS, change to jummpers	22	Delete R1124,R1125 add PJP605	01/04	SI
27	HDCP ROM fail. HDCP_SCL need pull high.	22	R224 no stuff. R213 stuff.	01/04	SI
28	Reserve capacitor on digital MIC for SED, WWAN noise	26	Add C499,C502	01/04	SI

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				LA-4102P Blade discrete	0.4
				Date	Sheet
				Monday, February 25, 2008	52 of 53

Item	Fix (Issues / Reason for change)	PAGE	Modify List	Date	Phase
1	Change transformer vendor	30	change U19 library	01/04	SI
2	XMIT_OFF add a diode to avoid leakage.	31	Add D88	01/04	SI
3	Card reader recommend	32	XD_ALE need pull +3VS not pull low.	01/04	SI
4	change Q54 from transistor to MOS for cardreader LED.	32	Change Q54	01/04	SI
5	speaker pop issue	35	Change C1488 to 1U	01/04	SI
6	Reserve capacitor on SPL_FSEL#,CLK#,FER for EMI request	36	Add C2125,C2126,C2127	01/04	SI
7	Change EC_PME pull high from +3VL to +3VALW	38	R585 stuff	01/04	SI
8	Reserve damping resistor on SPL_CLK for EMI request	38	Add R191	01/04	SI
9	WLAN LED issue,WL_BLUE_LED# pull +3VS	39	Add R716	01/04	SI
10	Add bypass capacitance on sensor bottom	39	Add C261(4.7U)	01/04	SI
11	EC can't detect DOCK_PRESENT.	40	change R754 to 22 Ohm,R623 to 2K	01/04	SI
12	Add DOCK_VOL_UP#,DOCK_VOL_Down# pull +3VS	40	Add R594,R596	01/04	SI
13	SPDIF issue	40	follow Vader	01/04	SI
14	Docking CRT blurred	40	Change ping 31,39,22 connect to GND	01/04	SI
15	Change R650 and C770 to modify the power sequence	41	change R650 to 1K, C770 to 0.1u	01/04	SI
16	Add 12P on CLK_14M_ICh for WWAN noise	17	Add 12P on CLK_14M_ICh	02/15	PV
17	BKOFF# reserve pull low 10K	19	reserve R717	02/15	PV
18	Reserve CMD27 to support 64M X16	7,8	Reserve CMD27 to support 64M X16	02/15	PV
19	Reserve cap on HDA_BITCLK for WWAN noise issue	26	Reserve cap on HDA_BITCLK	02/15	PV
20	Reserve to prevent ESD issue	30	Reserve ESD diode on LAN LED pin	02/15	PV
21	Change WLAN and WWAN 0402 resistor to 0805	31	Change WLAN and WWAN 0402 resistor to 0805, and WLAN change to +3VS power plane	02/15	PV
22	Direct drive LED, and add D3E function diode	32	Direct drive LED and XD_ALE Pull L, and add D86 for D3E function	02/15	PV
23	Change R1092 value on BT power switch Gate	36	Change R1092 to 10K	02/15	PV
24	Correct AC_LED control by EC	38	AC_LED Change controll by EC	02/15	PV
25	Change all LED limit current resistor to 200 ohm	39	Change all LED limit current resistor to 200 ohm and add Touch pad LED for PR	02/15	PV
26	Add 33 ohm for MUTE_LED and DOCK_SLP_BTN#	40	Add 33 ohm for MUTE_LED and DOCK_SLP_BTN#	02/15	PV
27	follow check list ver:1.5	6	change R13 to 56 ohm;change R2-R8 to 51 ohm;change R11 to 0ohm	02/20	PV
28	Reserve Cap for EMI	42	add C1250,C1249	02/20	PV

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				LA-4102P Blade discrete	0.4
				Date	Sheet
				Monday, February 25, 2008	53 of 53

Item	Fixes (Change)	PAGE	Modify List	Date	Phase
1	follow check list Ver:1.5	17	reserve R148	02/15	PV
2	follow check list Ver:1.5	9	change R45,R48 to 10K	02/15	PV
3	boot code "88" power sequence fail	27	add Diode from PWROK to RSMRST	02/15	PV
4	Change BT,LAN,DOCK,Multibay connect for DFX			02/15	PV
5	Change WWAN and WLAN LED	39		02/15	PV
6	For EMI	37	SPL_CLK add R2118 , R2119 , R2120 => 33ohm add C2125 , C2126 , C2127 => 22pF;R553, 554, 556 =>10ohm	02/15	PV
7	For EMI	30	LAN add C656 and C657 => 0.1uF	02/15	PV
8	For EMI	39	T/P add D28 and C729	02/15	PV
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				LA-4102P Blade discrete	0.4
Date	Monday, February 25, 2008	Sheet	54	of	53