

QT8 SYSTEM DIAGRAM



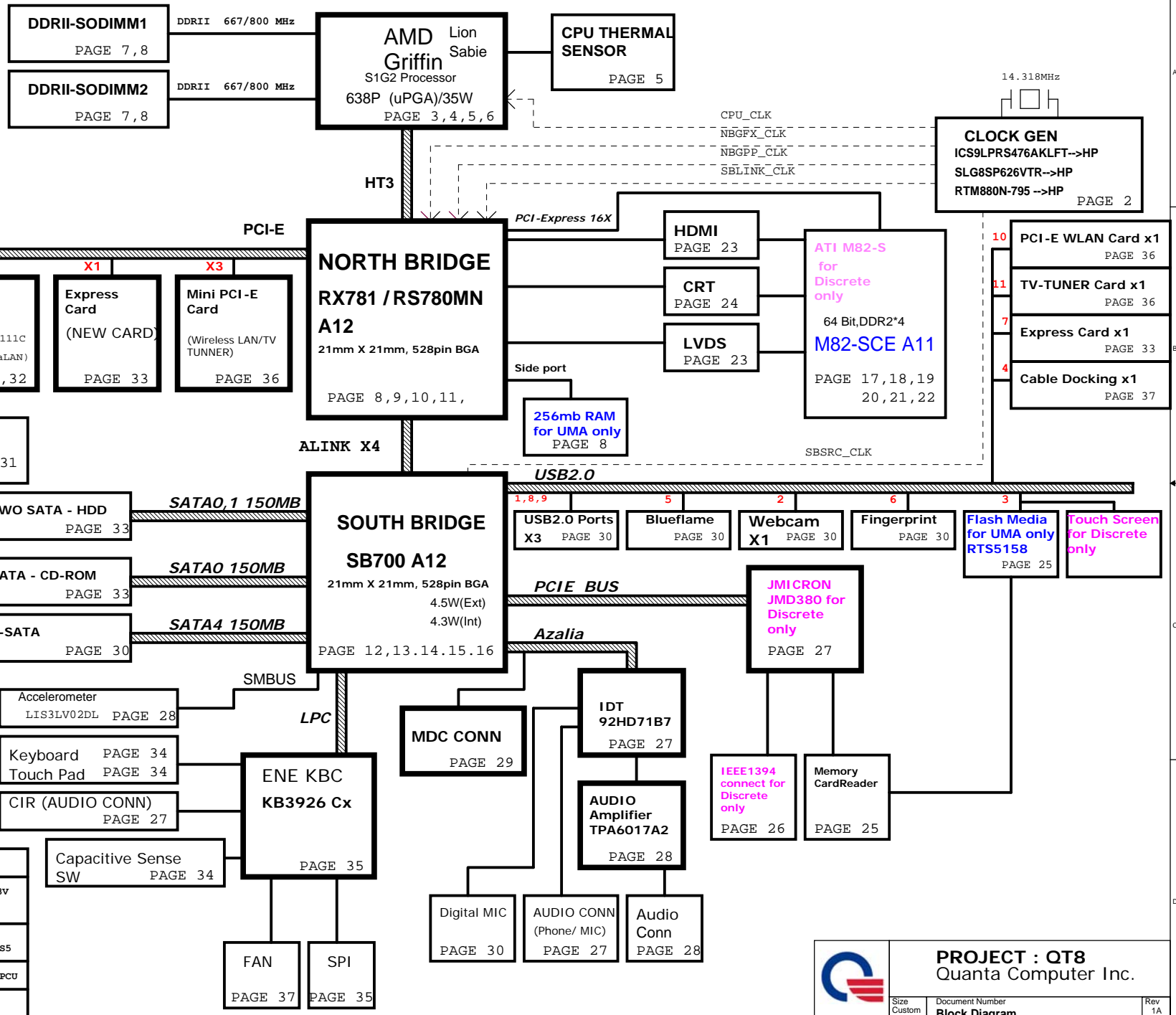
PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : IN1
- LAYER 3 : IN2
- LAYER 4 : VCC
- LAYER 5 : IN3
- LAYER 6 : BOT

- #### Cable Docking
- VGA
 - RJ-45
 - CIR/Pwr btn
 - SPDIF Out
 - Stereo MIC
 - Headphone Jack
 - USB Port
 - VOL Cntr
- PAGE 37

- SYSTEM CHARGER(ISL6251A) PAGE 44
- SYSTEM POWER ISL6236IRZA-T PAGE 38
- DDR II SMD DR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 41
- VCCP +1.1V AND +1.2V(MAX8717) PAGE 39
- VGACORE(1.1V~1.2V)Oz8118 PAGE 42
- CPU CORE ISL6265A PAGE 40

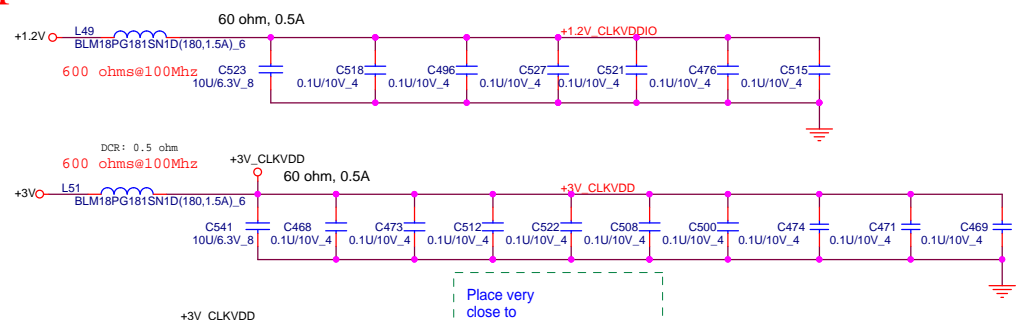
SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR thermal/Accelerometer	+3V
	epress card	+3VS5
	Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V



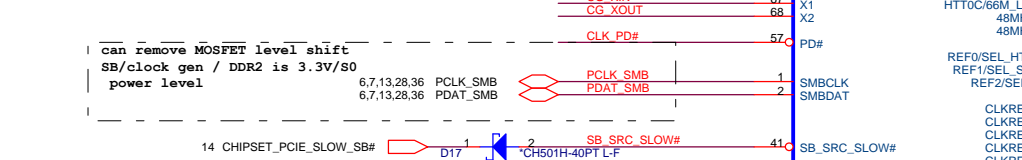
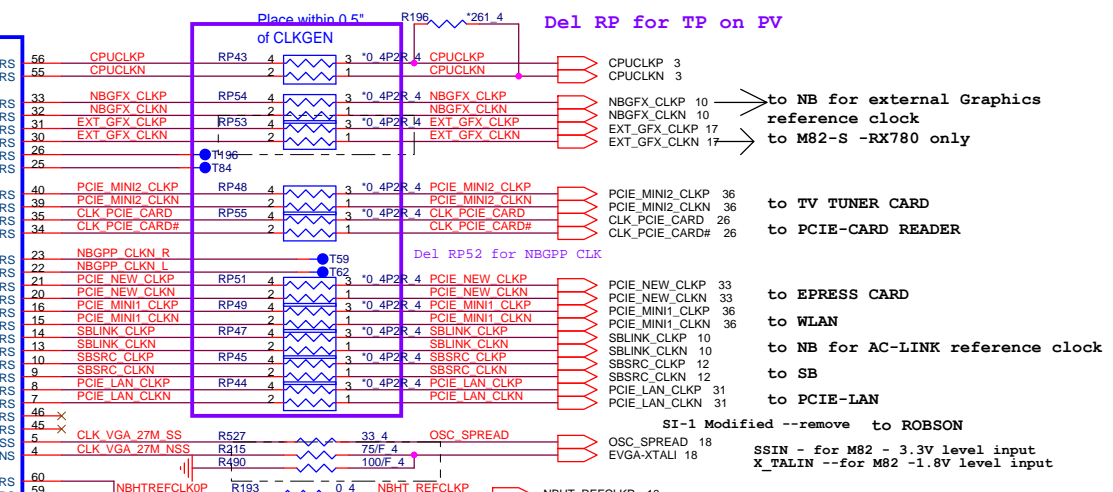
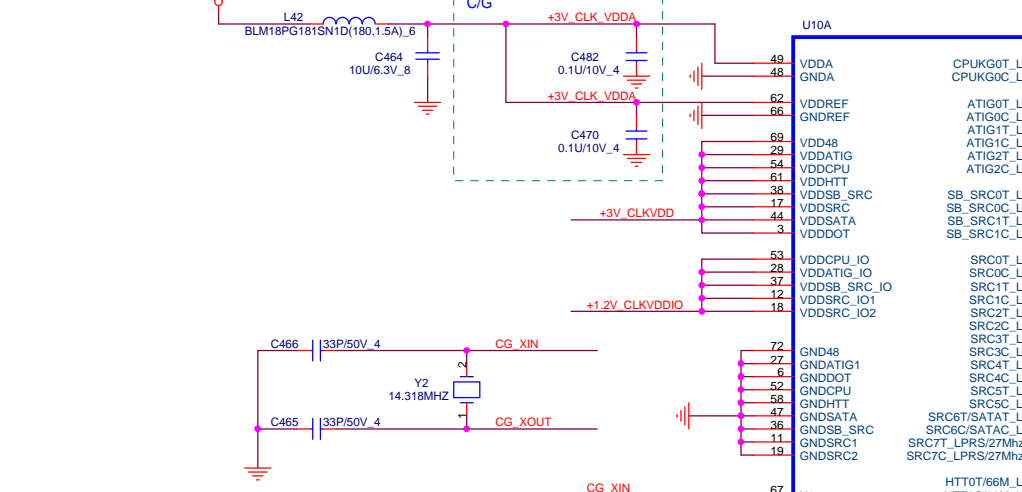
PROJECT : QT8
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Size Custom	Document Number	Rev 1A
Block Diagram		
Date: Tuesday, February 19, 2008 Sheet 1 of 45		

NBS/RD5



CLOCKS name	RX780	RS780	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT GFX_CLKP EXT GFX_CLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGP_P_CLKP NBGP_P_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock, RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R653, R656, R612 STUFF	R653, R656, R612 NC	To M82-S 27Mhz - RX780 only

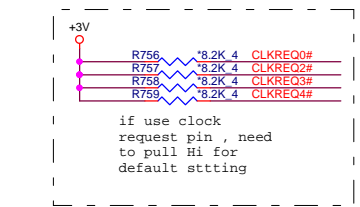
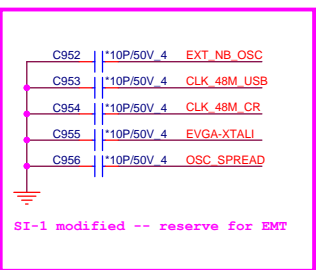


can remove MOSFET level shift
SB/clock gen / DDR2 is 3.3V/80
power level

6,7,13,28,36 PCLK_SMB
6,7,13,28,36 PDAT_SMB

14 CHIPSET_PCIE_SLOW_SB#

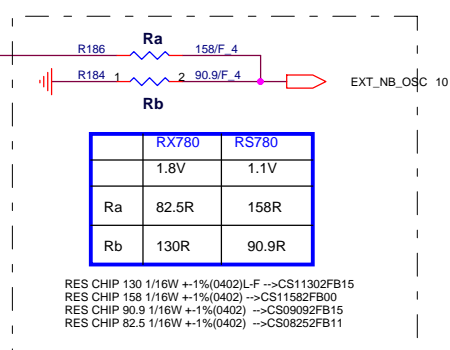
when driven low SB_SRC clocks slow only supported with
to reduced setpoint custom CG IC



ICS ICS9LPR476BKLFT--AJRS4760000
SLG SLG8SP626VTR--AJ006260000
RTL RTM880N-795-- AJ008800000

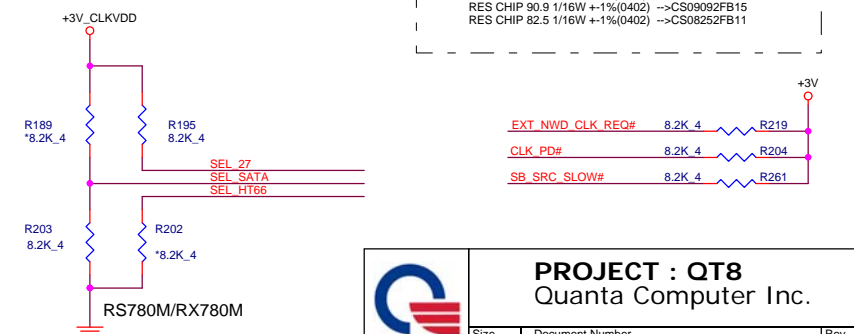
Signal	Function
SEL_HTT66	1: 66 MHz 3.3V single ended HTT clock 0*: 100 MHz differential HTT clock
SEL_SATA	1: 100 MHz non-spreading differential SRC clock 0*: 100 MHz spreading differential SRC clock
SEL_27	1*: 27MHz non-spreading singled clock 0: 100 MHz spreading differential SRC clock

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



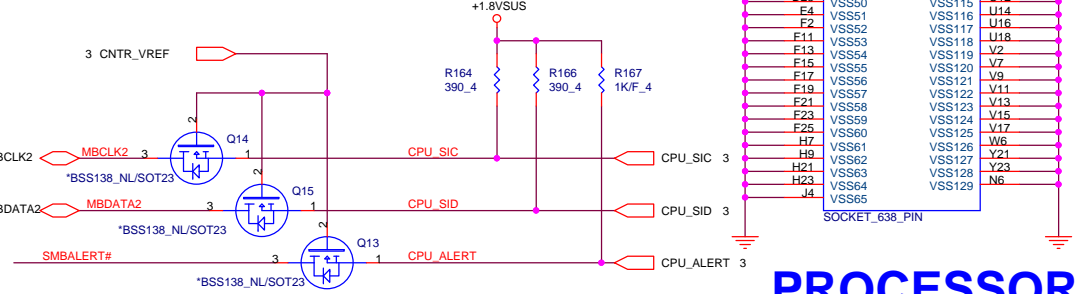
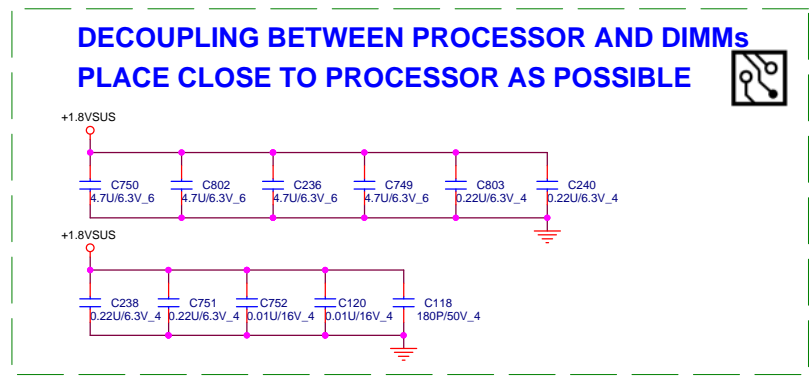
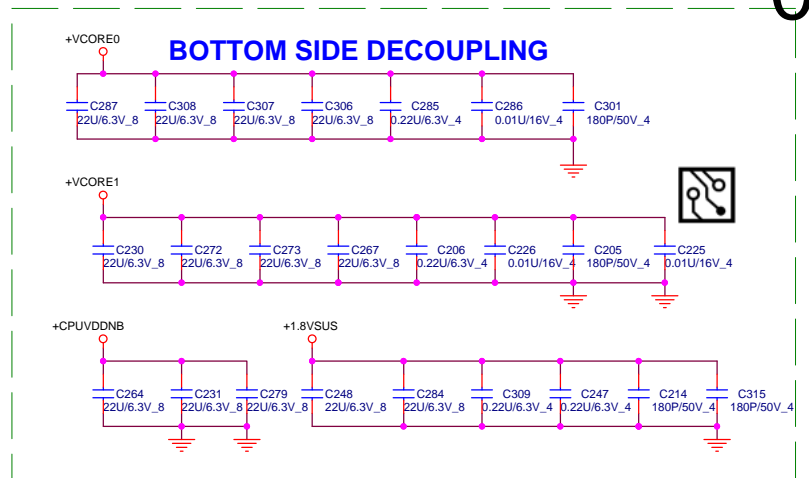
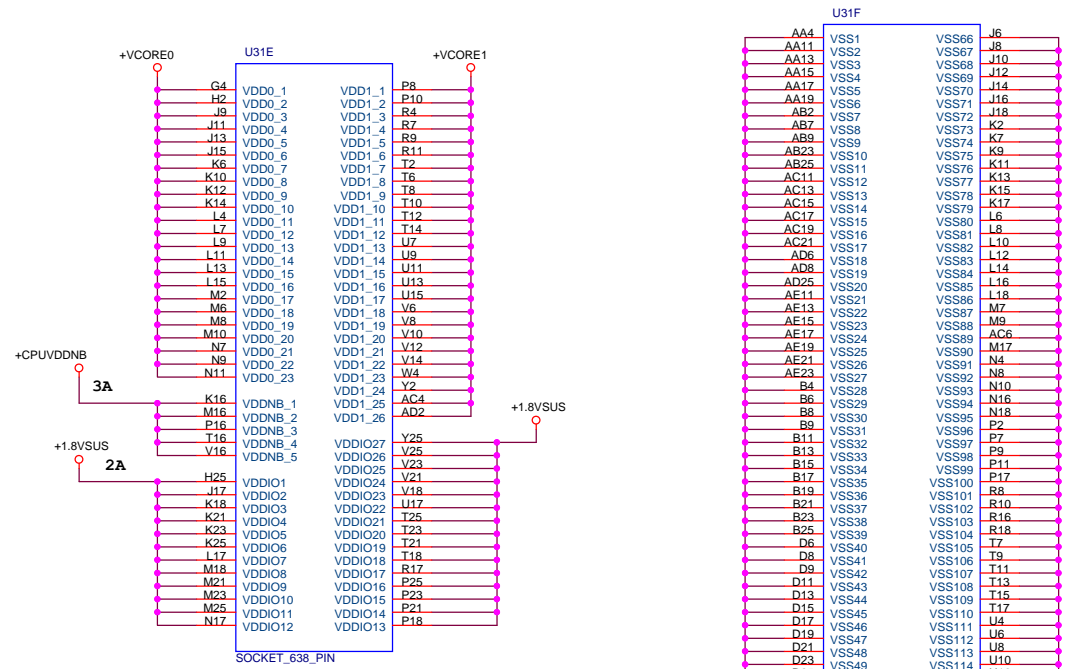
	RX780	RS780
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +1%(0402)-L-F -->CS11302FB15
RES CHIP 158 1/16W +1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +1%(0402) -->CS08252FB11

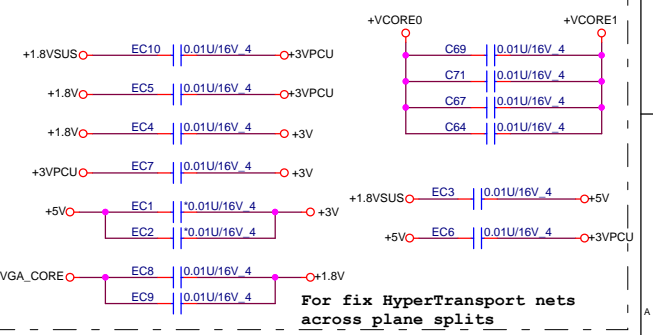
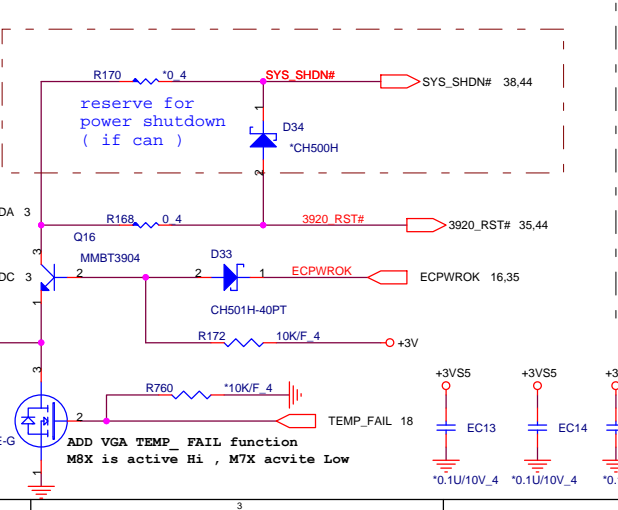
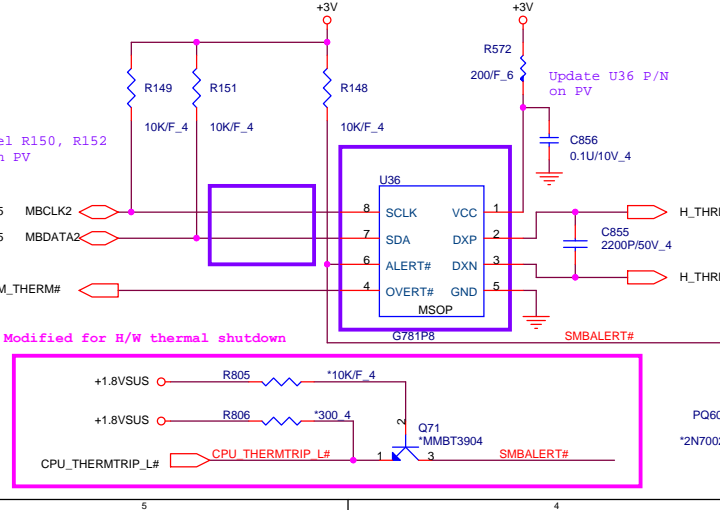


PROJECT : QT8
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Size Custom | Document Number **Clock Generator** | Rev 1A
Date: Tuesday, February 19, 2008 | Sheet 2 of 45

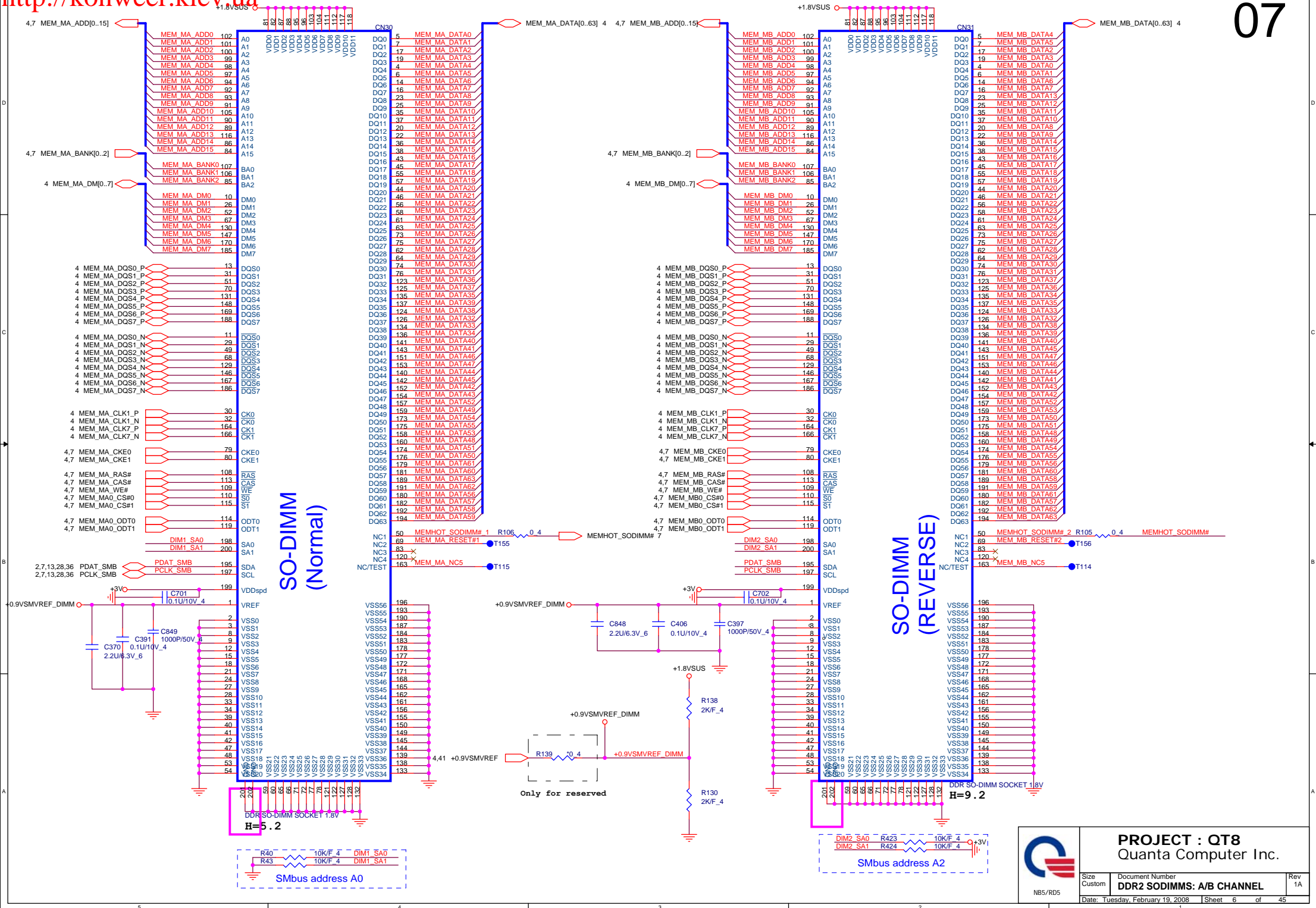


PROCESSOR POWER AND GROUND



PROJECT : QT8
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Size Custom	Document Number	Rev 1A
	SIG2 PWR & GND 3/3	
Date: Tuesday, February 19, 2008		Sheet 5 of 45



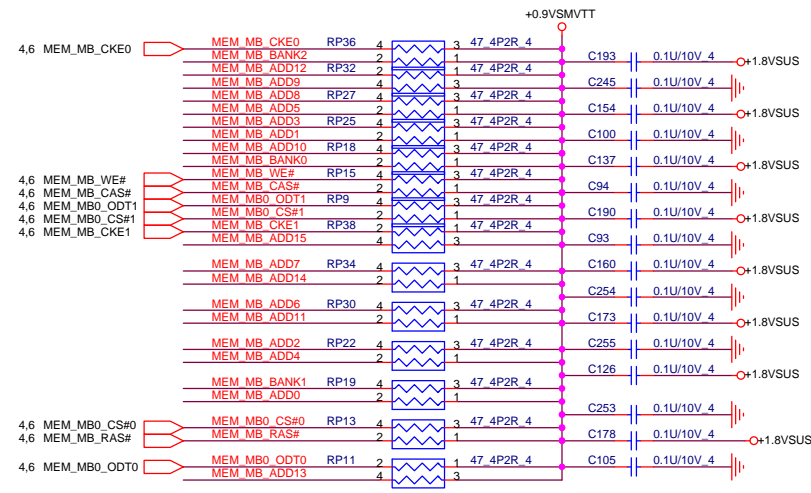
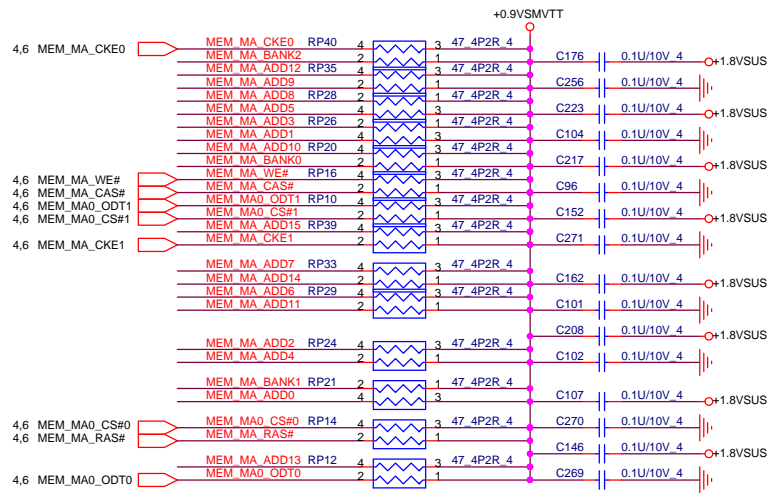
PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number **DDR2 SODIMMS: A/B CHANNEL** Rev 1A
 Date: Tuesday, February 19, 2008 Sheet 6 of 45

NB5/RD5

4,6 MEM_MA_ADD[0..15] MEM_MA_ADD[0..15]
4,6 MEM_MA_BANK[0..2] MEM_MA_BANK[0..2]

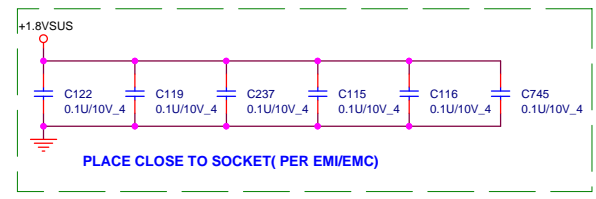
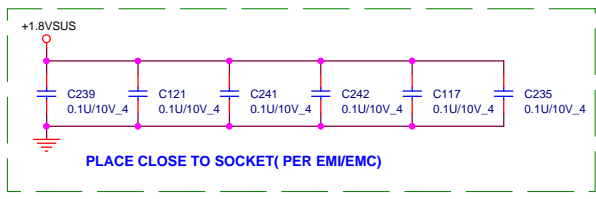
4,6 MEM_MB_ADD[0..15] MEM_MB_ADD[0..15]
4,6 MEM_MB_BANK[0..2] MEM_MB_BANK[0..2]



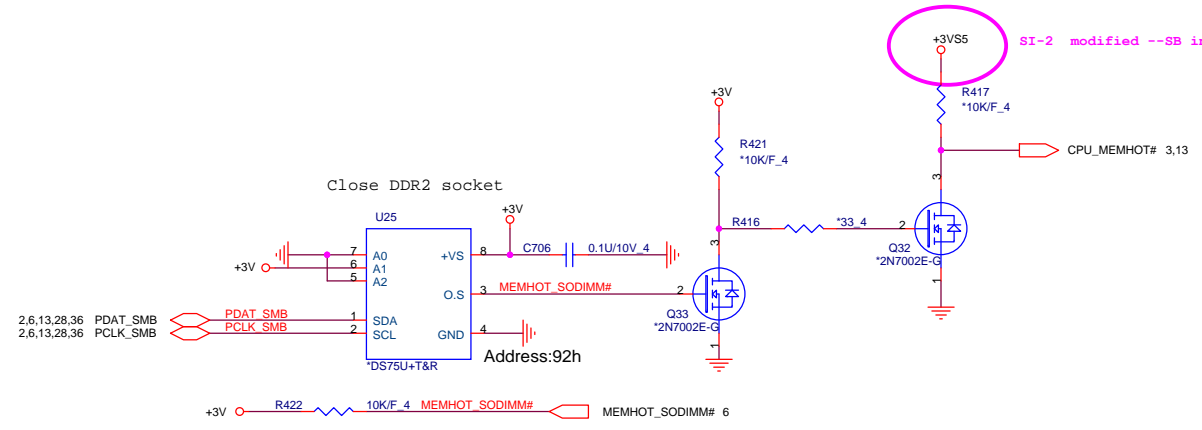
PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



SI-2 modified --SB internal pull HI to 3vs5



	PROJECT : QT8		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	DDR2 SODIMMS TERMINATIONS	
NB5/RD5	Date: Tuesday, February 19, 2008	Sheet 7 of 45	

PART 1 OF 6

HYPER TRANSPORT CPU I/F

HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	D24	HT_NB_CPU_CAD_H0	
HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	D25	HT_NB_CPU_CAD_L0	
HT_CPU_NB_CAD_H1	Y22	HT_RXCAD1P	E24	HT_NB_CPU_CAD_H1	
HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	E25	HT_NB_CPU_CAD_L1	
HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	F24	HT_NB_CPU_CAD_H2	
HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	F25	HT_NB_CPU_CAD_L2	
HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	F22	HT_NB_CPU_CAD_H3	
HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	F23	HT_NB_CPU_CAD_L3	
HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	H22	HT_NB_CPU_CAD_H4	
HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	H23	HT_NB_CPU_CAD_L4	
HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	H22	HT_NB_CPU_CAD_H5	
HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	H23	HT_NB_CPU_CAD_L5	
HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	J22	HT_NB_CPU_CAD_H6	
HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	J23	HT_NB_CPU_CAD_L6	
HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	K22	HT_NB_CPU_CAD_H7	
HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	K23	HT_NB_CPU_CAD_L7	
HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	E21	HT_NB_CPU_CAD_H8	
HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	G21	HT_NB_CPU_CAD_L8	
HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	G20	HT_NB_CPU_CAD_H9	
HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	H21	HT_NB_CPU_CAD_L9	
HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	J20	HT_NB_CPU_CAD_H10	
HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	J21	HT_NB_CPU_CAD_L10	
HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	J18	HT_NB_CPU_CAD_H11	
HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	K17	HT_NB_CPU_CAD_L11	
HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	L19	HT_NB_CPU_CAD_H12	
HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	J19	HT_NB_CPU_CAD_L12	
HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	M19	HT_NB_CPU_CAD_H13	
HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	L18	HT_NB_CPU_CAD_L13	
HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	M21	HT_NB_CPU_CAD_H14	
HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	P21	HT_NB_CPU_CAD_L14	
HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	P18	HT_NB_CPU_CAD_H15	
HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	M18	HT_NB_CPU_CAD_L15	
HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	H24	HT_NB_CPU_CLK_H0	
HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	H25	HT_NB_CPU_CLK_L0	
HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	L21	HT_NB_CPU_CLK_H1	
HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	L20	HT_NB_CPU_CLK_L1	
HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	M24	HT_NB_CPU_CTL_H0	
HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	M25	HT_NB_CPU_CTL_L0	
HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	P19	HT_NB_CPU_CTL_H1	
HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	P18	HT_NB_CPU_CTL_L1	

SI-2 modified
-- follow AMD
check list to
change part
number 300 ohm
to 301 ohm

SI-2 modified
-- follow AMD
check list to
change part
number 300 ohm
to 301 ohm

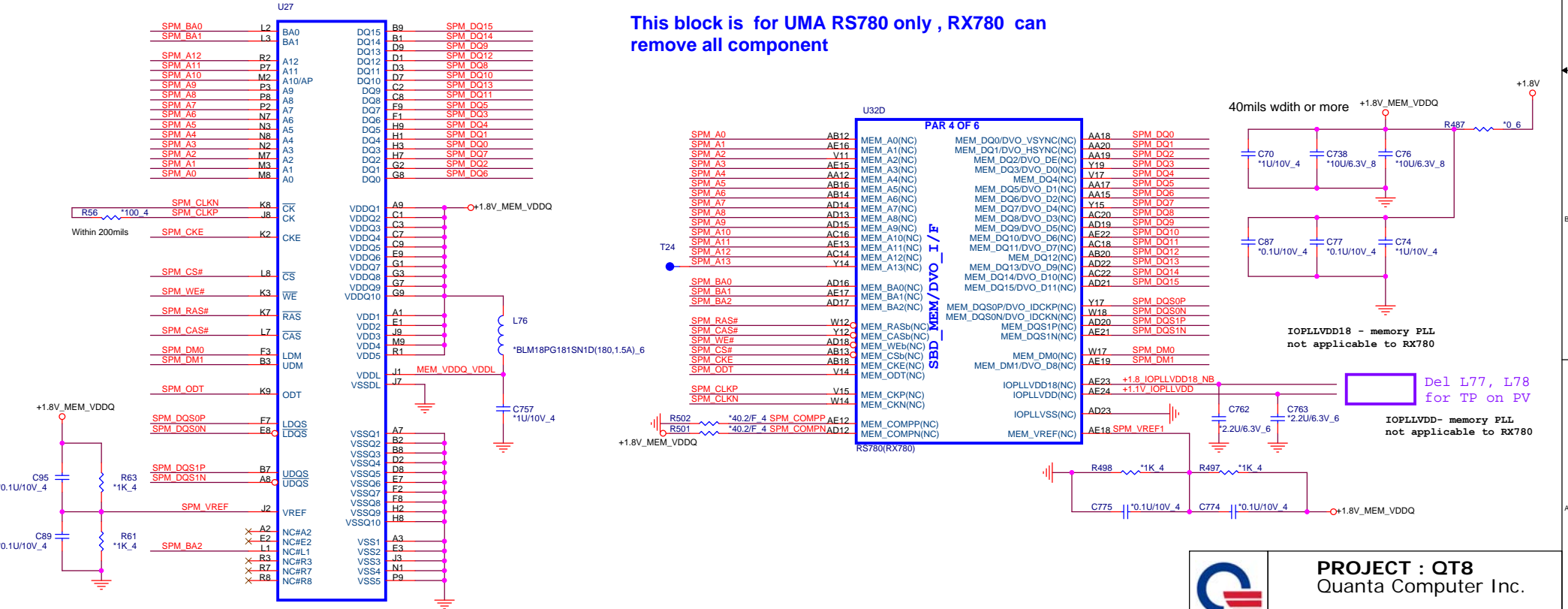
signals	RS780	RX780
HT_TXCALP	R641 301 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 301 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1% (0402)
P/N : CS21212FB18

RES CHIP 301 1/16W +-1% (0402)
P/N : CS13012FB14



This block is for UMA RS780 only , RX780 can remove all component



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PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB



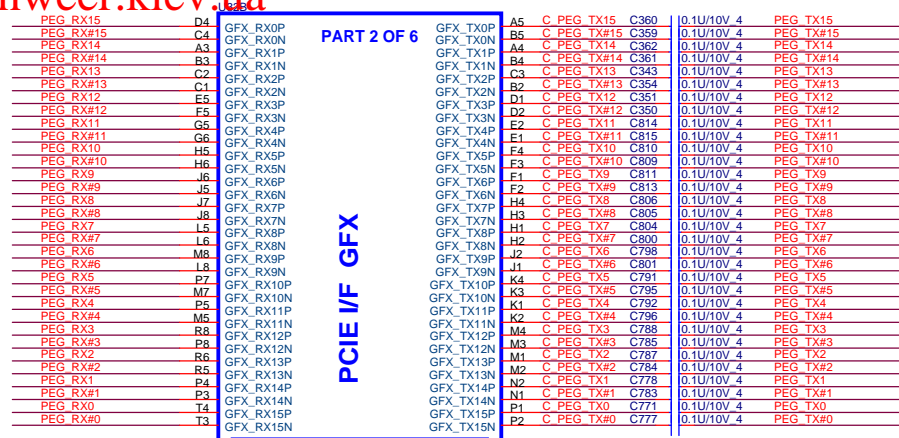
RS780(RX780)

RX780/RS740/RS780 difference table (PCIE LINK)

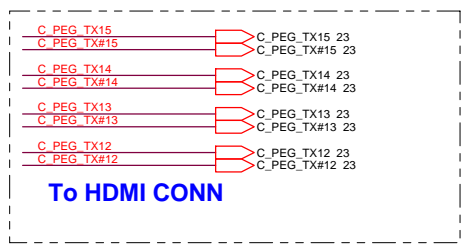
	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



Close to North Bridge



To HDMI CONN

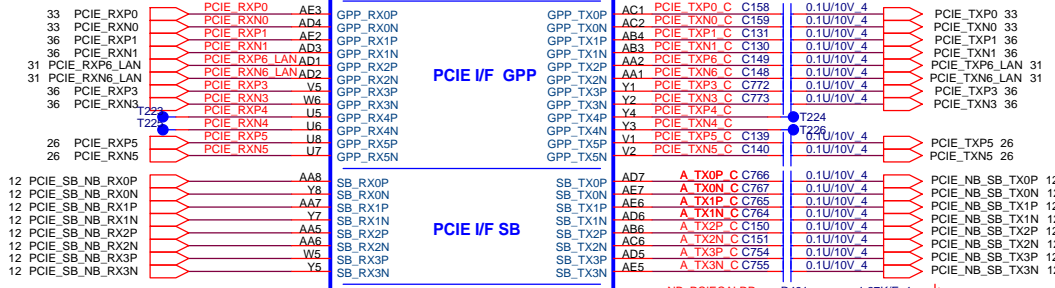
To EXPRESS CARD

To WLAN

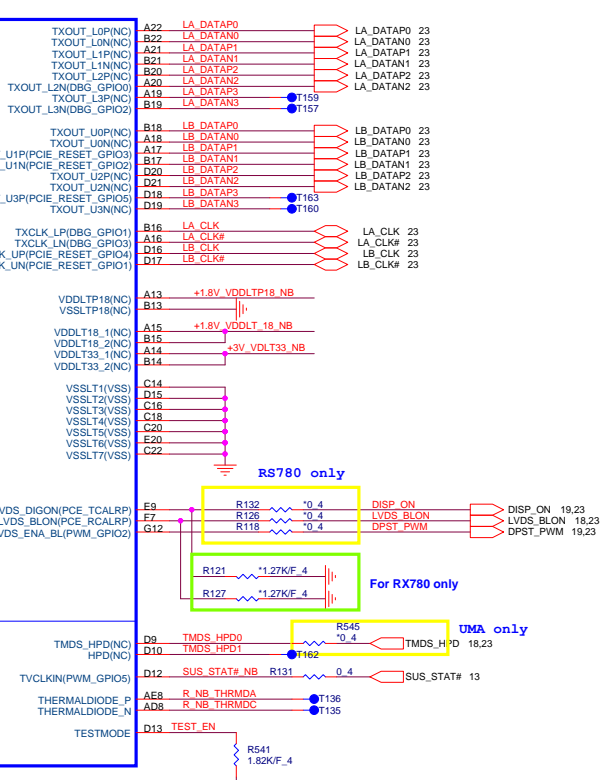
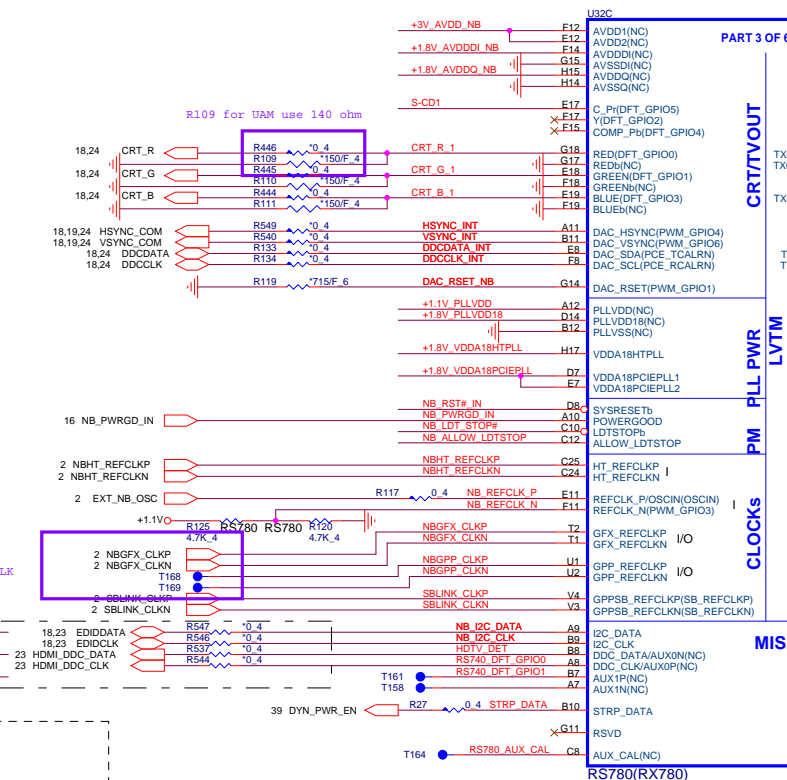
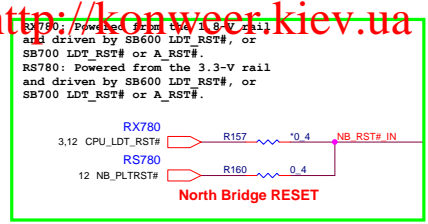
To PCIE-LAN

To TV TUNNER

To PCIE CARD READER



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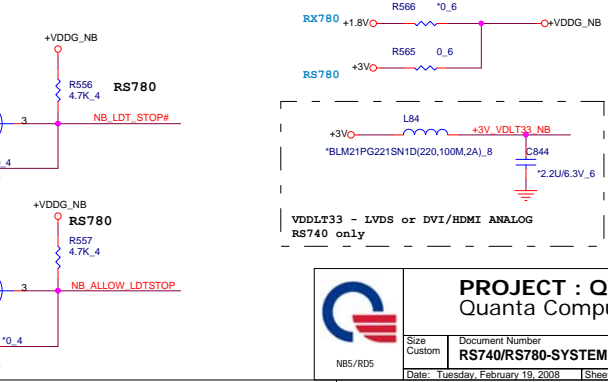
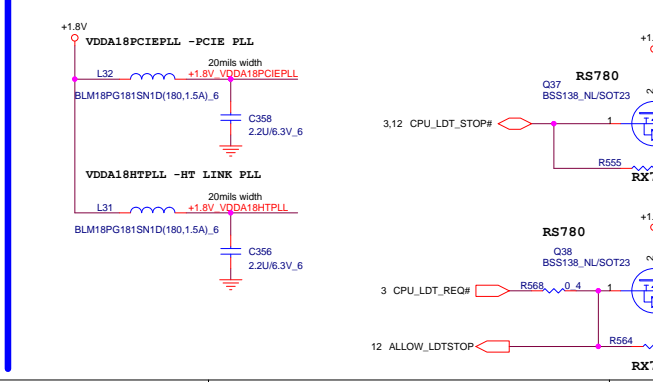
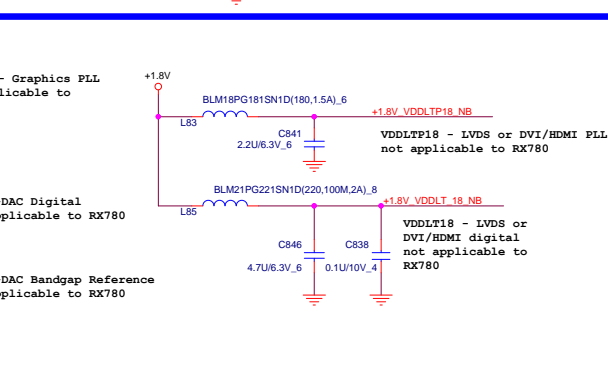
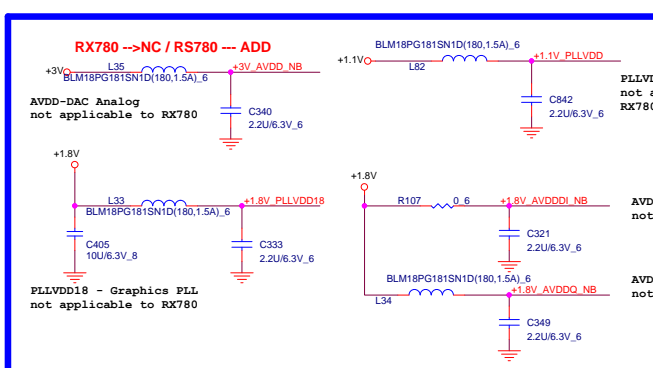
selects Loading of straps from EPROM
 1 : use default vaule , default
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RX780 --RS780_AUX_CAL
 RS780 -- SUS_ATAT

Enables Debug Bus access through memory T/O pads and GPIO.
 0 : Enable RS780 , Default
 1 : Disable RS780 (RS780 use VSYNCH#)

Indicates if memory Side port is available or not
 0 : available RS780 , Default
 1 : Not available RS780 (RS780 use HSYNCH#)

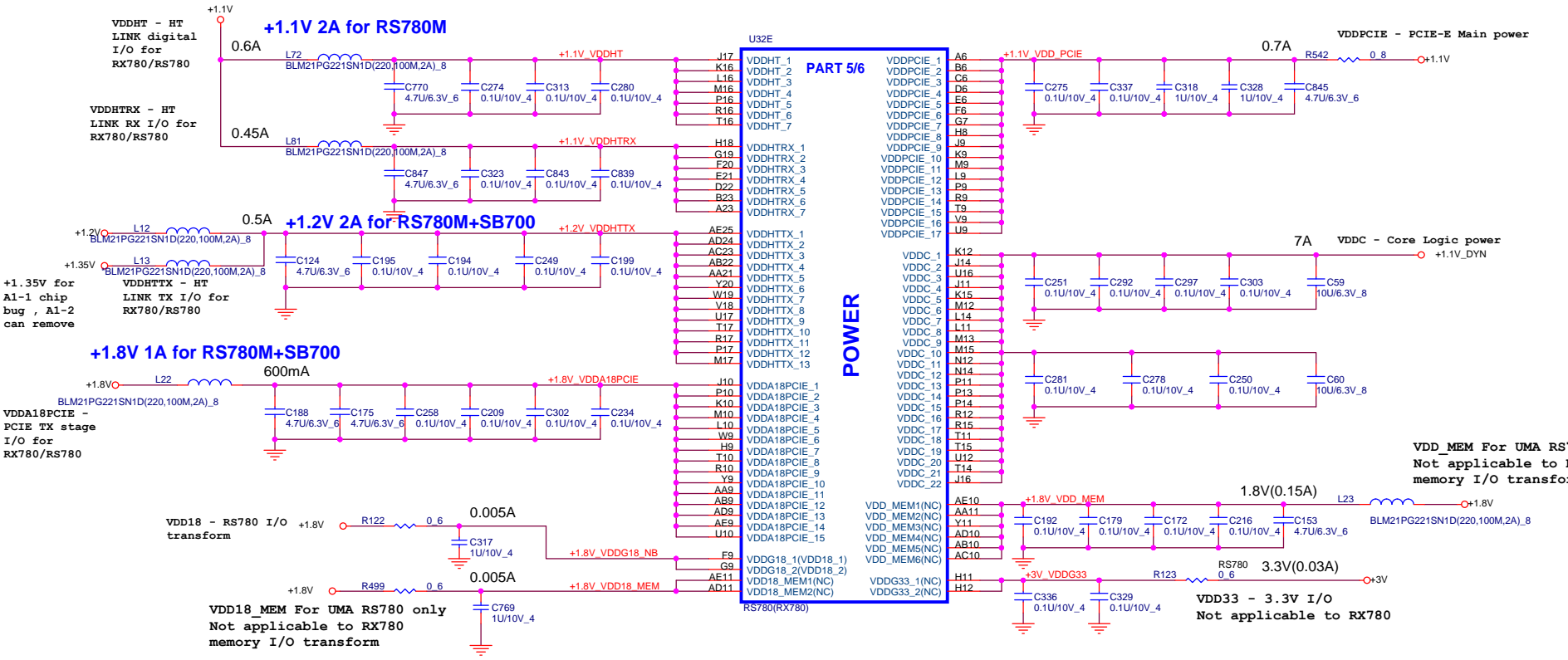
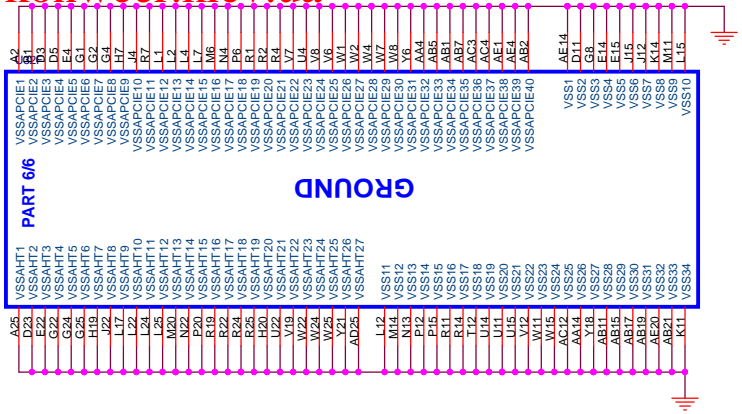
For external EEPROM Debug only

Enables Debug Bus access through memory T/O pads and GPIO.
 1 : Enable RX780 , Default
 0 : Disable RX780



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL33	NC	NC

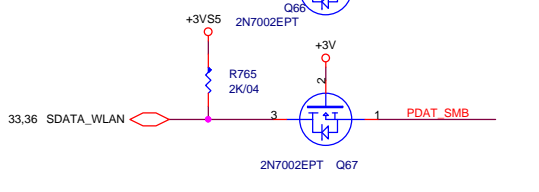
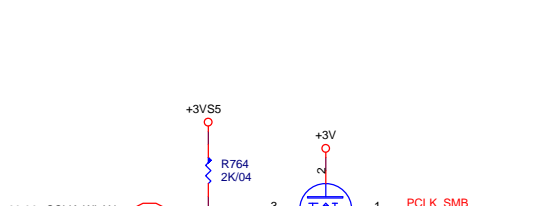
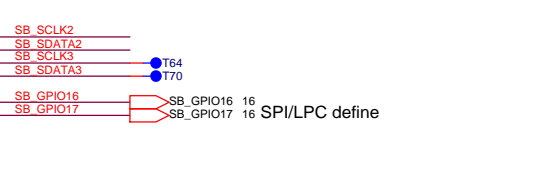
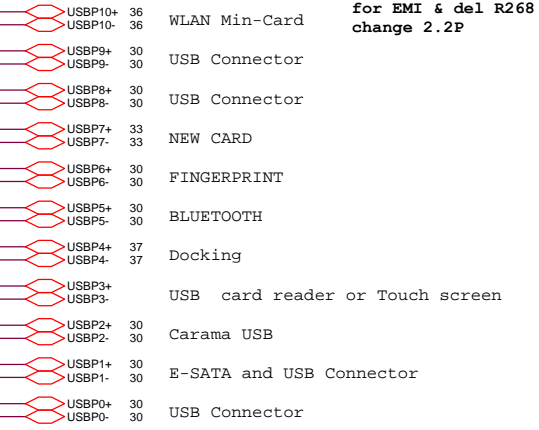
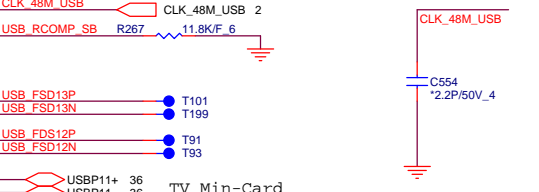
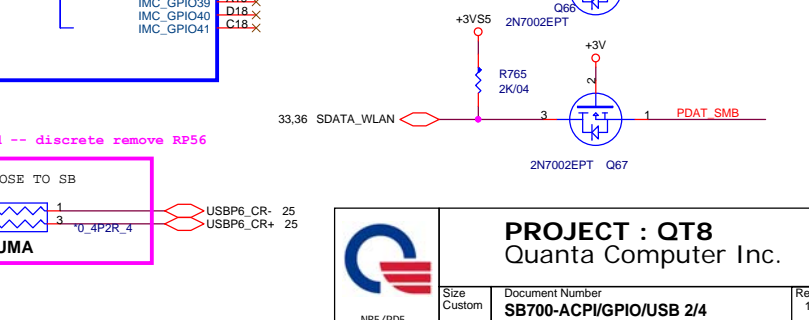
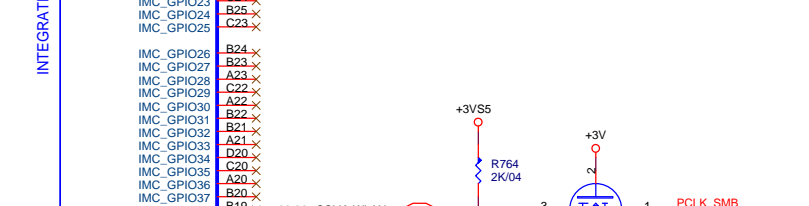
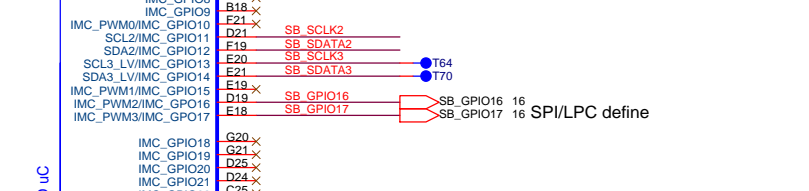
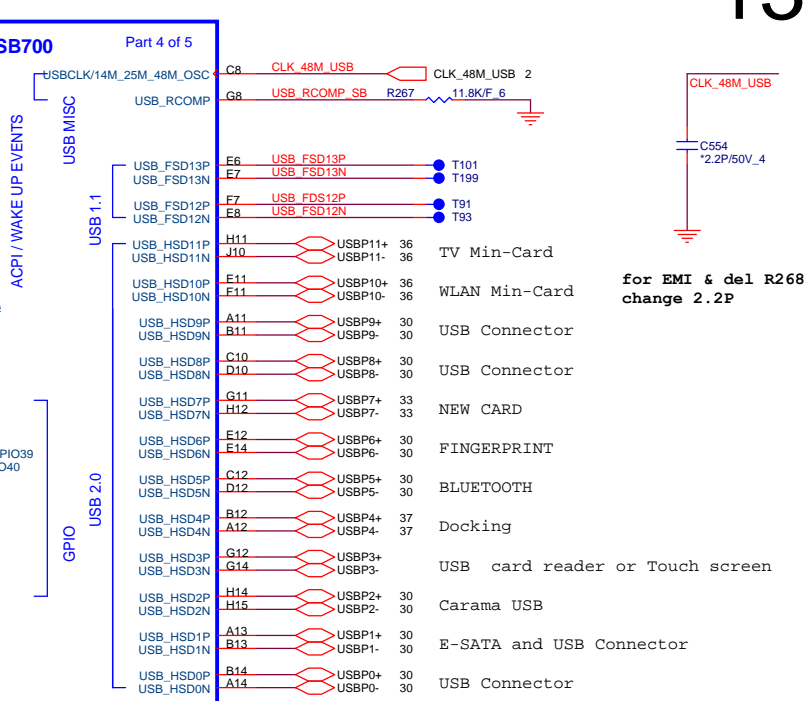
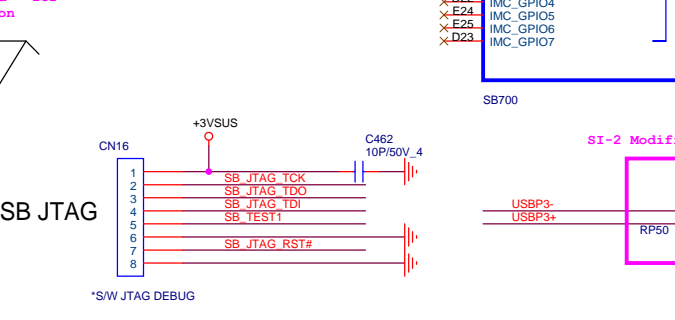
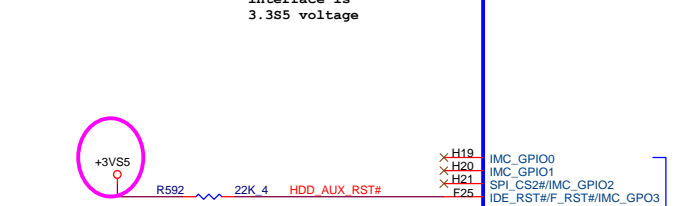
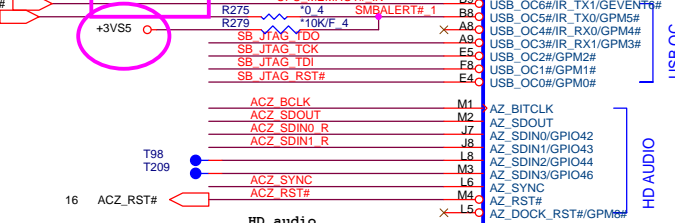
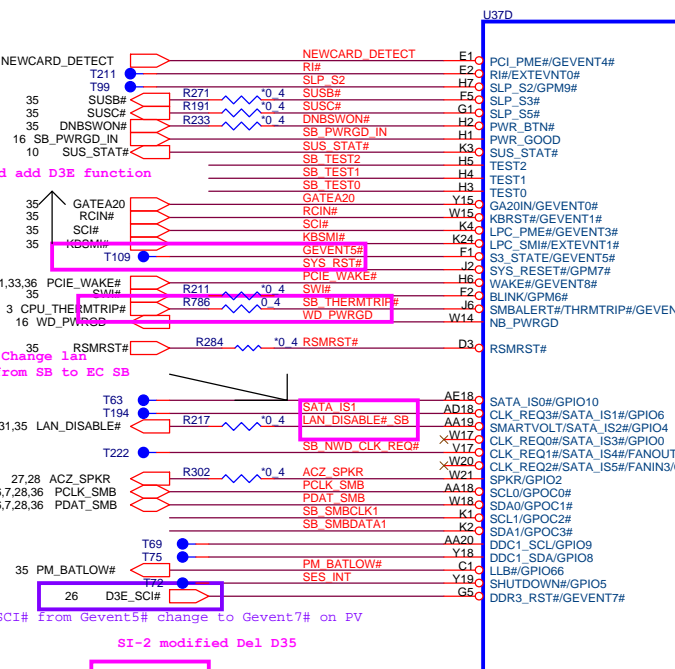
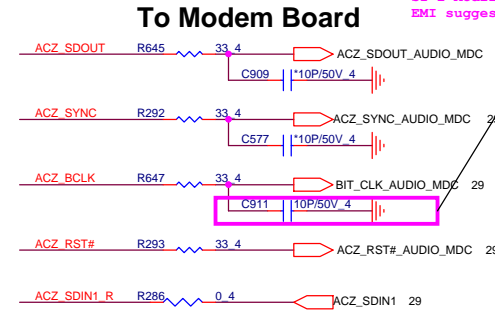
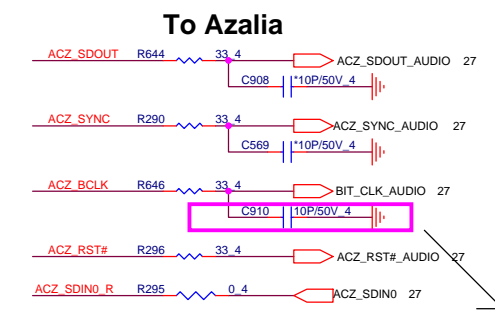
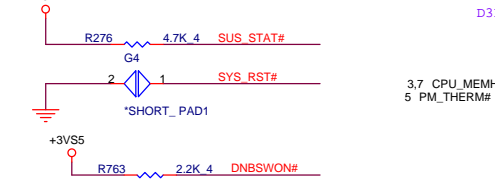
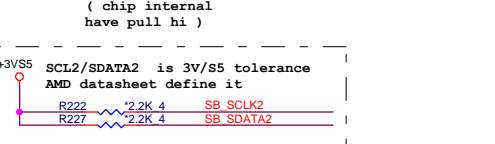
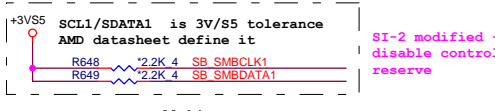
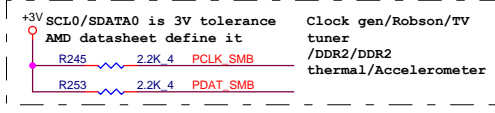
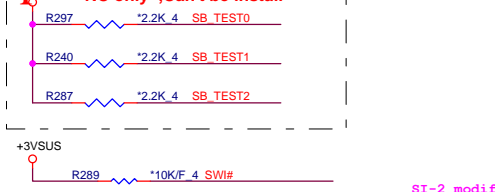


VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

VDD33 - 3.3V I/O
Not applicable to RX780



PROJECT : QT8
Quanta Computer Inc.



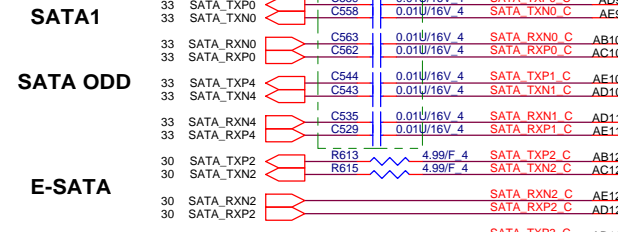
PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number
SB700-ACPI/GPIO/USB 2/4 Rev 1A

Date: Tuesday, February 19, 2008 Sheet 13 of 45

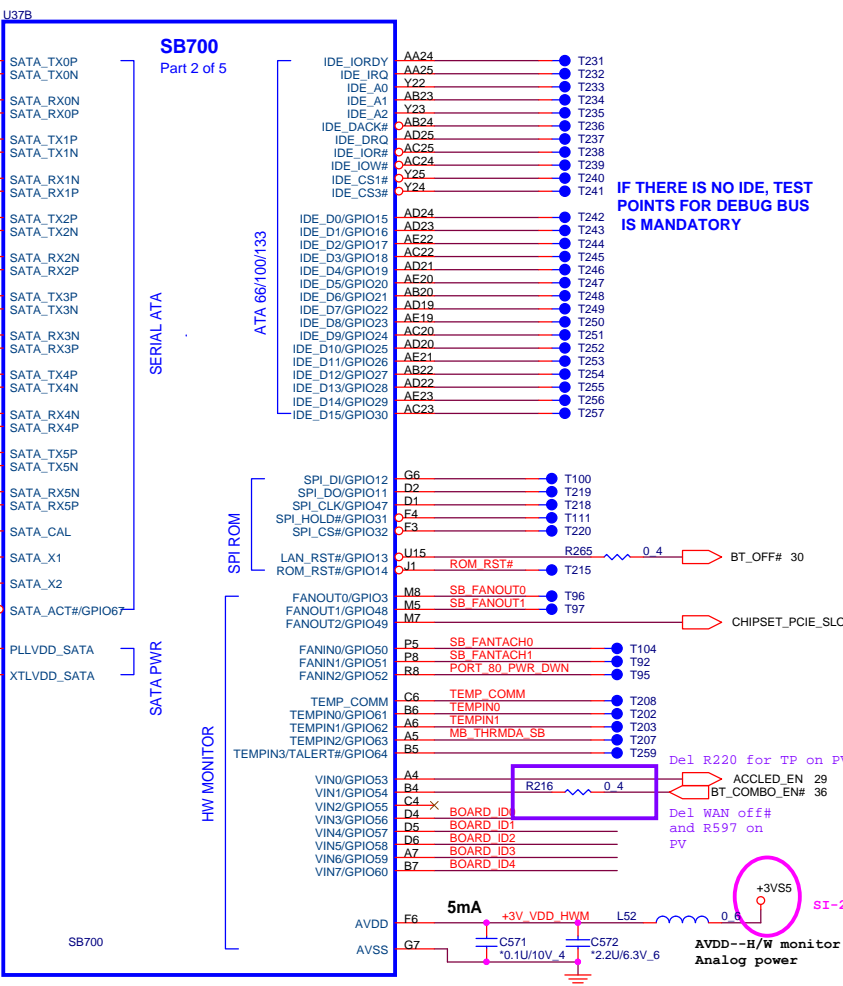
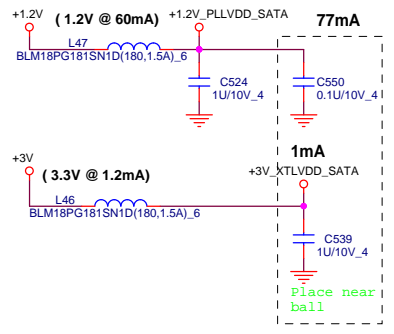
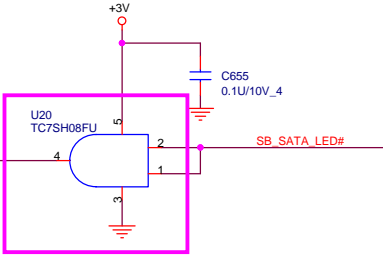
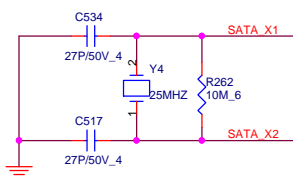
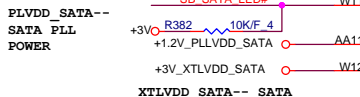
SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB600



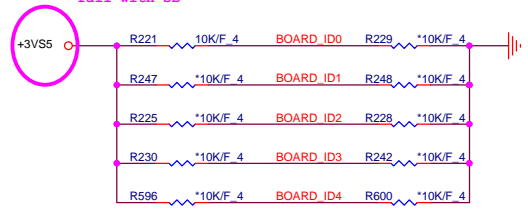
SATA PORT 4,5 are only support IDE mode

NOTE:
R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK



IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SI-2 modified -- SB internal pull Hi to 3V5S, modified to same power rail with SB



Del R220 for TP on PV

Del WAN off# and R597 on PV

SI-2 modified -- for fix +3V power leakage in S5 mode

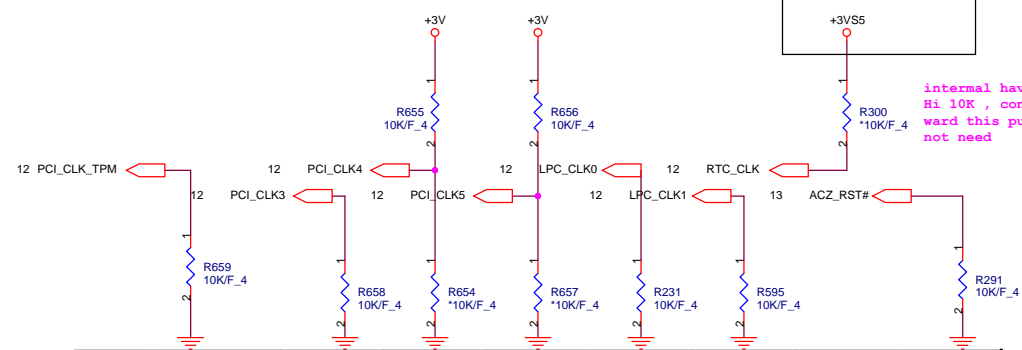
ID4	ID3	ID2	ID1	ID0	
X	X	X	0	0	UMA
X	X	X	0	1	discrete
X	X	X	X	X	
X	X	X	X	X	



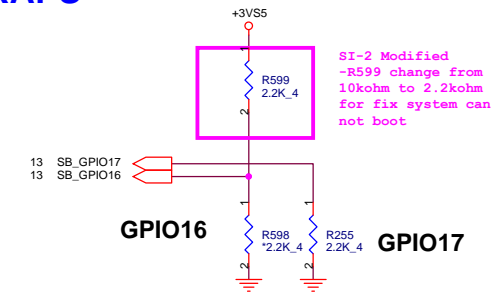
PROJECT : QT8
Quanta Computer Inc.

It must ready refore RSMRST#

REQUIRED STRAPS



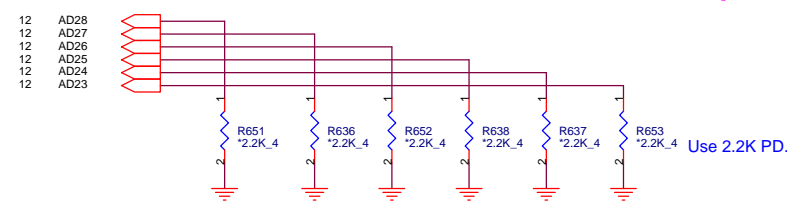
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

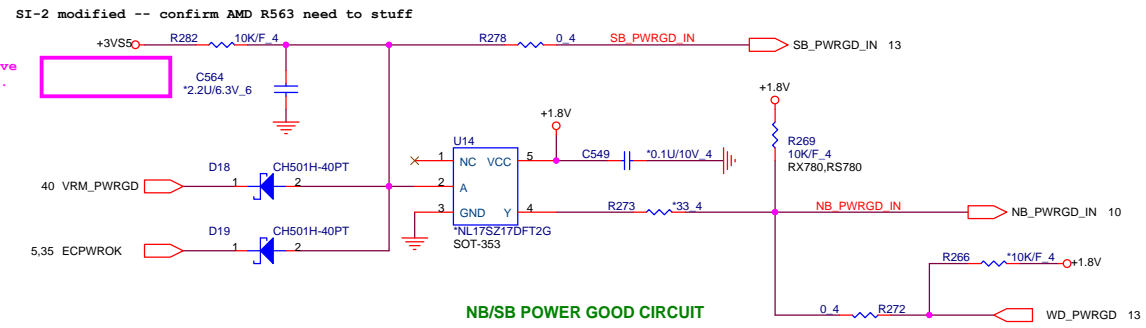
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

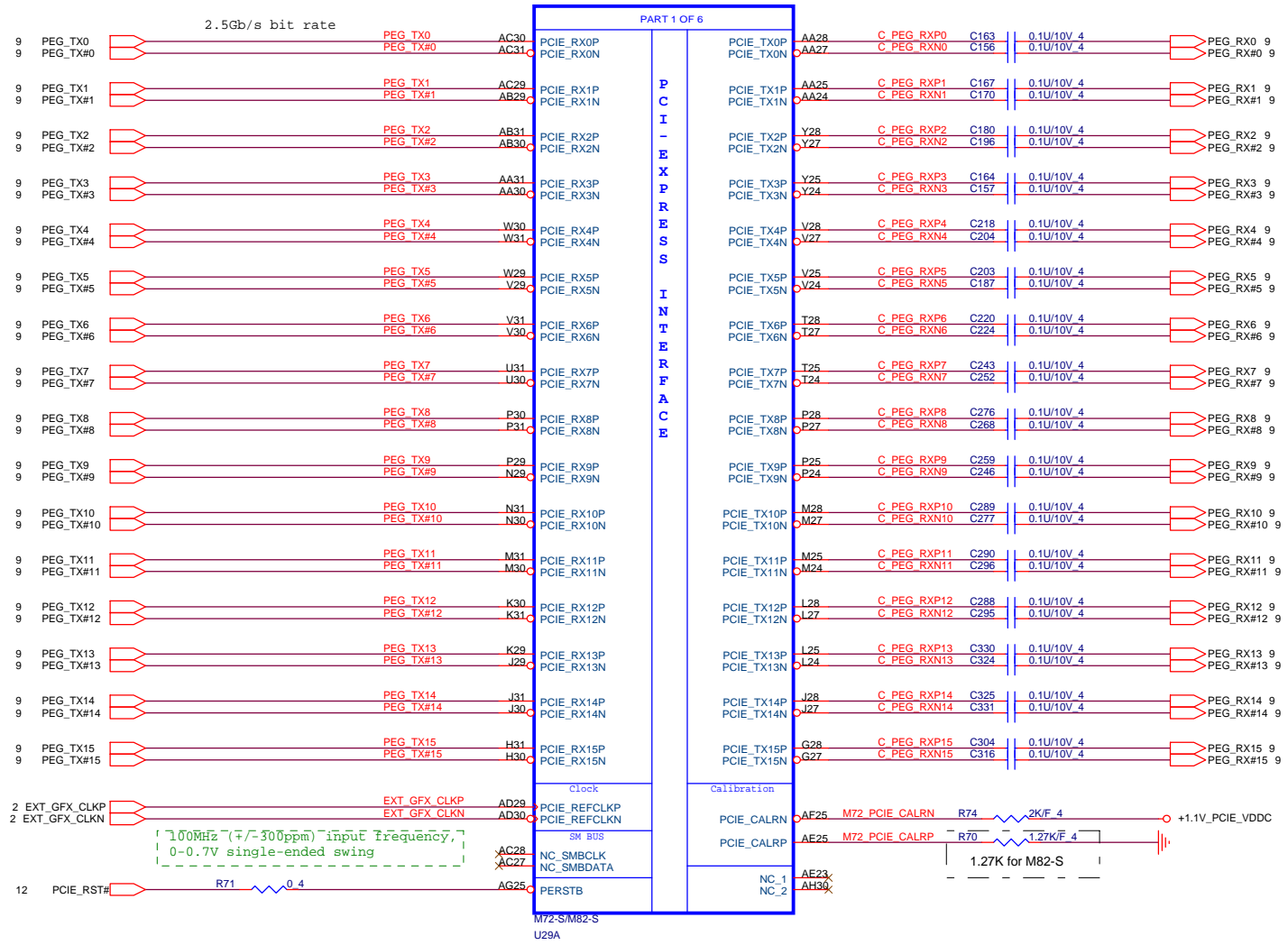


- AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
- ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

PROJECT : QT8
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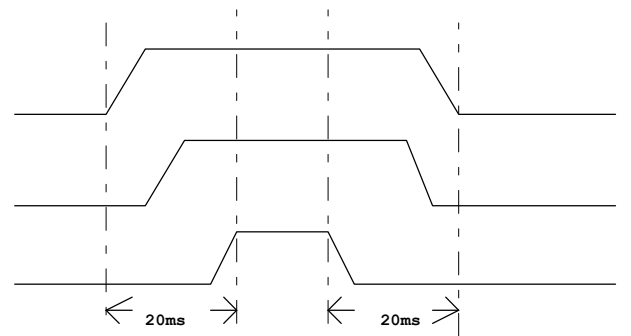
Size Custom Document Number **SB700-STRAPS** Rev 1A
Date: Tuesday, February 19, 2008 Sheet 16 of 45

IC CTRL (632P) 216-0707001-00 (BGA)
VGA P/N : AJ070700T00

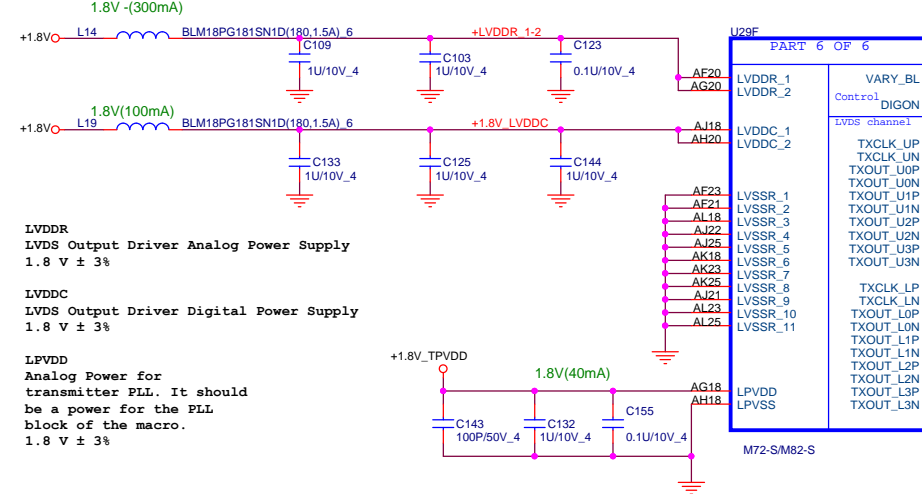
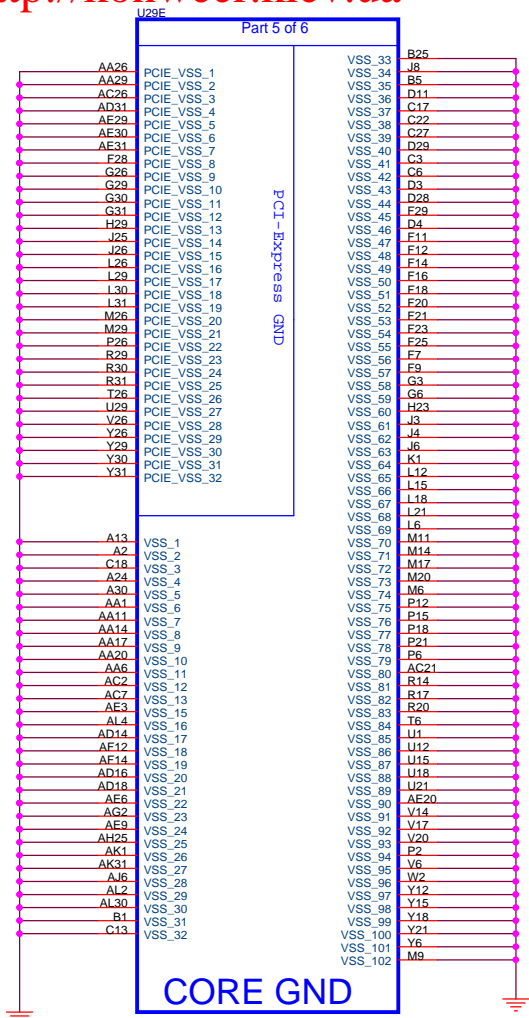


POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_COREB=1.0~1.1V - M62S,M71S
0.95~1.1V - M72S

VGA Core BPP
VGA Core VDDC
+1.8V PCIE_VDDR
+1.8V PCIE_PVDD
+1.8V VDDR1
3.3V_Delay VDDR3



PROJECT : QT8
Quantia Computer Inc.



LVDDR
LVDS Output Driver Analog Power Supply
1.8 V ± 3%

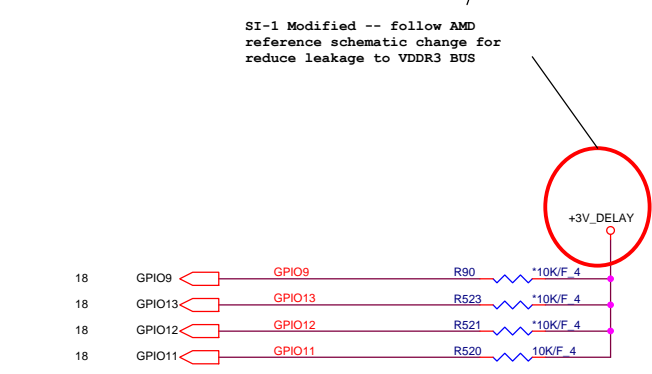
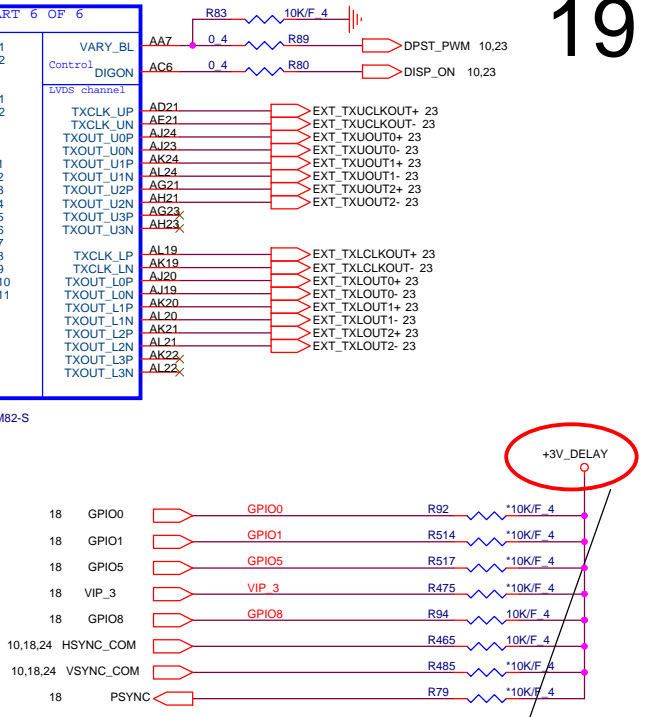
LVDDC
LVDS Output Driver Digital Power Supply
1.8 V ± 3%

LPVDD
Analog Power for transmitter PLL. It should be a power for the PLL block of the macro.
1.8 V ± 3%

CONFIGURATION STRAPS		
PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-S
GPIO0	PCIE FULL TX OUTPUT SWING	0
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
GPIO5	Allows either PCIe 2.5GT/s or 5GT/s operation	REV
VIP3	ENABLE HD AUDIO (M8X-M)	1
GPIO8	ENABLE HD AUDIO (M82-S)	1
HSYNC	ENABLED HDMI	1

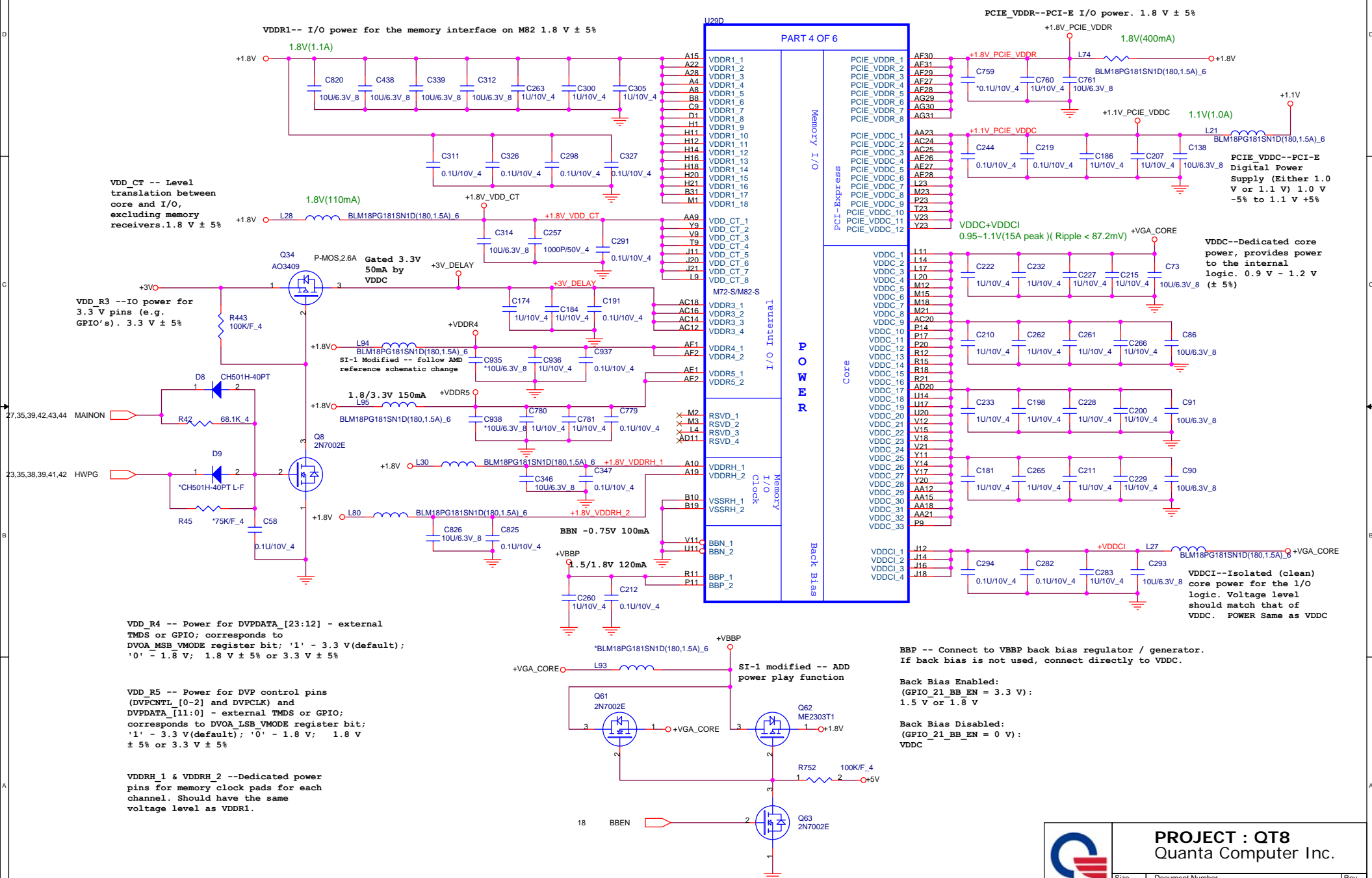
Memory Aperture size				
GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0	
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

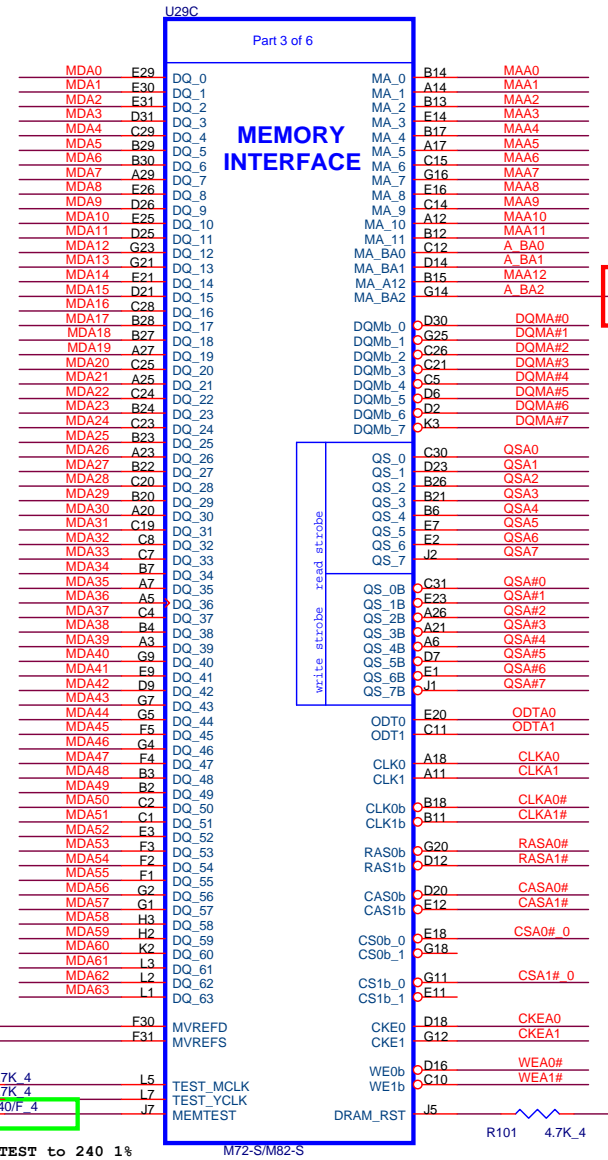
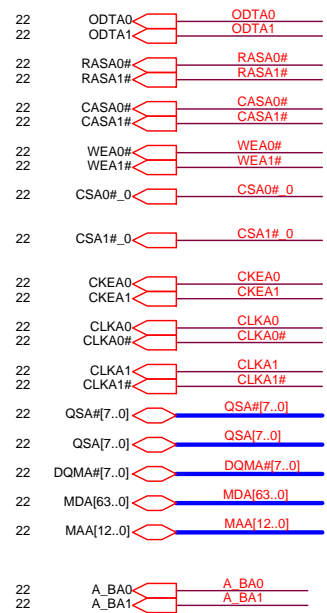
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



PROJECT : QT8
Quantas Computer Inc.

Size Custom	Document Number M7X/M8X_GND / LVDS/ Straps	Rev 1A
Date: Tuesday, February 19, 2008 Sheet 19 of 45		

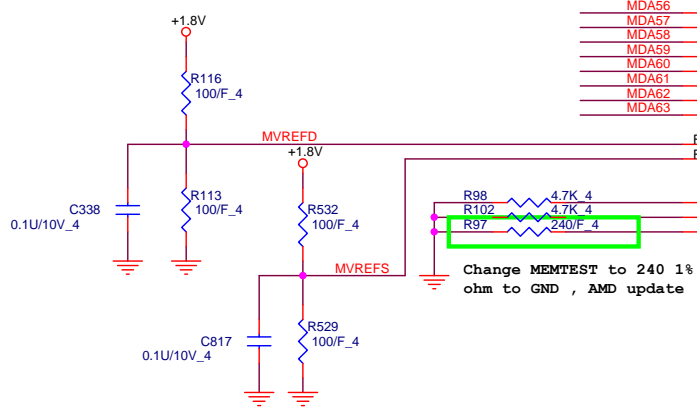




MEMORY INTERFACE

A_BA2 22

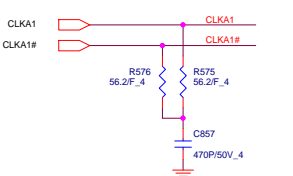
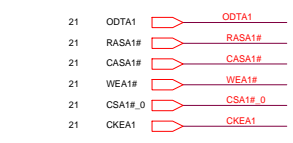
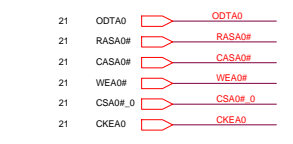
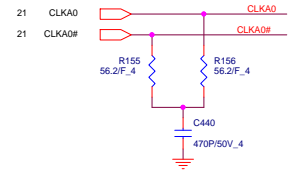
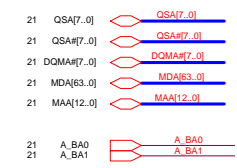
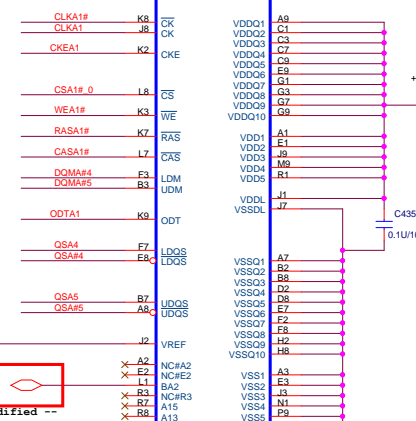
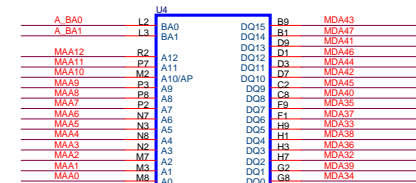
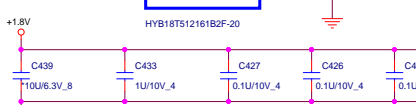
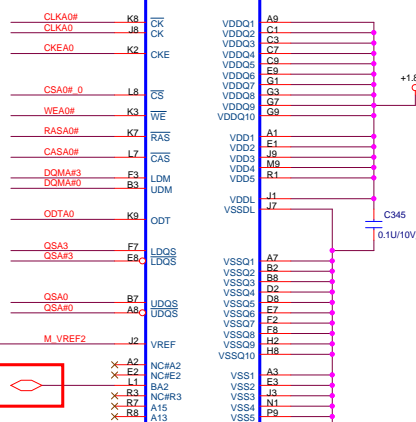
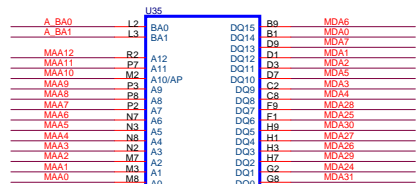
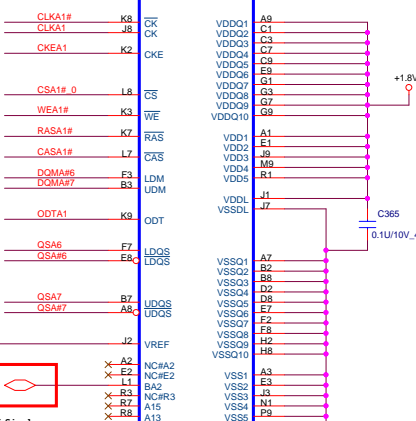
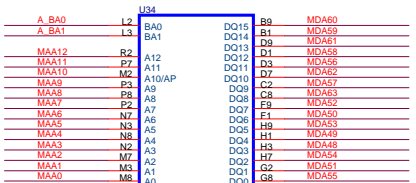
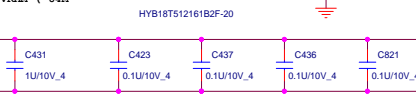
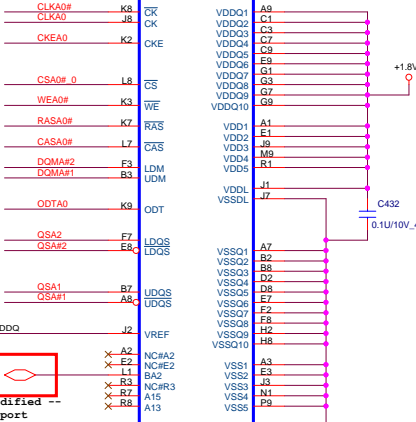
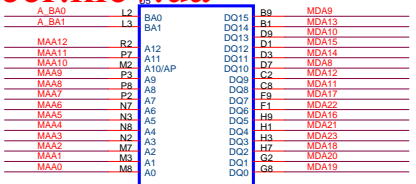
SI-1 modified --
for support
1Gbit VRAM (64M
x 16)



PROJECT : QT8
Quanta Computer Inc.

Size B	Document Number M7X/M8X/MEM_Interface	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 21	of 45

DDR2 BGA MEMORY

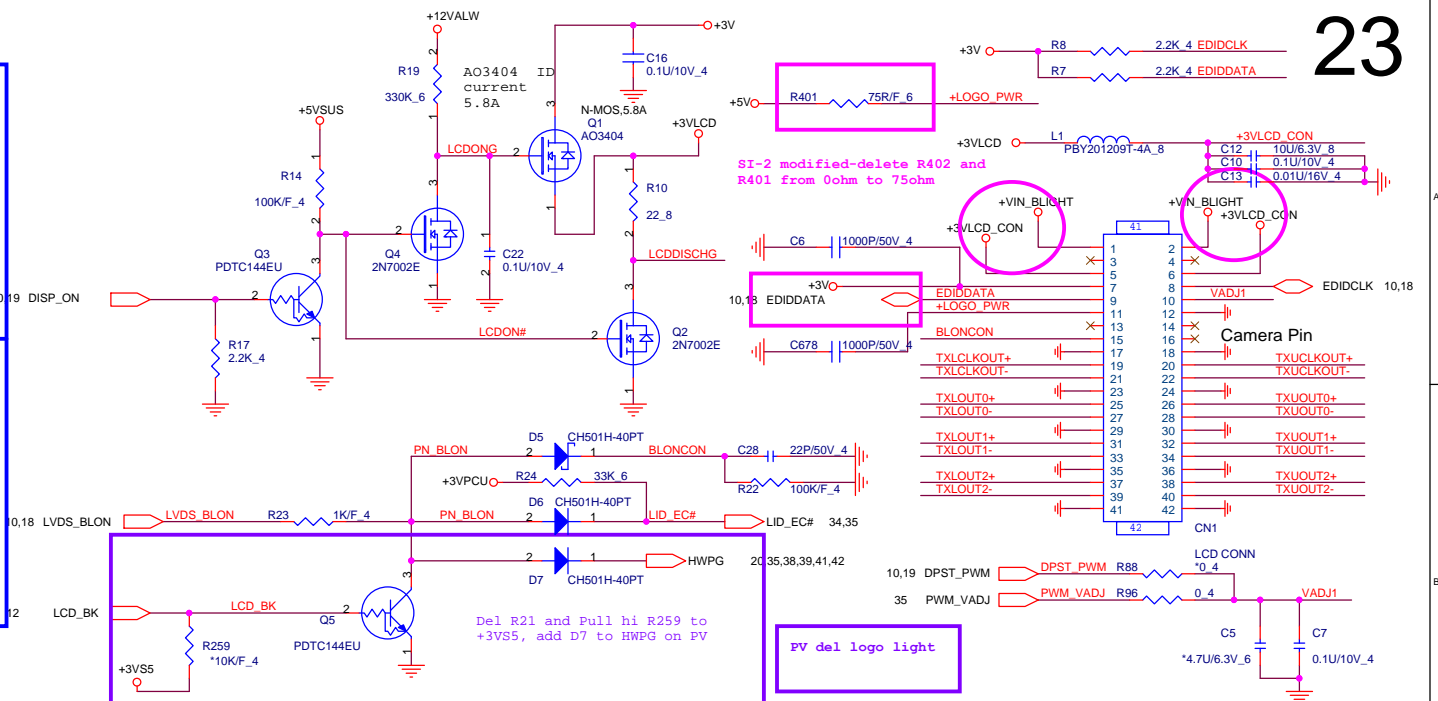
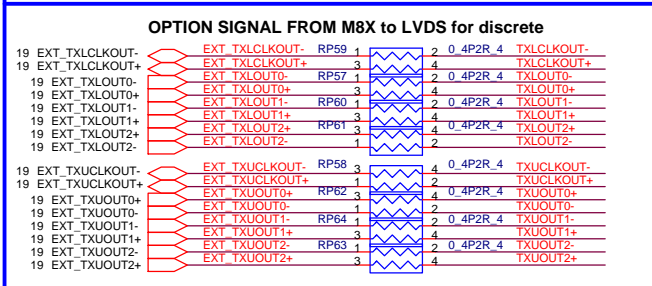
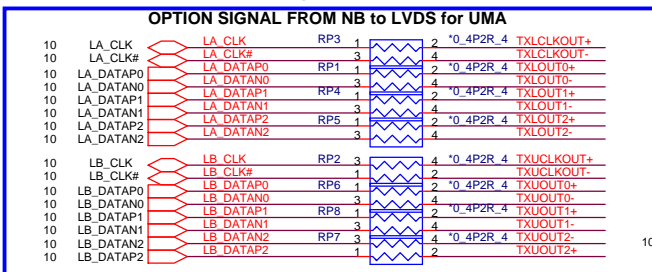


DDR2 BGA MEMORY

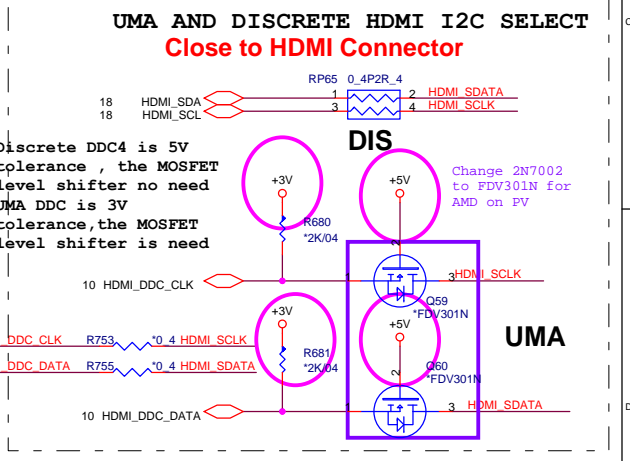
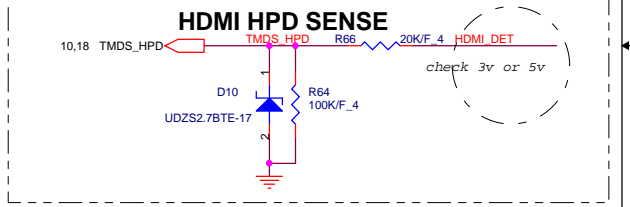
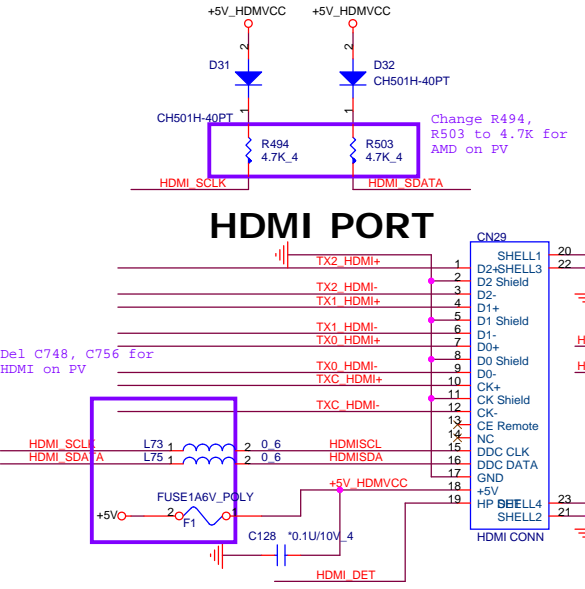
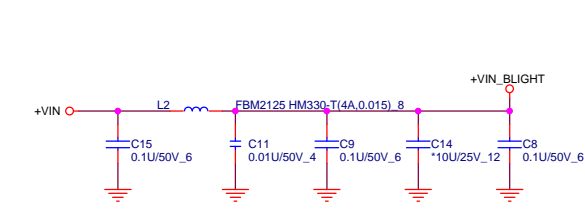
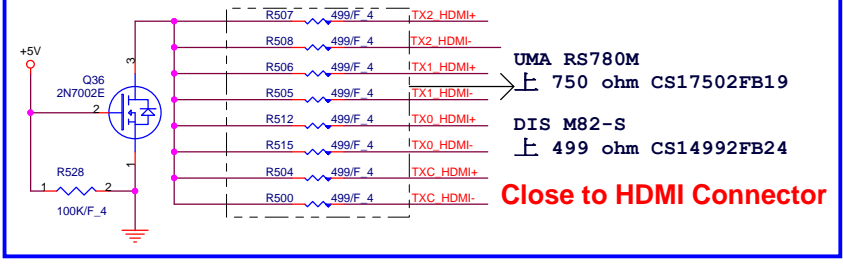
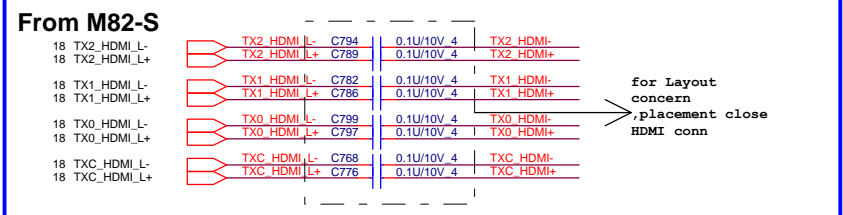
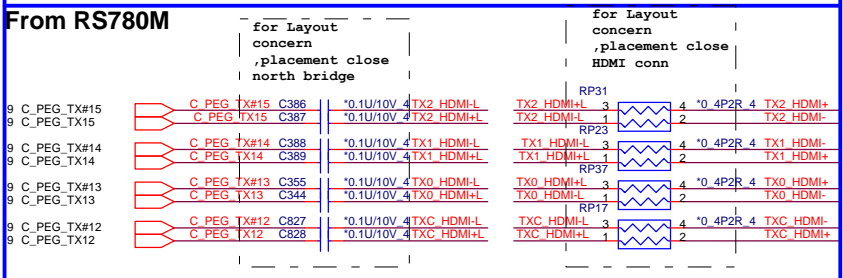
PROJECT : QT8
Quanta Computer Inc.

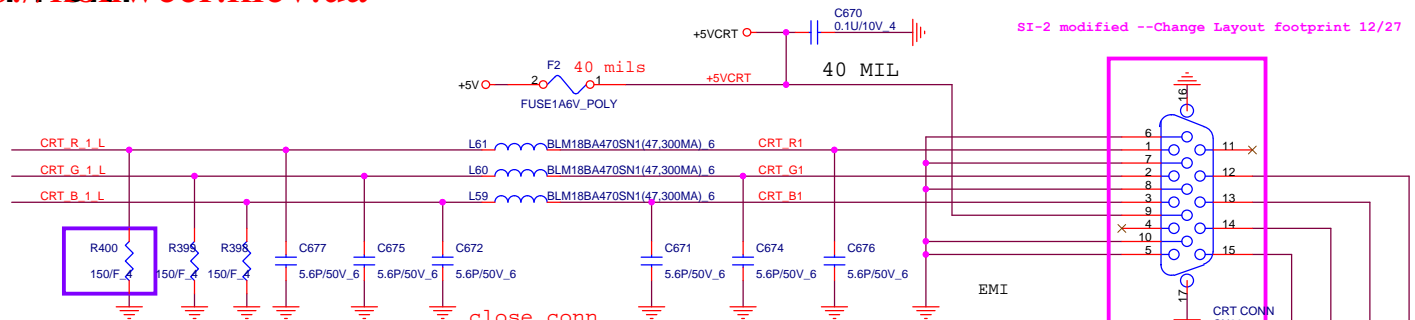
Size C	Document Number M7X/M8X/VRAM_A0,A1	Rev 1A
Date: Tuesday, February 19, 2008 Sheet 22 of 45		

1. If LCD connector near N/B, then place the series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B



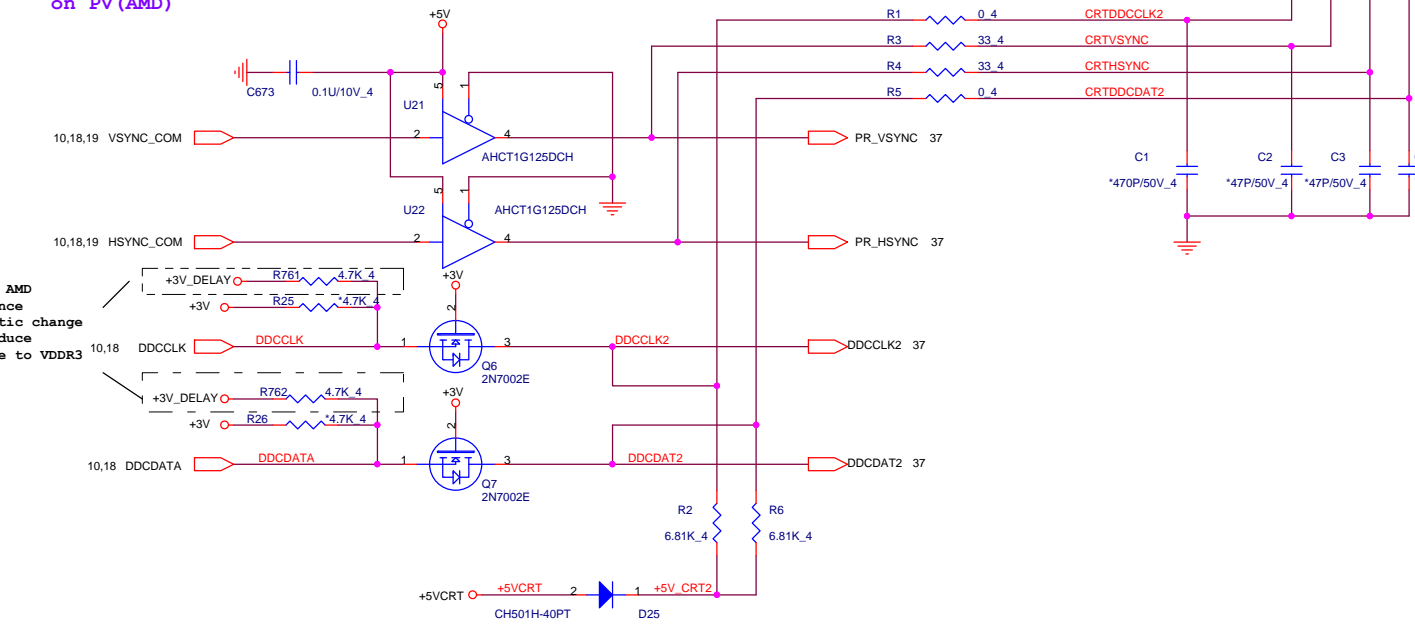
UMA/DISCRETE select for HDMI



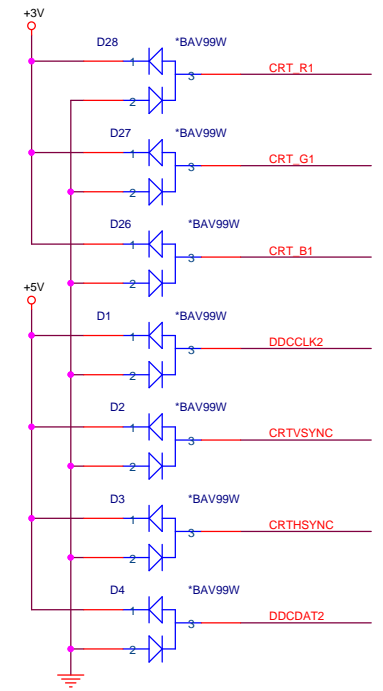


R400 for UAM use 140 ohm on PV (AMD)

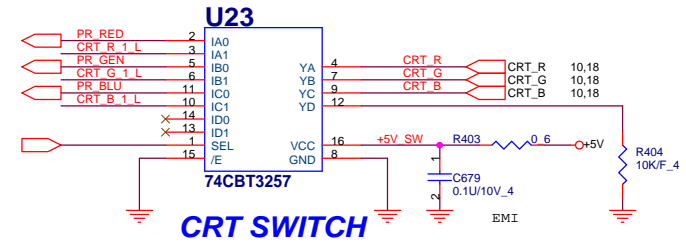
close conn within 600mils



Follow AMD reference schematic change for reduce leakage to VDDR3 BUS



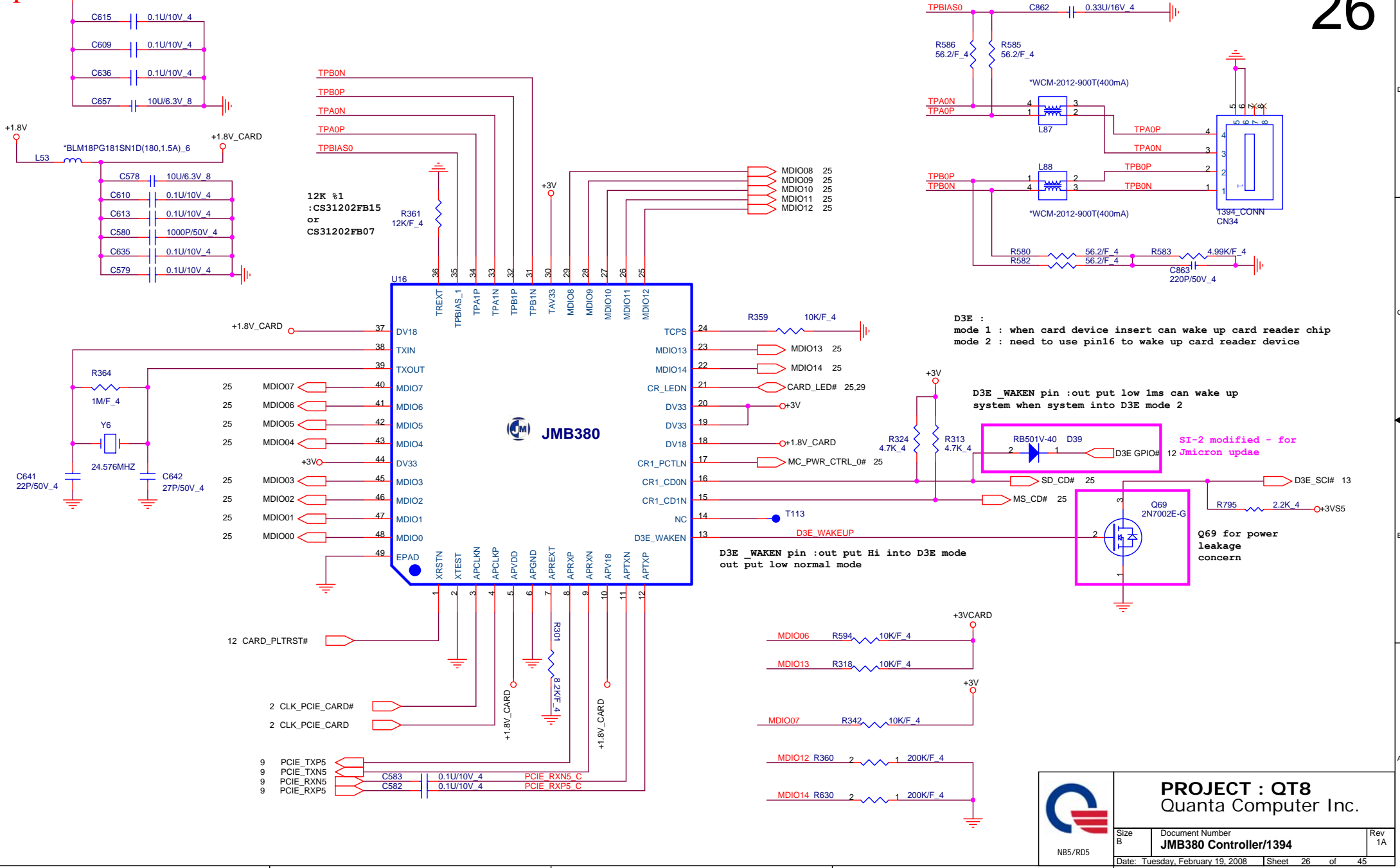
- 37 PR_RED
- 37 PR_GEN
- 37 PR_BLU
- 35,37 PR_INSERT#




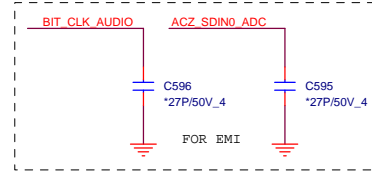
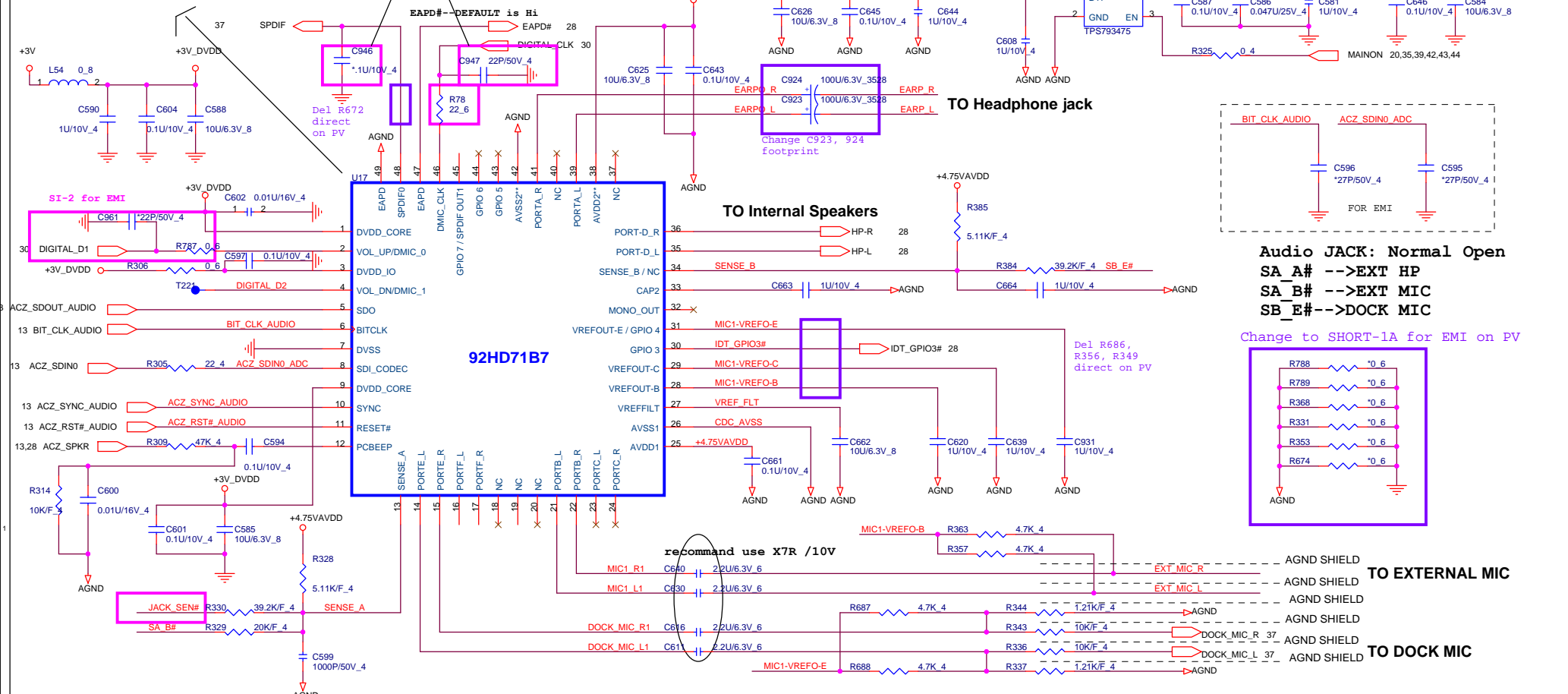
inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect



PROJECT : QT8
Quanta Computer Inc.

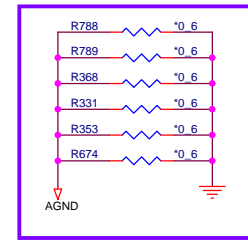


		PROJECT : QT8	
		Quanta Computer Inc.	
Size B	Document Number	Rev 1A	
	JMB380 Controller/1394		
Date: Tuesday, February 19, 2008	Sheet 26	of 45	



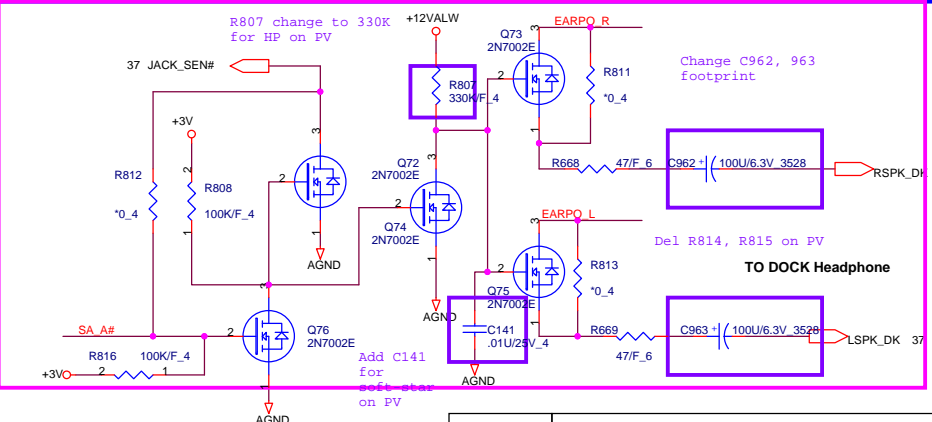
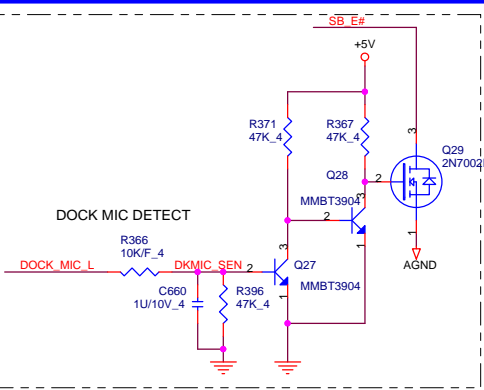
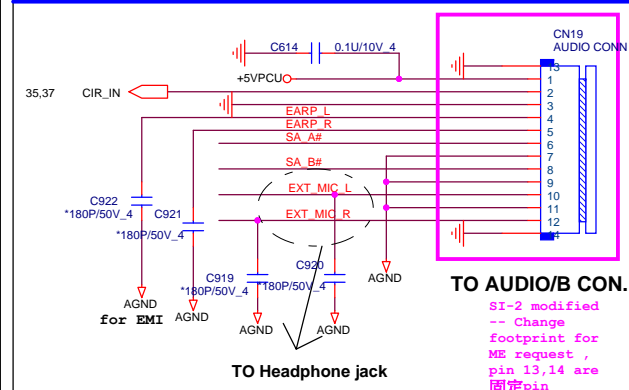
Audio JACK: Normal Open
 SA_A# -->EXT HP
 SA_B# -->EXOT MIC
 SB_E#-->DOCK MIC

Change to SHORT-1A for EMI on PV



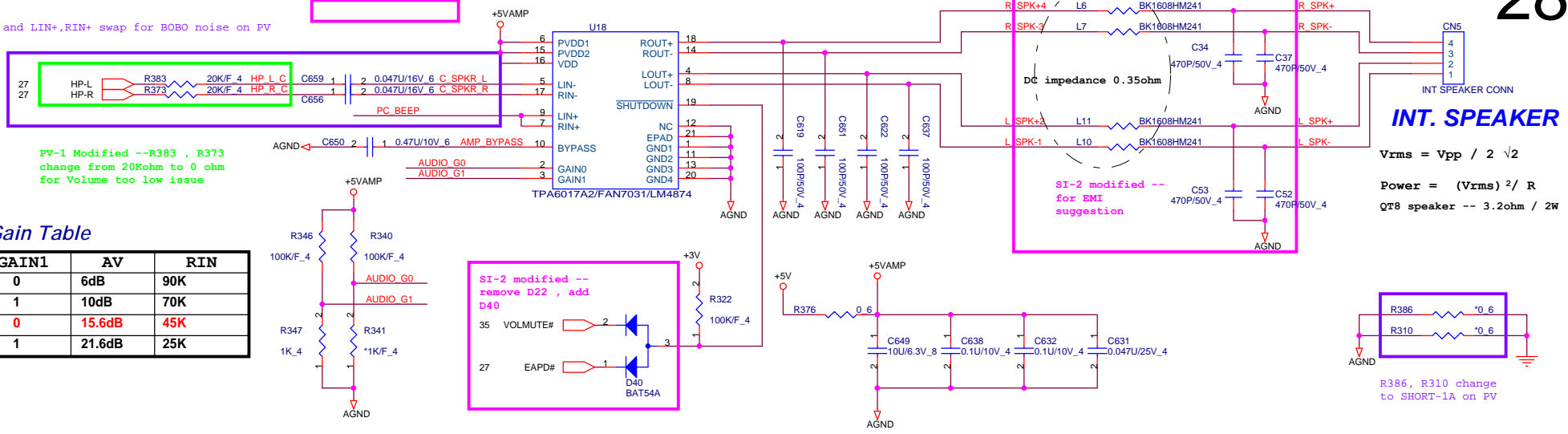
TO EXTERNAL MIC

TO DOCK MIC



SI-2 Modified -- remove C621/C623

LIN-, RIN- and LIN+, RIN+ swap for BOBO noise on PV

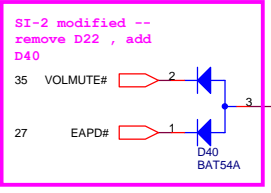


INT. SPEAKER

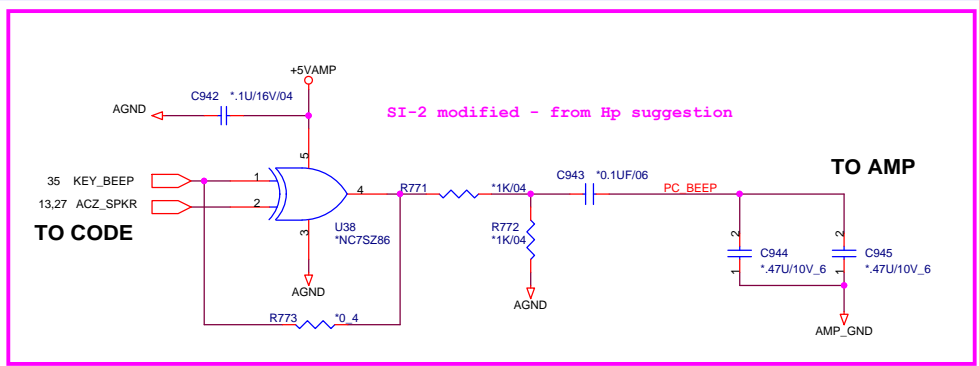
$V_{rms} = V_{pp} / 2 \sqrt{2}$
 $Power = (V_{rms})^2 / R$
 QT8 speaker -- 3.2ohm / 2W

6017A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

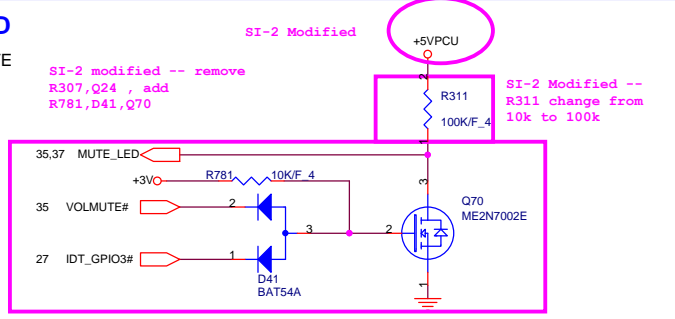


PC-BEEP

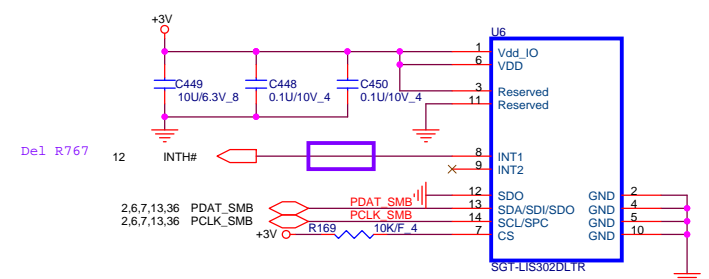


MUTE_LED

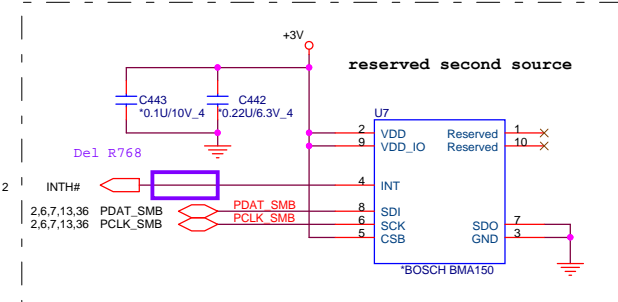
Low --> un-MUTE
 High --> Mute



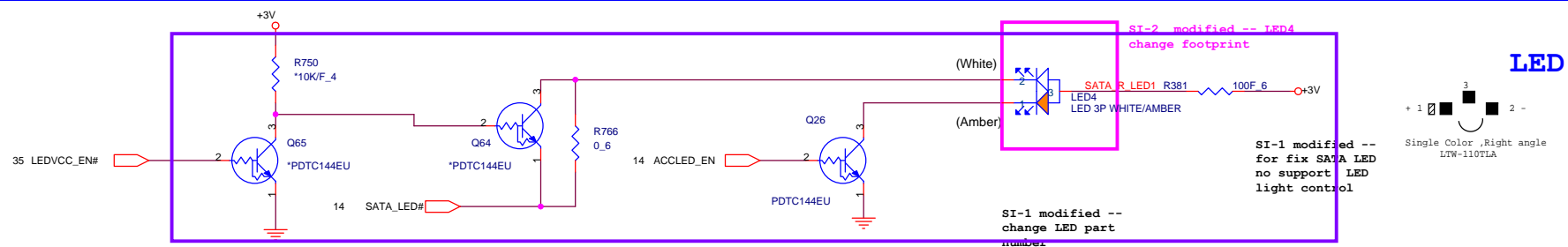
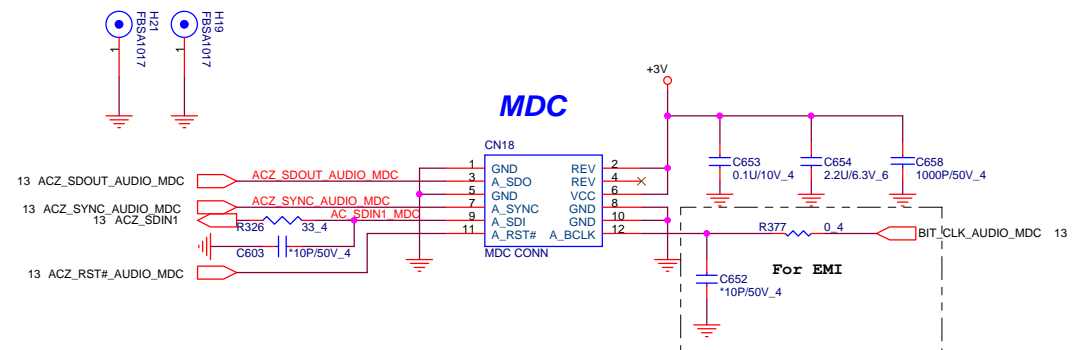
Acceleration sensor



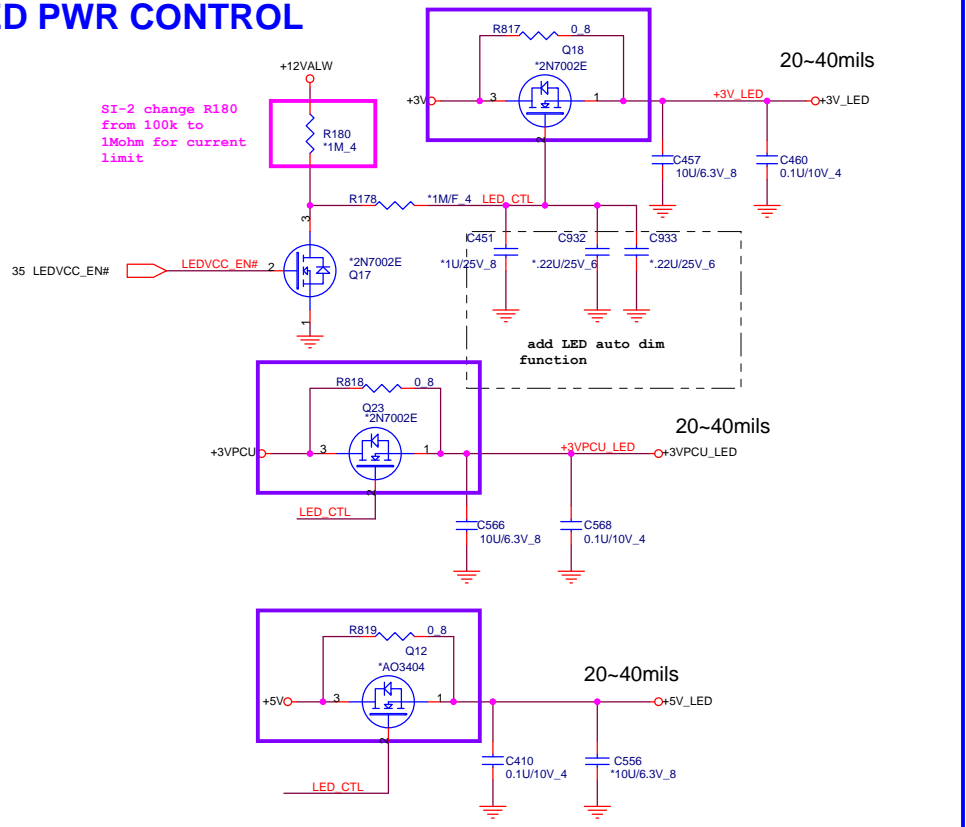
SGT-LIS302DLTR interrupt pin default is low / active Hi, BIOS need to programming 22h to change status from active Hi to low



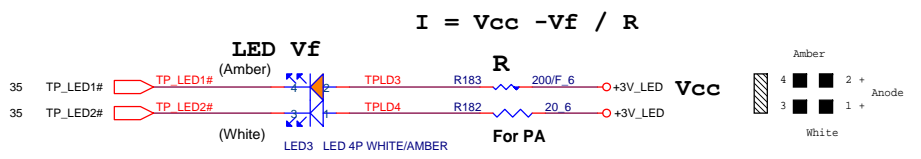
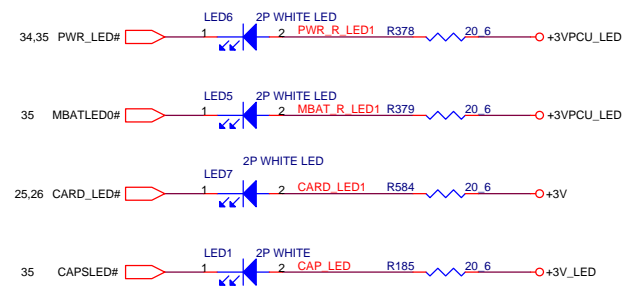
PROJECT : QT8
 Quanta Computer Inc.

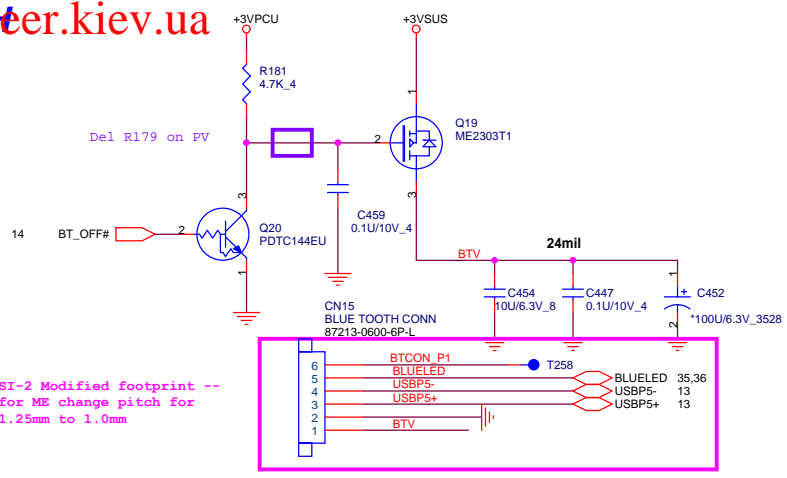


LED PWR CONTROL



Del R380
Change R381 to 100
Add R766, R817, R818,
R819
LED PWR control no-stuff
on PV



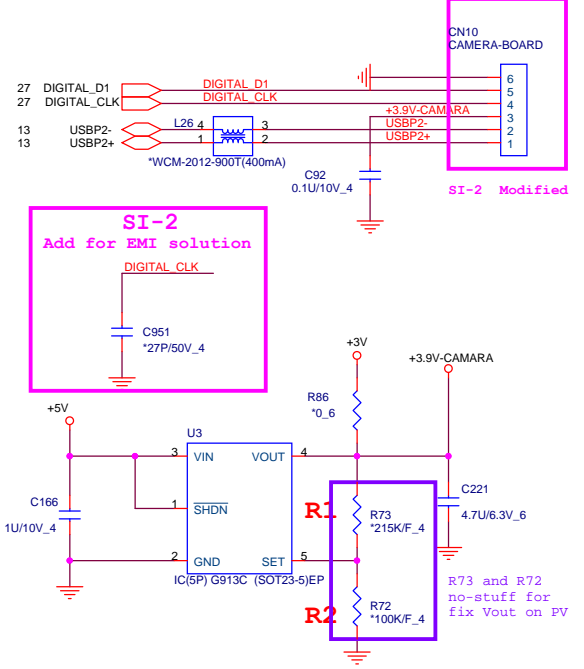


SI-2 Modified footprint -- for ME change pitch for 1.25mm to 1.0mm

For Discrete Touch-Screen



USB CAMERA CONNECT

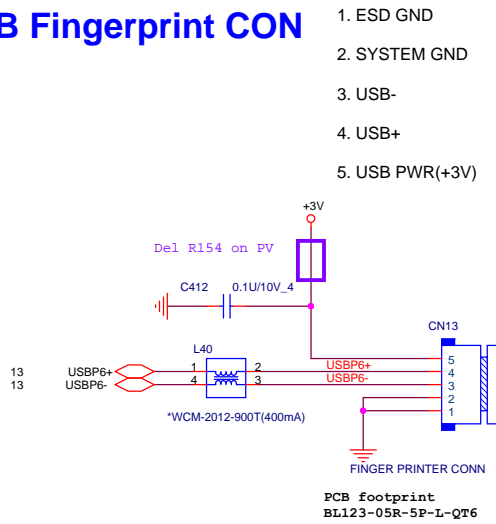


SI-2 Add for EMI solution
DIGITAL_CLK
C951 *27P/50V_4

SI-2 Modified

$V_{out} = 1.25 (1 + R1/R2)$

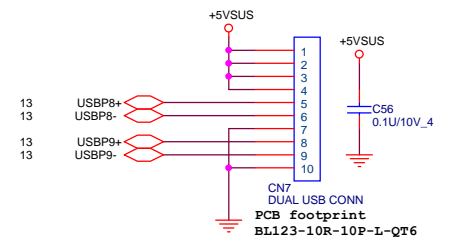
USB Fingerprint CON



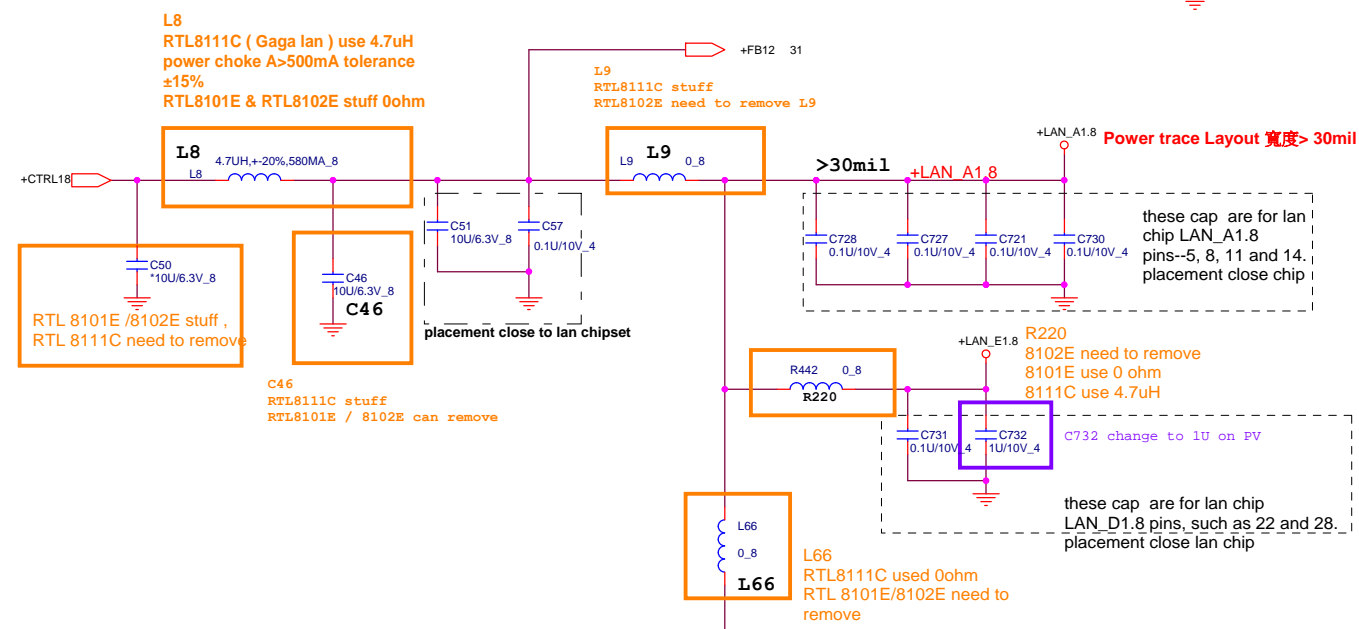
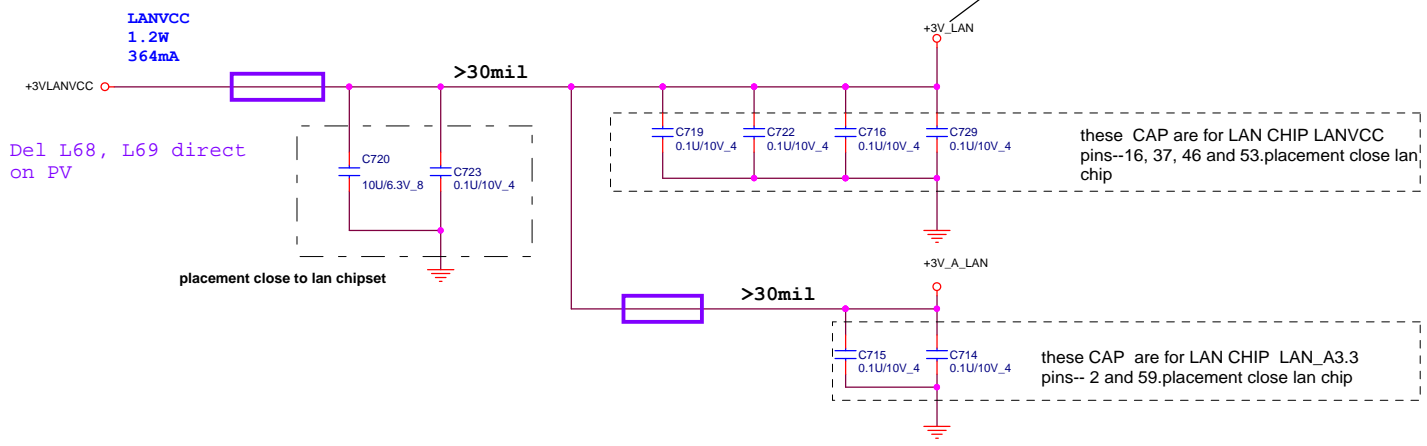
1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

PCB footprint BL123-05R-5P-L-QT6

RIGHT SIDE USBX2

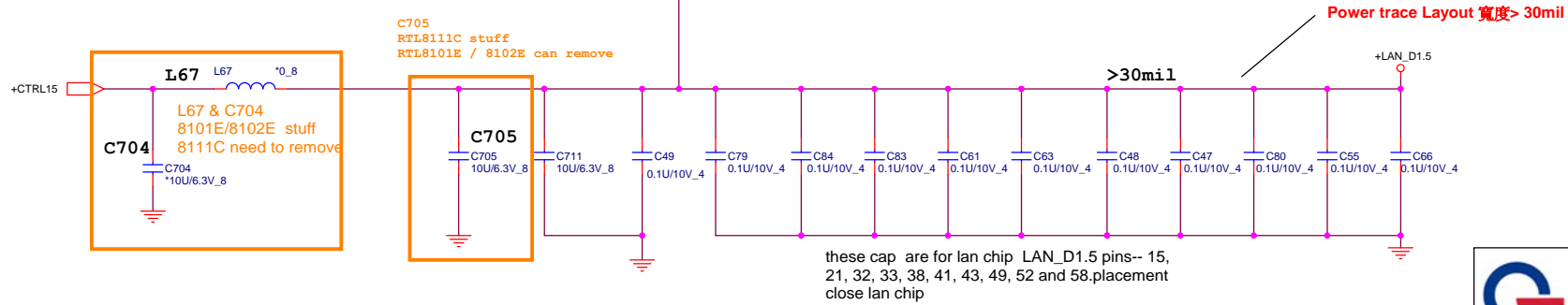


	<p>PROJECT : QT8 Quanta Computer Inc.</p>		
	<p>Size Custom</p>	<p>Document Number BT/WEBCAM/FT/USBX4/ESATA</p>	<p>Rev 1A</p>
<p>NBS/RD5</p>	<p>Date: Tuesday, February 19, 2008</p>	<p>Sheet 30 of 45</p>	



Power domain chart

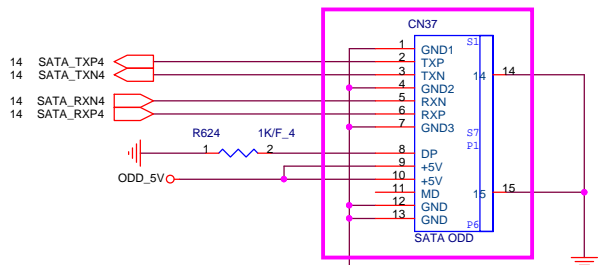
	RTL8111B / RTL8101E	RTL8111C RTL8102E
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V



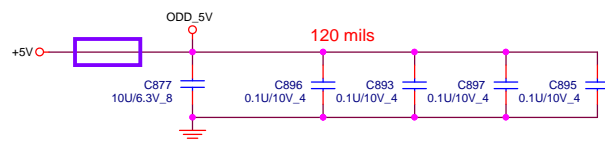
PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number LAN Power	Rev 1A
Date: Tuesday, February 19, 2008		Sheet 32 of 45

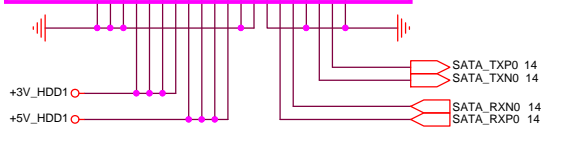
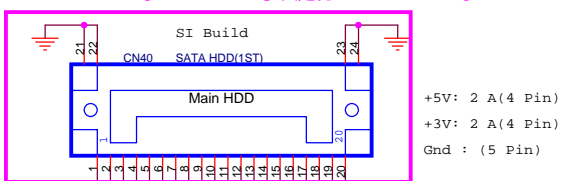
SI-2 Modified footprint -- Modify 12/27



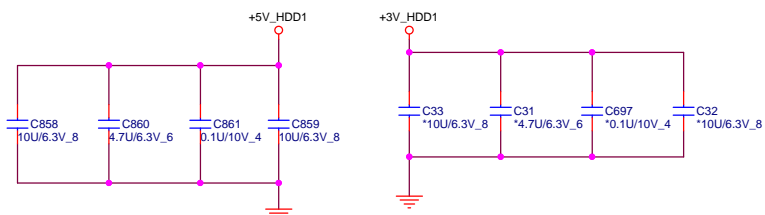
Del L90 direct on PV



SI-2 Modified footprint -- Modify 固定孔 Size as SMT request

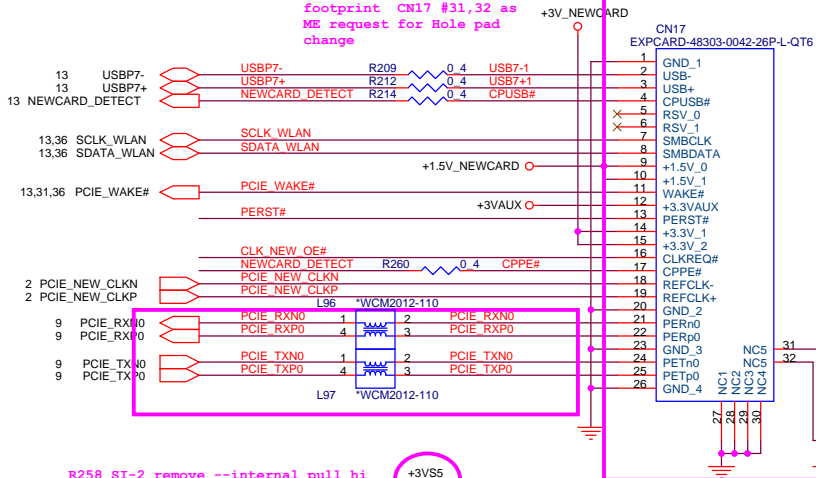


Del R578 direct on PV

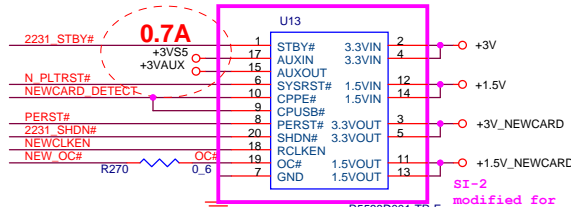


NEWCARD

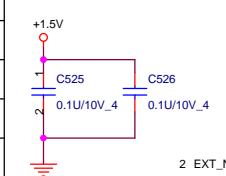
SI-1 modified -- change footprint CN17 #31,32 as ME request for Hole pad change



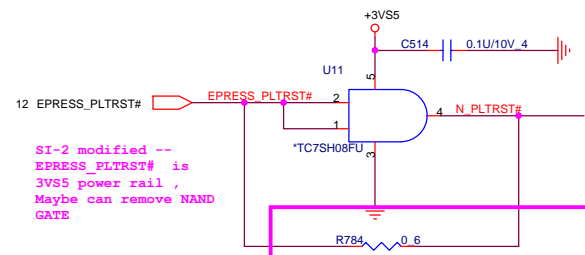
R258 SI-2 remove --internal pull hi



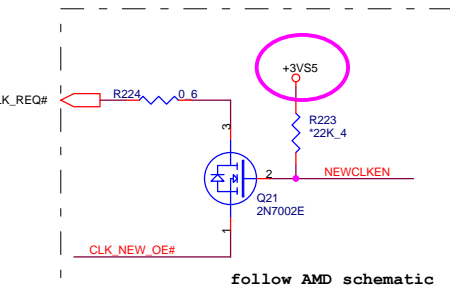
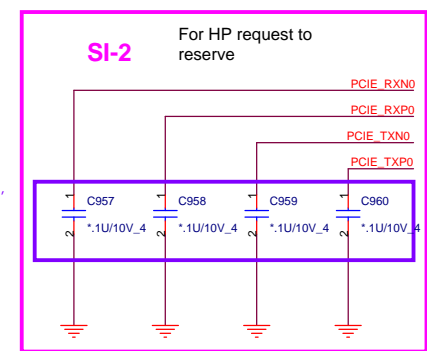
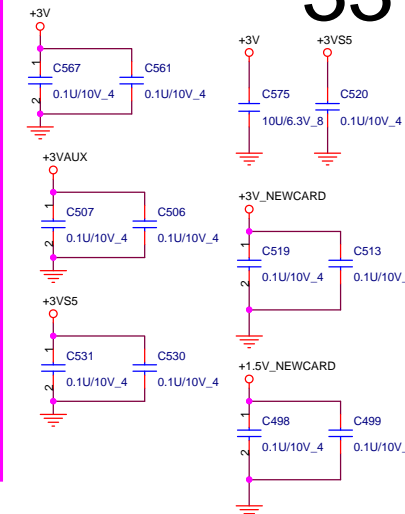
R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN



SI-2 modified -- EPRESS_PLTRST# is 3VS5 power rail, Maybe can remove NAND GATE



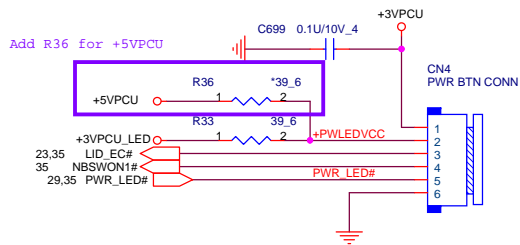
NEWCARD (PCIEXPRESS*1 + USB*1)



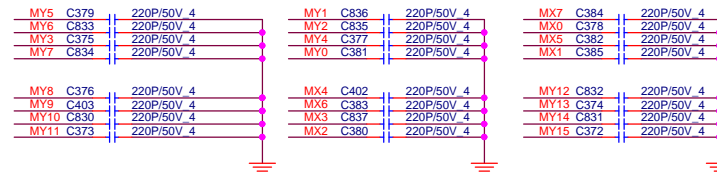
PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number NEW CARD/SATA ODD/SATA HDD	Rev 1A
Date: Tuesday, February 19, 2008 Sheet 33 of 45		

POWER BUTTON CONNECT

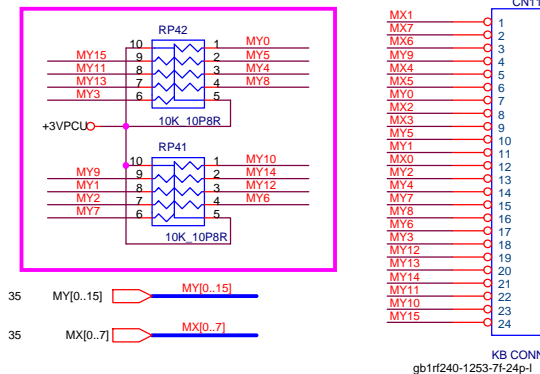


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND



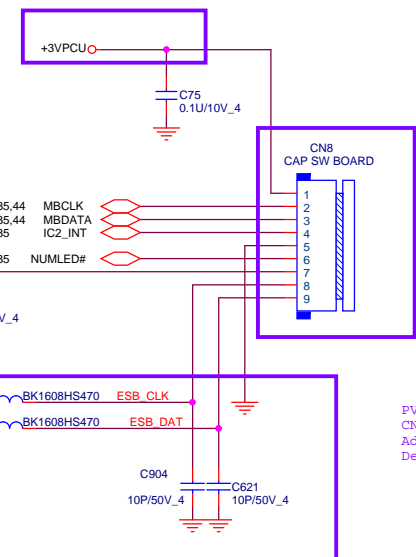
SI-2 Modified
-- net swap for
layout concern

KEYBOARD PULL-UP



KB CONN
gb1rf240-1253-7f-24p-1

CAP SW CONNECT

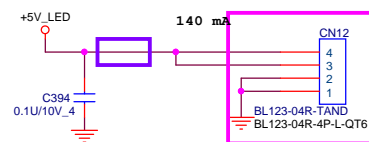


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT

PV modified:
CN8 update type
Add L57, L77, C904, C621 for ESB
Del R104, R103

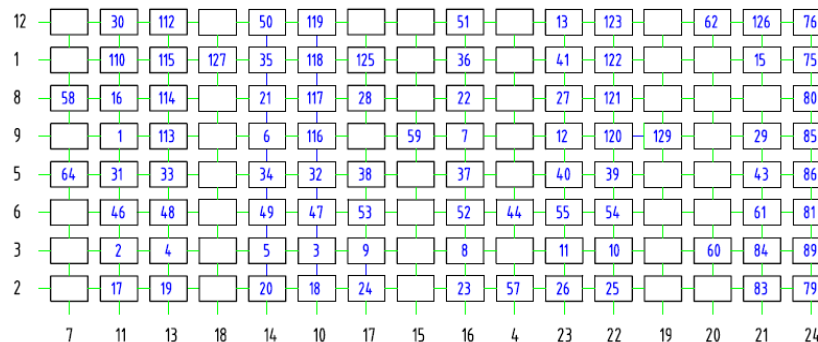
Del R770 on PV

SI-2 Modified 12/27

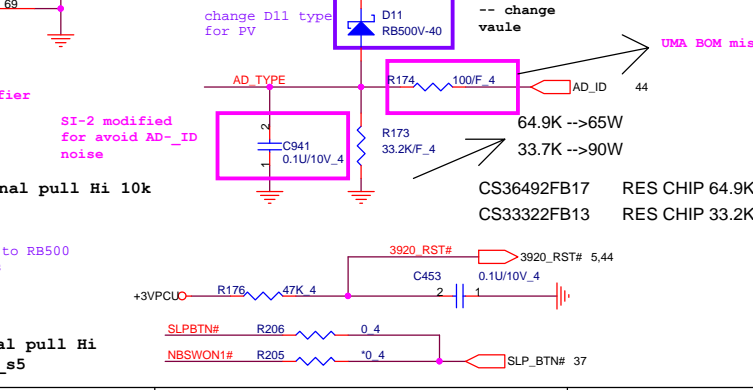
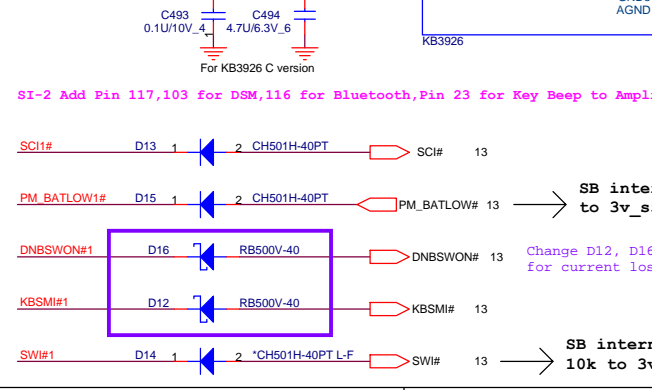
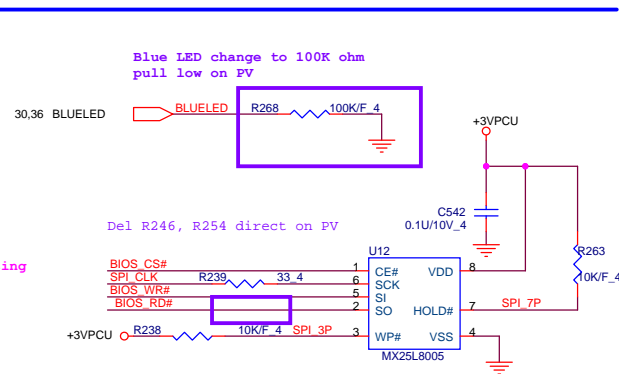
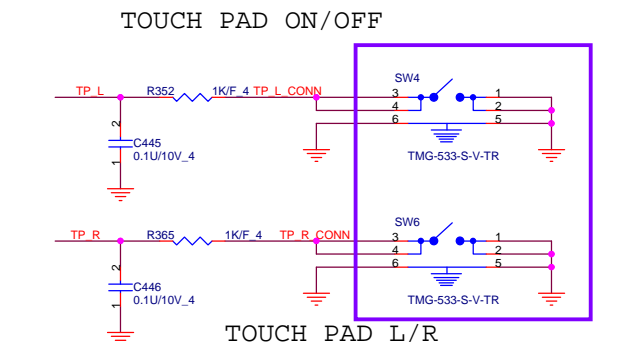
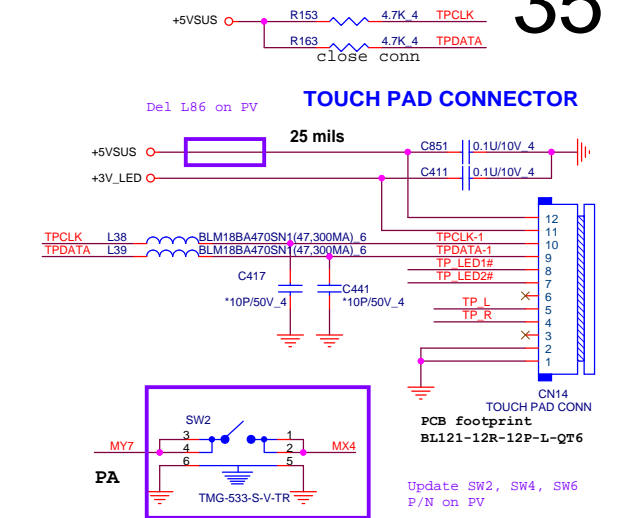
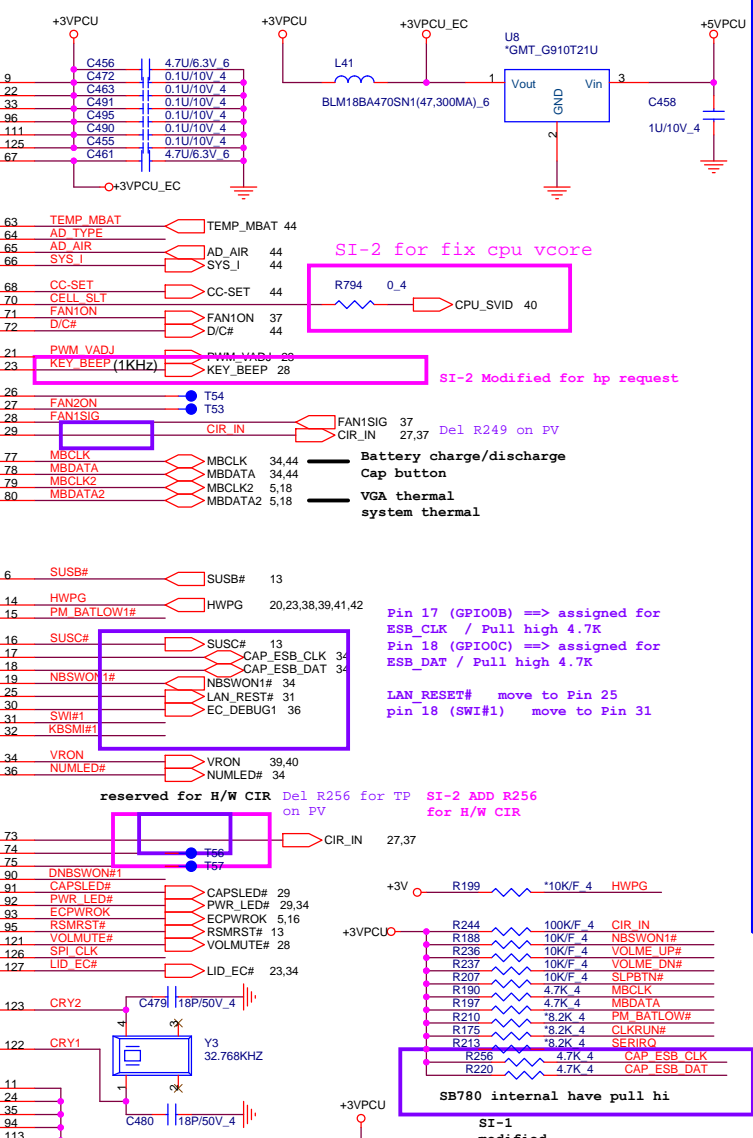
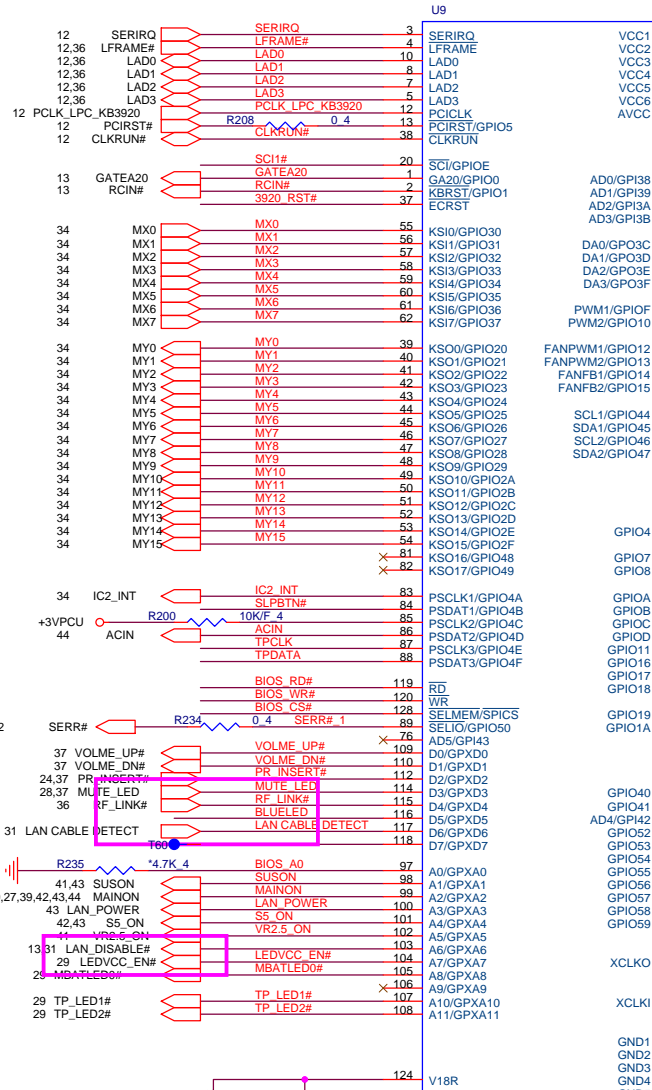


1. LEDVCC
2. LEDVCC
3. NC
4. GND

SI-2 Modified



PROJECT : QT8
Quanta Computer Inc.



Pin 17 (GPIO0B) ==> assigned for ESB_CLK / Pull high 4.7K
 Pin 18 (GPIO0C) ==> assigned for ESB_DAT / Pull high 4.7K
 LAN_RESET# move to Pin 25
 pin 18 (SWI#1) move to Pin 31

Del R256 for TP on PV
 SI-2 ADD R256 for H/W CIR

SB780 internal have pull hi

SI-1 modified -- change vaule

64.9K --> 65W
 33.7K --> 90W

CS36492FB17 RES CHIP 64.9K 1/16W +-1%(0402)
 CS33322FB13 RES CHIP 33.2K 1/16W +-1%(0402)

change D11 type for PV

change D12, D16 to RB500 for current loss

SB internal pull Hi 10k to 3v_s5

Blue LED change to 100K ohm pull low on PV

Del R246, R254 direct on PV

SST AKE5GFK0Z09 1M byte SPI BIOS

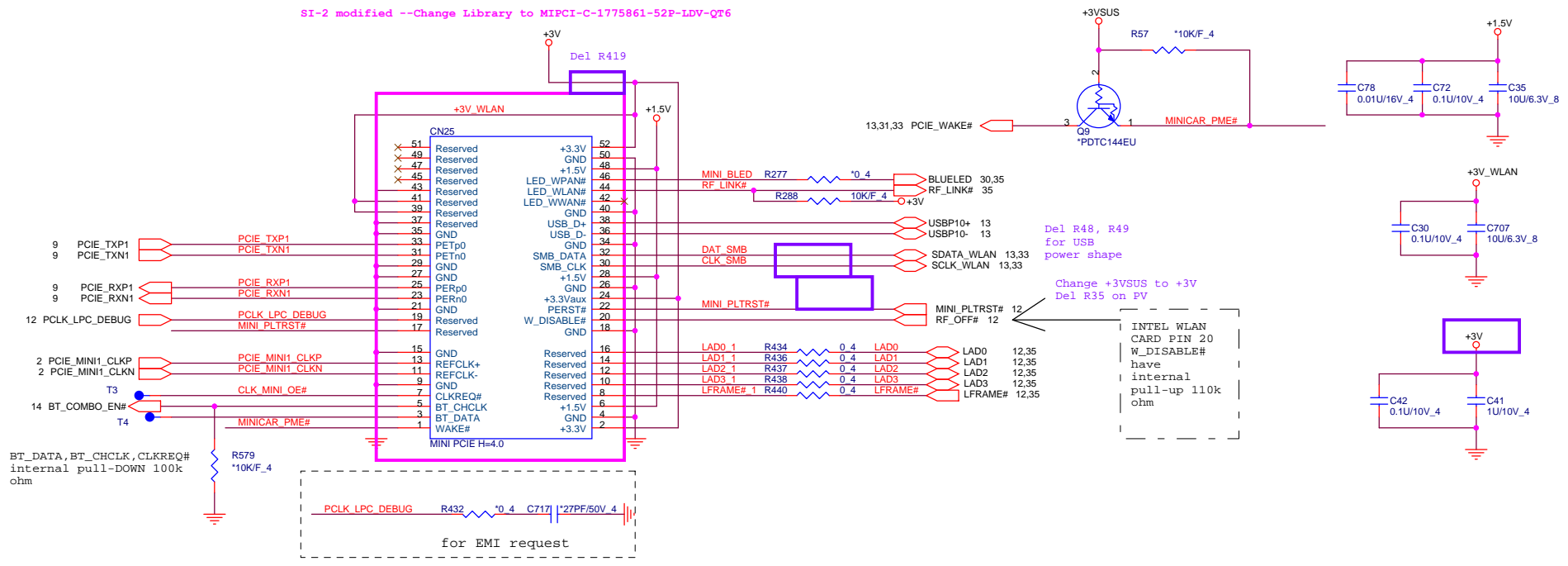
EON AKE3GZP0Q00

PROJECT : QT8
 Quanta Computer Inc.

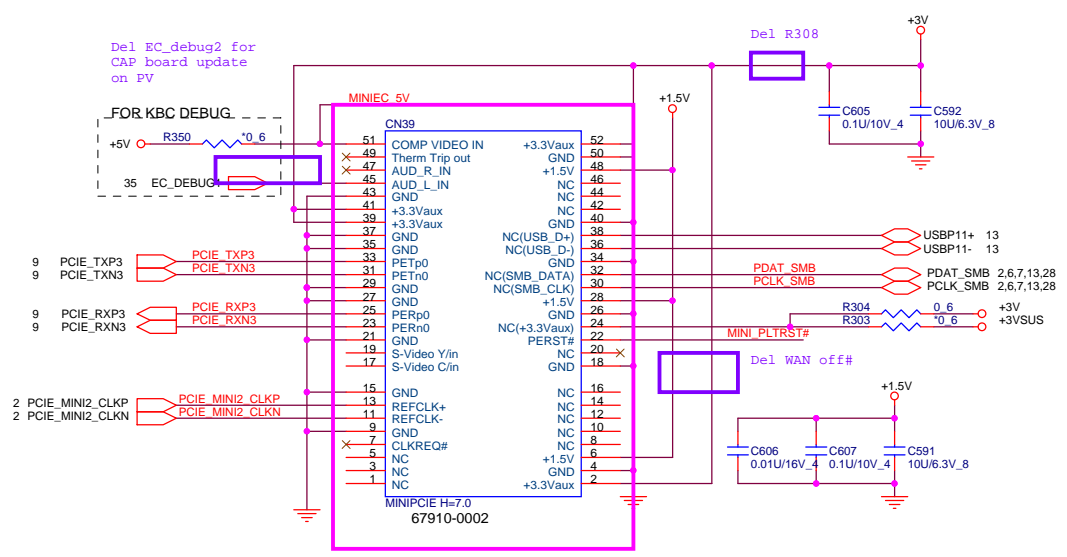
Size Custom	Document Number	Rev 1A
	KB3926/ROM/TP	
Date: Tuesday, February 19, 2008		Sheet 35 of 45

Mini PCI-E Card 1 WLAN


SI-2 modified --Change Library to MIPCI-C-1775861-52P-LDV-QT6

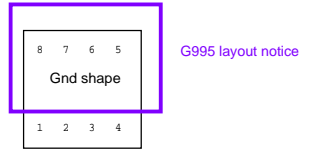
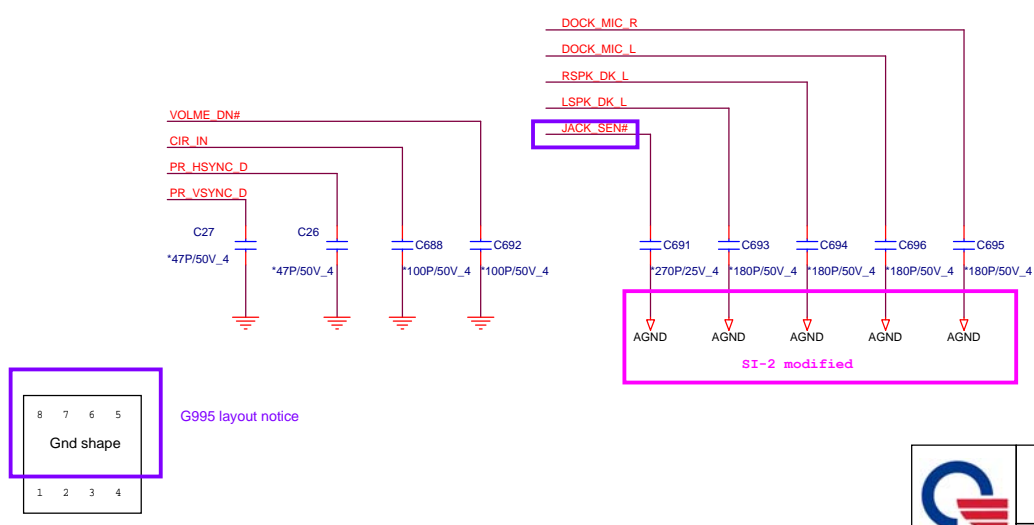
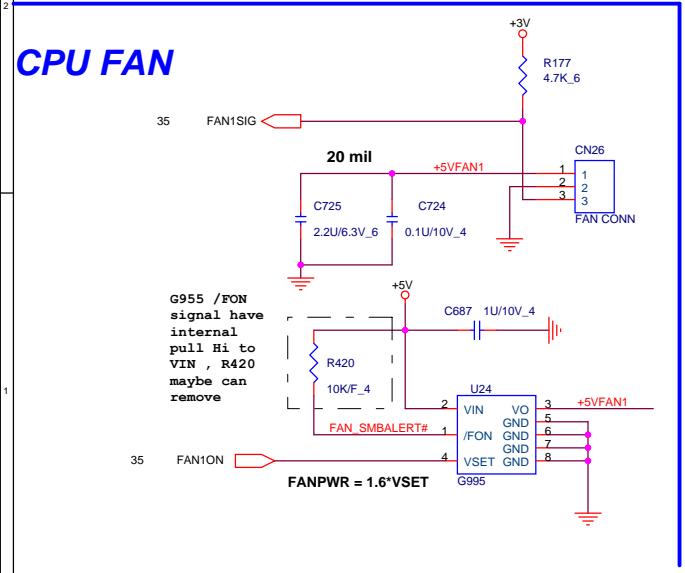
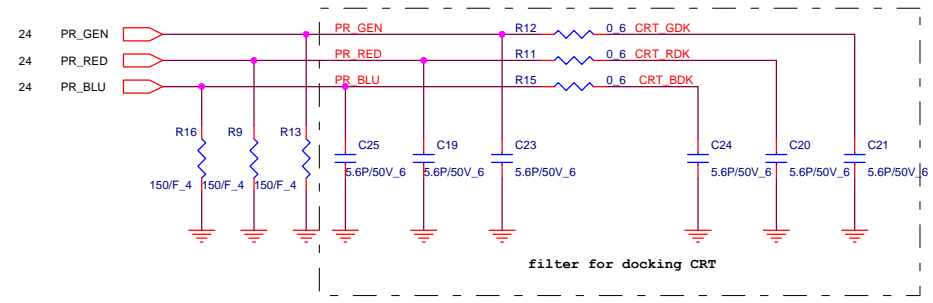
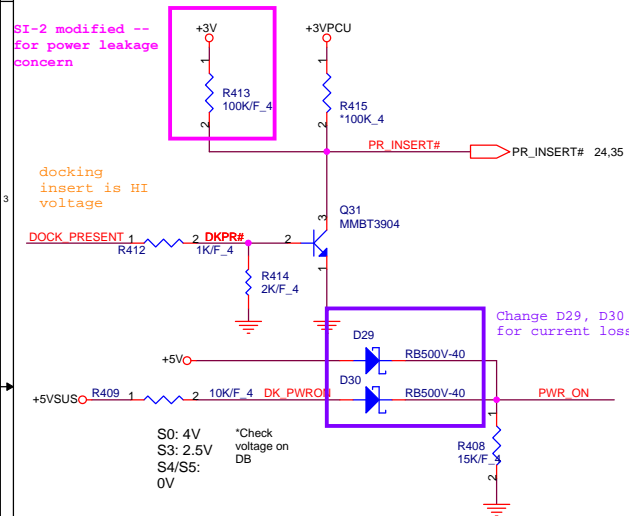
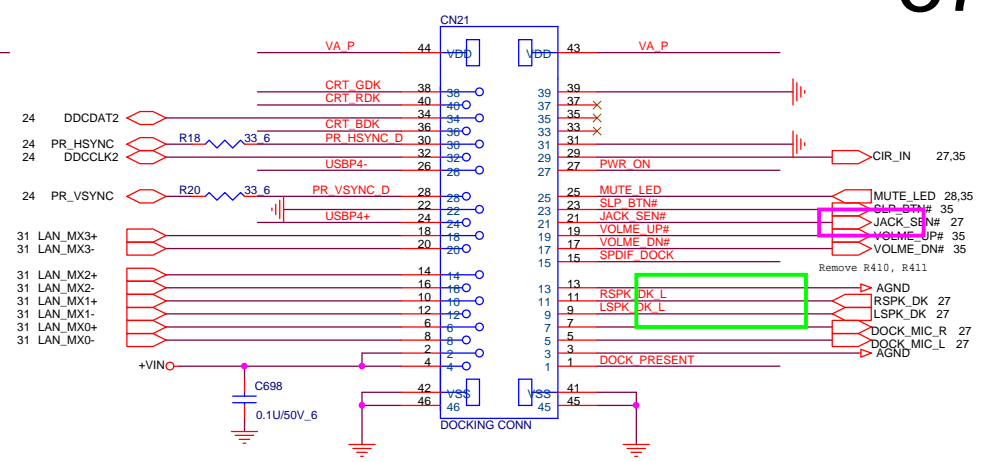
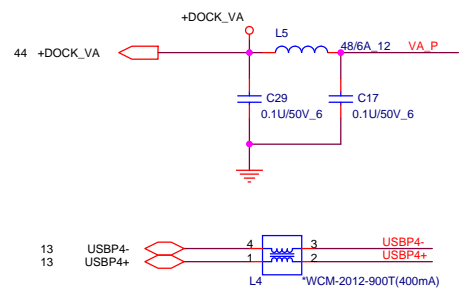
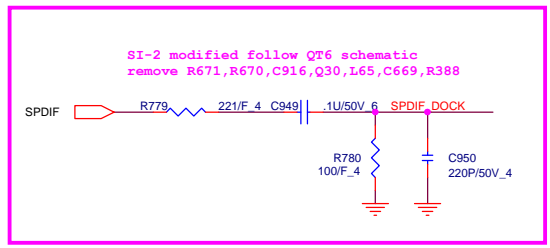


Mini PCI-E Card 2 TV tuner card



SI-2 modified --Change Library to MIPCI-E-P04-FJ504-170-52P-QT6

 NBS/RD5	PROJECT : QT8 Quanta Computer Inc.	
	Size Custom Date: Tuesday, February 19, 2008	Document Number Mini CARD X 3 Sheet 36 of 45



DC/DC +3VPCU/+ 5VPCU/ +12VALW

- +5VPCU 27,28,34,35,39,40,41,42,43
- +3VPCU 5,12,23,29,30,34,35,37,40,41,42,44
- +3VSUS 13,25,30,36,39,41,43
- +3VS5 5,7,12,13,14,15,16,23,26,33,43
- +5VSUS 23,30,35,37,43
- +5V 5,15,20,23,24,25,27,28,29,30,33,36,37,39,42,43
- +LANVCC

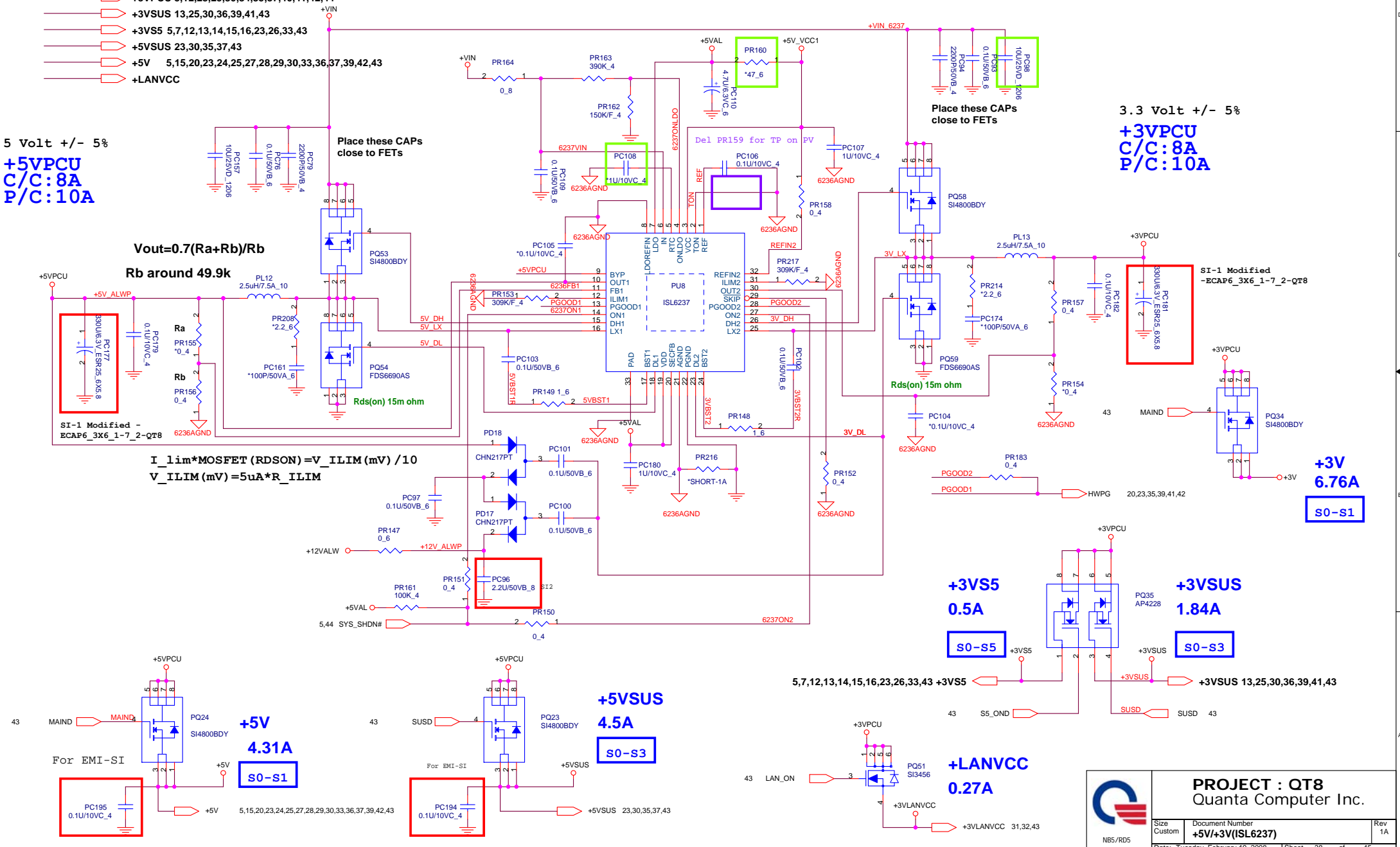
TON: 5V / 3.3V
 GND = 400 / 500KHz
 REF = 400 / 300KHz
 VCC = 200 / 300KHz

5 Volt +/- 5%
+5VPCU
 C/C: 8A
 P/C: 10A

3.3 Volt +/- 5%
+3VPCU
 C/C: 8A
 P/C: 10A

$V_{out} = 0.7(Ra + Rb) / Rb$
 Rb around 49.9k

$I_{lim} * MOSFET (RDSON) = V_{ILIM} (mV) / 10$
 $V_{ILIM} (mV) = 5uA * R_{ILIM}$



Place these CAPs close to FETs

Place these CAPs close to FETs

Rds(on) 15m ohm

+3V
 6.76A
 S0-S1

+3VS5
 0.5A
 S0-S5

+3VSUS
 1.84A
 S0-S3

+5VSUS
 4.5A
 S0-S3

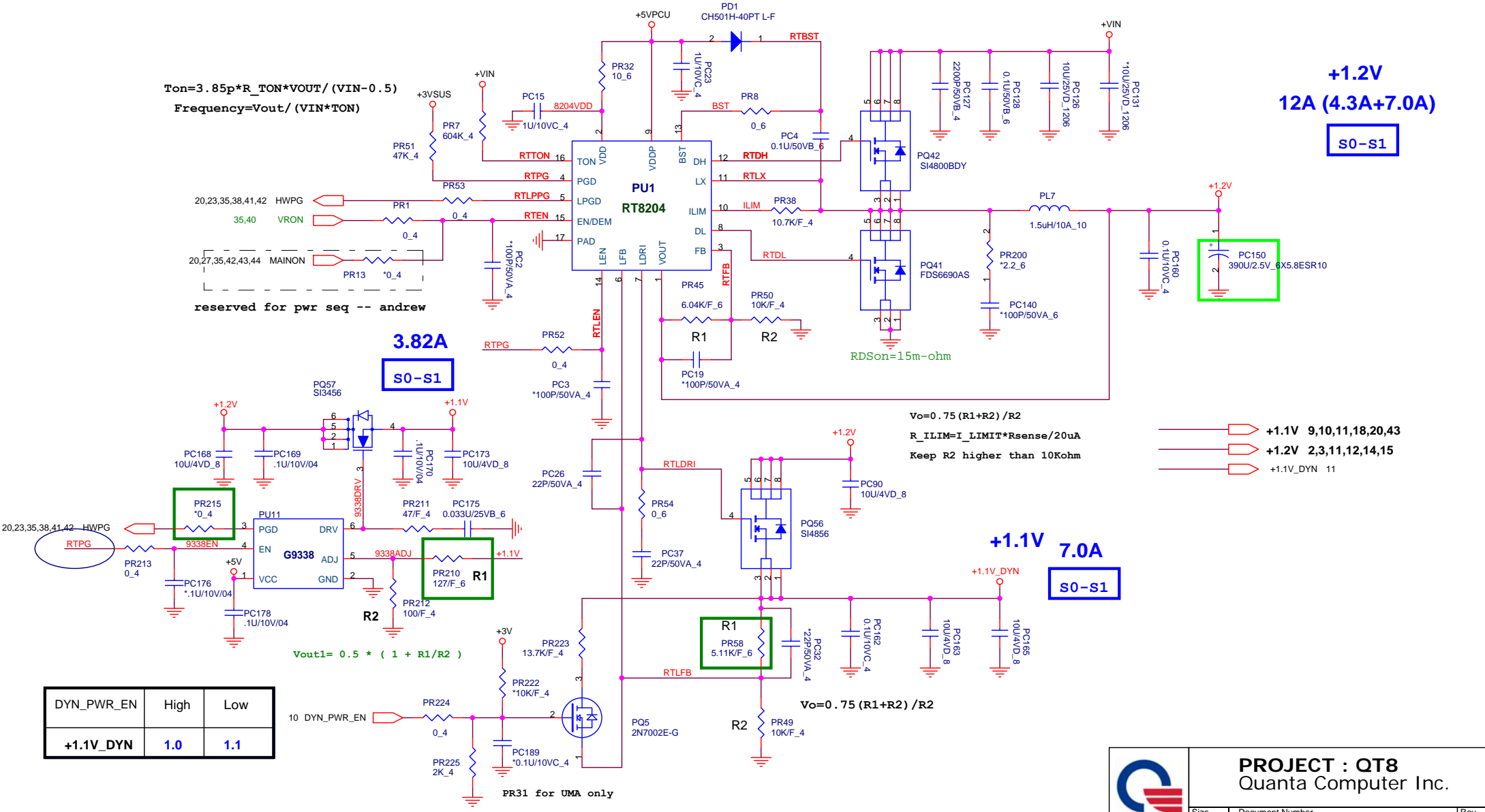
+5V
 4.31A
 S0-S1

+LANVCC
 0.27A

	PROJECT : QT8		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number +5V/+3V(ISL6237)	
Date: Tuesday, February 19, 2008	Sheet 38 of 45		

$Ton = 3.85p * R_{TON} * Vout / (VIN - 0.5)$
 $Frequency = Vout / (VIN * TON)$

+1.2V
12A (4.3A+7.0A)
S0-S1



reserved for pwr seq -- andrew

3.82A
S0-S1

$V_o = 0.75 (R1 + R2) / R2$
 $R_{ILIM} = I_{LIMIT} * R_{sense} / 20uA$
 Keep R2 higher than 10Kohm

- +1.1V 9,10,11,18,20,43
- +1.2V 2,3,11,12,14,15
- +1.1V_DYN 11

+1.1V 7.0A
S0-S1

$V_{out1} = 0.5 * (1 + R1/R2)$

DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

PR31 for UMA only



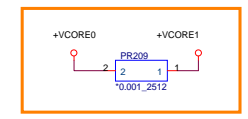
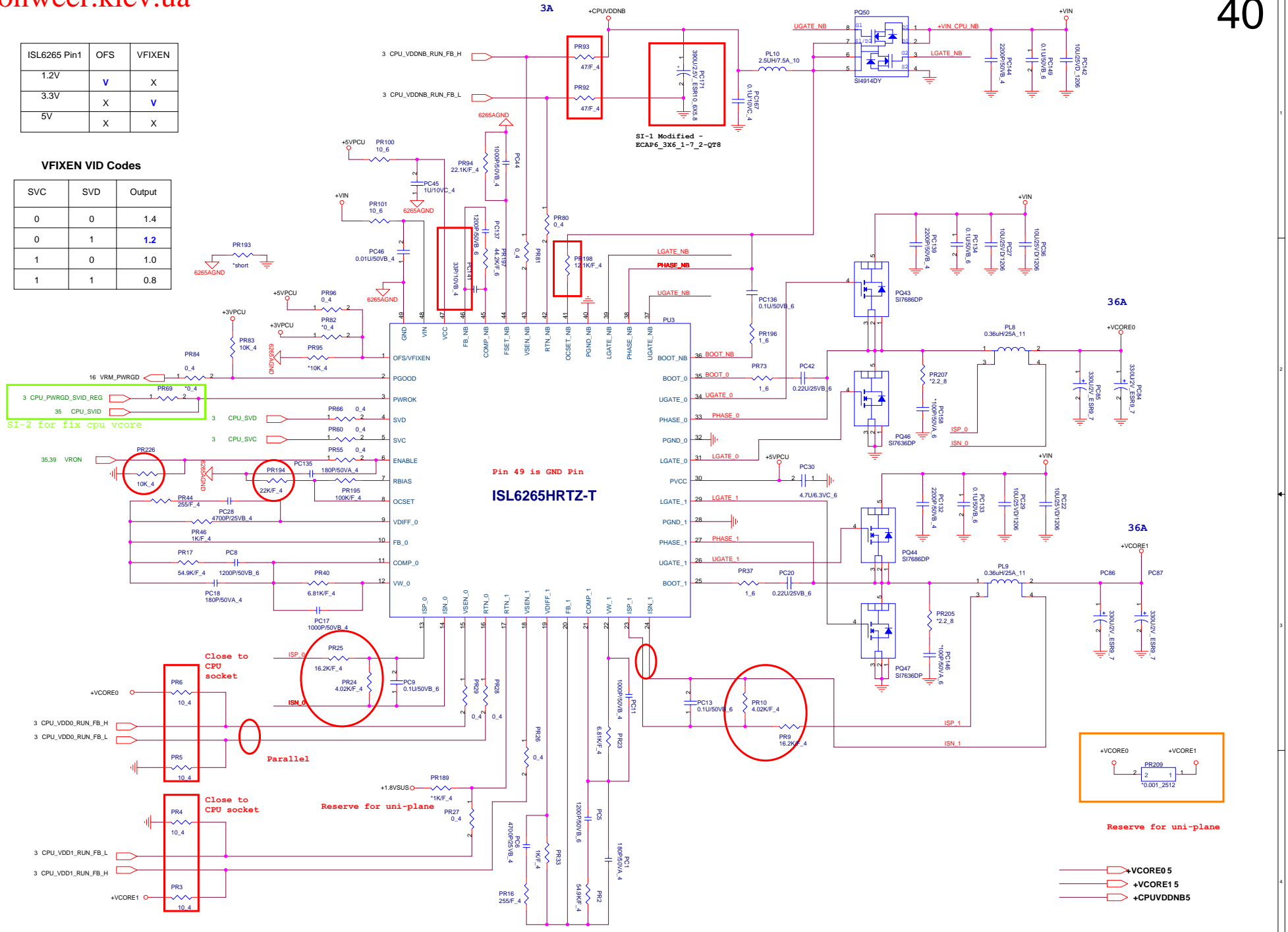
PROJECT : QT8
 Quanta Computer Inc.

Size B	Document Number +1.2V & +1.1V(RT8204)	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 39	of 45

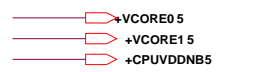
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

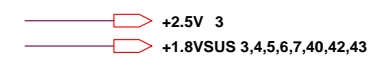
VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



Reserve for uni-plane

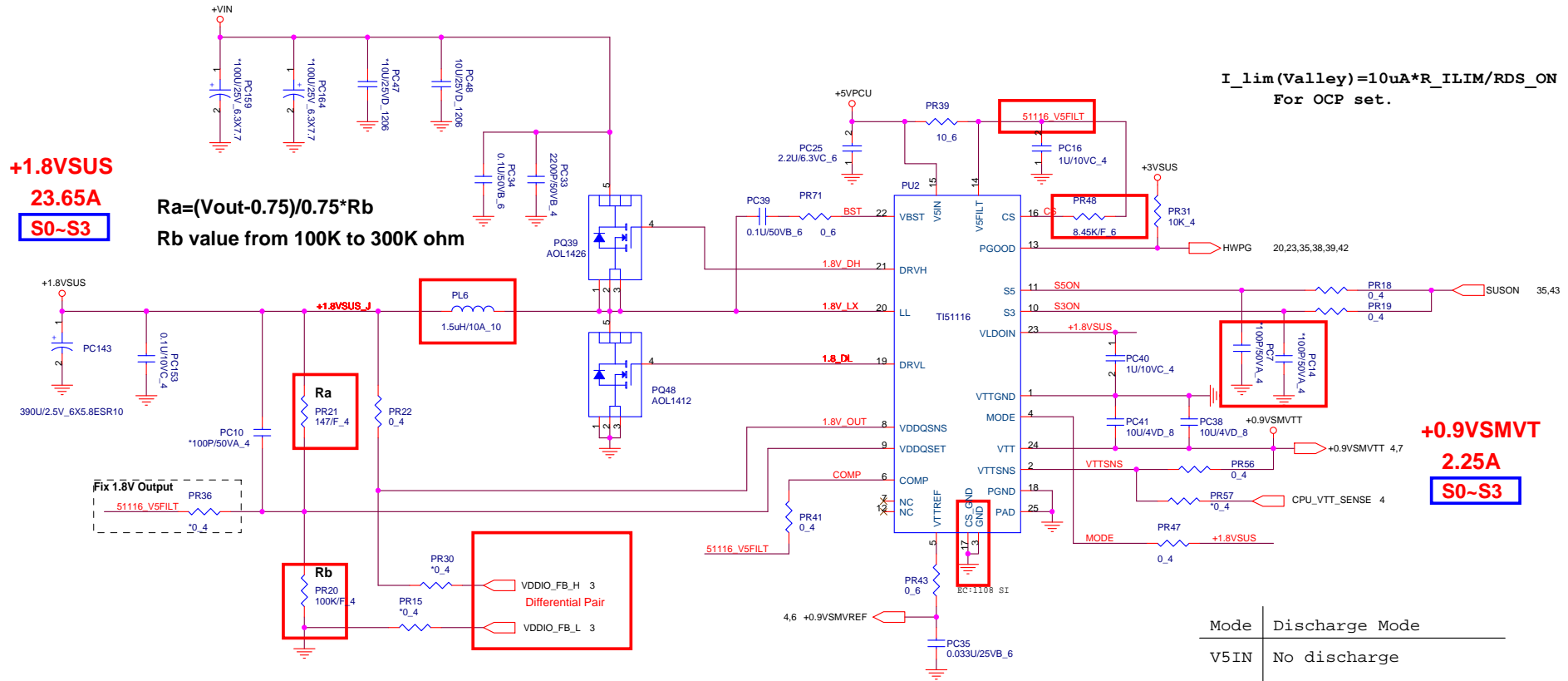




+1.8VSUS
23.65A
S0~S3

$Ra = (V_{out} - 0.75) / 0.75 * Rb$
 Rb value from 100K to 300K ohm

$I_{lim(Valley)} = 10\mu A * R_{ILIM} / R_{DS_ON}$
 For OCP set.

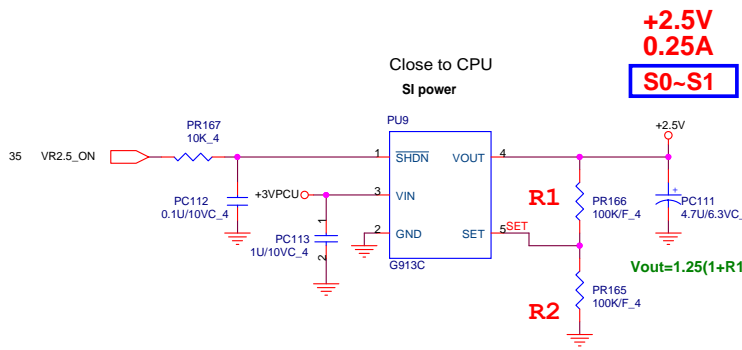


+0.9VSMVT
2.25A
S0~S3

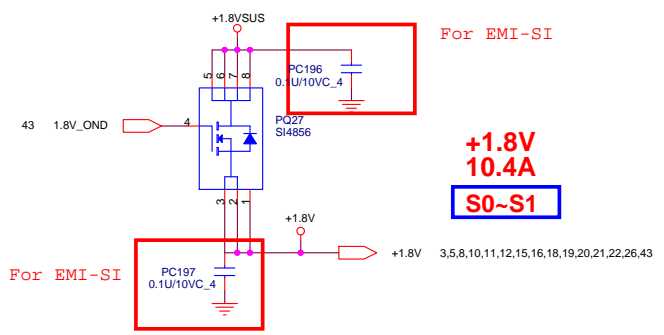
Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$V_TRIP(mV) = R_TRIP(Kohm) * 10(\mu A)$
 $I_OCP = V_trip / R_{ds_on} + I_Ripple / 2$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V_vddqsns / 2$	DDR
V5IN	1.8	$V_vddqsns / 2$	DDR2
FB	adjustable	$V_VDDQSNS / 2$	$1.5V < VDDQ < 3V$



+2.5V
0.25A
S0~S1



Discrete: SI4856
UMA: SI4800

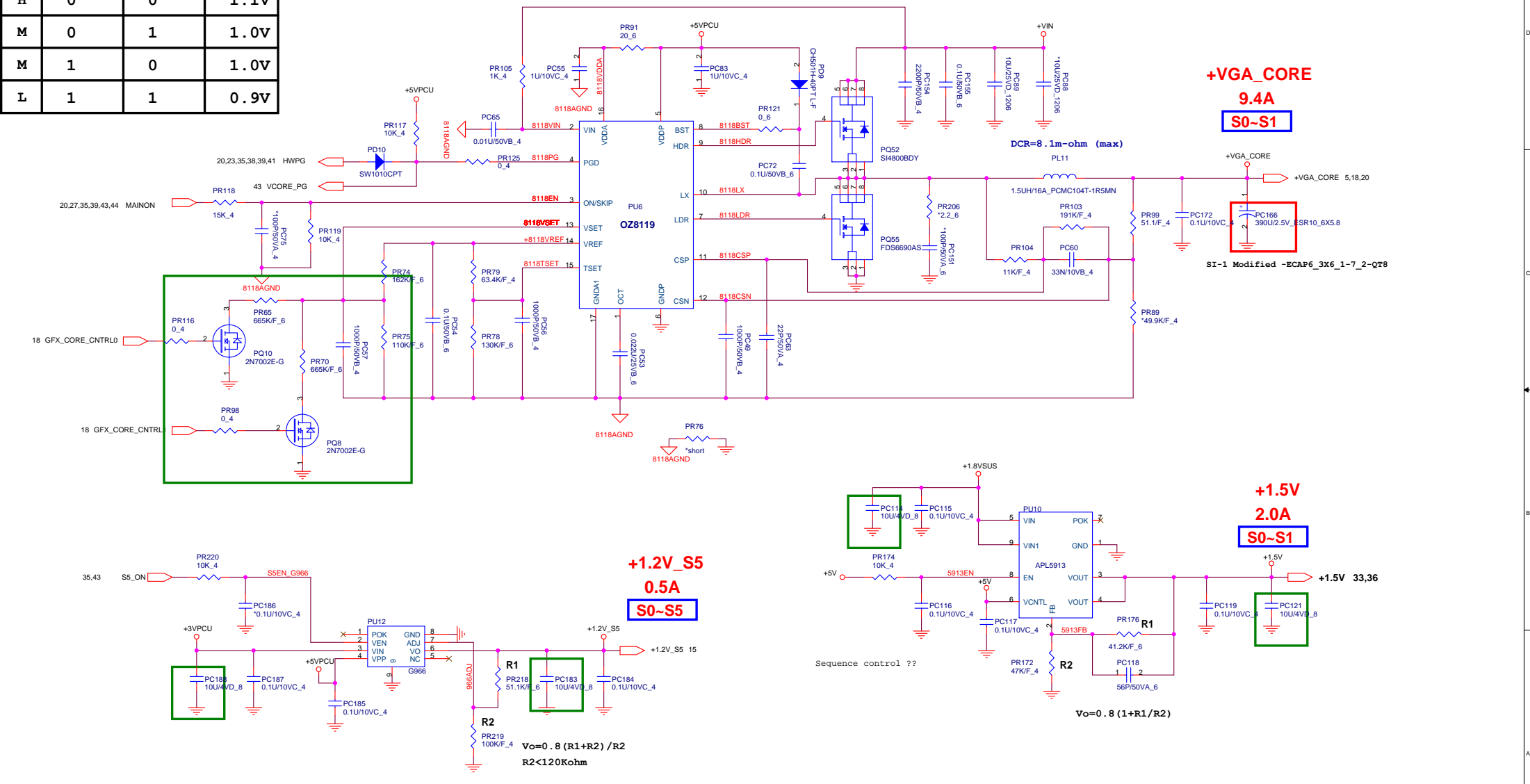
+1.8V
10.4A
S0~S1

	PROJECT : QT8		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number 1.8VSUS/DDR_VTER/+1.8V/2.5V	
Date: Tuesday, February 19, 2008		Sheet 41 of 45	

ATI M82-SE

+VGA_CORE5,18,20
 +1.2V_S5 15
 +1.5V 33,36

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

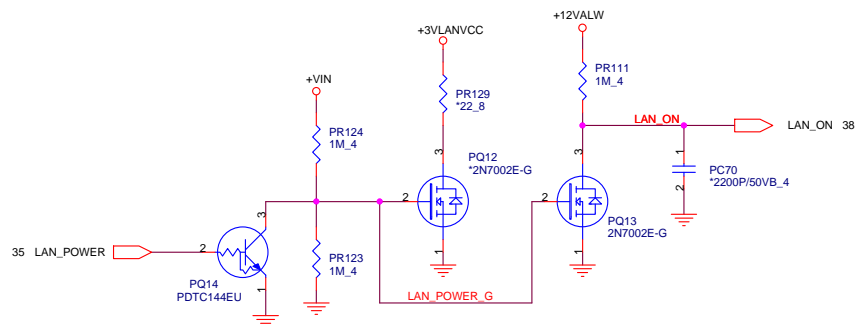
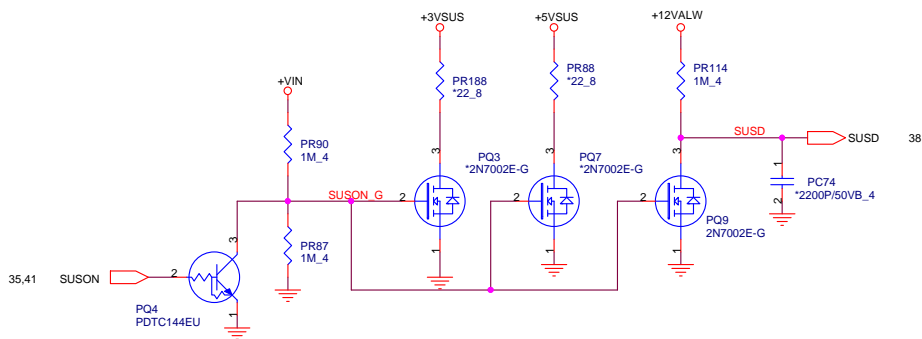
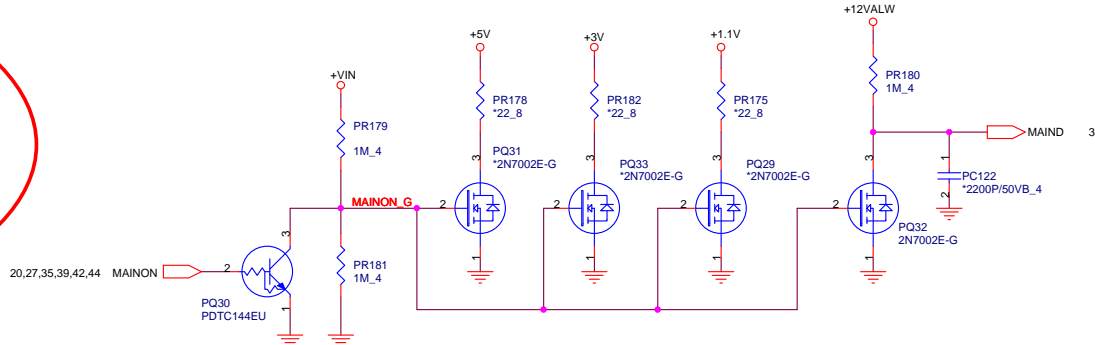
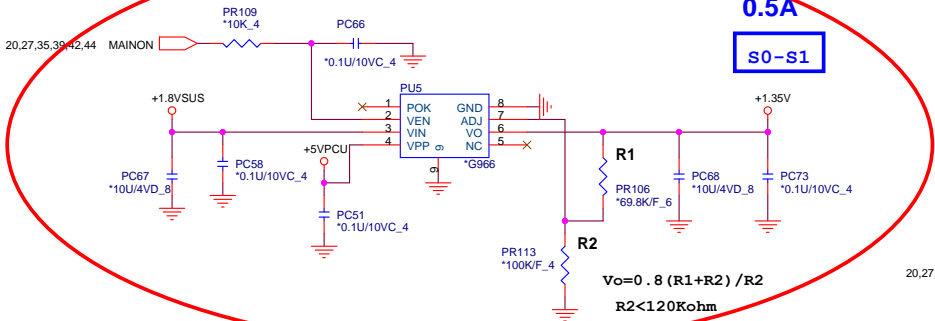


	PROJECT : QT8 Quanta Computer Inc.	
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SI-1 Modified - can remove +1.35V for AMD update

0.5A

S0-S1



For Discrete Only

