

Soyuz 2.0 SYSTEM DIAGRAM

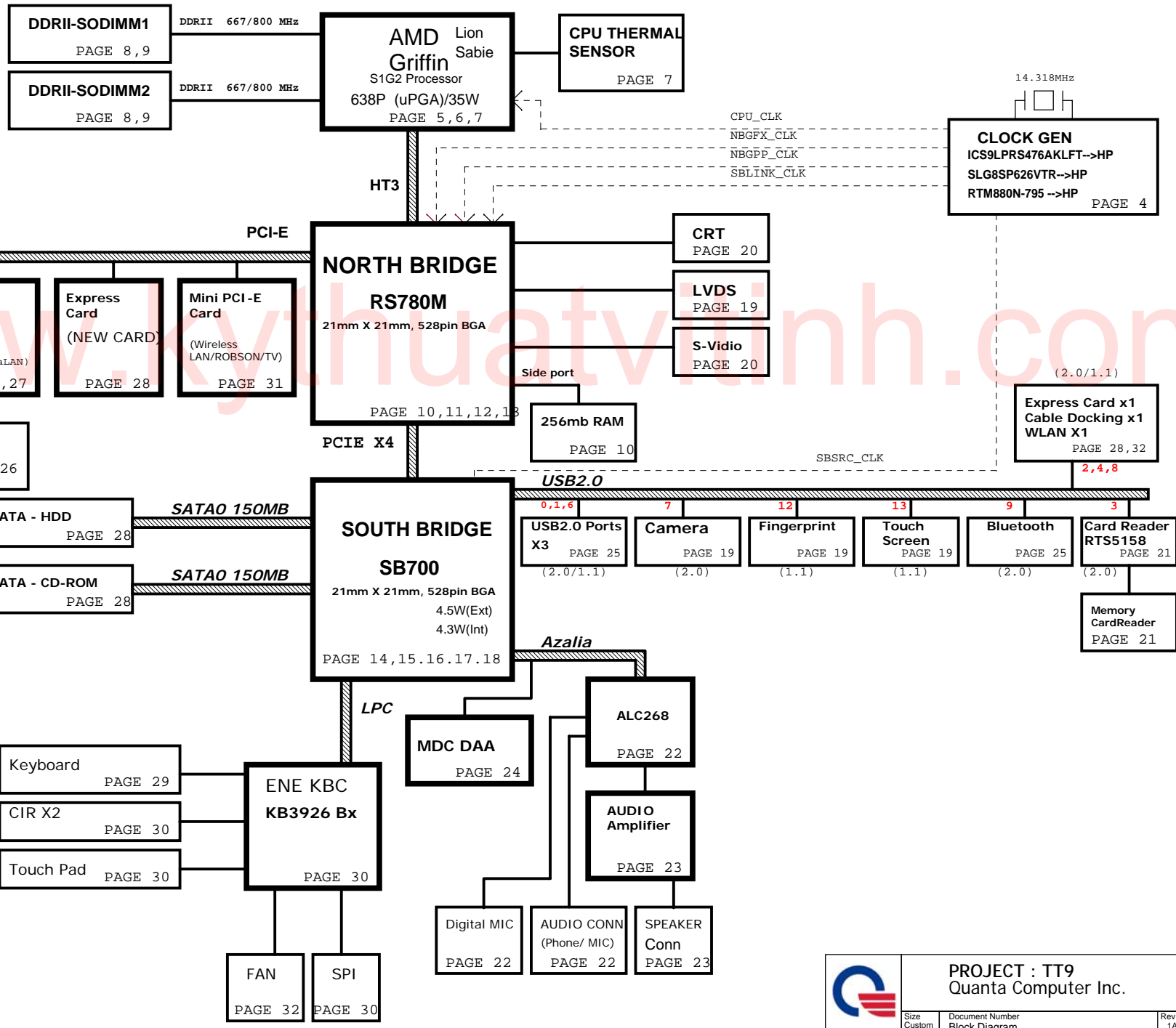


PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

- Cable Docking**
- TV_OUT
 - VGA
 - RJ-45
 - CIR/Pwr btn
 - SPDIF Out
 - Stereo MIC
 - Headphone Jack
 - USB Port
 - VOL Cntr
- PAGE 32

- SYSTEM CHARGER(ISL6251A) PAGE 39
- SYSTEM POWER MAX1631A PAGE 33
- DDR II SMDR_VTERM 1.8V/1.8VSUS PAGE 36
- VCCP +1.1V AND +1.2V(RT8204) PAGE 34
- CPU CORE ISL6265A PAGE 35



Pg#	Description	NOTE
1	Schematic Block Diagram	
2	System Information	
3	Power sequence chart	
4	CLOCL GENERATOR	
5-7	AMD CPU S1G2 Griffin	
8-9	DDR II SO-DIMM	
10-13	RS780M	
14-18	SB700	
19	LCD CONNECTOR / LCD PWR / LID	
20	20--CRT,TV_OUT	
21	RTS5158E & CR SOCKET	
22	Azalia ALC268	
23	JACK/AMP_TPA0312	
24	Si3080 and MDC1.5 Connector	
25	Blue Tooth / USBX3 / TPM	
26	RTL8111C/RJ45	
27	LAN Power	
28	NEW CARD/SATA ODD/SATA HDD	
29	LED/KEYBOARD/SW	
30	KB3926/ROM/TP	
31	Mini CARD/Hole	
32	CABLE DOCKING/FAN	
33	3V/5V(MAX1631A)	
34	+1.2V/+1.1V (RT8204)	
35	+CPU_CORE ISL6265	
36	+1.8VSUS/+1.8V/+2.5V	
37	+1.1V/+1.2V_S5/+1.5V	
38	DISCHARGE	
39	Charger (ISL6251)	

* --> Un-stuff (ex. *1K/04)
 04-- 0402 footprint
 06-- 0603 footprint
 08-- 0805 footprint
 12-- 1206 footprint
 F-- 1% tolerance

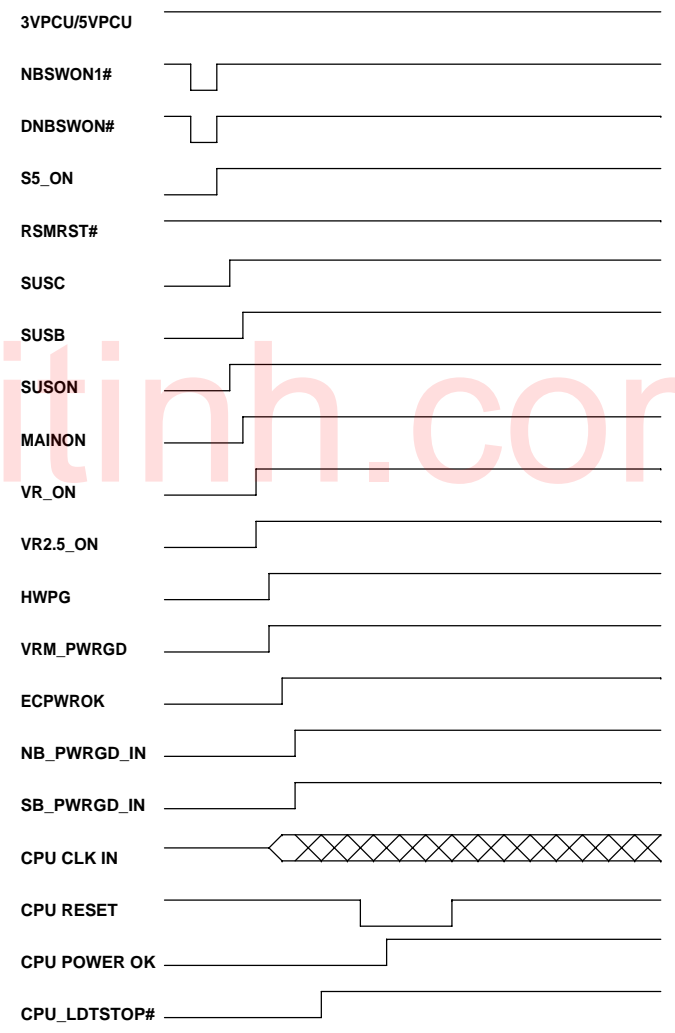
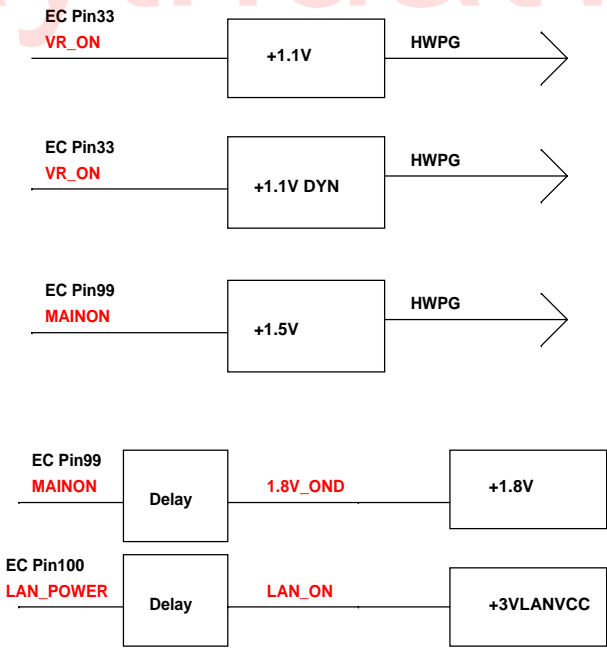
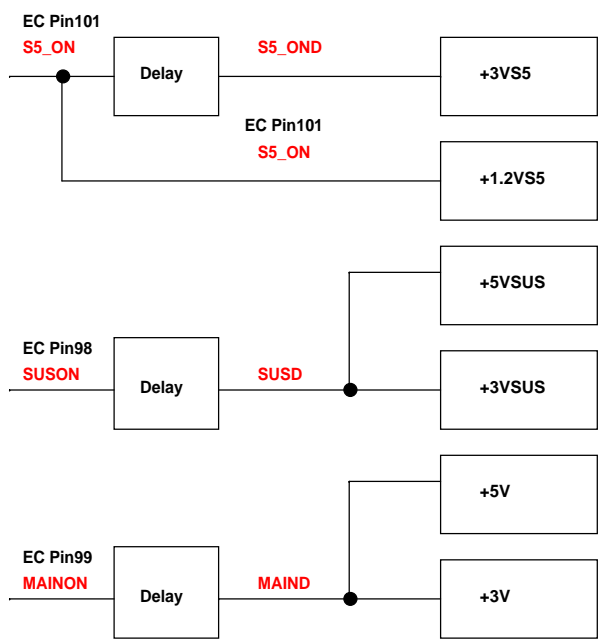
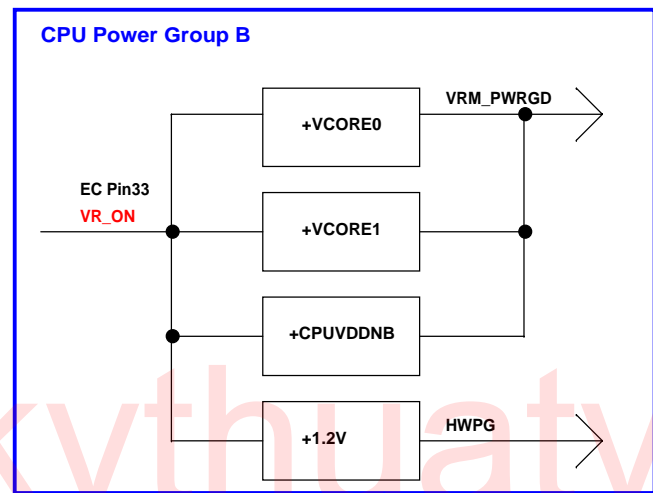
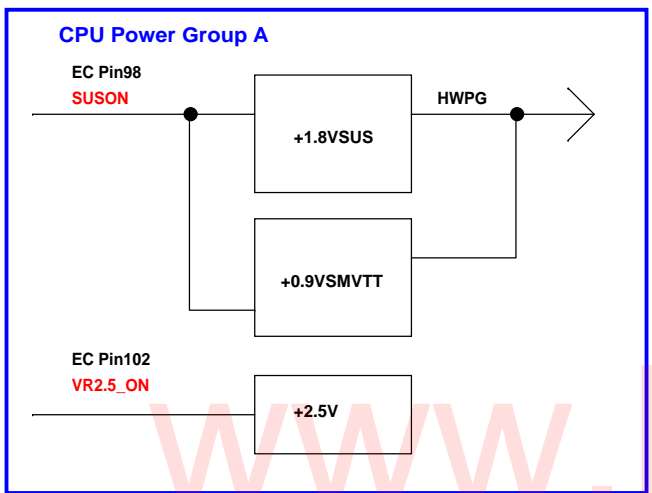
Power & Ground

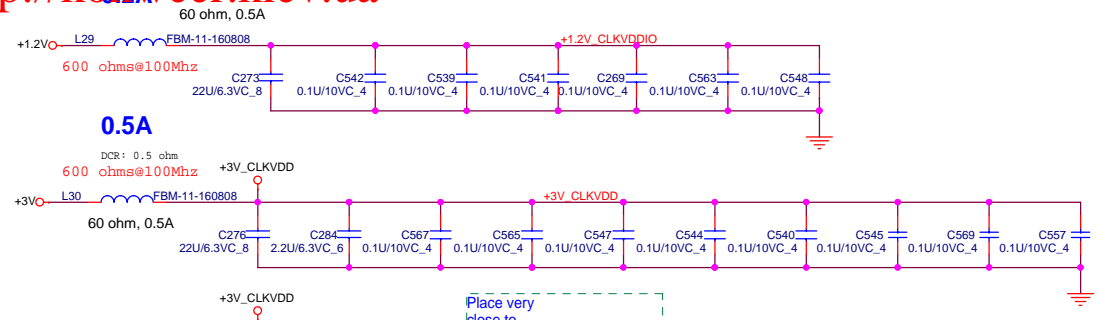
Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (18.5V)	
+BATT	S0, S3, S4, S5	MAIN BATTERY + (6.2V-8.4V)	
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3.3V)	
+12VALW	S0, S3, S4, S5	+12V	
+VCORE	S0	CPU CORE POWER (0.375-1.5V)	VRON
+CPUVDDNB	S0	CPU CORE POWER (1.375-1.5V)	VRON
+1.1V_NB	S0	+1.1 to +1.0 DYN	VRON
+1.1V	S0	+1.1V	VRON
+1.2VS5	S0, S3, S4, S5		S5_ON
+1.2V	S0	+1.2V	VRON
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+5V	S0		MAIND
+5VSUS	S0, S3		SUSON
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+1.5V	S0		MAIND
+1.8VSUS	S0, S3	DDR CORE POWER	SUSON
+1.8V	S0		MAINON
+2.5V	S0	CPU VDDA	VR2.5_ON
+0.9VSMVTT	S0	DDR COMMAND & CONTROL PULL UP POWER	MAINON
+0.9VSMVREF_DIMM	S0, S3	DDR REF POWER	SUSON
+AVDD	S0	AUDIO ANALOG POWER (5V)	MAINON
+3VLAVCC	S0, S3, S4, S5	LAN Power	LAN_ON
⏏ GND	ALL PAGES	DIGITAL GROUND	
⏏ AGND		AUDIO GND	

SMBUS	SMBUS function define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card (+3VS5)
SMBCLK2 SMBDAT2	New CARD (+3VS5)



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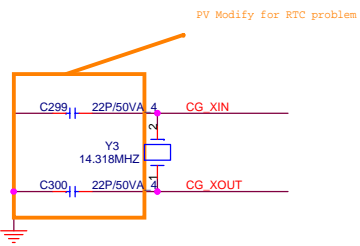
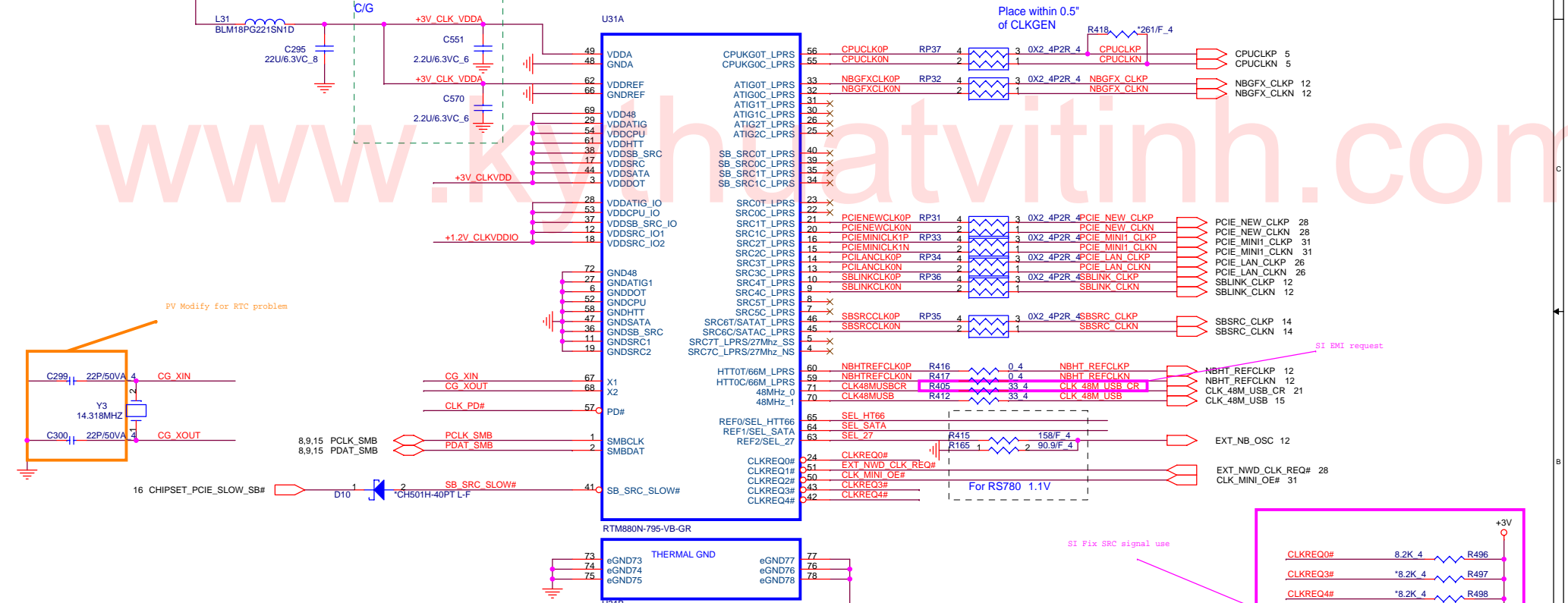




Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

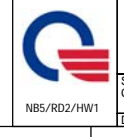
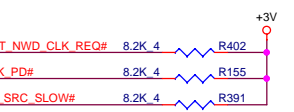
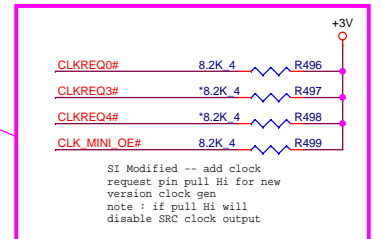
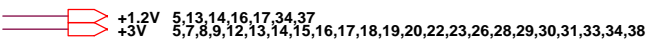


* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	0	100 MHz spreading differential SRC clock
	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

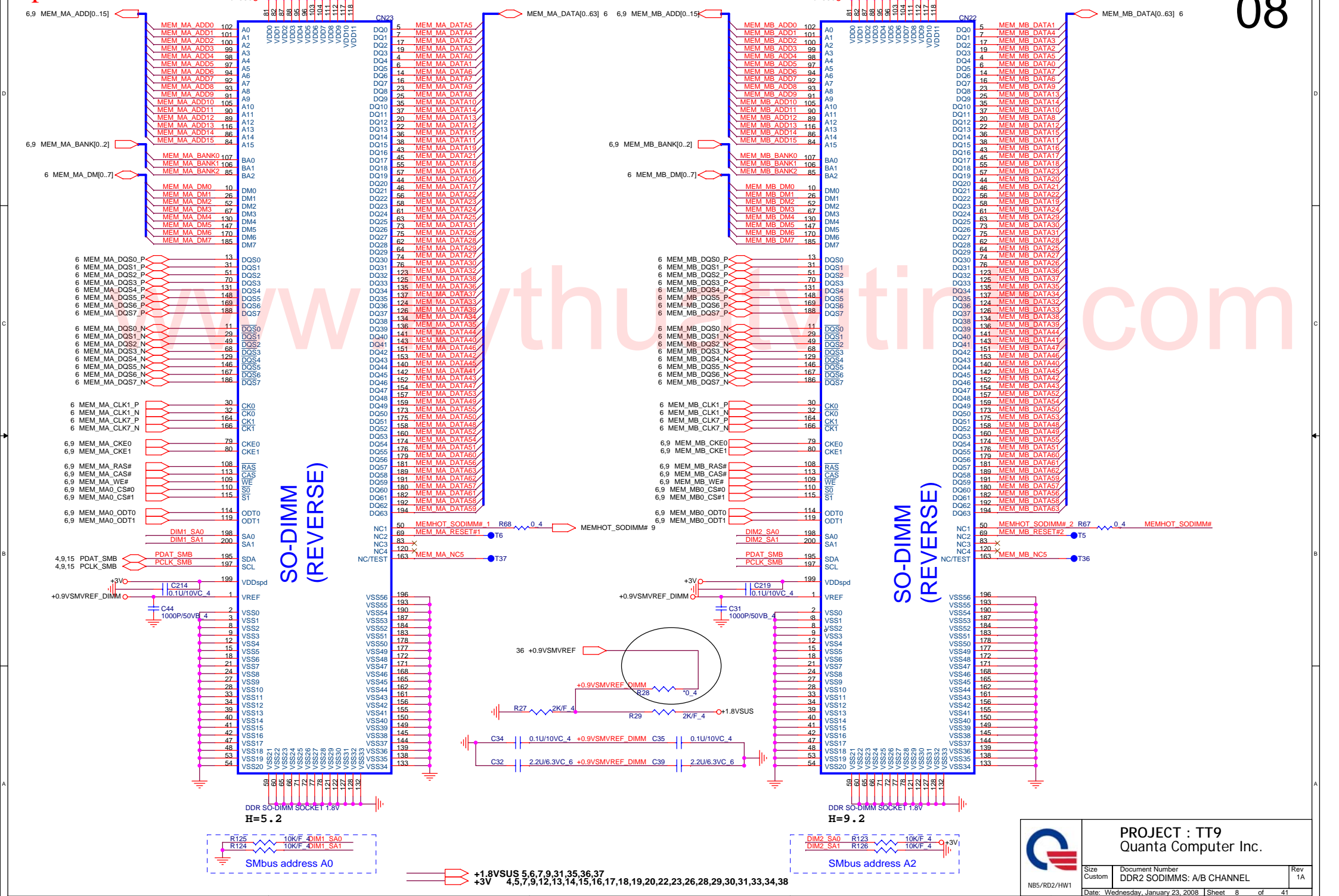
when driven low SB_SRC clocks slow only supported with to reduced setpoint custom CG IC

* RS780 can be used as clock buffer to output two PCIE reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.



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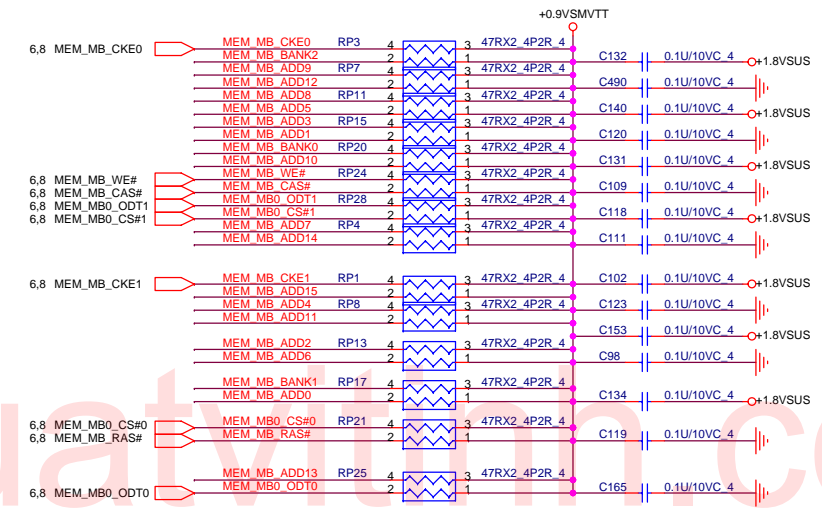
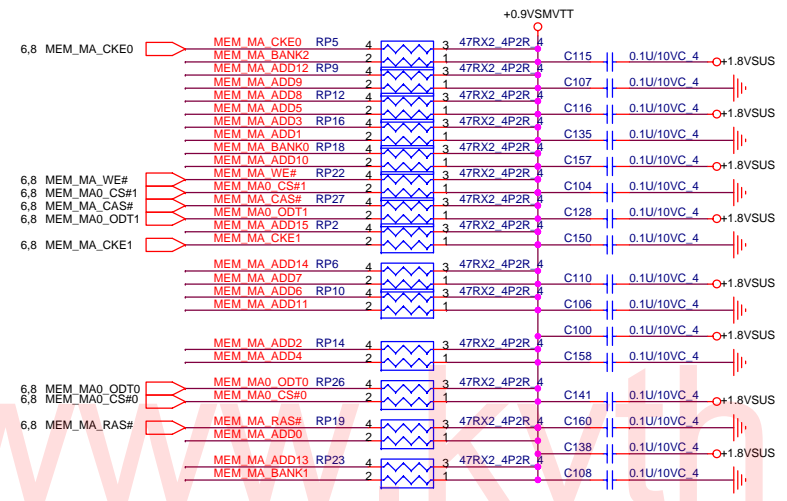
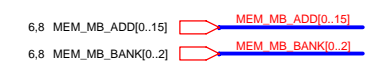
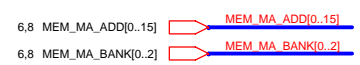
Size Custom	Document Number Clock generator	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 4 of 41		



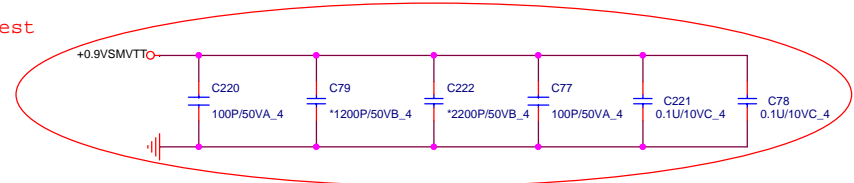
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Size Custom Document Number DDR2 SODIMMS: A/B CHANNEL Rev 1A
 Date: Wednesday, January 23, 2008 1 Sheet 8 of 41

NBS/RD2/HW1



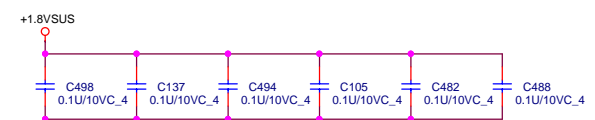
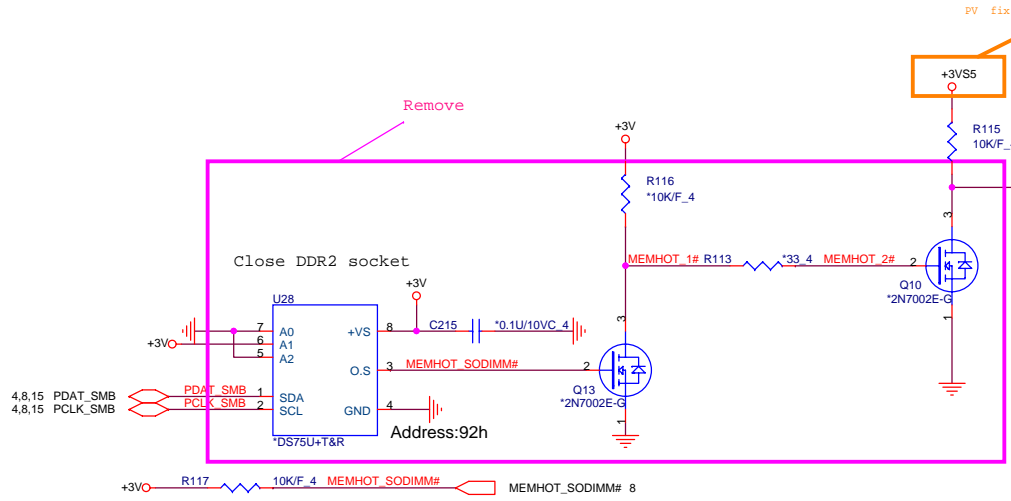
Emi request



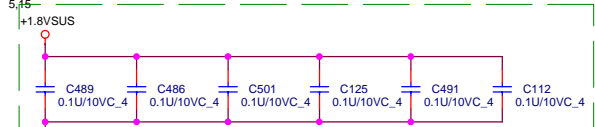
PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



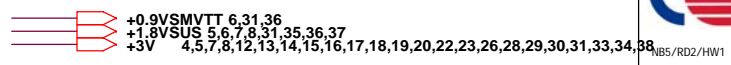
PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



PLACE CLOSE TO SOCKET (PER EMI/EMC)



PLACE CLOSE TO SOCKET (PER EMI/EMC)



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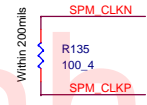
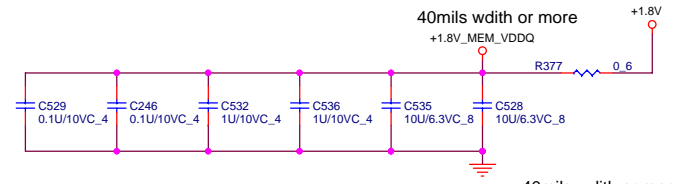
Size Custom	Document Number DDR2 SODIMMS TERMINATIONS	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 9 of 41		

PART 1 OF 6

HYPER TRANSPORT CPU I/F

HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	D24	HT_NB_CPU_CAD_H0
HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	D25	HT_NB_CPU_CAD_L0
HT_CPU_NB_CAD_H1	Y22	HT_RXCAD1P	E24	HT_NB_CPU_CAD_H1
HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	E25	HT_NB_CPU_CAD_L1
HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	F24	HT_NB_CPU_CAD_H2
HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	F25	HT_NB_CPU_CAD_L2
HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	F23	HT_NB_CPU_CAD_H3
HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	F22	HT_NB_CPU_CAD_L3
HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	H23	HT_NB_CPU_CAD_H4
HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	H22	HT_NB_CPU_CAD_L4
HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	J25	HT_NB_CPU_CAD_H5
HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	J24	HT_NB_CPU_CAD_L5
HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	K24	HT_NB_CPU_CAD_H6
HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	K25	HT_NB_CPU_CAD_L6
HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	K23	HT_NB_CPU_CAD_H7
HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	K22	HT_NB_CPU_CAD_L7
HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	F21	HT_NB_CPU_CAD_H8
HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	G21	HT_NB_CPU_CAD_L8
HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	G20	HT_NB_CPU_CAD_H9
HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	H21	HT_NB_CPU_CAD_L9
HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	J21	HT_NB_CPU_CAD_H10
HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	J21	HT_NB_CPU_CAD_L10
HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	J18	HT_NB_CPU_CAD_H11
HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	K17	HT_NB_CPU_CAD_L11
HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	L18	HT_NB_CPU_CAD_H12
HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	L19	HT_NB_CPU_CAD_L12
HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	M19	HT_NB_CPU_CAD_H13
HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	L18	HT_NB_CPU_CAD_L13
HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	M21	HT_NB_CPU_CAD_H14
HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	P21	HT_NB_CPU_CAD_L14
HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	P18	HT_NB_CPU_CAD_H15
HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	M18	HT_NB_CPU_CAD_L15
HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	H24	HT_NB_CPU_CLK_H0
HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	H25	HT_NB_CPU_CLK_L0
HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	L21	HT_NB_CPU_CLK_H1
HT_CPU_NB_CLK_L1	AB22	HT_RXCLK1N	L20	HT_NB_CPU_CLK_L1
HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	M24	HT_NB_CPU_CTL_H0
HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	M25	HT_NB_CPU_CTL_L0
HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	P19	HT_NB_CPU_CTL_H1
HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	P18	HT_NB_CPU_CTL_L1
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HT_RXCALN	C23	HT_RXCALN	B25	HT_TXCALN

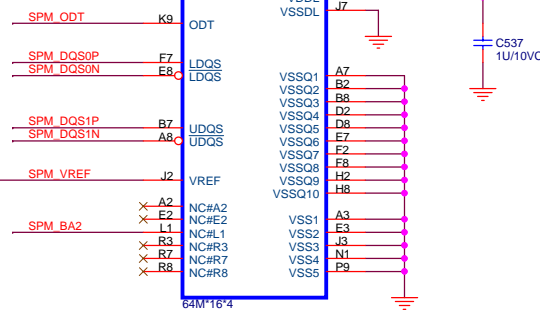
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HT_CPU_NB_CAD_L[15..0]	HT_CPU_NB_CAD_L[15..0]	5
HT_CPU_NB_CLK_H[1..0]	HT_CPU_NB_CLK_H[1..0]	5
HT_CPU_NB_CLK_L[1..0]	HT_CPU_NB_CLK_L[1..0]	5
HT_CPU_NB_CTL_H[1..0]	HT_CPU_NB_CTL_H[1..0]	5
HT_CPU_NB_CTL_L[1..0]	HT_CPU_NB_CTL_L[1..0]	5
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HT_NB_CPU_CAD_L[15..0]	HT_NB_CPU_CAD_L[15..0]	5
HT_NB_CPU_CLK_H[1..0]	HT_NB_CPU_CLK_H[1..0]	5
HT_NB_CPU_CLK_L[1..0]	HT_NB_CPU_CLK_L[1..0]	5
HT_NB_CPU_CTL_H[1..0]	HT_NB_CPU_CTL_H[1..0]	5
HT_NB_CPU_CTL_L[1..0]	HT_NB_CPU_CTL_L[1..0]	5



Close to U23

SPM BA0	L2	BA0	DD15	B9	SPM DO15
SPM BA1	L3	BA1	DD14	B1	SPM DO14
SPM A12	R3	A12	DD13	D9	SPM DO9
SPM A11	P7	A11	DD12	D1	SPM DO12
SPM A10	M2	A10/AP	DD11	D7	SPM DO8
SPM A9	A11	A9	DD10	C2	SPM DO10
SPM A8	P8	A8	DD9	C8	SPM DO11
SPM A7	P2	A7	DD8	F9	SPM DO5
SPM A6	N7	A6	DD7	F1	SPM DO3
SPM A5	N3	A5	DD6	H9	SPM DO4
SPM A4	N8	A4	DD5	H1	SPM DO1
SPM A3	M2	A3	DD4	L1	SPM DO3
SPM A2	MZ	A2	DD3	H3	SPM DO7
SPM A1	M3	A1	DD2	G2	SPM DO2
SPM A0	A0	A0	DD1	L8	SPM DO6

SPM CLKN	K8	CK	VDDQ1	A8	MEM_VDDQ
SPM CLKP	J8	CK	VDDQ2	C1	MEM_VDDQ
SPM CKE	K2	CKE	VDDQ3	C3	MEM_VDDQ
SPM CS#	L8	CS	VDDQ4	C7	MEM_VDDQ
SPM WE#	K3	WE	VDDQ5	C9	MEM_VDDQ
SPM RAS#	K7	RAS	VDDQ6	G1	MEM_VDDQ
SPM CAS#	L7	CAS	VDDQ7	G3	MEM_VDDQ
SPM DM0	F3	LDM	VDDQ8	G7	MEM_VDDQ
SPM DM1	B3	UDM	VDDQ9	G9	MEM_VDDQ
SPM ODT	K9	ODT	VDDQ10	J7	MEM_VDDQ
SPM DQS0P	F7	LDQS	VDDQ11	A7	MEM_VDDQ
SPM DQS0N	E8	LDQS	VDDQ12	B8	MEM_VDDQ
SPM DQS1P	B7	UDQS	VDDQ13	D2	MEM_VDDQ
SPM DQS1N	A8	UDQS	VDDQ14	D8	MEM_VDDQ
SPM VREF	J2	VREF	VDDQ15	E7	MEM_VDDQ
SPM BA2	X2	NC#2	VDDQ16	F8	MEM_VDDQ
	X3	NC#1	VDDQ17	F2	MEM_VDDQ
	X4	NC#3	VDDQ18	H2	MEM_VDDQ
	X5	NC#7	VDDQ19	H8	MEM_VDDQ
	X6	NC#8	VDDQ20	J2	MEM_VDDQ
	X7	NC#9	VDDQ21	J8	MEM_VDDQ
	X8	NC#8	VDDQ22	L2	MEM_VDDQ
	X9	NC#9	VDDQ23	L8	MEM_VDDQ
	X10	NC#1	VDDQ24	M2	MEM_VDDQ
	X11	NC#2	VDDQ25	M8	MEM_VDDQ
	X12	NC#3	VDDQ26	N2	MEM_VDDQ
	X13	NC#7	VDDQ27	N8	MEM_VDDQ
	X14	NC#8	VDDQ28	P2	MEM_VDDQ
	X15	NC#9	VDDQ29	P8	MEM_VDDQ
	X16	NC#1	VDDQ30	R2	MEM_VDDQ
	X17	NC#2	VDDQ31	R8	MEM_VDDQ
	X18	NC#3	VDDQ32	T2	MEM_VDDQ
	X19	NC#7	VDDQ33	T8	MEM_VDDQ
	X20	NC#8	VDDQ34	U2	MEM_VDDQ
	X21	NC#9	VDDQ35	U8	MEM_VDDQ

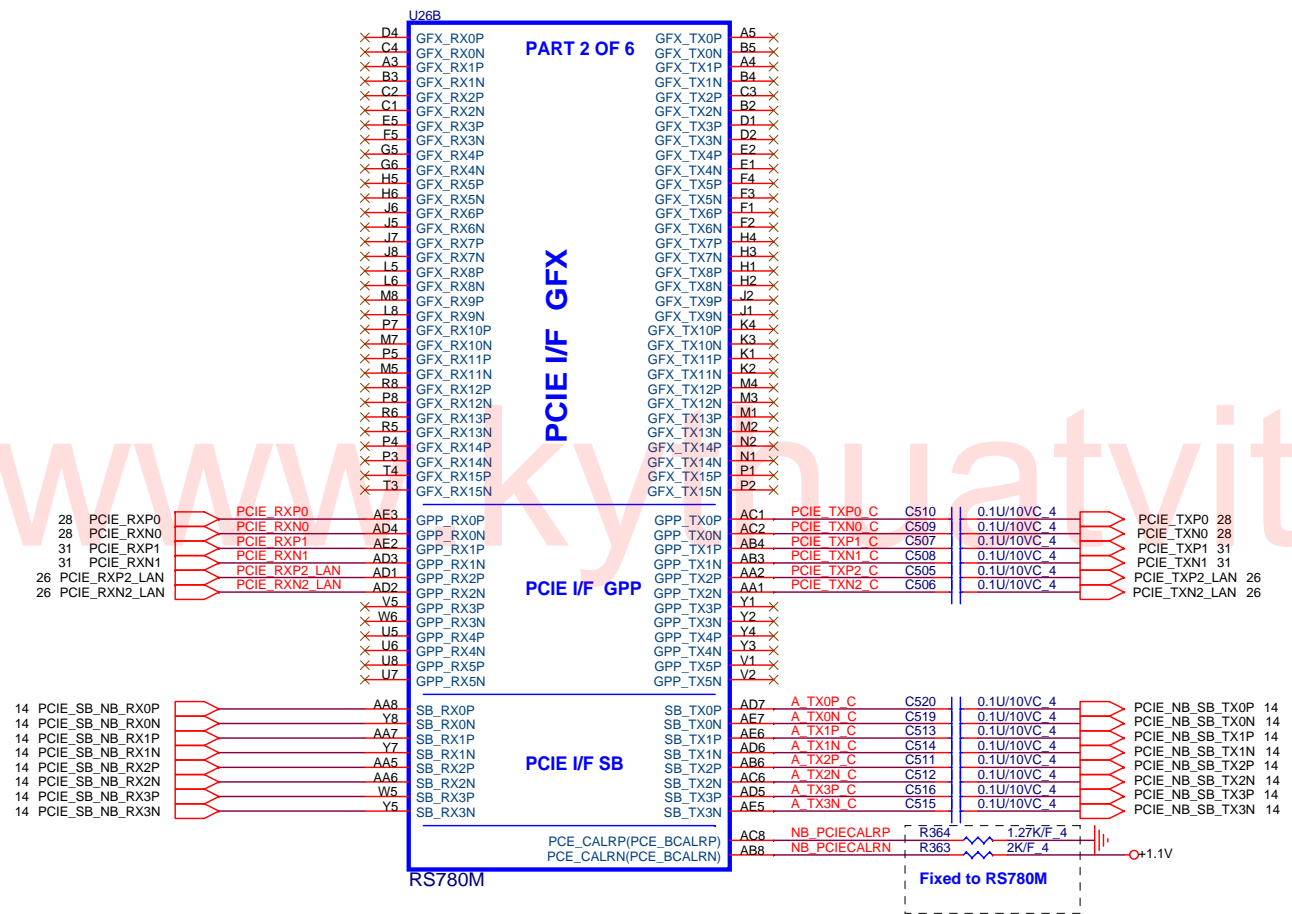


PV modified --
follow AMD
check list to
change part
number 300 ohm
to 301 ohm

PV modified --
follow AMD
check list to
change part
number 300 ohm
to 301 ohm

All external components connected to SPME signals must be removed for RX780

+0.9VSMVTT	6,9,31,36
+1.1V	11,12,13,37
+1.8V	5,12,13,14,15,18,36,38



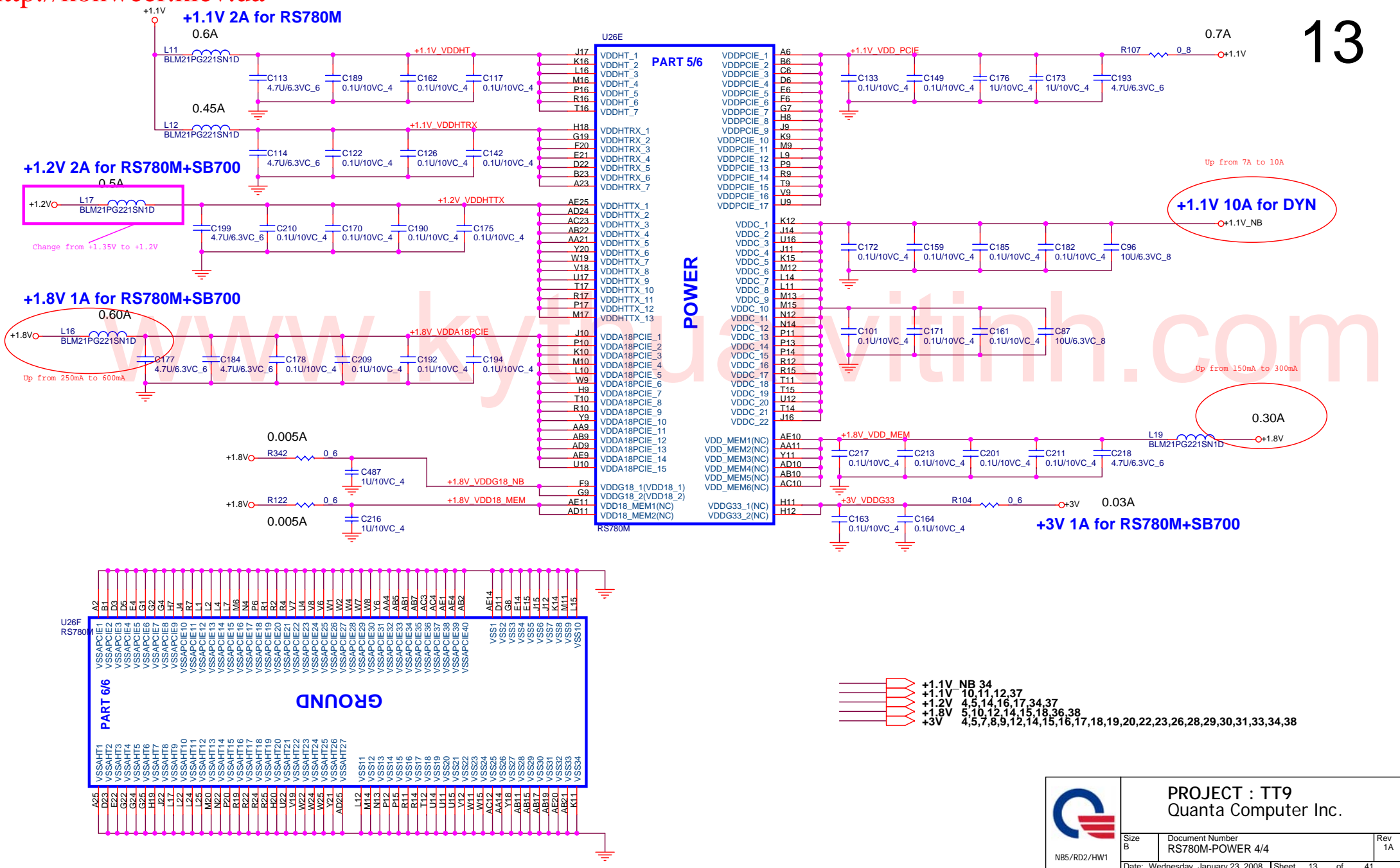
GPP0	EXPRESS CARD (NEW CARD)
GPP1	Wireless Lan
GPP2	PCIE LAN(Realtek)

➔ +1.1V 10,12,13,37



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Size B	Document Number RS780M-PCIE I/F 2/4	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 11 of 41		



- +1.1V NB 34
- +1.1V 10,11,12,37
- +1.2V 4,5,14,16,17,34,37
- +1.8V 5,10,12,14,15,18,36,38
- +3V 4,5,7,8,9,12,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38

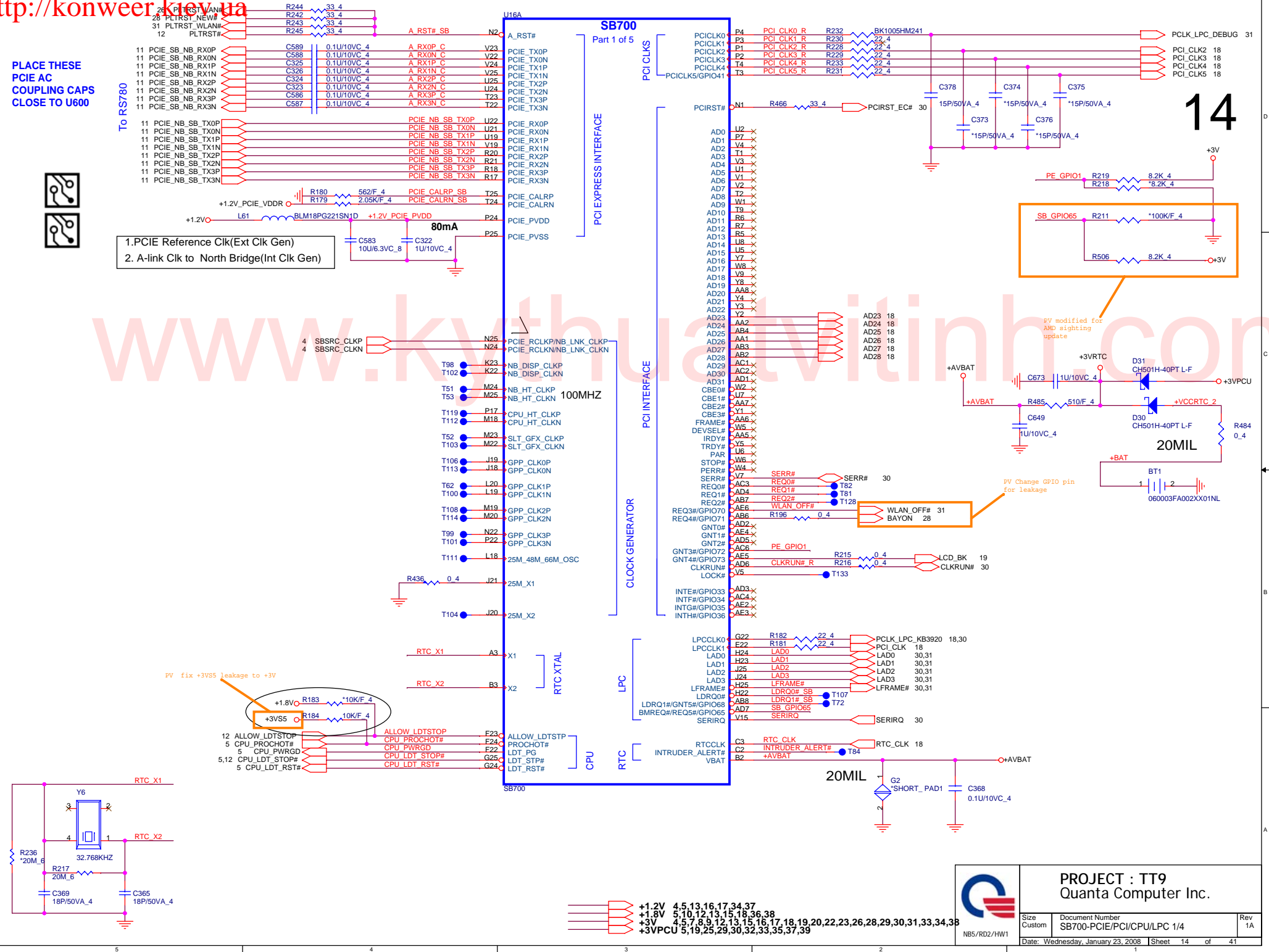
			PROJECT : TT9 Quanta Computer Inc.		
NB5/RD2/HW1			Date: Wednesday, January 23, 2008	Sheet 13	of 41

PLACE THESE
PCIIE AC
COUPLING CAPS
CLOSE TO U600

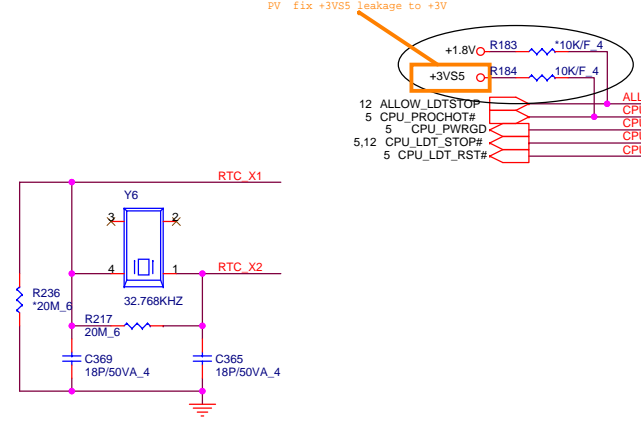
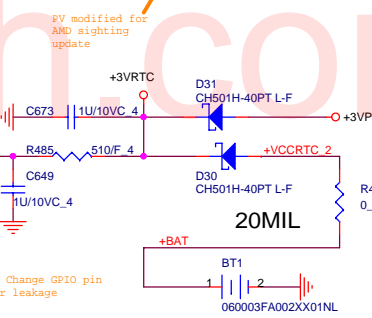
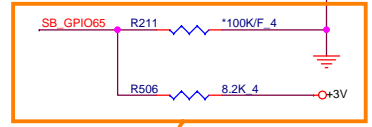


To RS780

- 1. PCIE Reference Clk (Ext Clk Gen)
- 2. A-link Clk to North Bridge (Int Clk Gen)



14



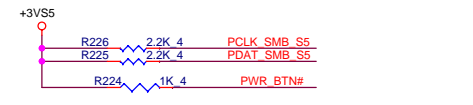
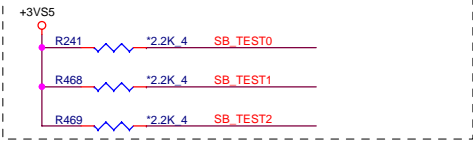
- +1.2V 4,5,13,16,17,34,37
- +1.8V 5,10,12,13,15,18,36,38
- +3V 4,5,7,8,9,12,13,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38
- +3VPCU 5,19,25,29,30,32,33,35,37,39



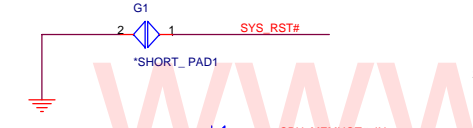
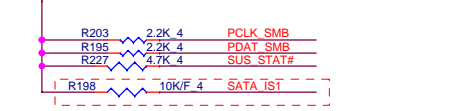
PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number SB700-PCIE/PCI/CPU/LPC 1/4	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 14 of 41		

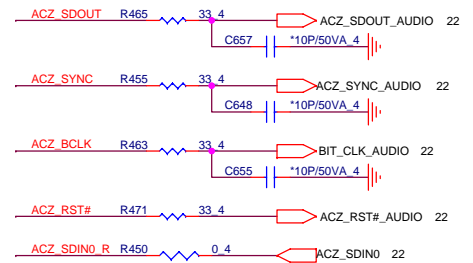
SB700 SBTEST0/1/2 has internal 10K PD.



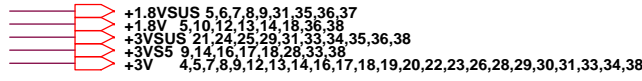
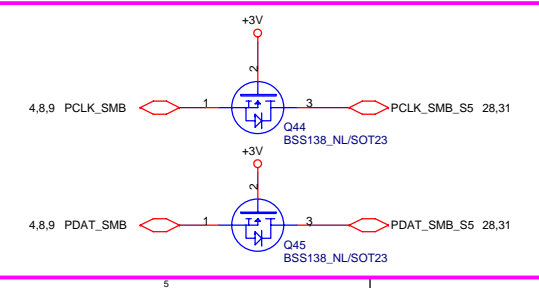
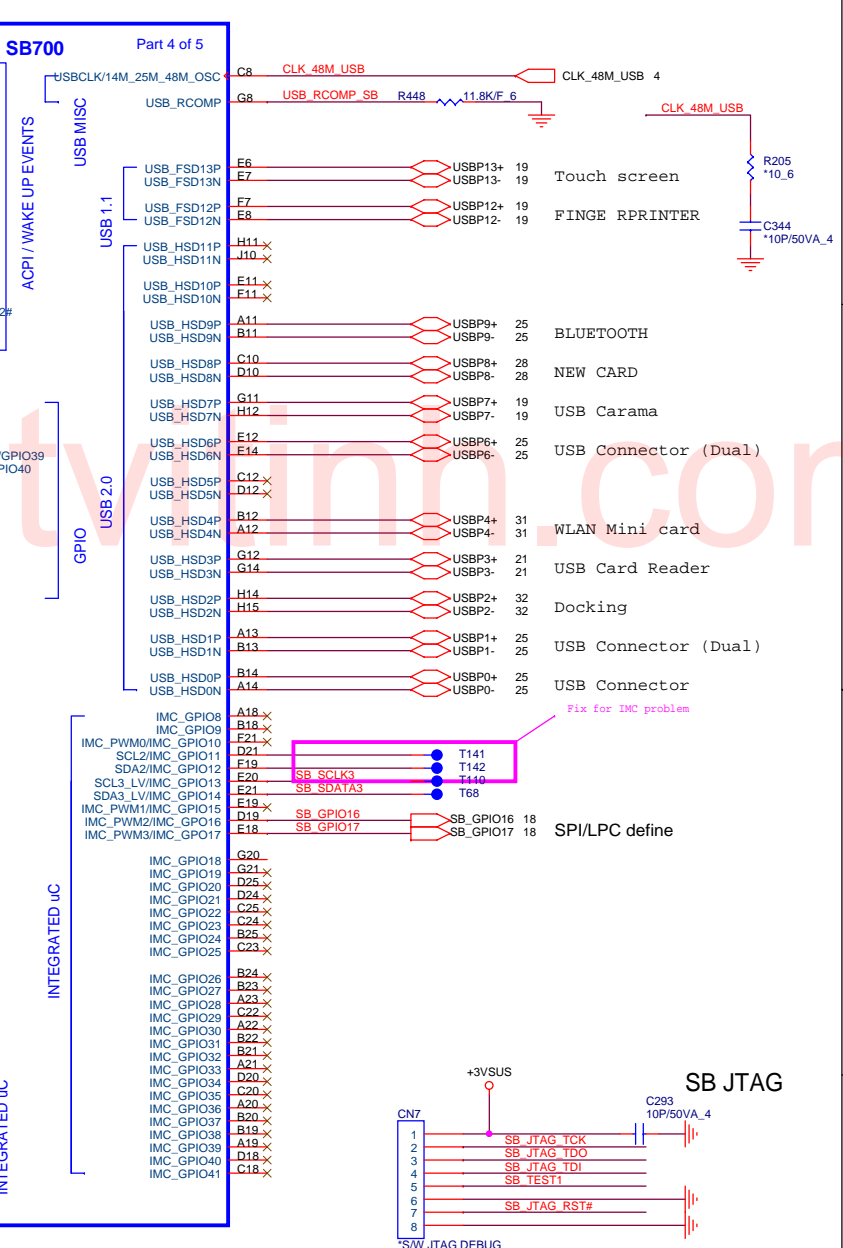
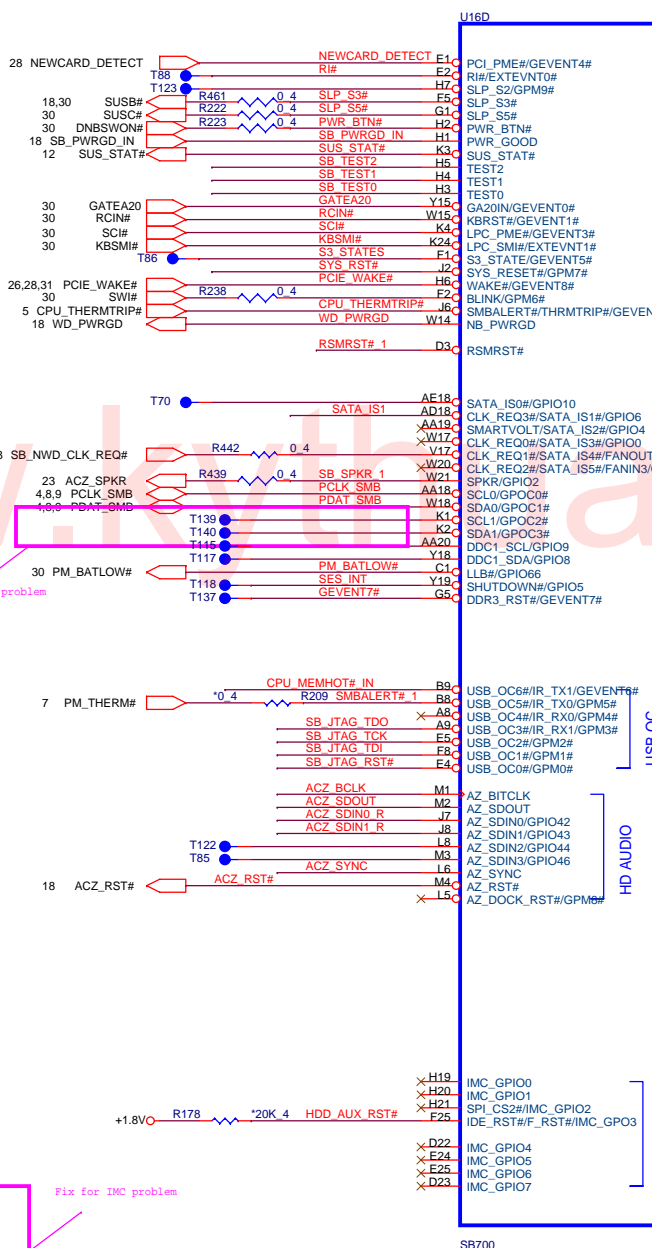
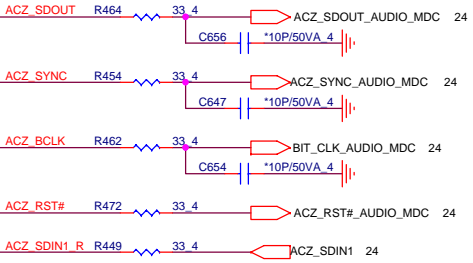
For SATA ODD hot plug



To Azalia



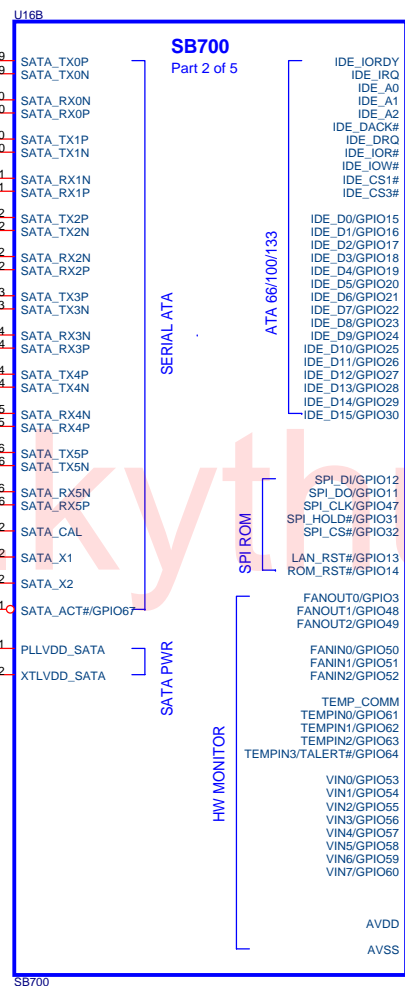
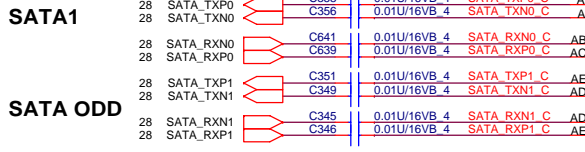
To Modem Board



PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number SB700-ACPI/GPIO/USB 2/4	Rev 1A
Date: Wednesday, January 23, 2008		Sheet 15 of 41

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

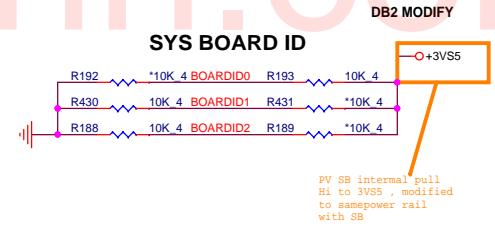
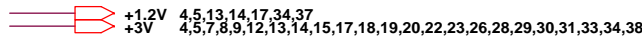
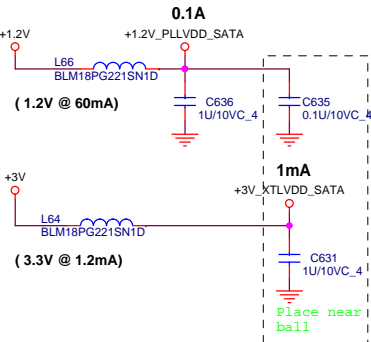
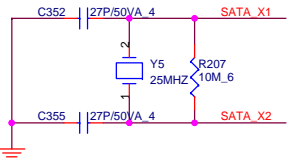
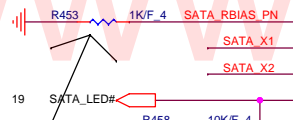


IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

VRAM / Clock Gen	Samsung Realtek	Qimonda ICS	Hynix Siligo
Board ID	(0.0.0)	(1.0.0)	(0.1.0)
BOARDID0	R192 Stuff	R193 Stuff	R192 Stuff
BOARDID1	R430 Stuff	R430 Stuff	R431 Stuff
BOARDID2	R188 Stuff	R188 Stuff	R188 Stuff

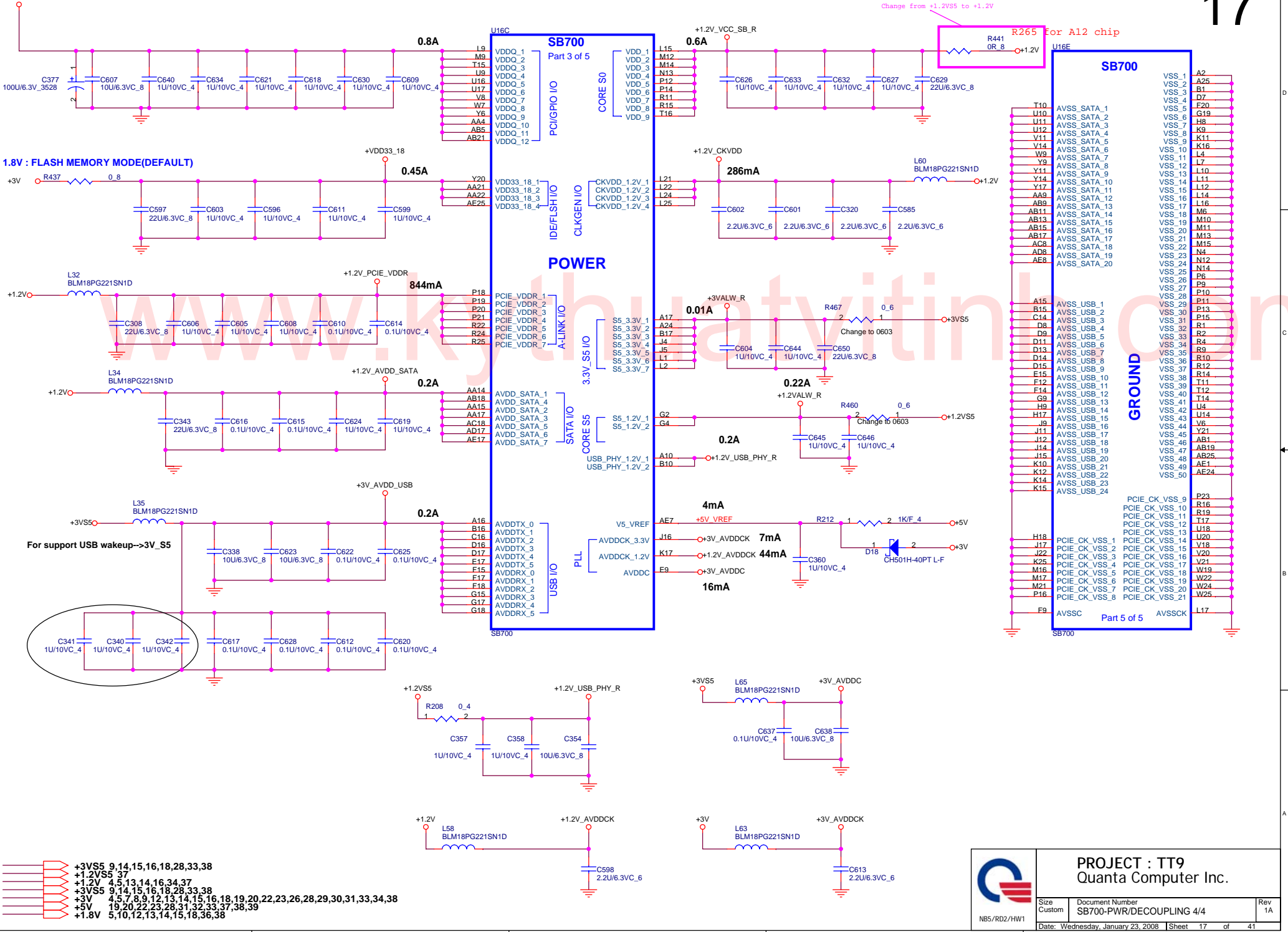
PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

NOTE:
R635 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK



PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number SB700-SATA/IDE/HWM/SPI 3/4	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 16 of 41		

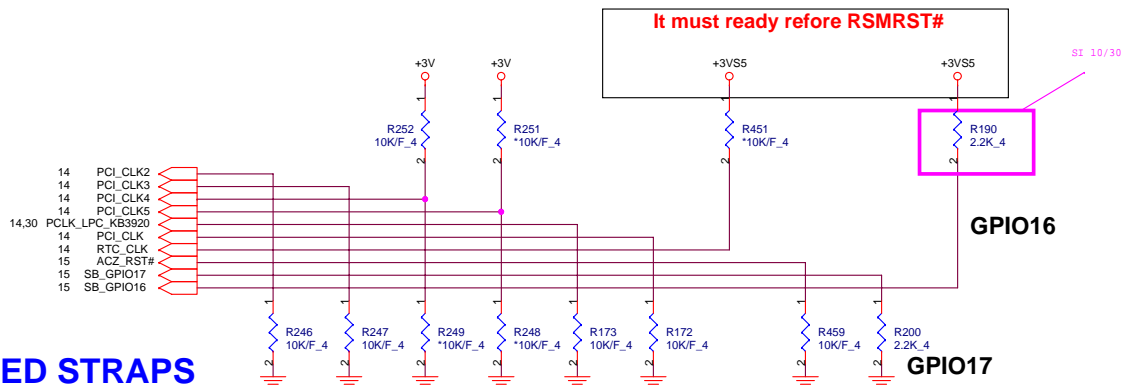


- +3V_S5 9,14,15,16,18,28,33,38
- +1.2V_V55 37
- +1.2V_V55 4,5,13,14,16,34,37
- +3V_S5 9,14,15,16,18,28,33,38
- +3V 4,5,7,8,9,12,13,14,15,16,18,19,20,22,23,26,28,29,30,31,33,34,38
- +5V 19,20,22,23,28,31,32,33,37,38,39
- +1.8V 5,10,12,13,14,15,18,36,38



PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number SB700-PWR/DECOUPLING 4/4	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 17 of 41		



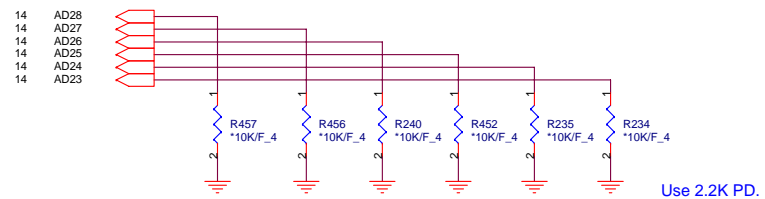
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

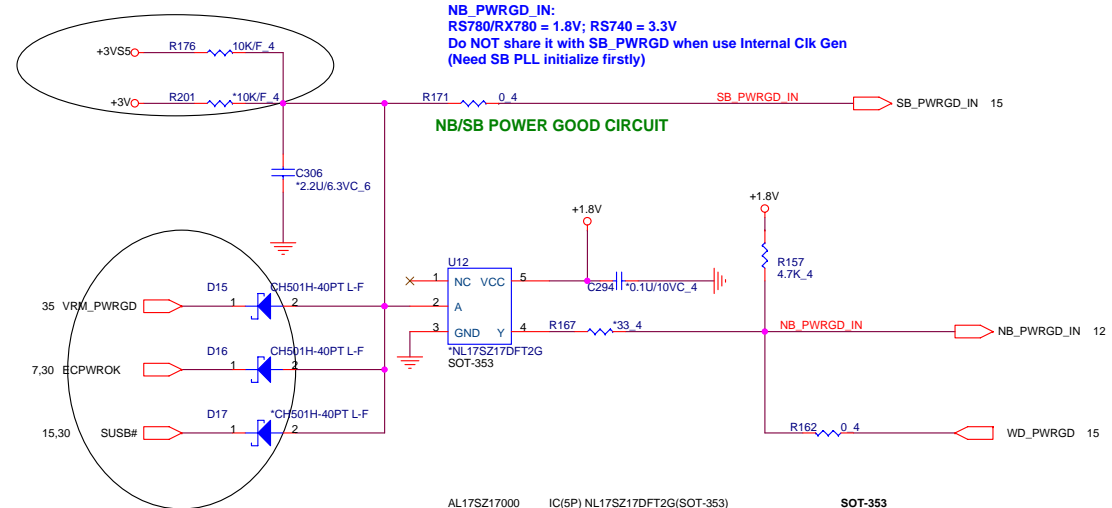
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCLK_LPC_KB3920	PCI_CLK	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC <small>DEFAULT</small>	ENABLE PCI MEM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED <small>DEFAULT</small>	IGNORE DEBUG STRAPS <small>DEFAULT</small>			EC DISABLED <small>DEFAULT</small>	CLKGEN DISABLED <small>DEFAULT</small>	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT <small>DEFAULT</small>	L, H = LPC ROM L, L = FWH ROM <small>DEFAULT</small>	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



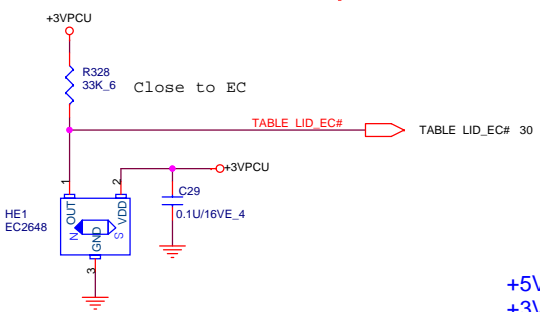
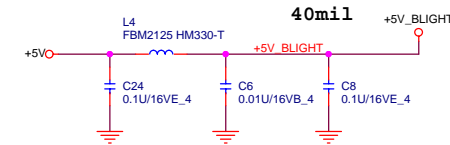
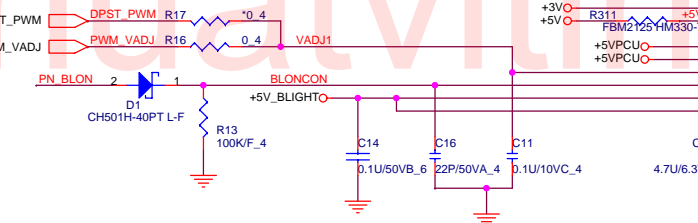
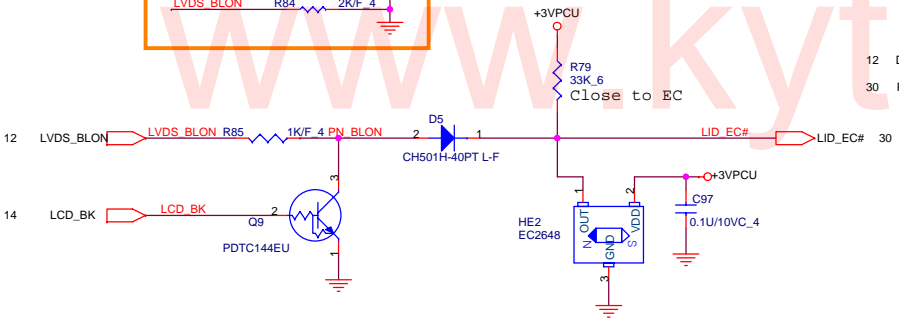
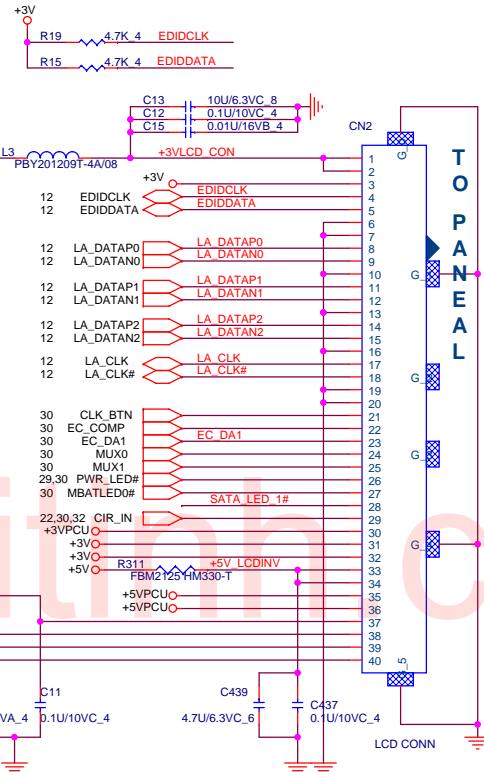
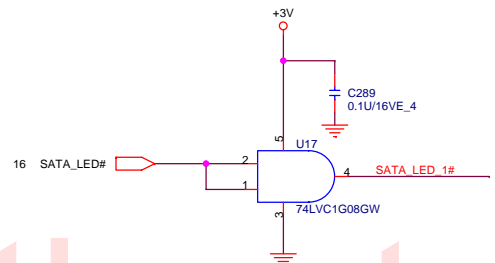
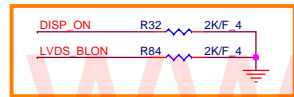
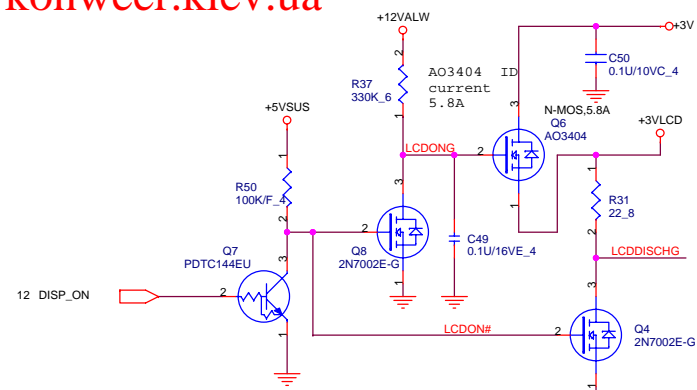
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET <small>DEFAULT</small>	USE PCI PLL <small>DEFAULT</small>	USE ACPI BCLK <small>DEFAULT</small>	USE IDE PLL <small>DEFAULT</small>	USE DEFAULT PCIE STRAPS <small>DEFAULT</small>	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



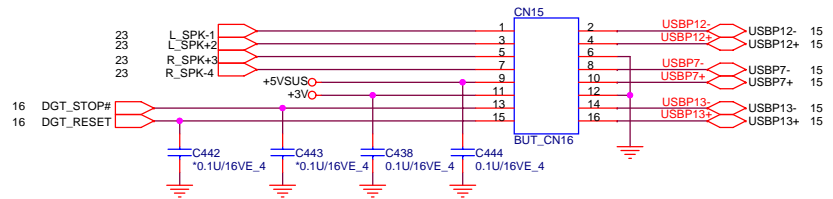
NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

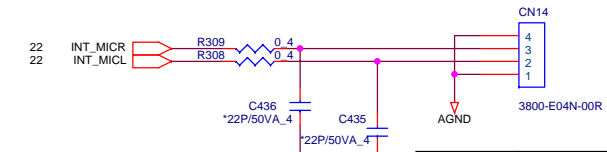
Legend for power supply connections:
 +1.8V 5,10,12,13,14,15,36,38
 +3V 4,5,7,8,9,12,13,14,15,16,17,19,20,22,23,26,28,29,30,31,33,34,36
 +3V5S 9,14,15,16,17,28,33,38



Speaker
+5VSUS --> Camera
+3V --> FP/Digitizer
Digitizer control signal



Finger Printer
Camera
Digitizer

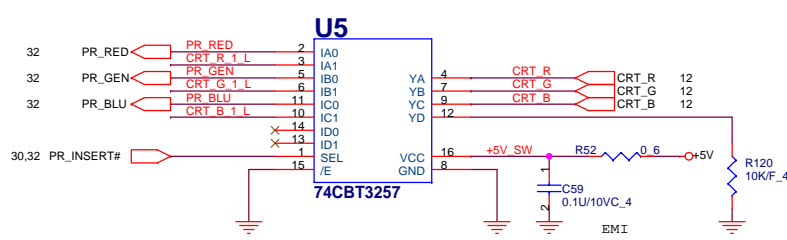


- +3VPCU 5,14,25,29,30,32,33,35,37,39
- +3V 4,5,7,8,9,12,13,14,15,16,17,18,20,22,23,26,28,29,30,31,33,34,38
- +3VSUS 15,21,24,25,29,31,33,34,35,36,38
- +5V 17,20,22,23,28,31,32,33,37,38,39
- +12VALW 28,31,33,38

PROJECT : TT9
Quanta Computer Inc.

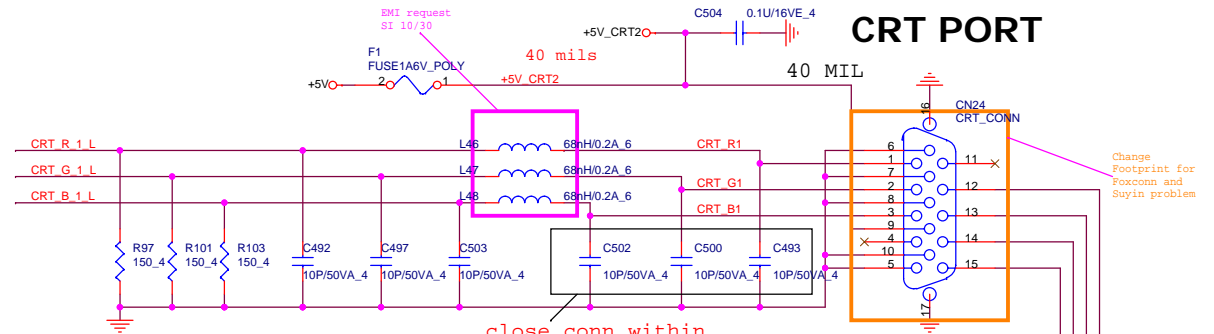
Size Custom Document Number LCD CONN,HDMI CONN Rev 1A
Date: Wednesday, January 23, 2008 | Sheet 19 of 41

CRT SWITCH



inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

CRT PORT

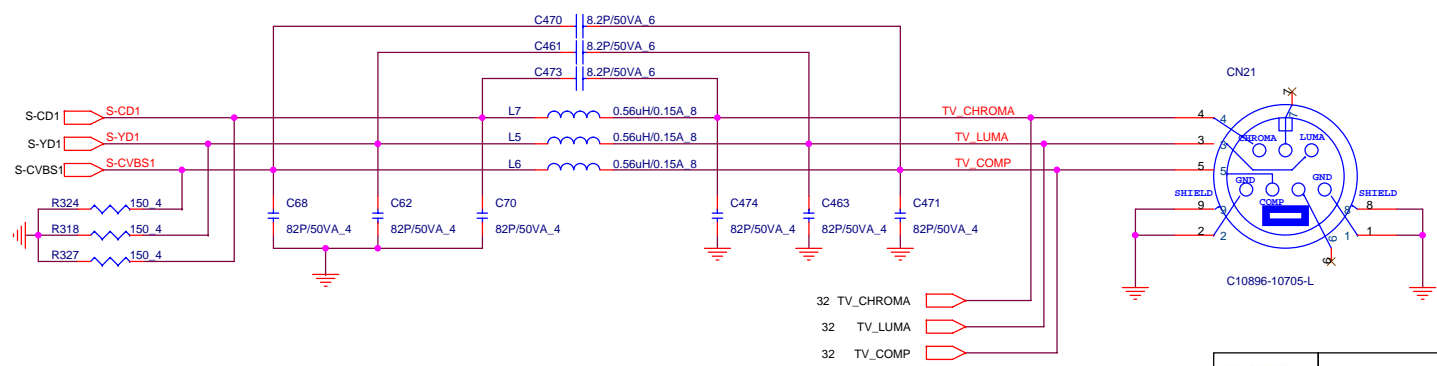
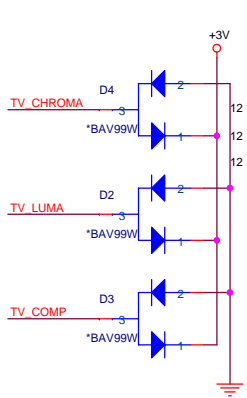
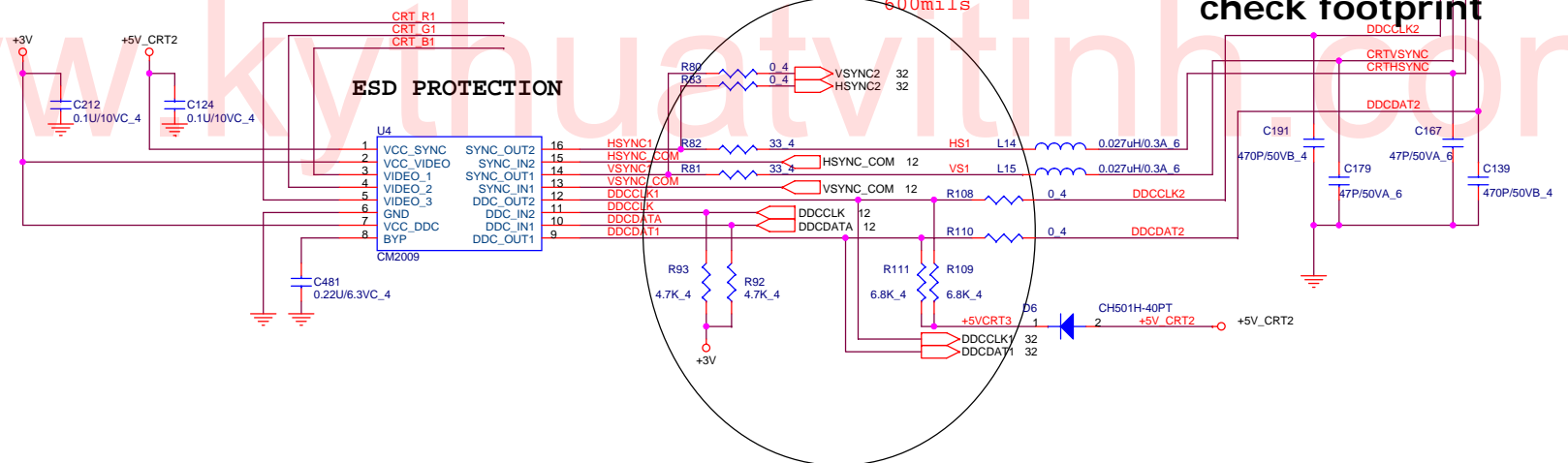


Change Footprint for Foxconn and Suyin problem

close conn within 600mils

check footprint

ESD PROTECTION

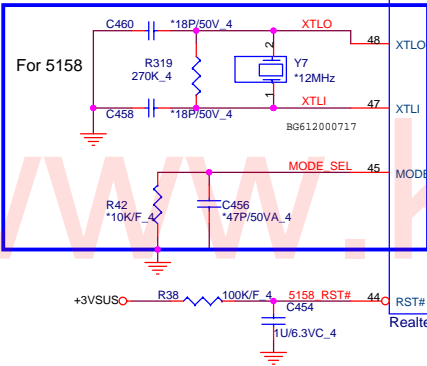
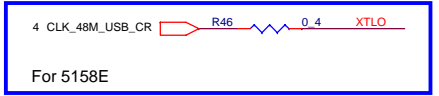


+3V 4,5,7,8,9,12,13,14,15,16,17,18,19,22,23,26,28,29,30,31,33,34,38
+5V 17,19,22,23,28,31,32,33,37,38,39

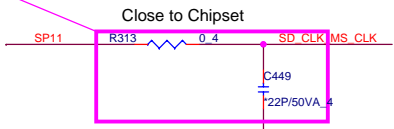
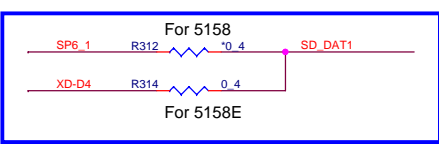
PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number CRT_TV_OUT	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 20 of 41		

Fix card reader led problem



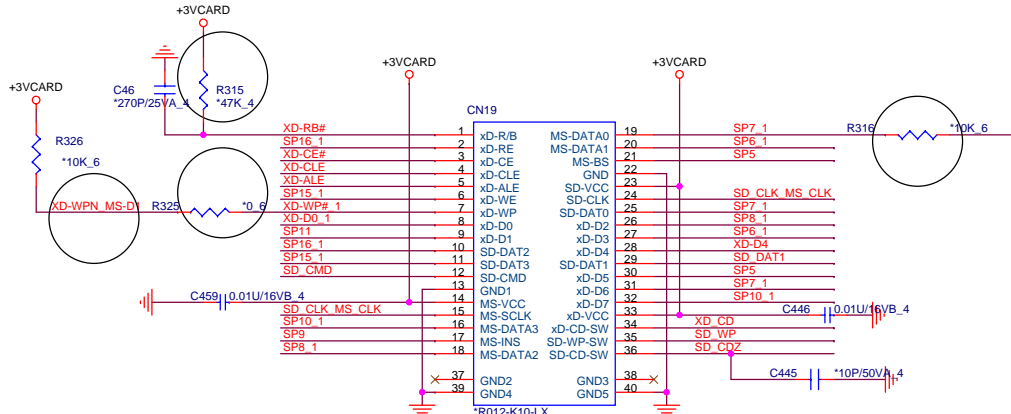
43	XD-CLE
42	XD-CE#
41	XD-ALE
40	SD_DAT2/XD_RE#/CF_D12
39	SD_DAT3/XD_WE#/CF_D5
38	XD-RB#
37	XD-WP#
36	SD_CMD
35	XD-D0
34	SP11
33	SP10
32	SD_CMD
31	SP10
30	SP9
29	SP8
28	SP7
27	SP6
26	SP5
25	SP5



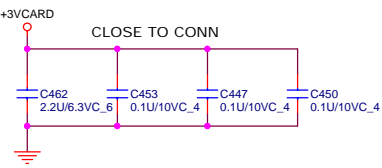
Note:

SP0	SD/MMC	MS	XD
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4			XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

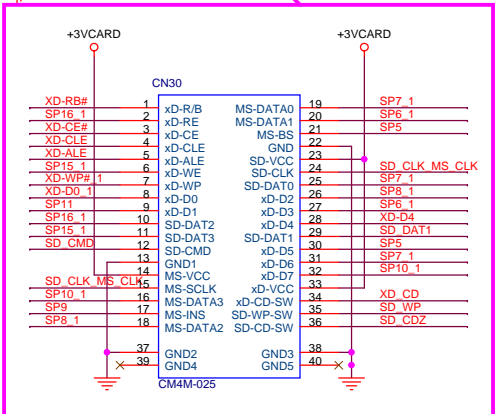
4 IN1 CARD READER XD, MMC / SD, MS / MSP



- SP7 R39 56.4 SP7_1
- SP8 R44 56.4 SP8_1
- SP10 R48 56.4 SP10_1
- XD-D0 R55 56.4 XD-D0_1
- XD-WP# R58 56.4 XD-WP#_1
- SP15 R59 56.4 SP15_1
- SP16 R61 56.4 SP16_1
- SP6 R502 56.4 SP6_1



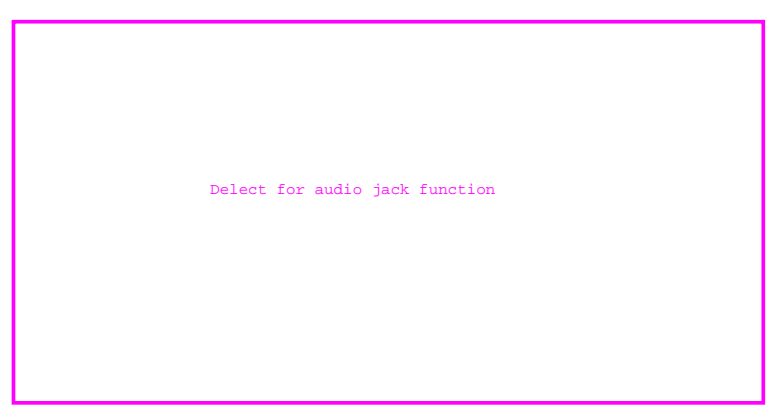
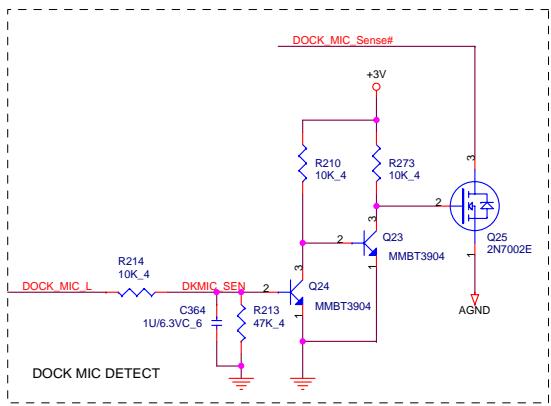
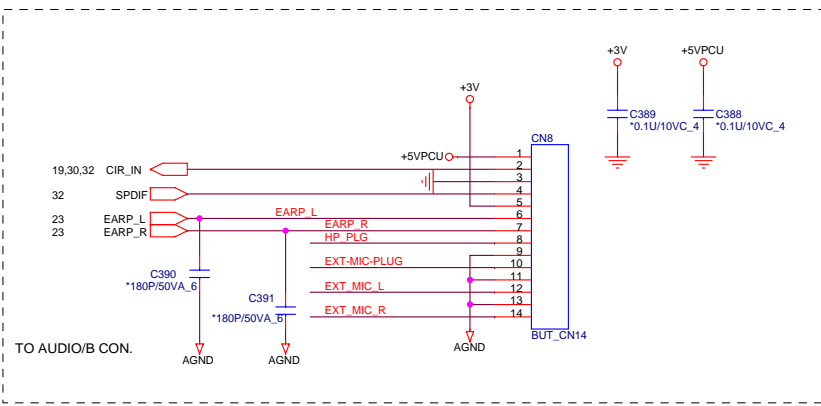
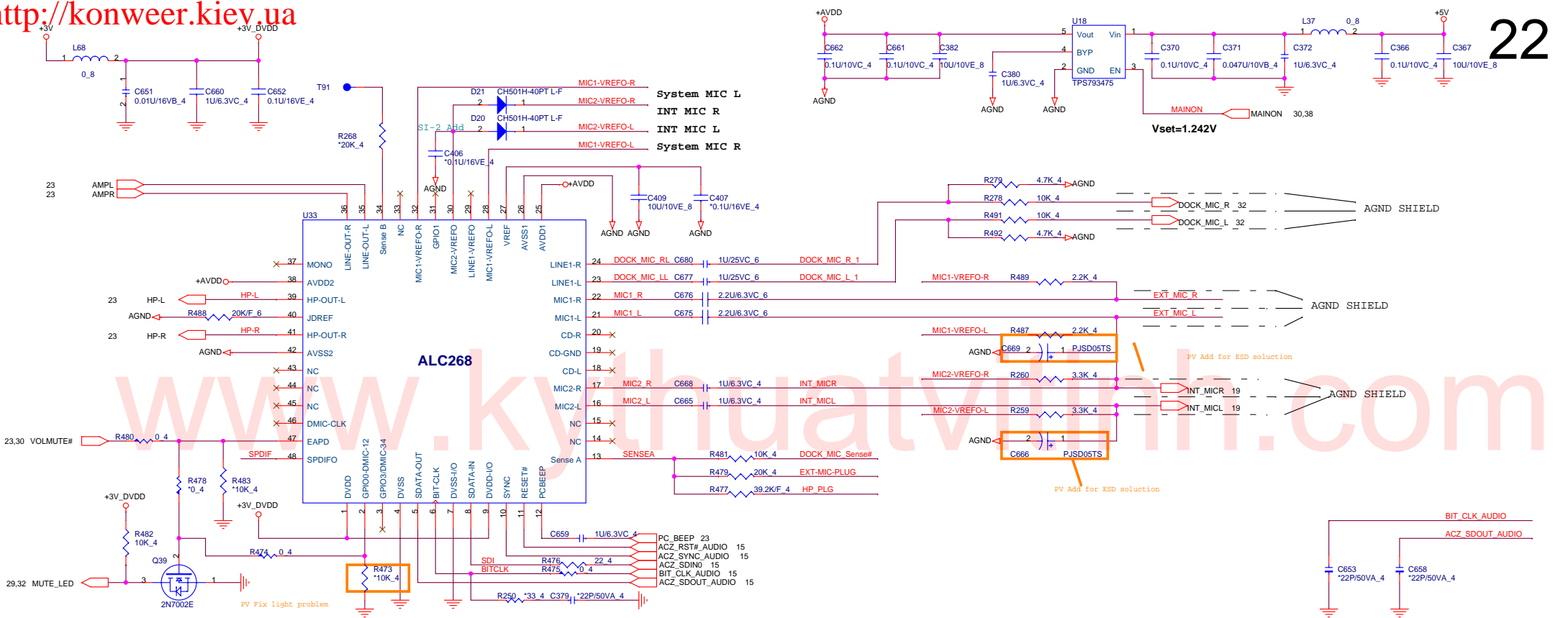
Add Connector for joint



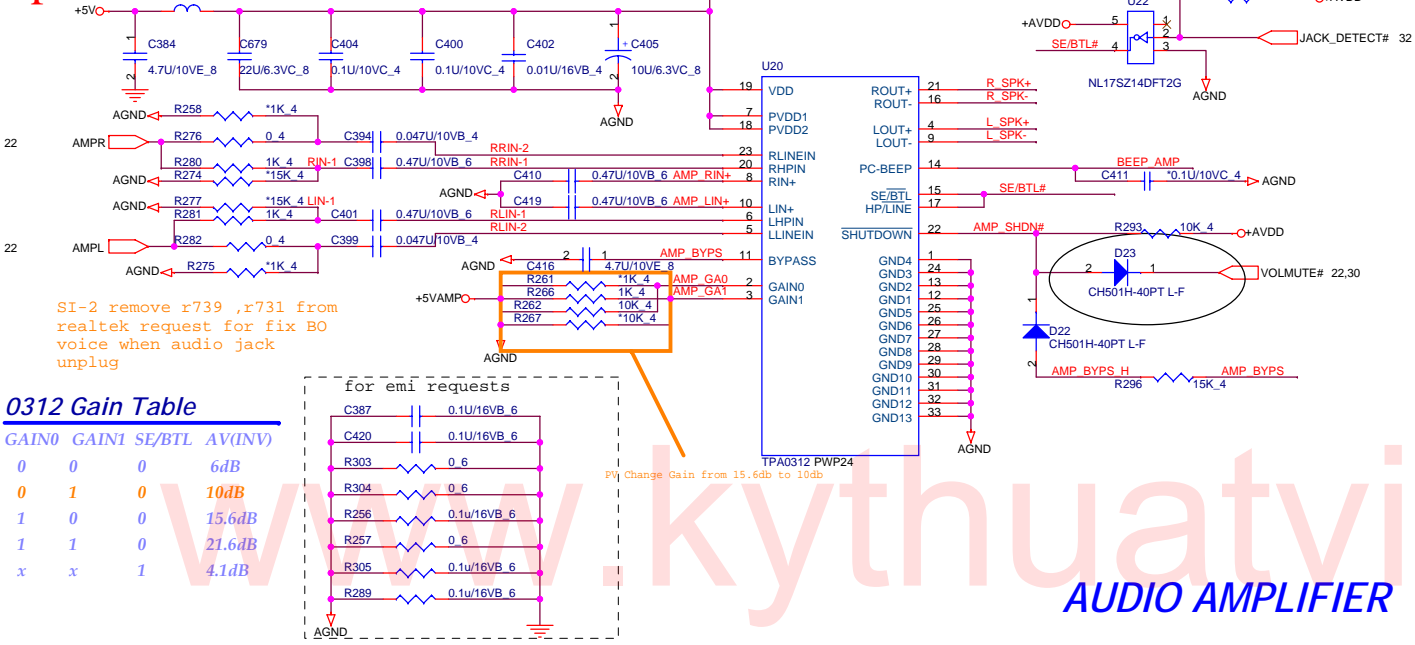
Remove Acces from HP information



PROJECT : TT9
Quanta Computer Inc.



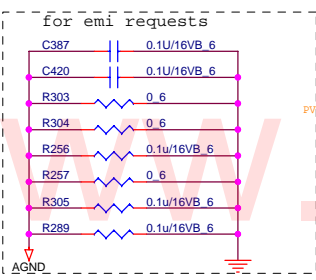
- +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,23,26,28,29,30,31,33,34,38
- +5V 17,19,20,23,28,31,32,33,37,38,39
- +AVDD 23
- +5VPCU 19,28,29,30,33,34,35,36,37



SI-2 remove r739 ,r731 from realtek request for fix B0 voice when audio jack unplug

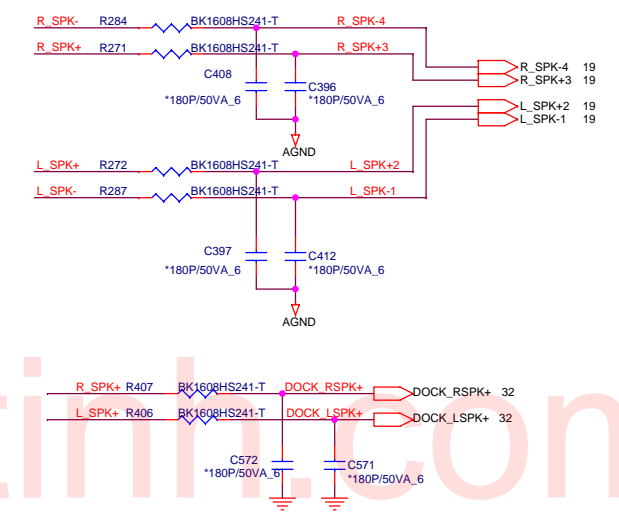
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

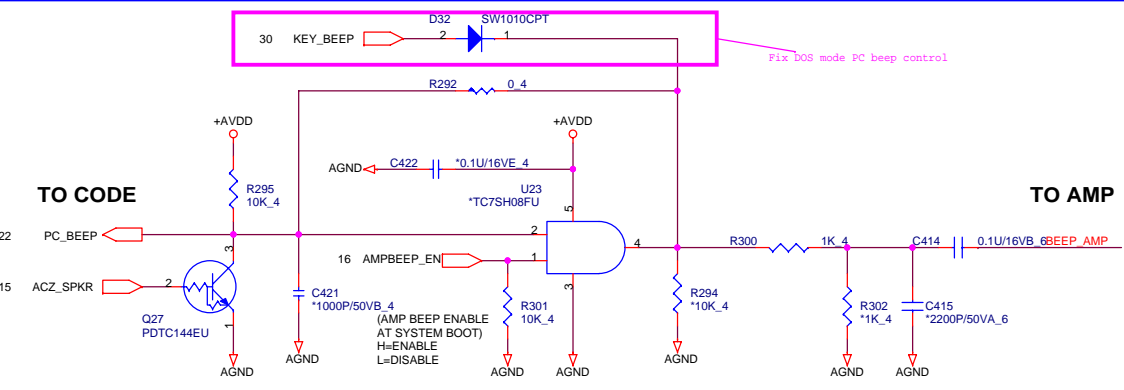


Change Gain from 15.6db to 10db

AUDIO AMPLIFIER

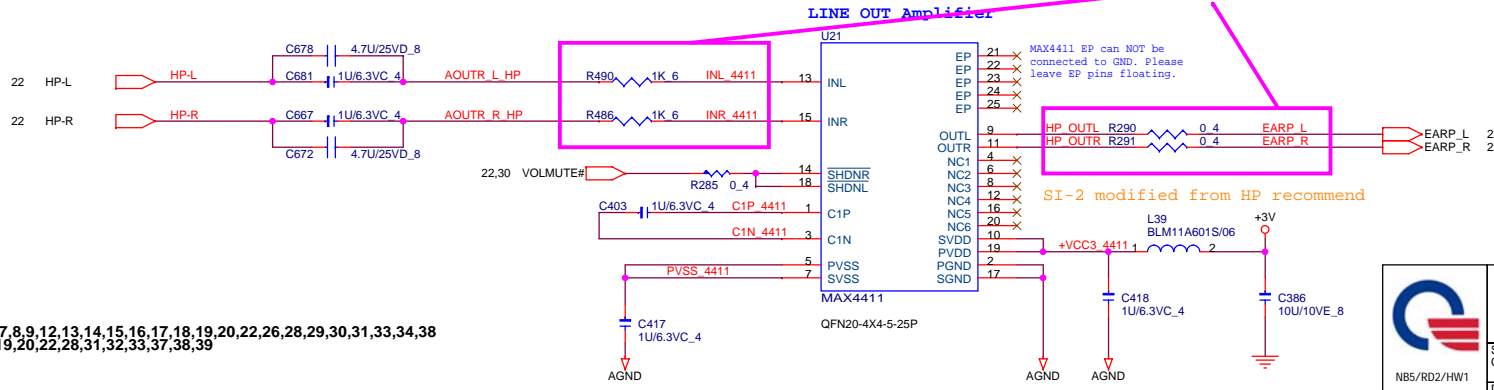


PCSPK BEEP



Fix DOS mode PC beep control

LINE OUT Amplifier



MAX4411 EP can NOT be connected to GND, Please leave EP pins floating.

SI-2 modified from HP recommend

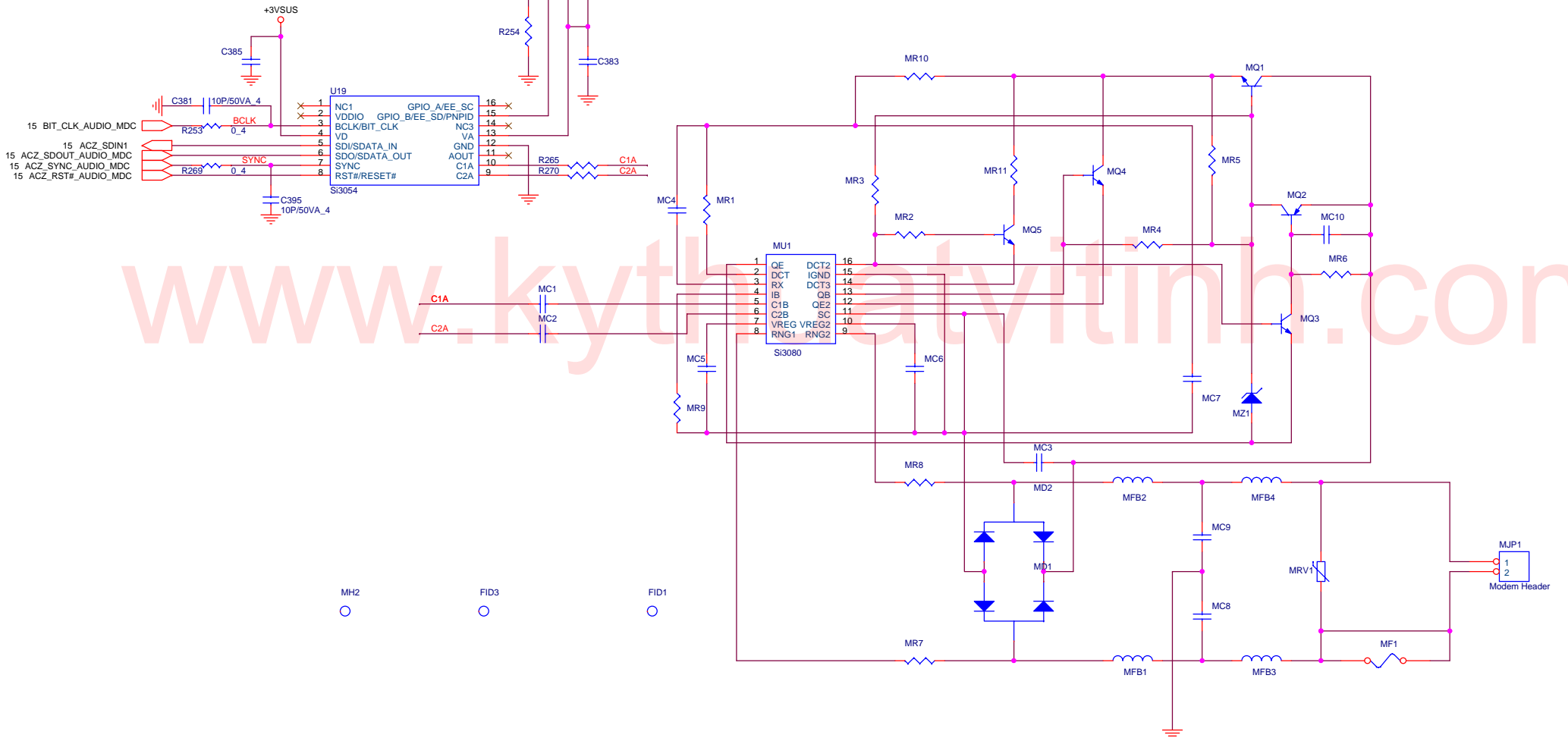
- +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,26,28,29,30,31,33,34,38
- +5V 17,19,20,22,28,31,32,33,37,38,39
- +AVDD 22

PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number JACK/AMP_TAP0312	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 23 of 41		

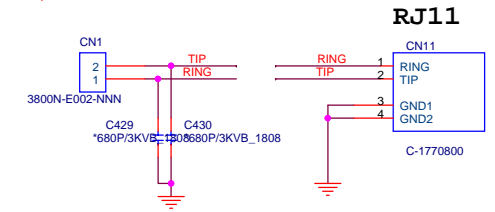
No Ground Plane In DAA Section


Homologation Area



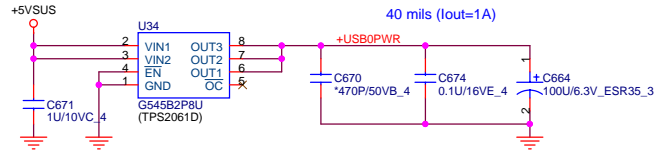
DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL

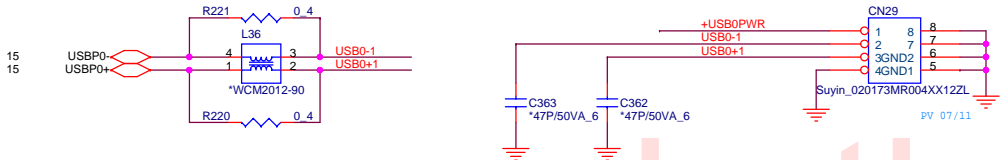


 NB5/RD2/HW1	PROJECT : TT9 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number MODEM (DAA)	Date: Wednesday, January 23, 2008 Sheet 24 of 41

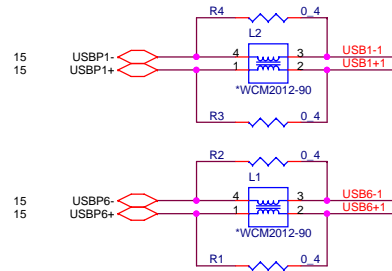
USBX1



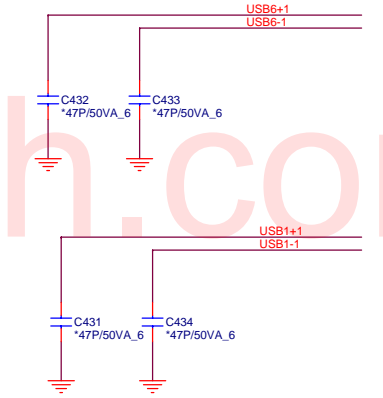
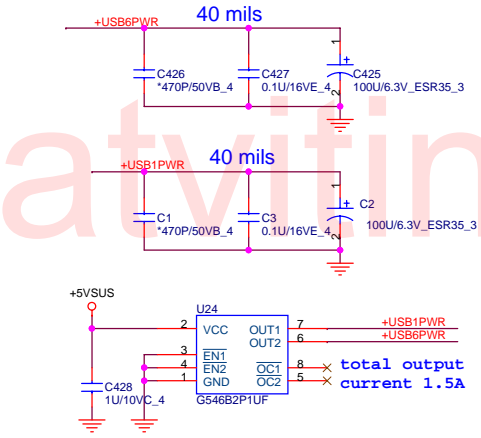
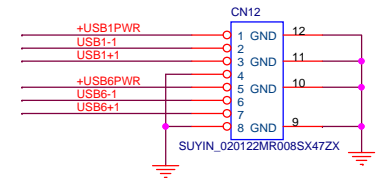
USB 0



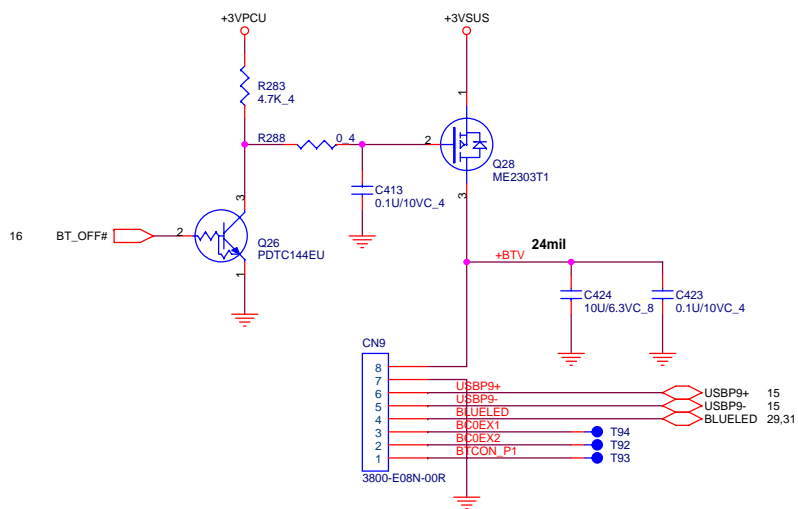
USBX2



USB 1 & 6



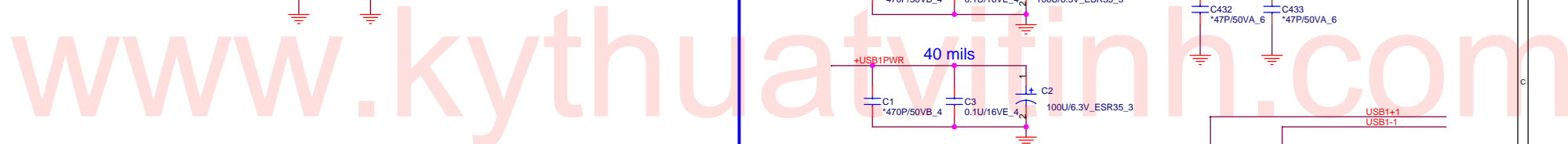
BLUETOOTH

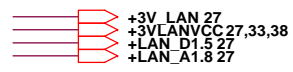
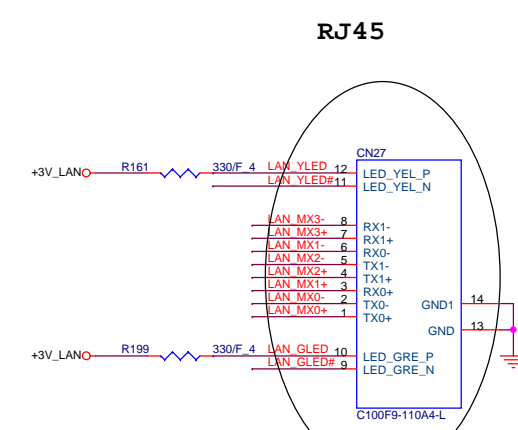
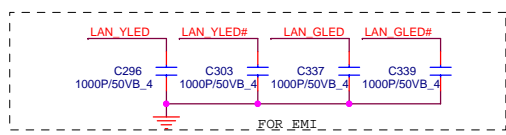
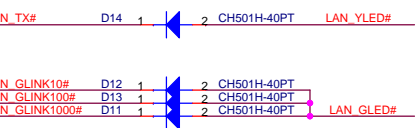
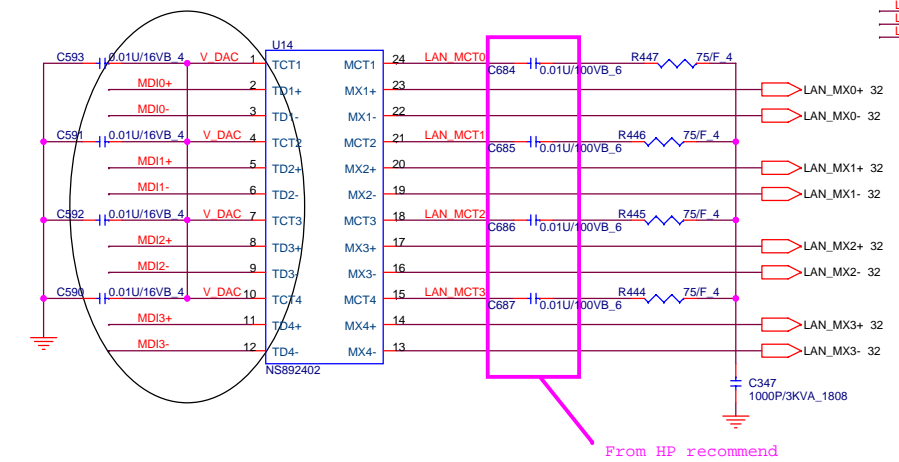
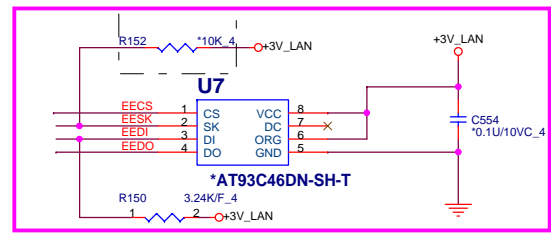
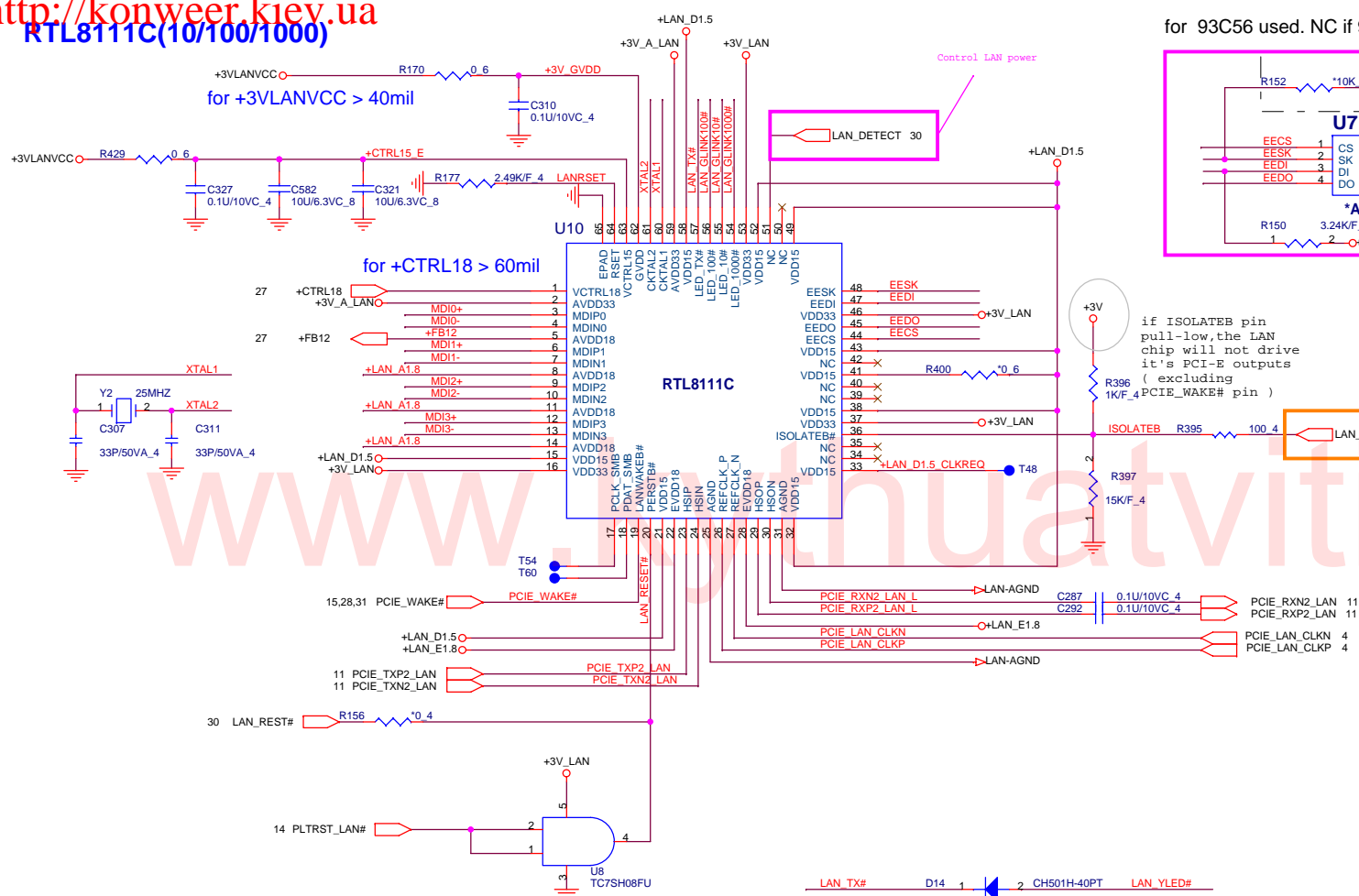


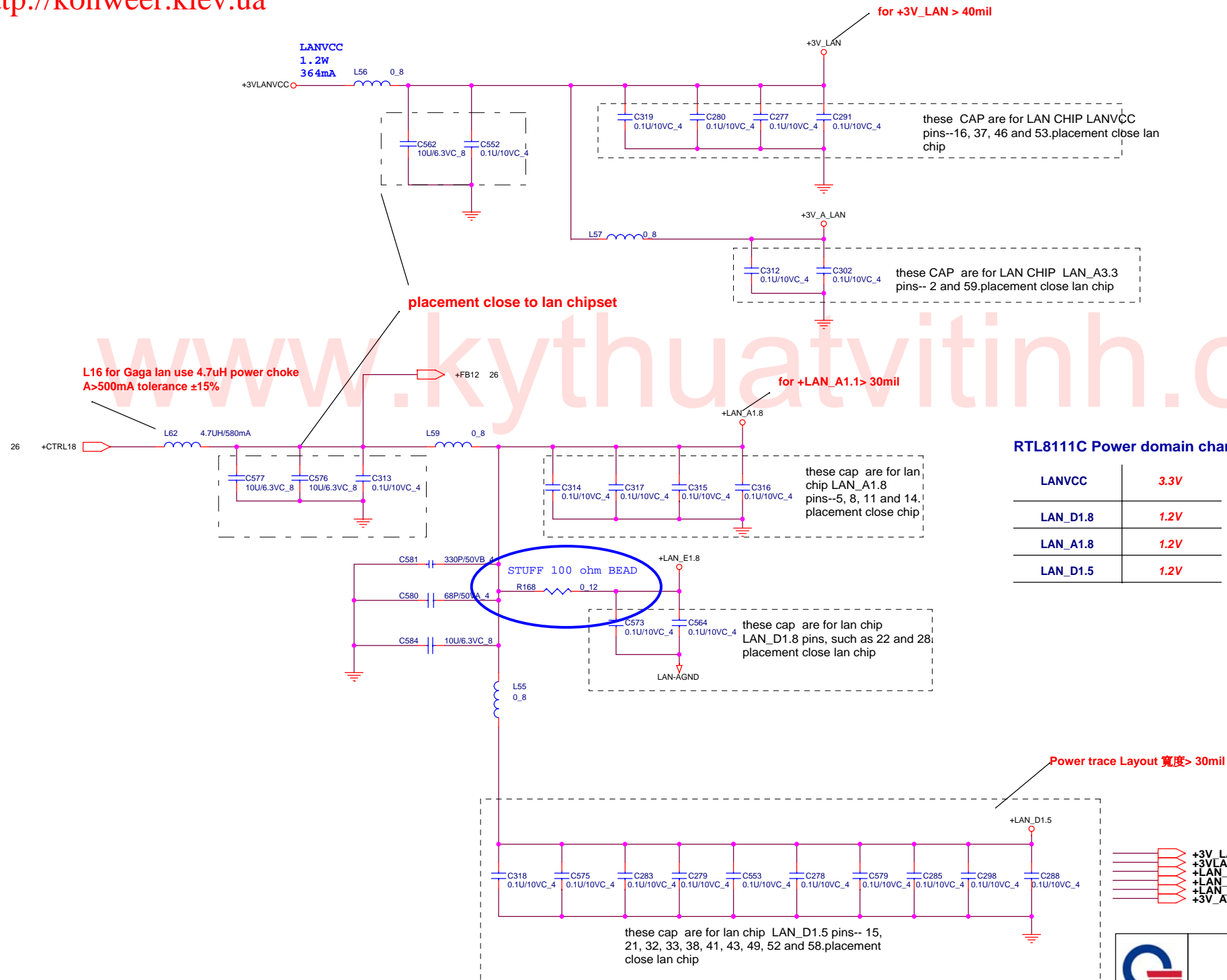
Select TPM function from HP information

- +3VPCU 5,14,19,29,30,32,33,35,37,39
- +3VSUS 15,21,24,29,31,33,34,35,36,38
- +5VSUS 19,30,32,33,38

			PROJECT : TT9	
			Quanta Computer Inc.	
Size Custom	Document Number Blue Tooth/USBX3	Rev 1A		
Date: Wednesday, January 23, 2008 Sheet 25 of 41				







RTL8111C Power domain chart

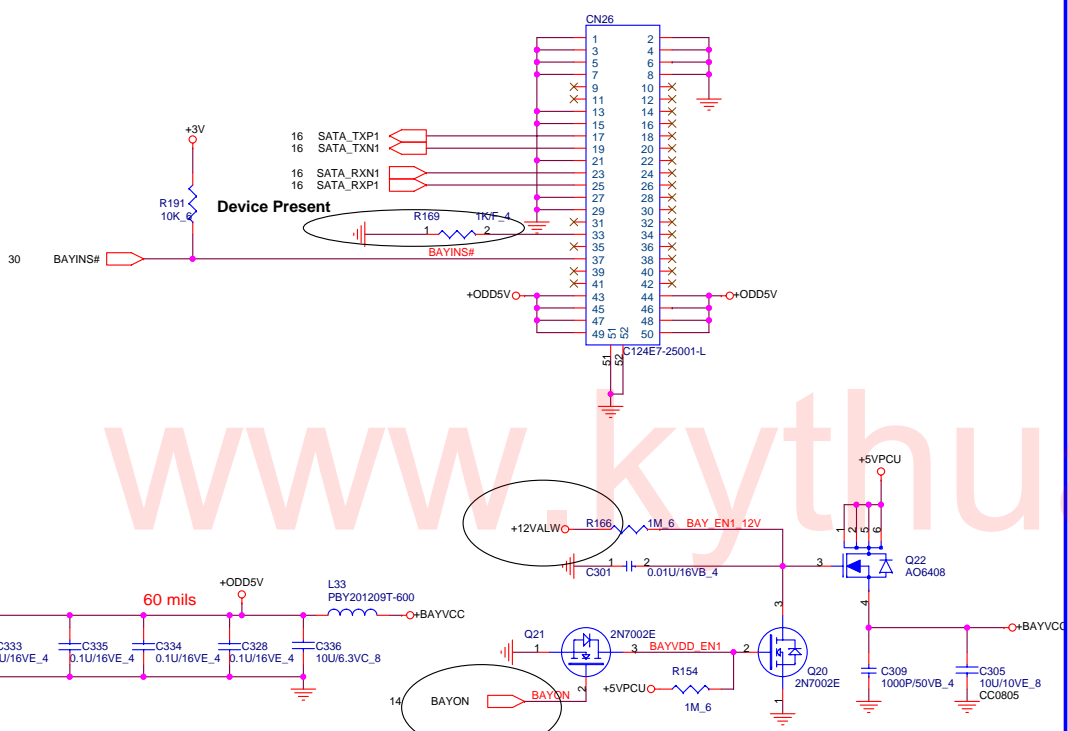
LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V

- +3V_LAN 26
- +3VLANVCC 26,33,38
- +LAN_D1.8 26
- +LAN_A1.8 26
- +LAN_E1.8 26
- +3V_A_LAN 26



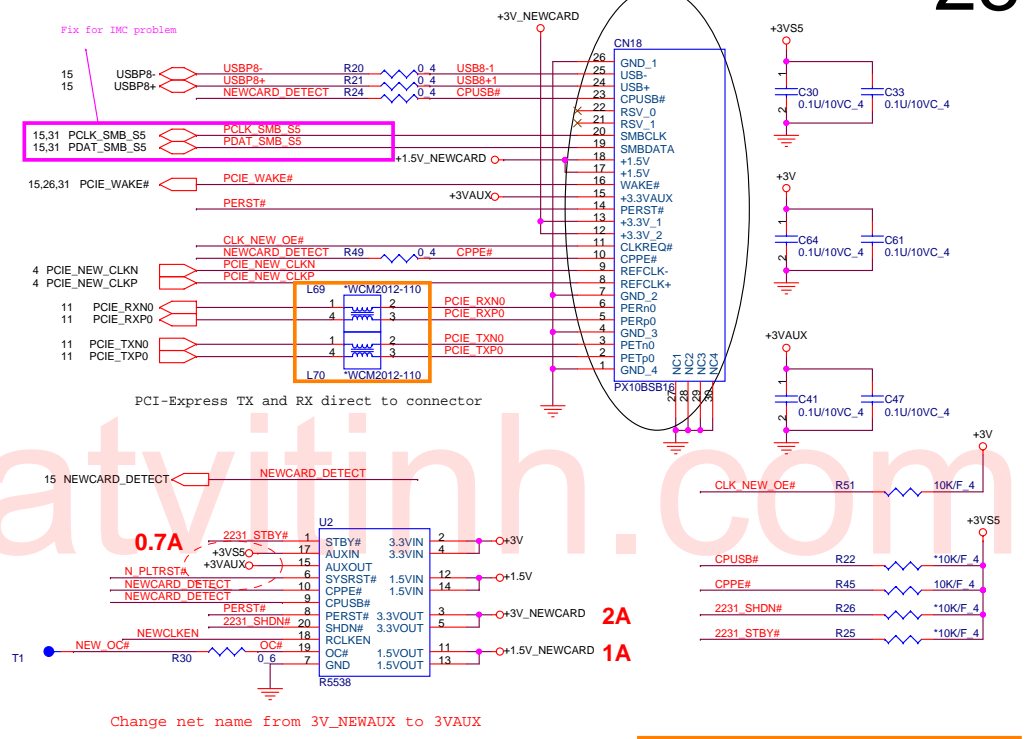
PROJECT : TT9
Quanta Computer Inc.

SATA ODD

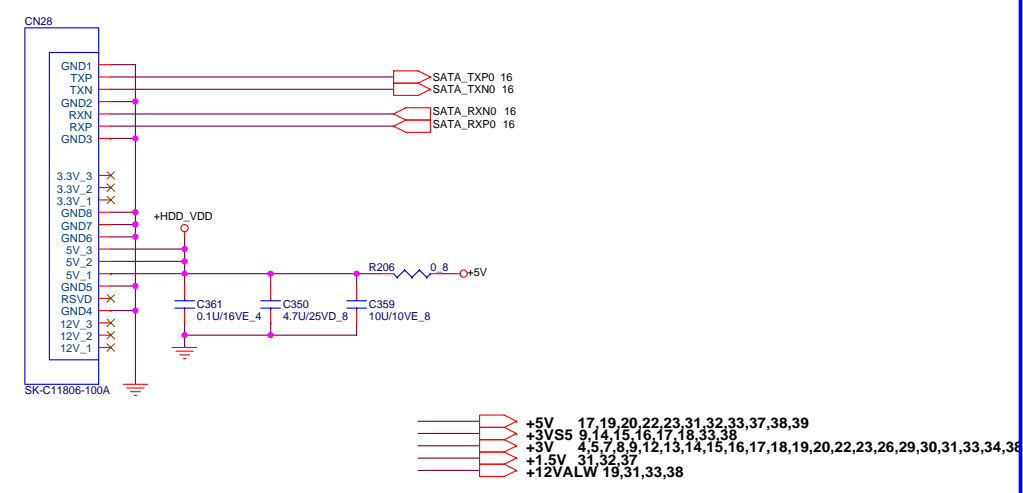


NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)



SATA CONNECTOR

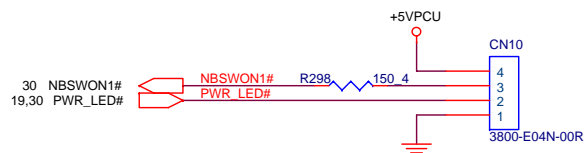


PROJECT : TT9
Quanta Computer Inc.

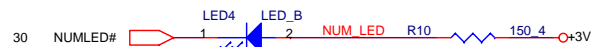
Size Custom	Document Number NEW_CARD/SATA ODD/SATA HDD	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 28 of 41		

NB5/RD2/HW1

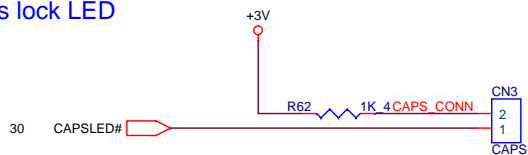
FOR POWER ON SW BOARD



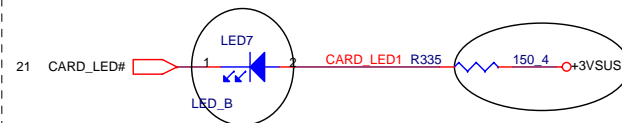
Num lock LED



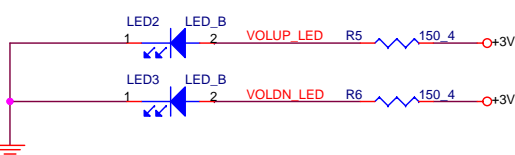
Caps lock LED



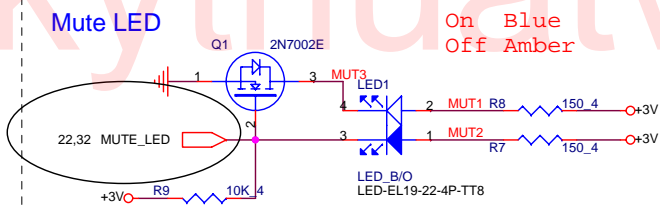
Card Reader LED



Volume up/down LED

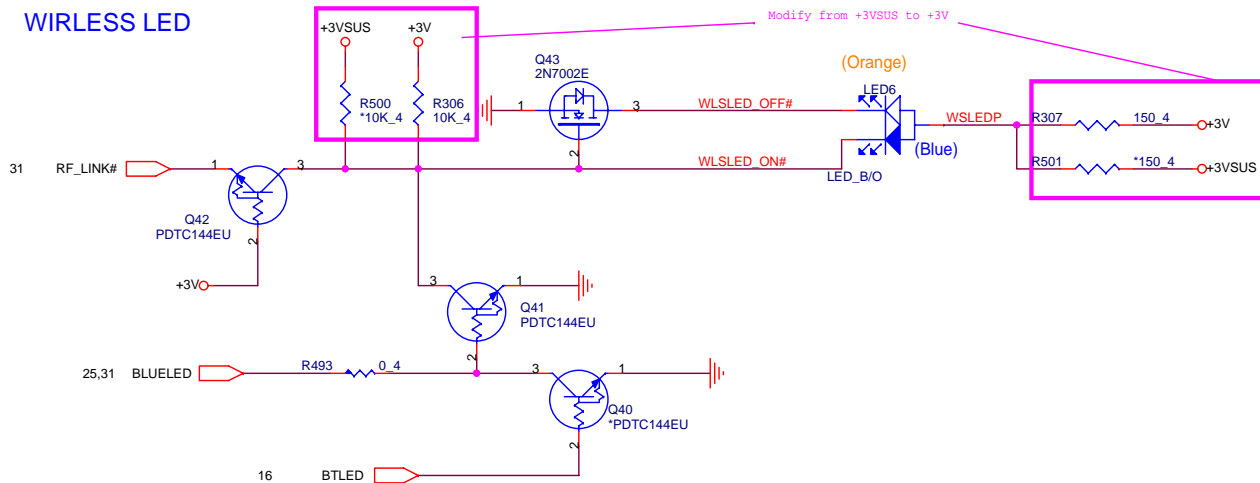


Mute LED

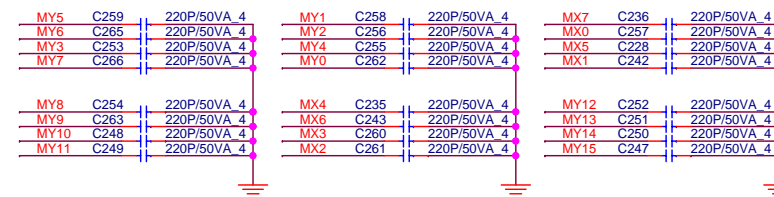


On Blue
Off Amber

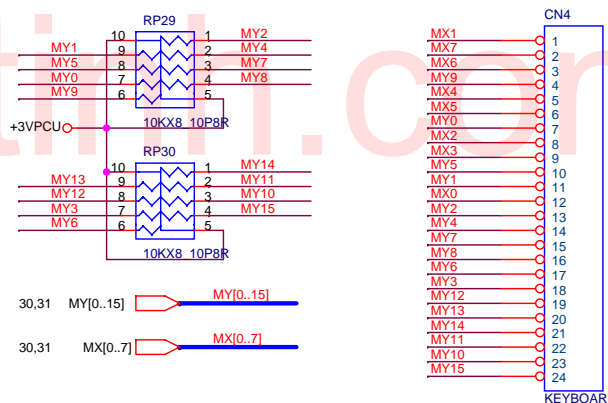
WIRLESS LED



Keyboard



KEYBOARD PULL-UP

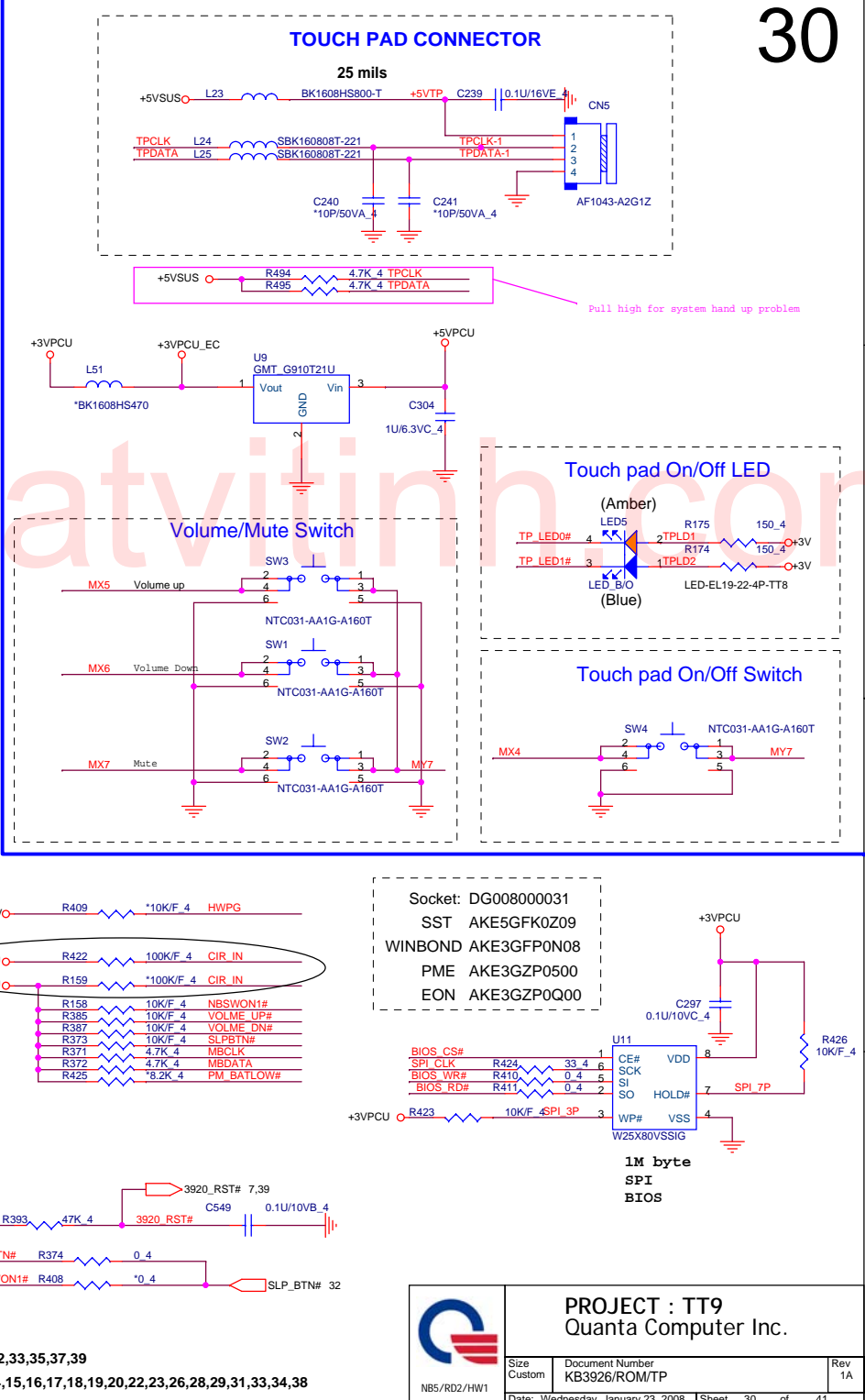
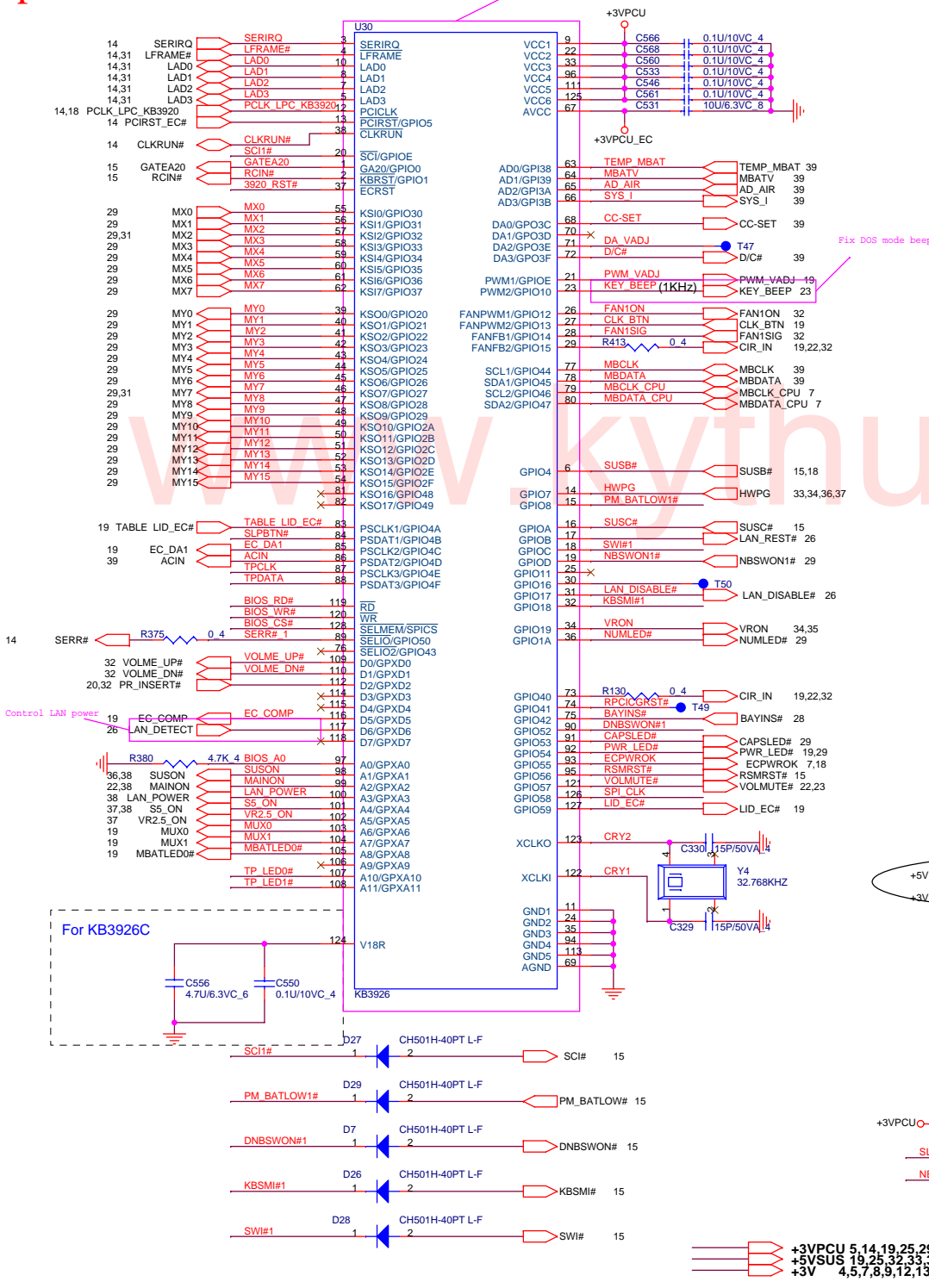


+5VPCU 19,22,28,30,33,34,35,36,37
 +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,30,31,33,34,38
 +3VSUS 15,21,24,25,31,33,34,35,36,38



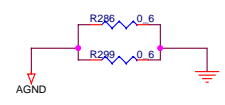
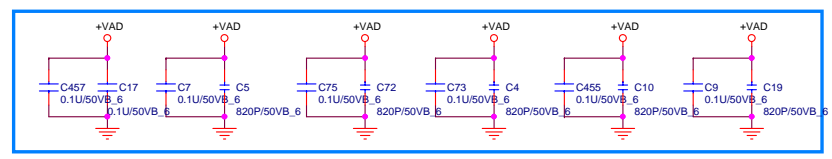
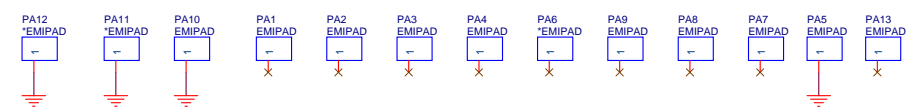
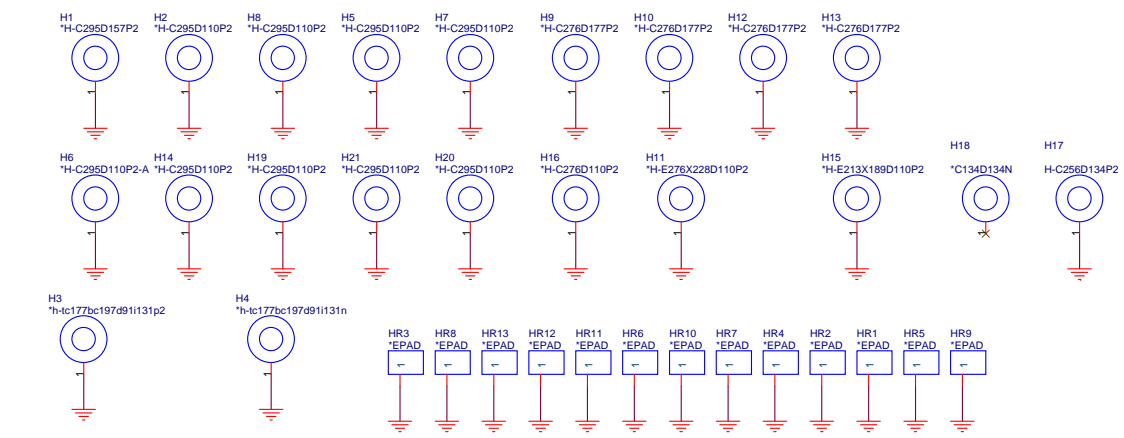
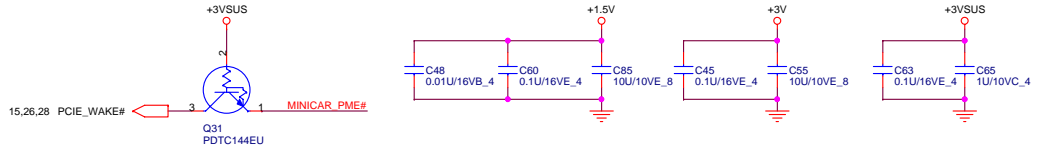
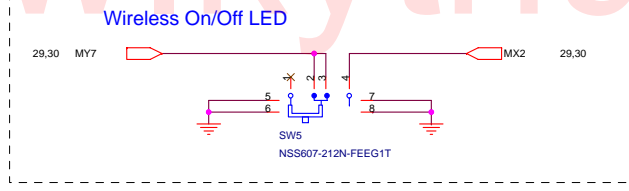
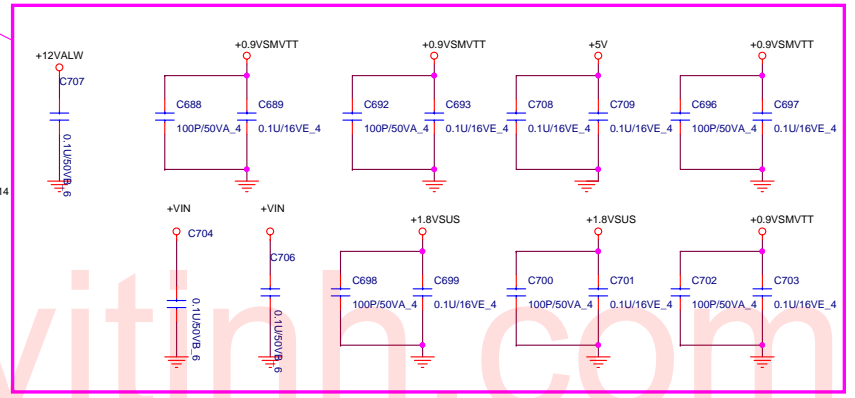
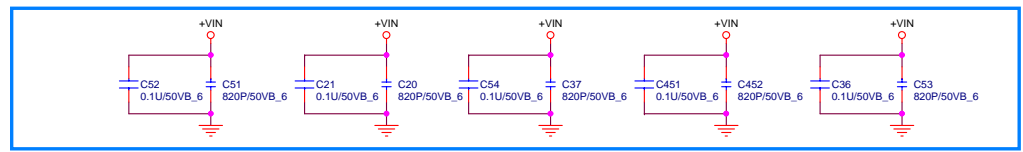
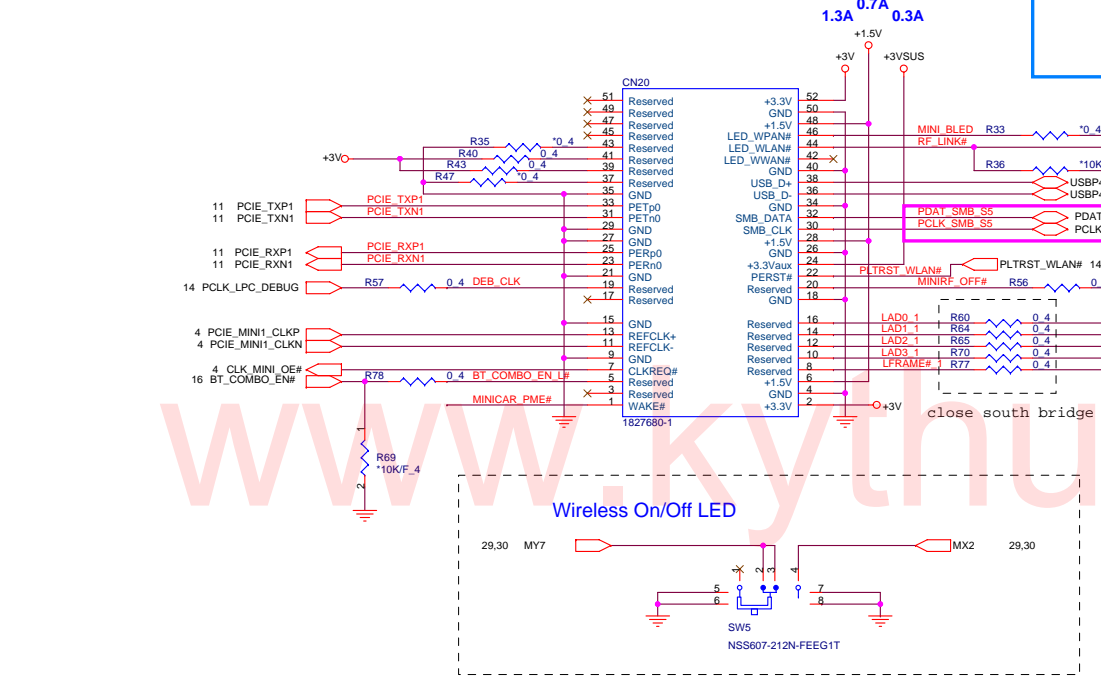
PROJECT : TT9
Quanta Computer Inc.

Size B	Document Number LED/KEYBOARD/SW	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 29 of 41		



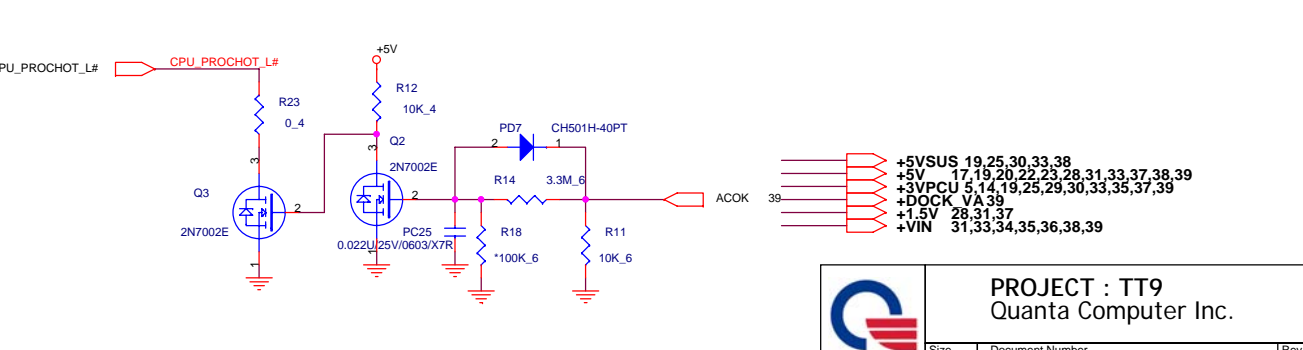
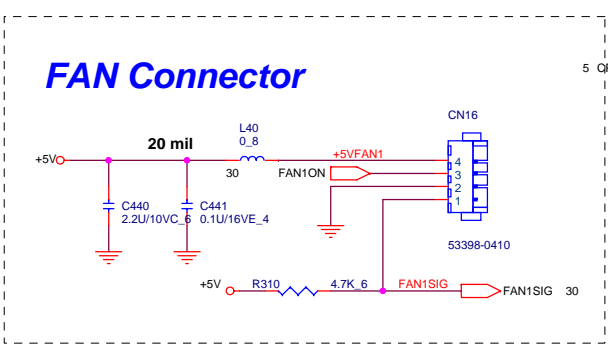
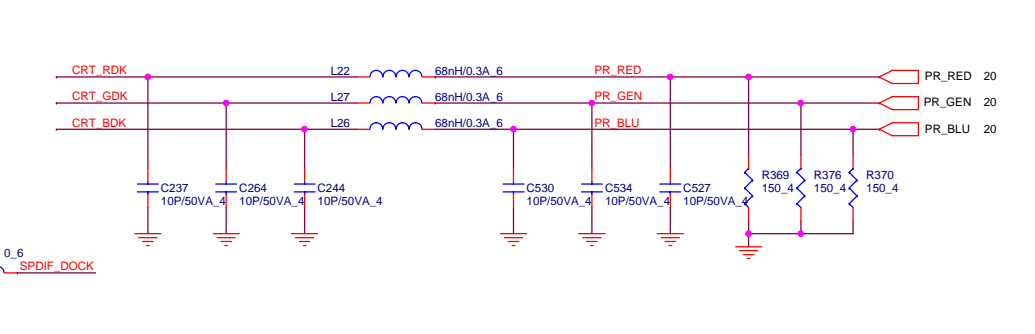
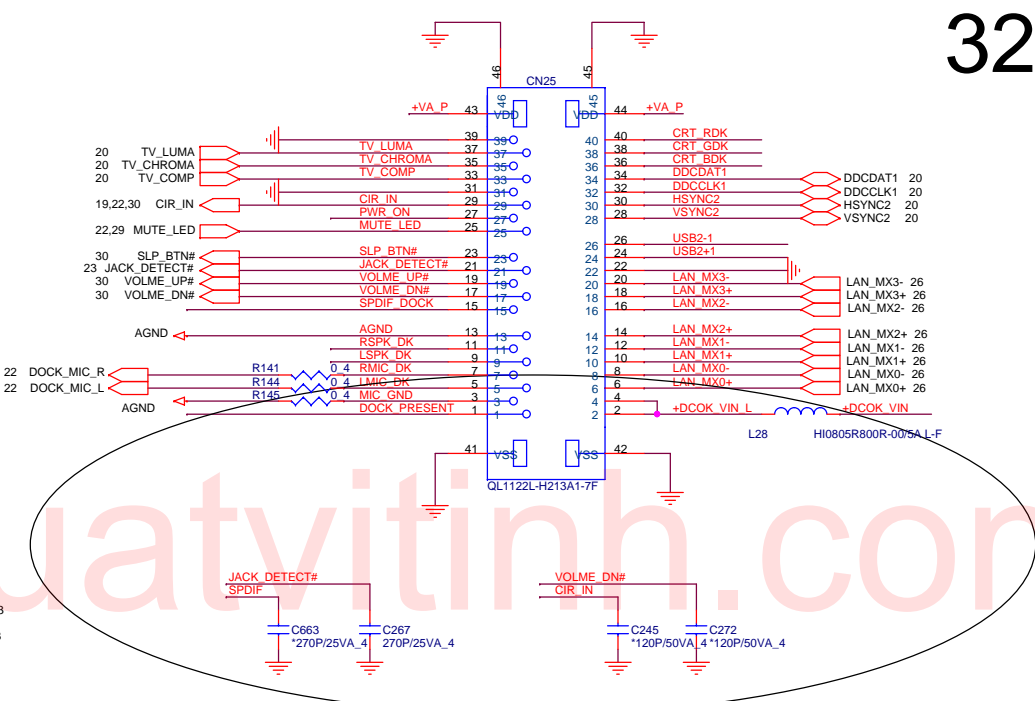
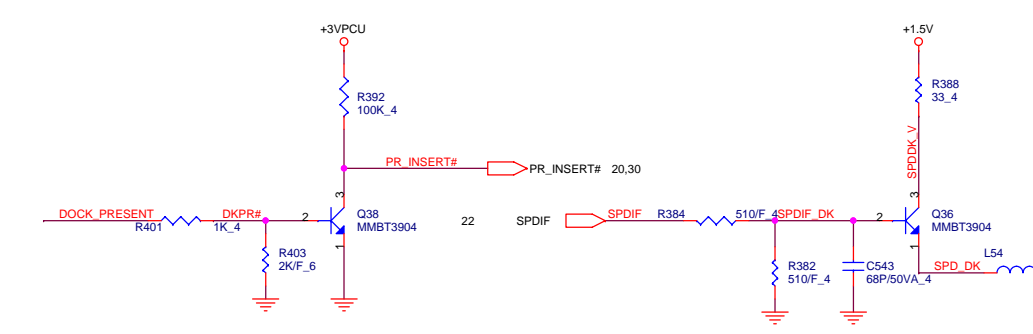
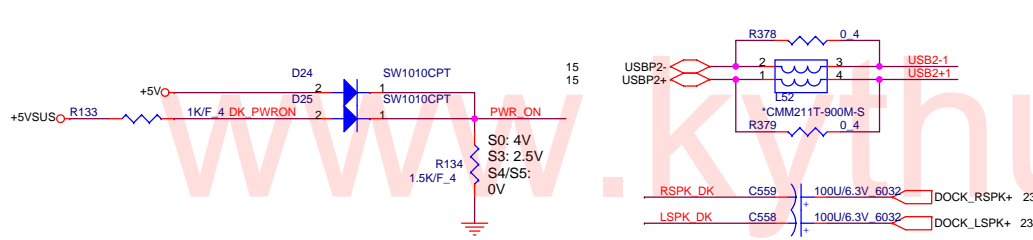
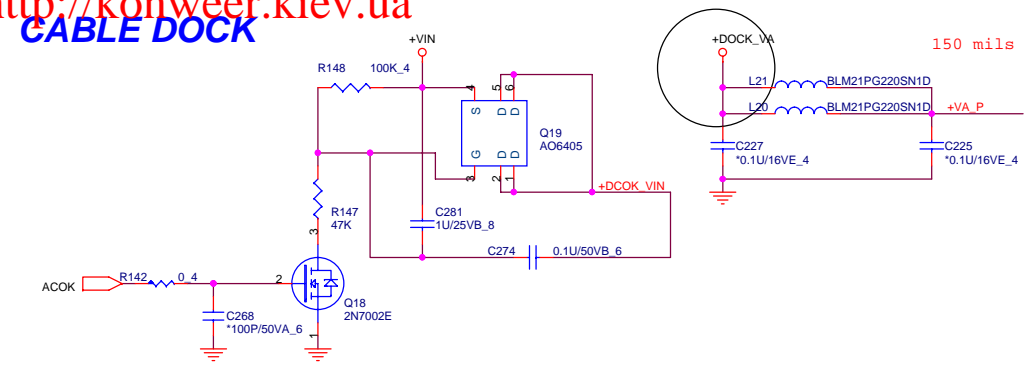
+1.5V 28,32,37
+3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,33,34,38
+3VSUS 15,21,24,25,29,33,34,35,36,38
+VIN 32,33,34,35,36,38,39

Mini PCI-E Card 1 WLAN



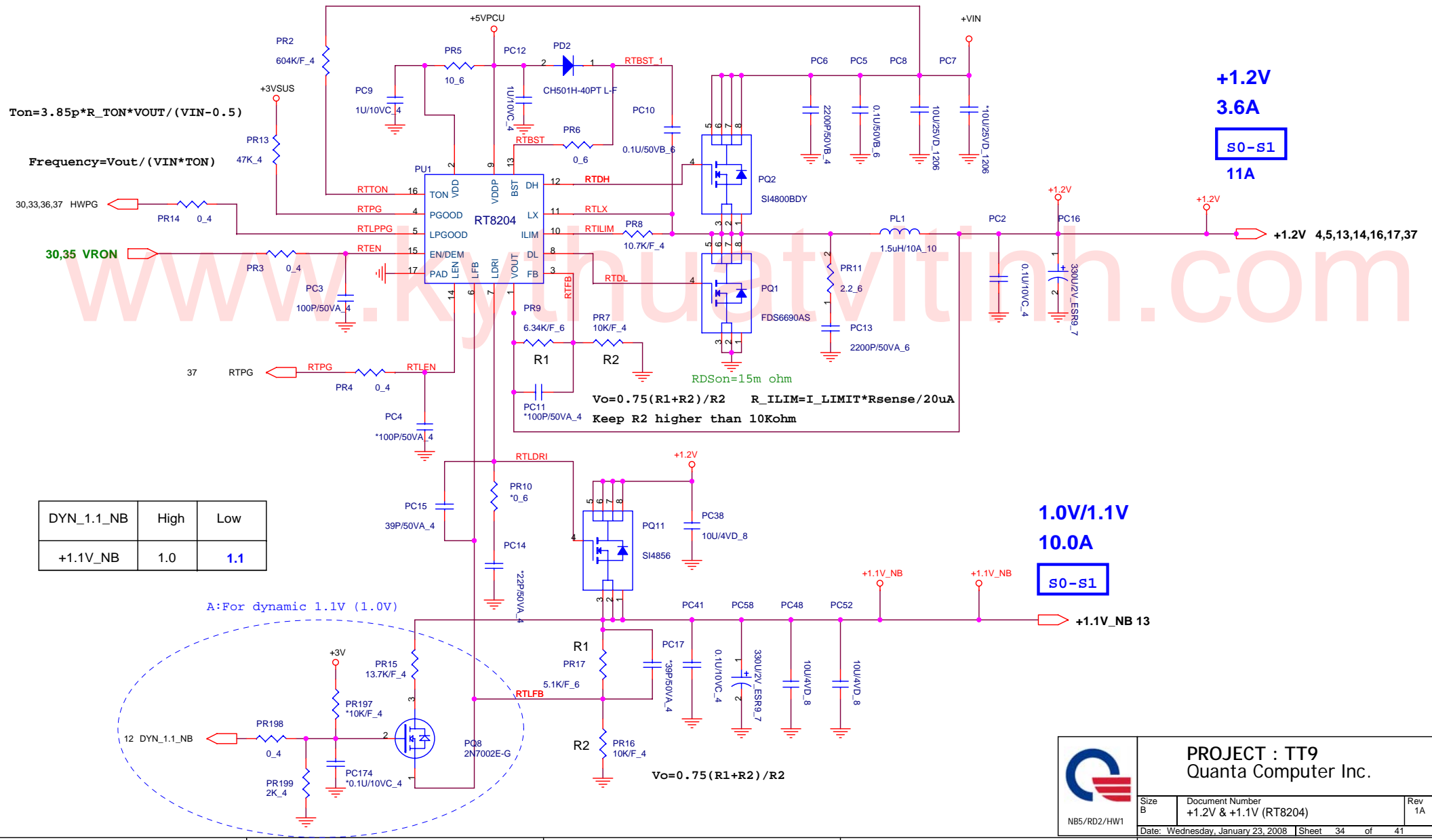
PROJECT : TT9
Quanta Computer Inc.

Size Custom	Document Number Mini CARD/Hole	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 31 of 41		



	PROJECT : TT9 Quanta Computer Inc.	
	Size Custom Document Number CABLE DOCKING	Rev 1A
Date: Wednesday, January 23, 2008		Sheet 32 of 41

NB5/RD2/HW1



$Ton = 3.85p * R_TON * VOUT / (VIN - 0.5)$

$Frequency = Vout / (VIN * TON)$

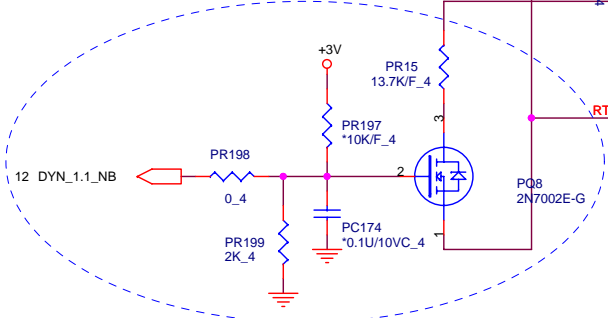
30,33,36,37 HWPG

30,35 VRON

$R_{DSon} = 15m\ ohm$
 $V_o = 0.75 (R1 + R2) / R2$ $R_ILIM = I_LIMIT * R_{sense} / 20uA$
Keep R2 higher than 10Kohm

DYN_1.1_NB	High	Low
+1.1V_NB	1.0	1.1

A: For dynamic 1.1V (1.0V)




$V_o = 0.75 (R1 + R2) / R2$

+1.2V
3.6A
S0-S1
11A

1.0V/1.1V
10.0A
S0-S1

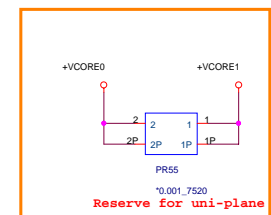
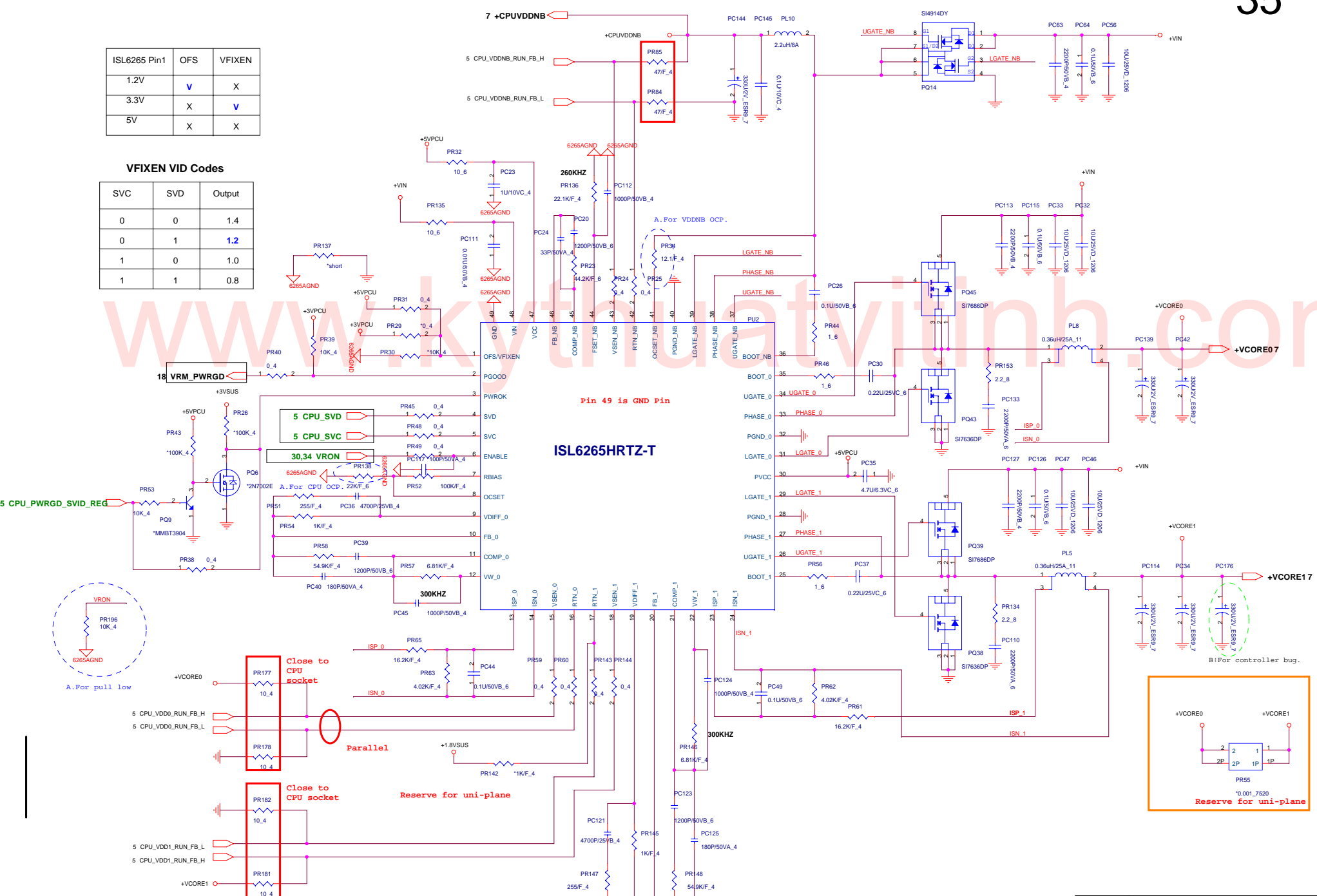
+1.2V 4,5,13,14,16,17,37

 NBS/RD2/HW1	PROJECT : TT9 Quanta Computer Inc.	
	Document Number +1.2V & +1.1V (RT8204)	Rev 1A
Date: Wednesday, January 23, 2008 Sheet 34 of 41		

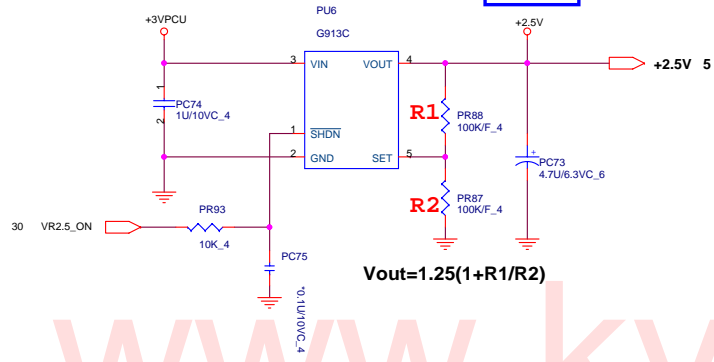
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

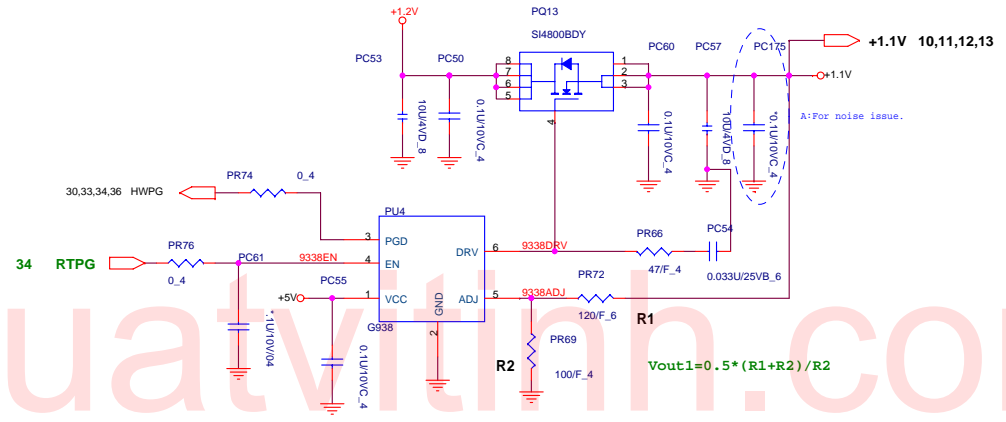
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



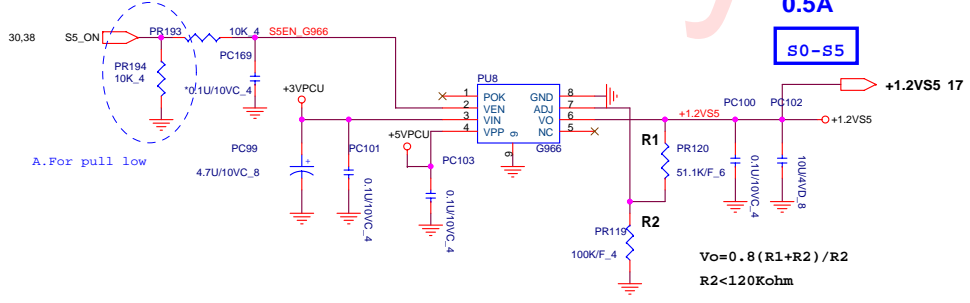
+2.5V
0.25A
S0-S1



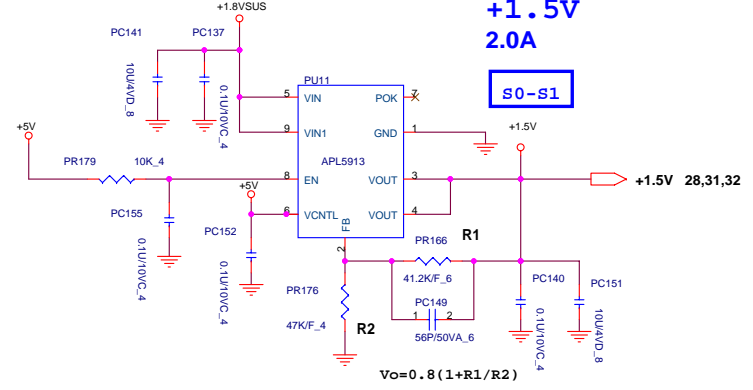
+1.1V
2.A
S0-S1

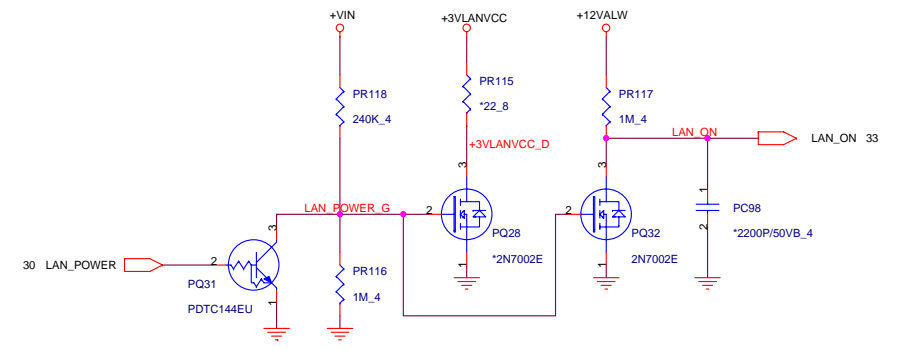
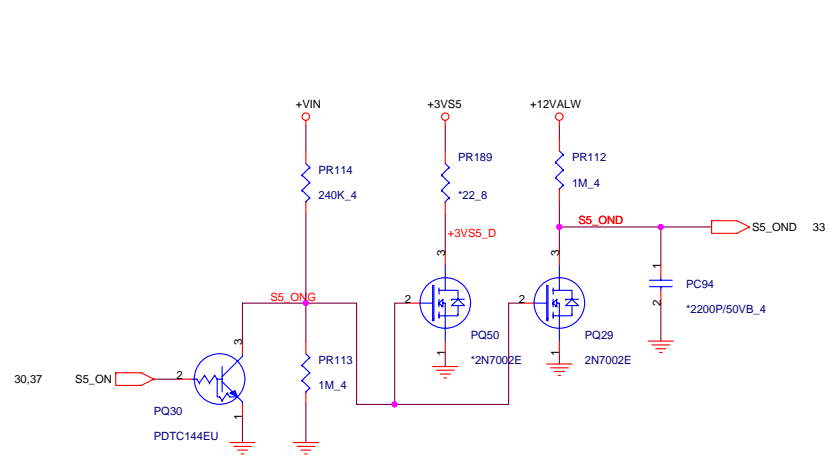
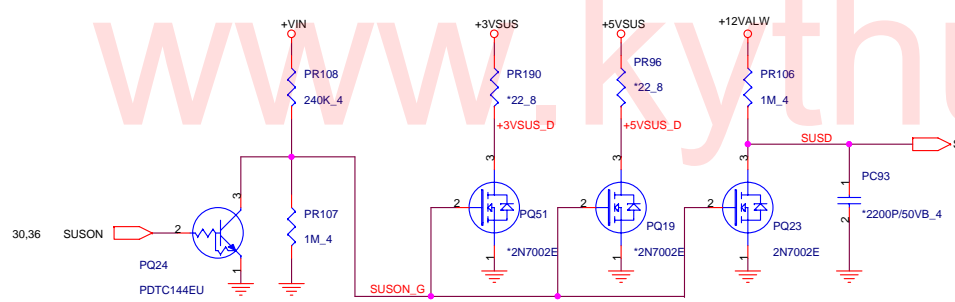
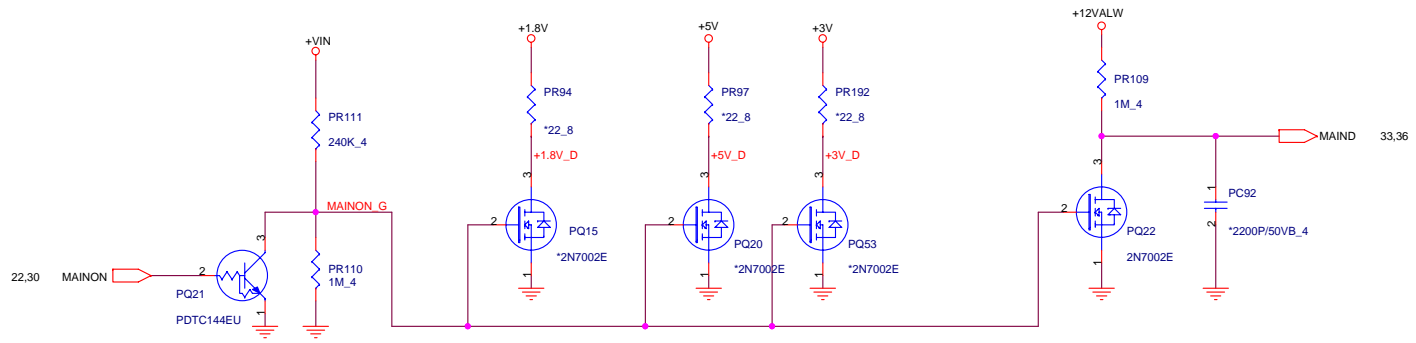



+1.2VS5
0.5A
S0-S5



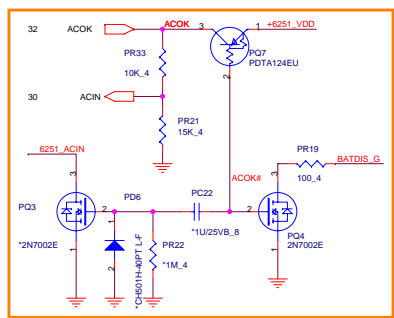
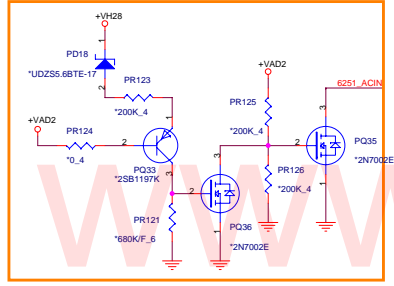
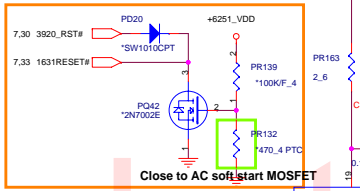
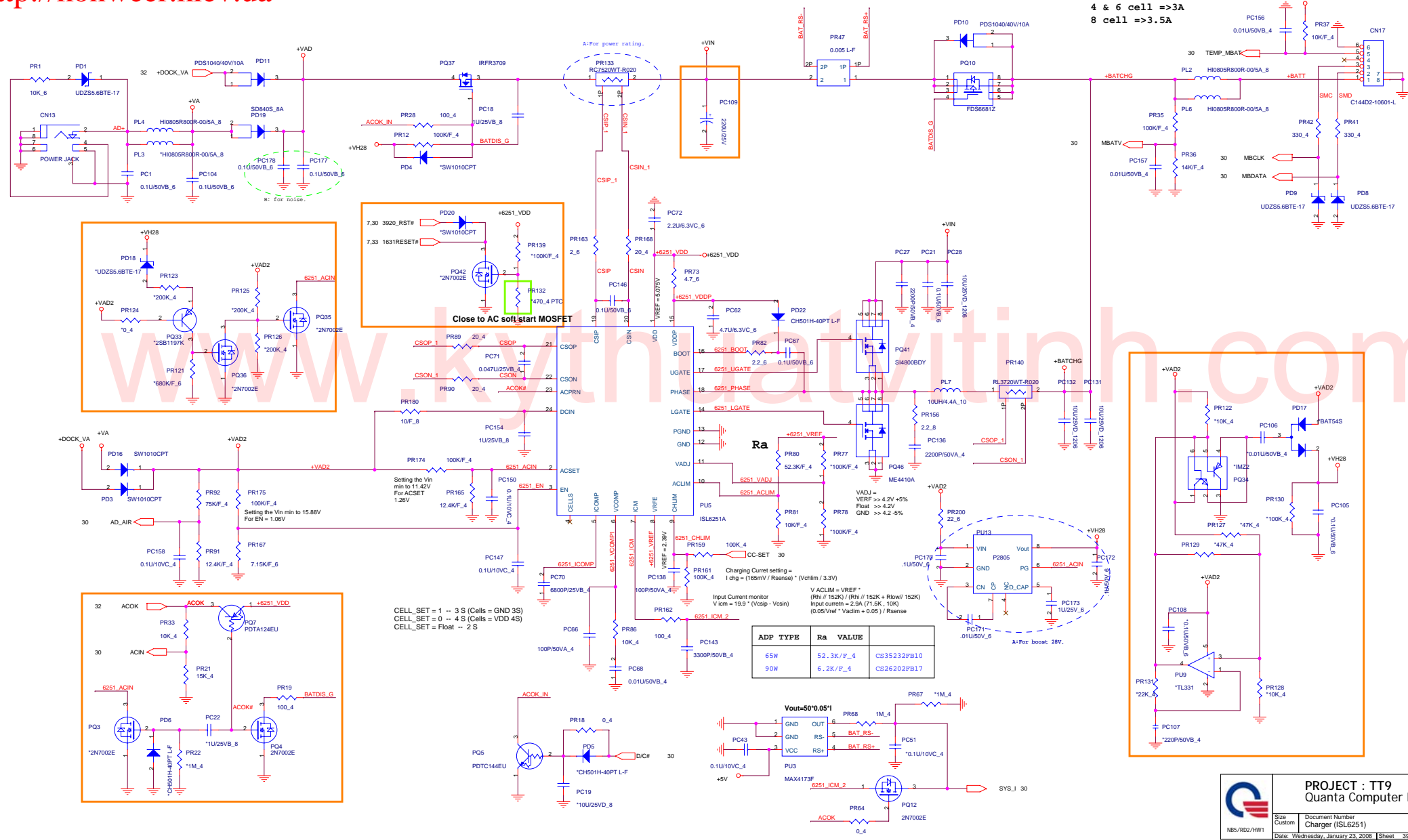
+1.5V
2.0A
S0-S1





 NB5/RD2/HW1	PROJECT : TT9 Quanta Computer Inc.	
	Size Custom	Document Number DISCHARGE
Date: Wednesday, January 23, 2008 Sheet 38 of 41		

Charge current =>3A
4 & 6 cell =>3A
8 cell =>3.5A



CELL_SET = 1 -- 3 S (Cells = GND 3S)
 CELL_SET = 0 -- 4 S (Cells = VDD 4S)
 CELL_SET = Float -- 2 S

ADP TYPE	Ra VALUE
65W	52.3K/F_4
90W	6.2K/F_4

