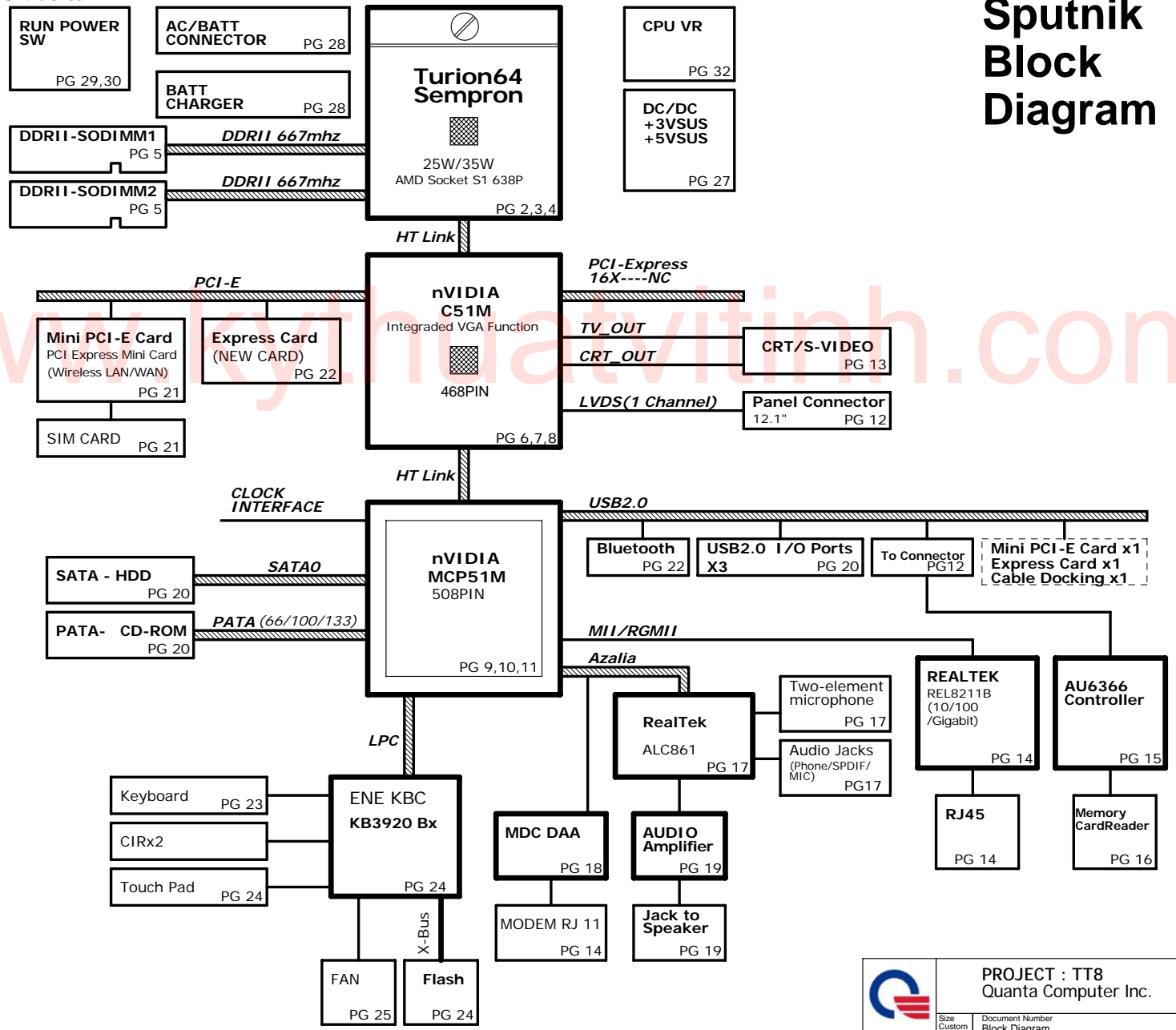


# Sputnik Block Diagram

## PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

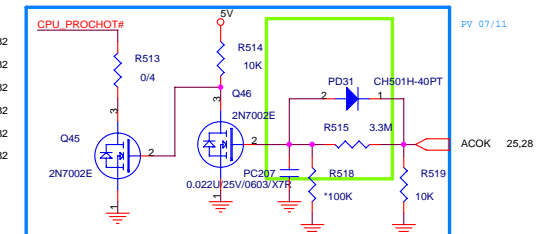
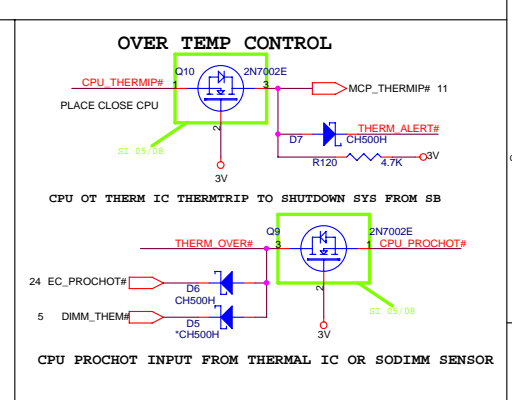
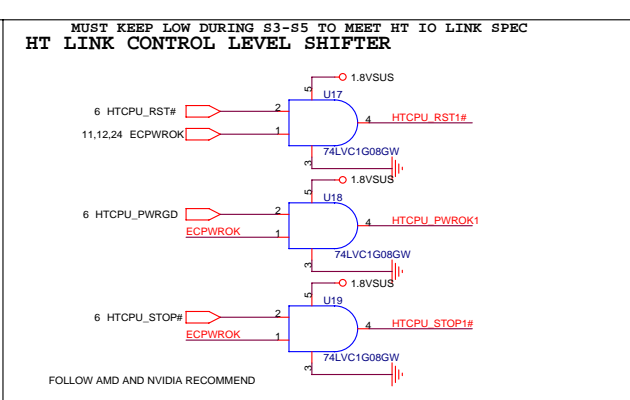
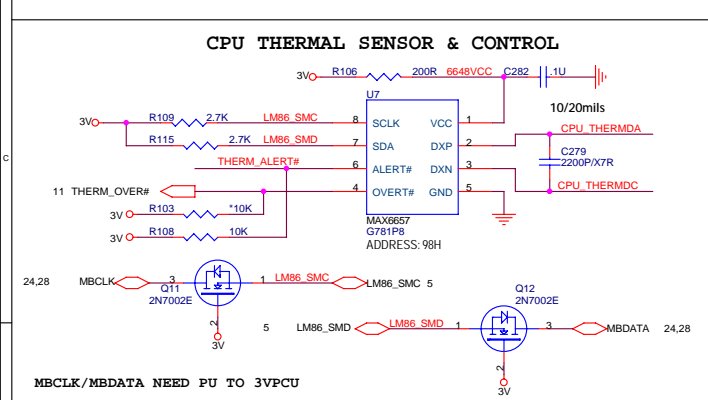
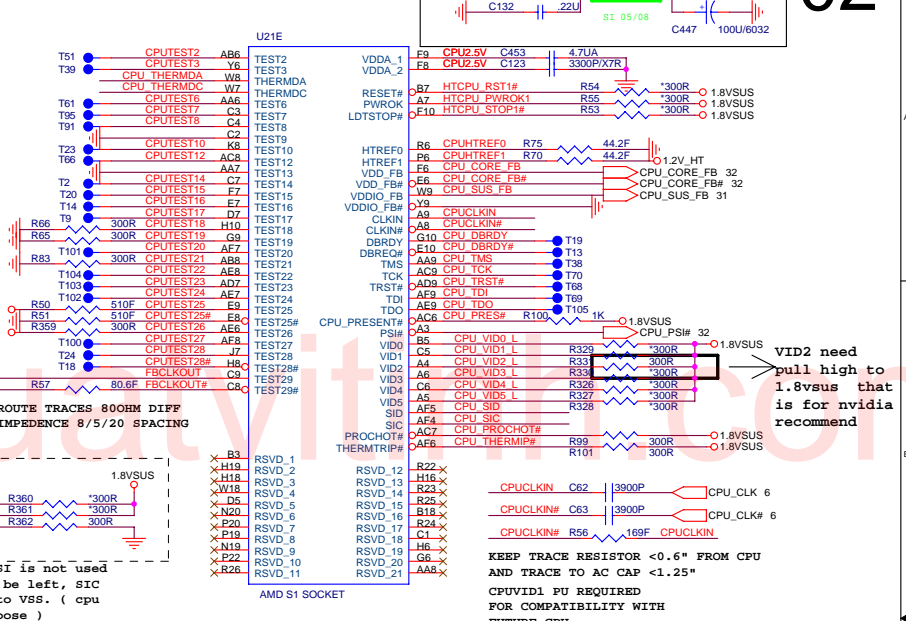
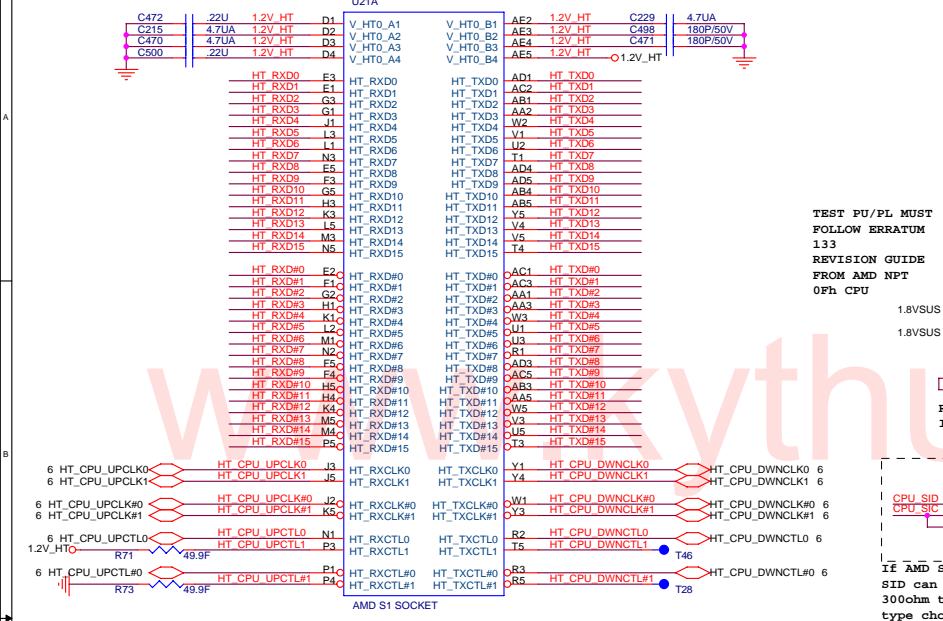
- ### Cable Docking
- TV\_OUT
  - VGA
  - RJ-45
  - CIR/Pwr btn
  - SPDIF Out
  - Stereo MIC
  - Headphone Jack
  - USB Port
  - VOL Cntr
- PG 25



### VAULE DEFINE

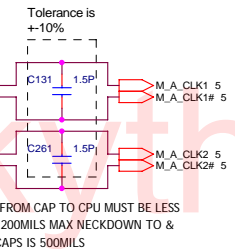
A=0603,B=0805,C=1206,F=1%, OTHER IS 0402

EXAMPLE  
 10R=10ohm(0402)  
 10A=10ohm(0603)  
 10B=10ohm(0805)  
 10C=10ohm(1206)  
 10/F=10ohm(0402 and 1%)



M_A_D063_AA12	MA_DATA[63]
M_A_D062_AB12	MA_DATA[62]
M_A_D061_AA14	MA_DATA[61]
M_A_D060_AB14	MA_DATA[60]
M_A_D059_WA11	MA_DATA[59]
M_A_D058_Y12	MA_DATA[58]
M_A_D057_AD13	MA_DATA[57]
M_A_D056_AB13	MA_DATA[56]
M_A_D055_AB15	MA_DATA[55]
M_A_D054_AB15	MA_DATA[54]
M_A_D053_AB17	MA_DATA[53]
M_A_D052_Y17	MA_DATA[52]
M_A_D051_Y14	MA_DATA[51]
M_A_D050_W14	MA_DATA[50]
M_A_D049_W16	MA_DATA[49]
M_A_D048_AD17	MA_DATA[48]
M_A_D047_Y18	MA_DATA[47]
M_A_D046_AD19	MA_DATA[46]
M_A_D045_AD21	MA_DATA[45]
M_A_D044_AB21	MA_DATA[44]
M_A_D043_AB18	MA_DATA[43]
M_A_D042_AA18	MA_DATA[42]
M_A_D041_AA20	MA_DATA[41]
M_A_D040_Y20	MA_DATA[40]
M_A_D039_AA22	MA_DATA[39]
M_A_D038_Y22	MA_DATA[38]
M_A_D037_W21	MA_DATA[37]
M_A_D036_W22	MA_DATA[36]
M_A_D035_AA21	MA_DATA[35]
M_A_D034_AB22	MA_DATA[34]
M_A_D033_AB24	MA_DATA[33]
M_A_D032_Y24	MA_DATA[32]
M_A_D031_H22	MA_DATA[31]
M_A_D030_H20	MA_DATA[30]
M_A_D029_E21	MA_DATA[29]
M_A_D028_E19	MA_DATA[28]
M_A_D027_H19	MA_DATA[27]
M_A_D026_H24	MA_DATA[26]
M_A_D025_F22	MA_DATA[25]
M_A_D024_F20	MA_DATA[24]
M_A_D023_C23	MA_DATA[23]
M_A_D022_B22	MA_DATA[22]
M_A_D021_E18	MA_DATA[21]
M_A_D020_E18	MA_DATA[20]
M_A_D019_E20	MA_DATA[19]
M_A_D018_D22	MA_DATA[18]
M_A_D017_C19	MA_DATA[17]
M_A_D016_G18	MA_DATA[16]
M_A_D015_G17	MA_DATA[15]
M_A_D014_C17	MA_DATA[14]
M_A_D013_C14	MA_DATA[13]
M_A_D012_E14	MA_DATA[12]
M_A_D011_H17	MA_DATA[11]
M_A_D010_E17	MA_DATA[10]
M_A_D09_E15	MA_DATA[9]
M_A_D08_H15	MA_DATA[8]
M_A_D07_E13	MA_DATA[7]
M_A_D06_C13	MA_DATA[6]
M_A_D05_H12	MA_DATA[5]
M_A_D04_H11	MA_DATA[4]
M_A_D03_G14	MA_DATA[3]
M_A_D02_H14	MA_DATA[2]
M_A_D01_F12	MA_DATA[1]
M_A_D00_G12	MA_DATA[0]

Y13 M_A_D0M7	MA_DQM[7..0] 5
AB16 M_A_D0M6	MA_DQS[7..0] 5
Y19 M_A_D0M5	MA_DQS# [7..0] 5
AC24 M_A_D0M3	MA_BA[2..0] 4,5
F24 M_A_D0M2	MA_CAS# 4,5
E19 M_A_D0M1	MA_RAS# 4,5
C15 M_A_D0M0	MA_CAS# 4,5
E12 M_A_D0M0	MA_WE# 4,5
MA_DM[0]	MA_CKE1 4,5
MA_DM[5]	MA_CKE0 4,5
MA_DM[6]	MA_ODT1 4,5
MA_DM[7]	MA_ODT0 4,5

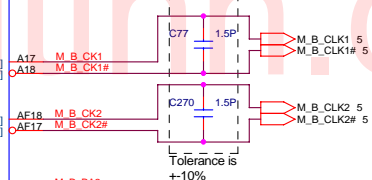


TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS

M_B_D063_AD11	MB_DATA[63]
M_B_D062_AF11	MB_DATA[62]
M_B_D061_AF14	MB_DATA[61]
M_B_D060_AE14	MB_DATA[60]
M_B_D059_Y12	MB_DATA[59]
M_B_D058_AB11	MB_DATA[58]
M_B_D057_AC12	MB_DATA[57]
M_B_D056_AE13	MB_DATA[56]
M_B_D054_AF16	MB_DATA[55]
M_B_D053_AC18	MB_DATA[54]
M_B_D052_AE19	MB_DATA[53]
M_B_D051_AD14	MB_DATA[52]
M_B_D050_AC14	MB_DATA[51]
M_B_D049_AE18	MB_DATA[50]
M_B_D048_AD18	MB_DATA[49]
M_B_D047_AD20	MB_DATA[48]
M_B_D046_AC20	MB_DATA[47]
M_B_D045_AE23	MB_DATA[46]
M_B_D044_AE24	MB_DATA[45]
M_B_D043_AF20	MB_DATA[44]
M_B_D042_AE20	MB_DATA[43]
M_B_D040_AC22	MB_DATA[42]
M_B_D039_AE25	MB_DATA[41]
M_B_D038_AD26	MB_DATA[40]
M_B_D037_AA25	MB_DATA[39]
M_B_D036_AA26	MB_DATA[38]
M_B_D035_AE24	MB_DATA[37]
M_B_D034_AD24	MB_DATA[36]
M_B_D033_AA23	MB_DATA[35]
M_B_D032_AA24	MB_DATA[34]
M_B_D031_G23	MB_DATA[33]
M_B_D030_G23	MB_DATA[32]
M_B_D029_D26	MB_DATA[31]
M_B_D028_C26	MB_DATA[30]
M_B_D027_G26	MB_DATA[29]
M_B_D026_G25	MB_DATA[28]
M_B_D025_E24	MB_DATA[27]
M_B_D024_E23	MB_DATA[26]
M_B_D023_C24	MB_DATA[25]
M_B_D022_B24	MB_DATA[24]
M_B_D021_C20	MB_DATA[23]
M_B_D020_B20	MB_DATA[22]
M_B_D019_C25	MB_DATA[21]
M_B_D018_D24	MB_DATA[20]
M_B_D017_A21	MB_DATA[19]
M_B_D016_D20	MB_DATA[18]
M_B_D015_D18	MB_DATA[17]
M_B_D014_C14	MB_DATA[16]
M_B_D013_D14	MB_DATA[15]
M_B_D012_C14	MB_DATA[14]
M_B_D011_A20	MB_DATA[13]
M_B_D010_A12	MB_DATA[12]
M_B_D09_A16	MB_DATA[11]
M_B_D08_A15	MB_DATA[10]
M_B_D07_A13	MB_DATA[9]
M_B_D06_D12	MB_DATA[8]
M_B_D05_E11	MB_DATA[7]
M_B_D04_G11	MB_DATA[6]
M_B_D03_B14	MB_DATA[5]
M_B_D02_A14	MB_DATA[4]
M_B_D01_A11	MB_DATA[3]
M_B_D00_C11	MB_DATA[2]
M_B_D00_C11	MB_DATA[1]
M_B_D00_C11	MB_DATA[0]

AD12 M_B_D0M7	MB_DM[7]
AC16 M_B_D0M6	MB_DM[6]
AE22 M_B_D0M5	MB_DM[5]
AB26 M_B_D0M3	MB_DM[4]
E28 M_B_D0M3	MB_DM[3]
A22 M_B_D0M2	MB_DM[2]
B16 M_B_D0M1	MB_DM[1]
A12 M_B_D0M0	MB_DM[0]
AF12 M_B_D0S7	MB_DQS[7]
AE16 M_B_D0S6	MB_DQS[6]
AF21 M_B_D0S5	MB_DQS[5]
AC25 M_B_D0S4	MB_DQS[4]
F26 M_B_D0S3	MB_DQS[3]
A24 M_B_D0S2	MB_DQS[2]
D16 M_B_D0S1	MB_DQS[1]
C12 M_B_D0S0	MB_DQS[0]
AE12 M_B_D0SF7	MB_DQS# [7]
AD16 M_B_D0SF6	MB_DQS# [6]
AF22 M_B_D0SF5	MB_DQS# [5]
AC26 M_B_D0SF4	MB_DQS# [4]
E26 M_B_D0SF3	MB_DQS# [3]
AD24 M_B_D0SF2	MB_DQS# [2]
C16 M_B_D0SF1	MB_DQS# [1]
B12 M_B_D0SF0	MB_DQS# [0]

TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS



5 M\_A\_DQ[63..0] M\_A\_DQ[63..0]  
4.5 M\_A\_A[15..0] M\_A\_A[15..0]

M\_A\_DQM[7..0] M\_A\_DQM[7..0] 5  
M\_A\_DQS[7..0] M\_A\_DQS[7..0] 5  
M\_A\_BA[2..0] M\_A\_BA[2..0] 4,5  
M\_A\_CAS# [3..0] M\_A\_CAS# [3..0] 4,5  
M\_A\_RAS# M\_A\_RAS# 4,5  
M\_A\_CAS# M\_A\_CAS# 4,5  
M\_A\_WE# M\_A\_WE# 4,5  
M\_A\_CKE1 M\_A\_CKE1 4,5  
M\_A\_CKE0 M\_A\_CKE0 4,5  
M\_A\_ODT1 M\_A\_ODT1 4,5  
M\_A\_ODT0 M\_A\_ODT0 4,5

5 M\_B\_DQ[63..0] M\_B\_DQ[63..0]  
4.5 M\_B\_A[15..0] M\_B\_A[15..0]

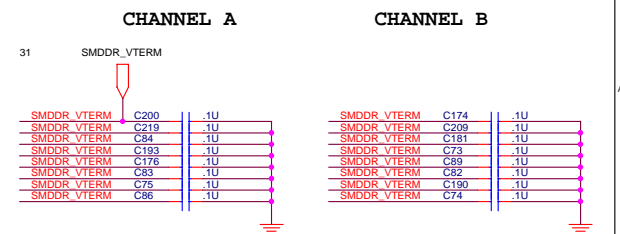
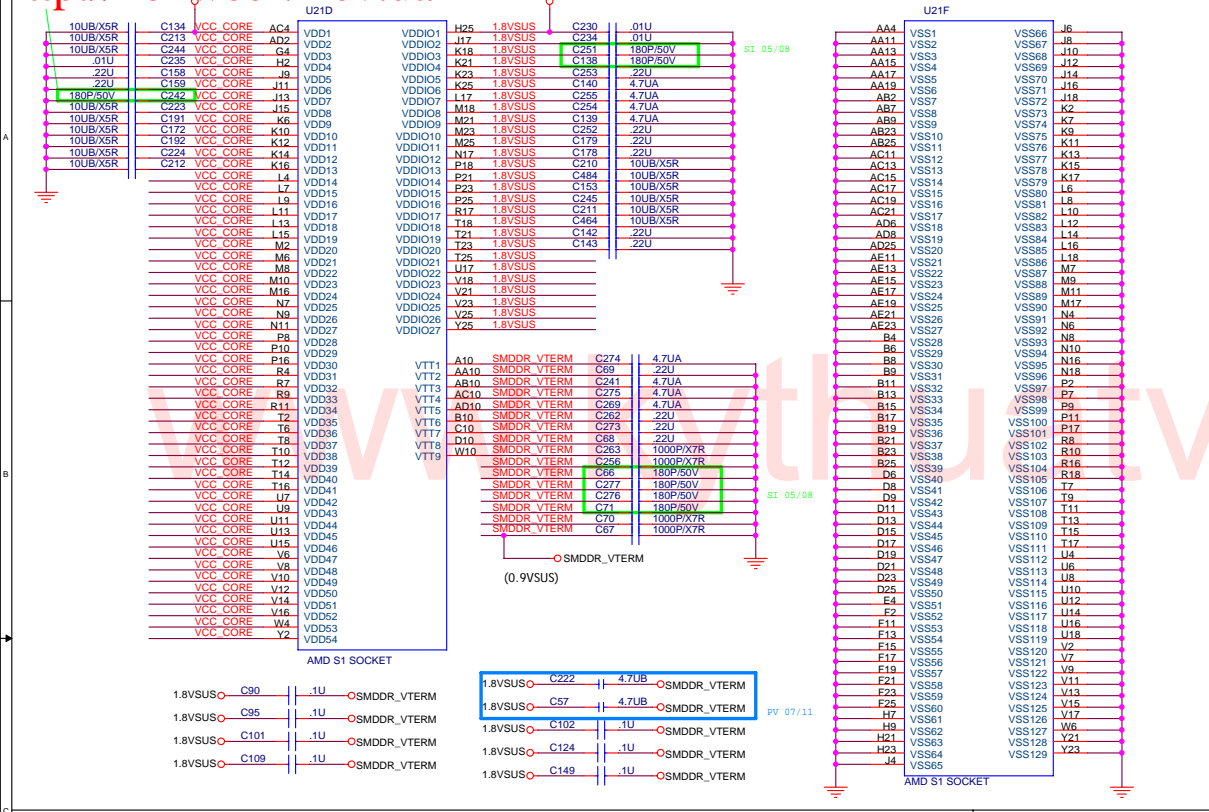
M\_B\_DQM[7..0] M\_B\_DQM[7..0] 5  
M\_B\_DQS[7..0] M\_B\_DQS[7..0] 5  
M\_B\_DQS# [7..0] M\_B\_DQS# [7..0] 5  
M\_B\_BA[2..0] M\_B\_BA[2..0] 4,5  
M\_B\_CAS# [3..0] M\_B\_CAS# [3..0] 4,5  
M\_B\_RAS# M\_B\_RAS# 4,5  
M\_B\_CAS# M\_B\_CAS# 4,5  
M\_B\_WE# M\_B\_WE# 4,5  
M\_B\_CKE1 M\_B\_CKE1 4,5  
M\_B\_CKE0 M\_B\_CKE0 4,5  
M\_B\_ODT1 M\_B\_ODT1 4,5  
M\_B\_ODT0 M\_B\_ODT0 4,5

C51M[VREF] : W = 20MIL AND SPACE = 20MIL

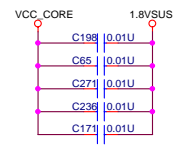
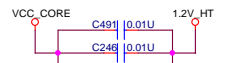
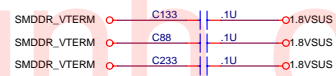
### CPU POWER PLANE AND BY PASS CAP

### DDR2 TERMINATION BYPASS CAP

# 04

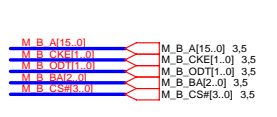
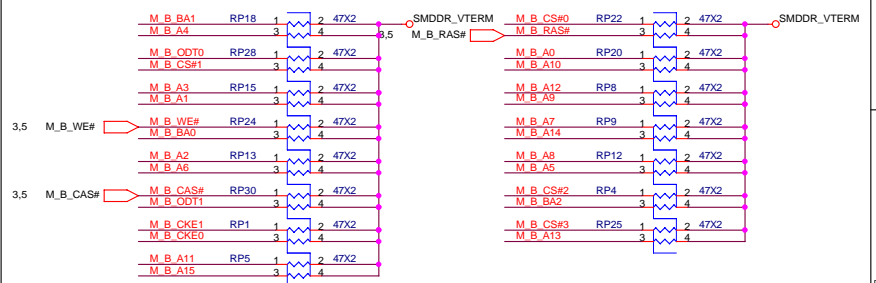
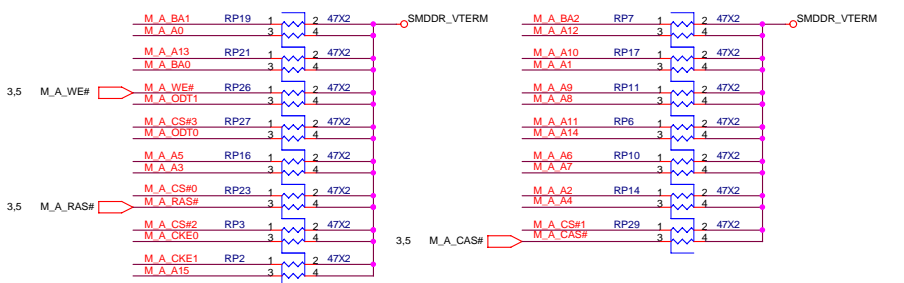


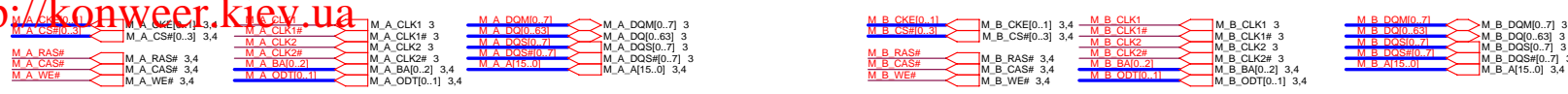
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR\_VTERM



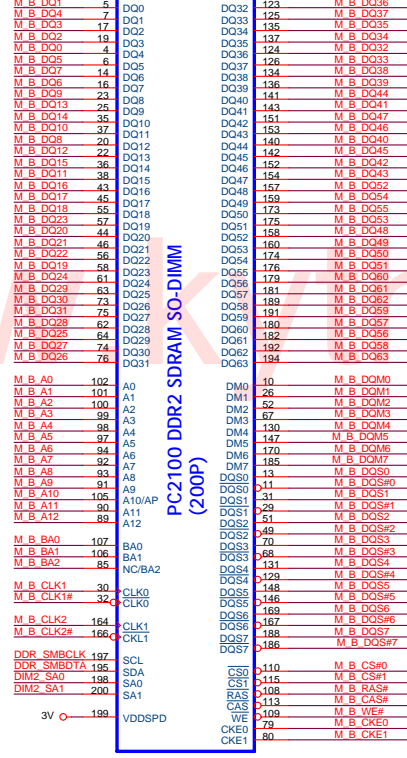
### DDR1 CHANNEL A TERMINATION

### DDR1 CHANNEL B TERMINATION

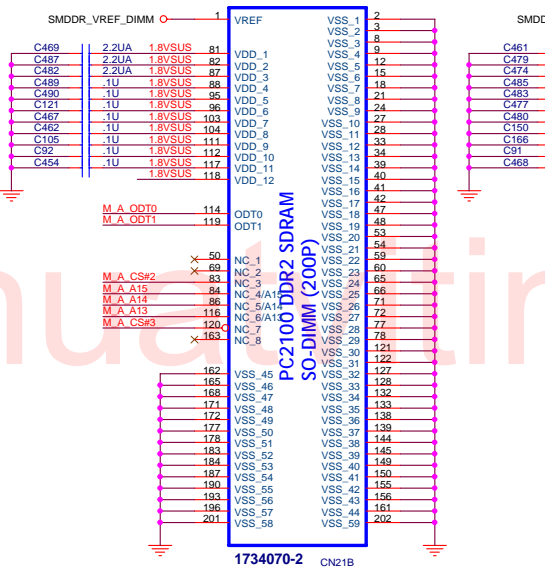




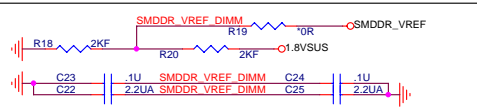
CKE 0,1 REV type : H 6.5



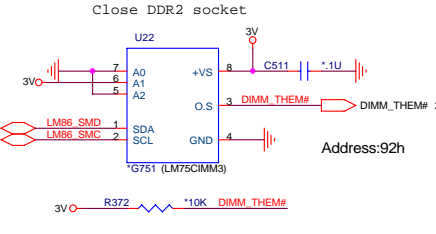
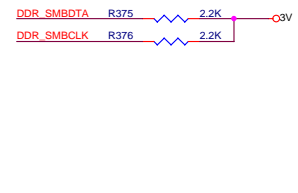
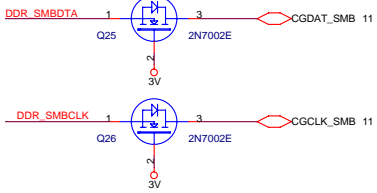
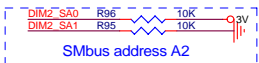
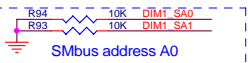
CKE 2,3 REV type : H 11

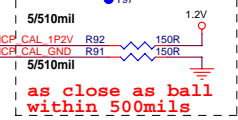
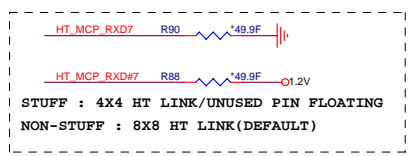
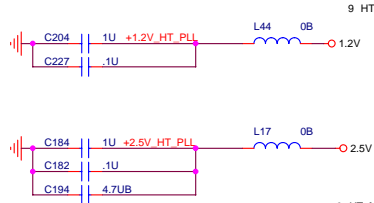
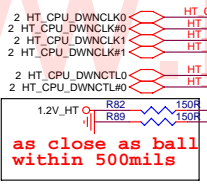
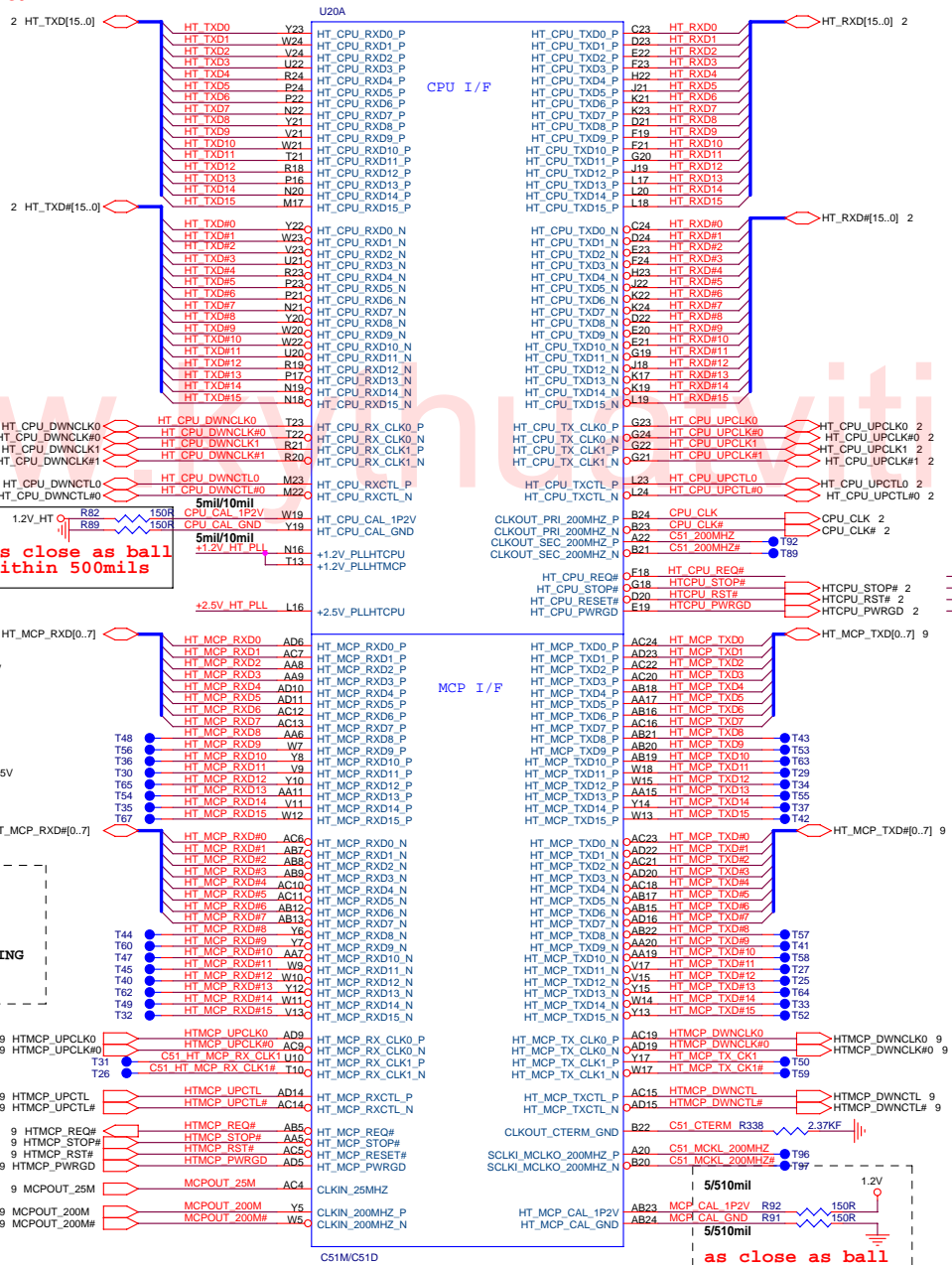


SO-DIMM BYPASS PLACEMENT : Place these Caps near So-Dimm1. No Vias Between the Trace of PIN to CAP.



SMDDR\_VREF\_DIMM : TRACE WIDTH > 20 MIL PUT BYPASS CAP ON EACH DIMM

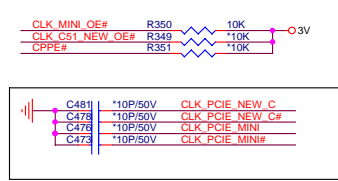
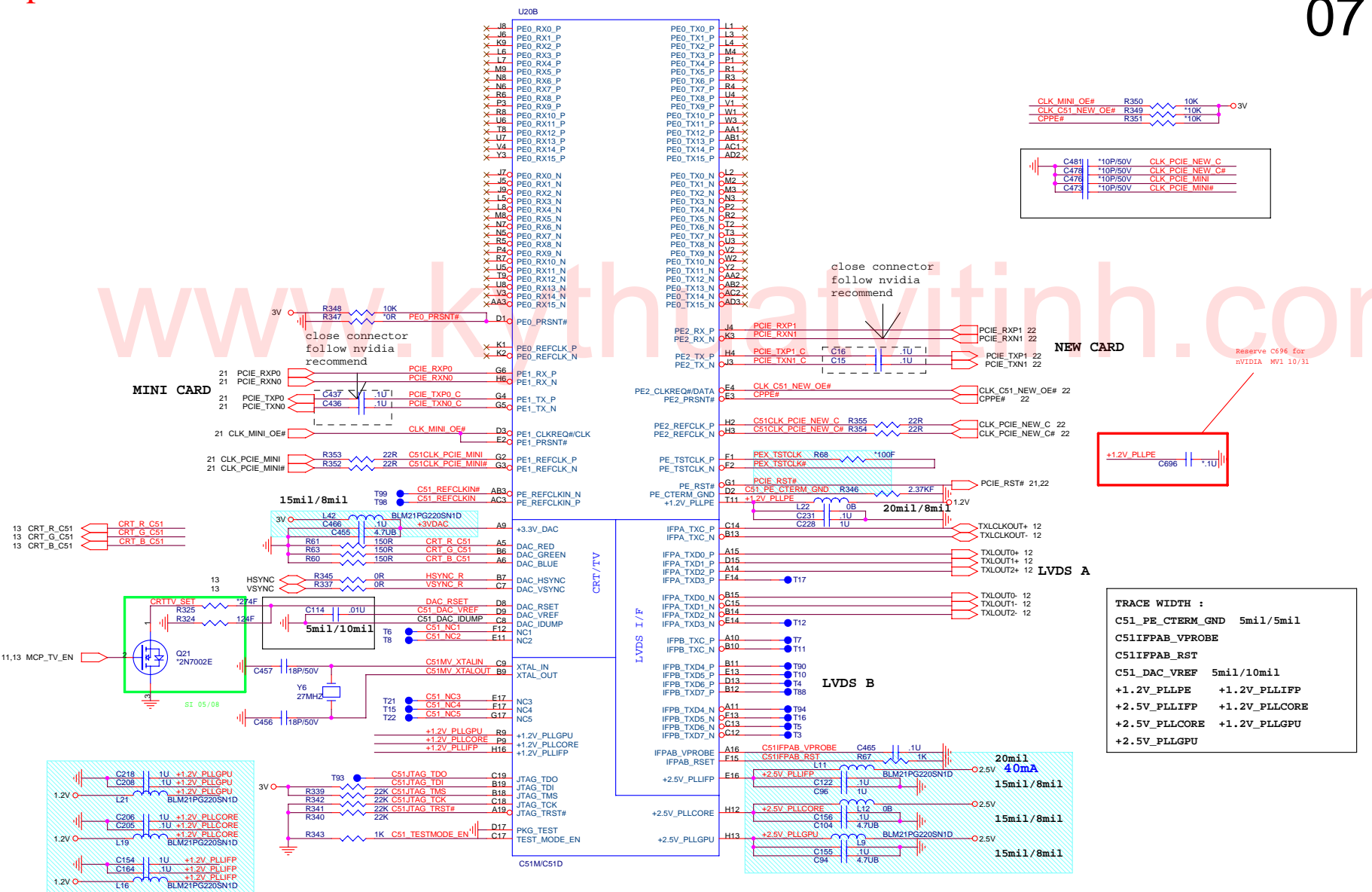




#note from nv design guide  
 Pull-Hi for rise time  
 ○ 2.5V



	PROJECT : TT8		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number C51MV (HT LINK)	Date: Friday, November 24, 2006	Sheet 6 of 36



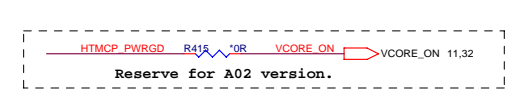
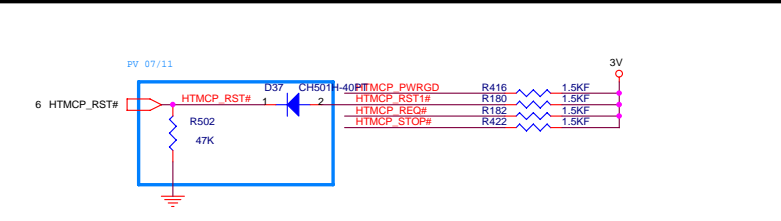
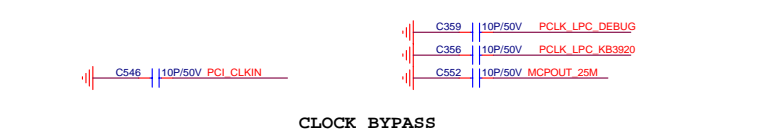
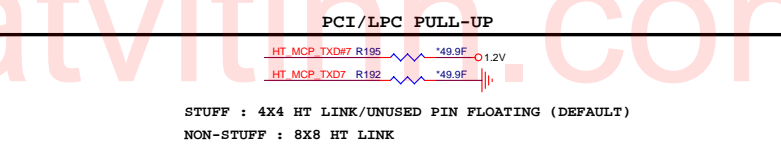
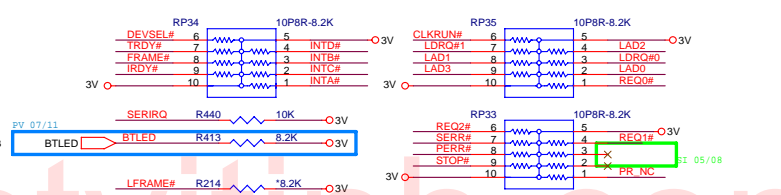
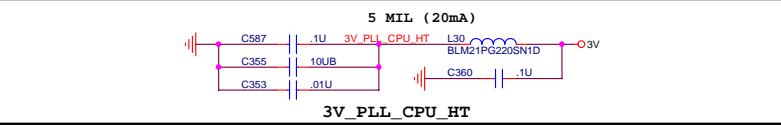
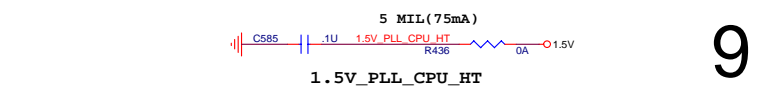
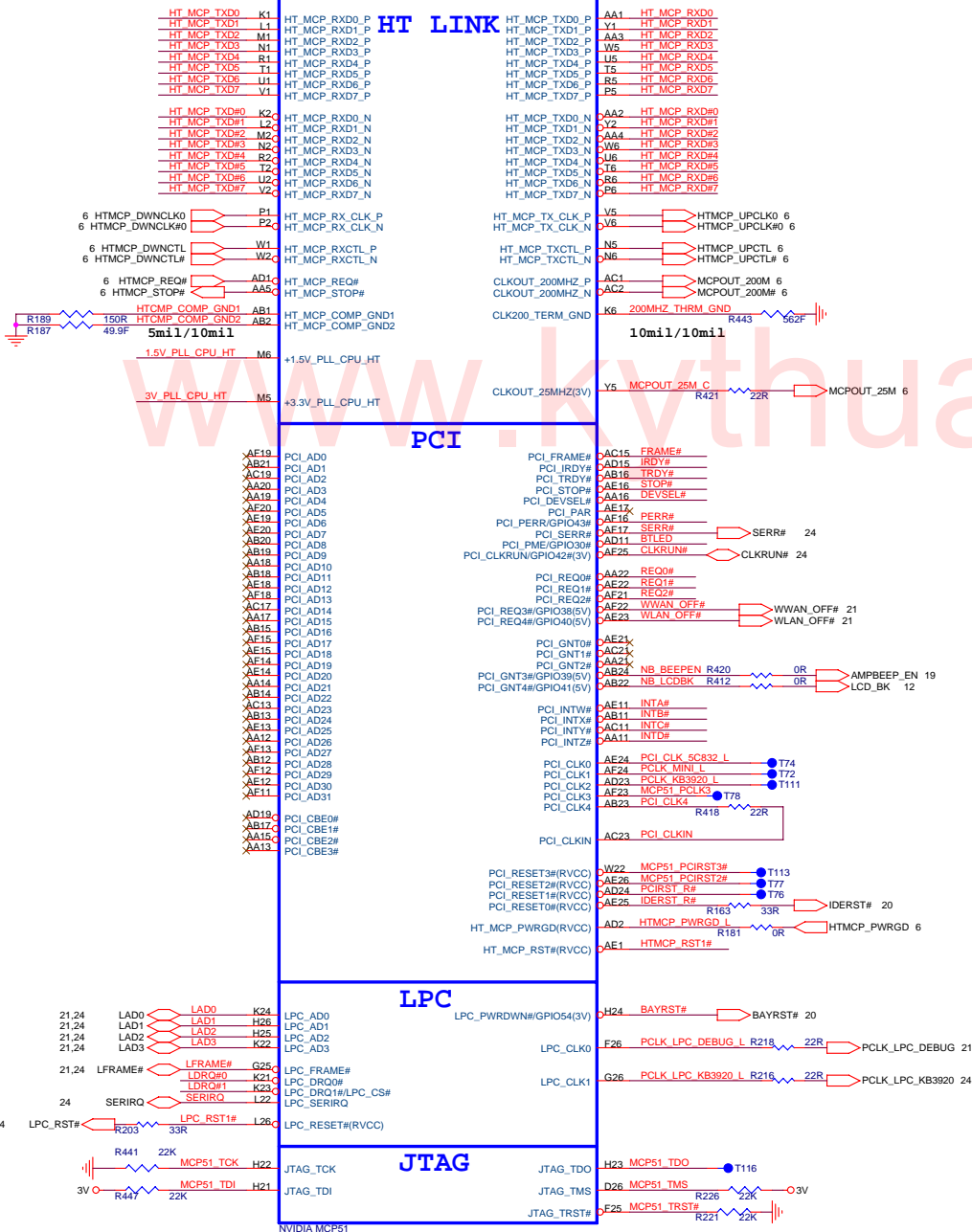
NEW CARD



TRACE WIDTH :

C51_PE_CTERM_GND	5mil/5mil
C51IFPAB_VPROBE	
C51IFPAB_RST	
C51_DAC_VREF	5mil/10mil
+1.2V_PLLPE	+1.2V_PLLIFF
+2.5V_PLLIFF	+1.2V_PLLGPU
+2.5V_PLLCORE	+1.2V_PLLGPU
+2.5V_PLLGPU	

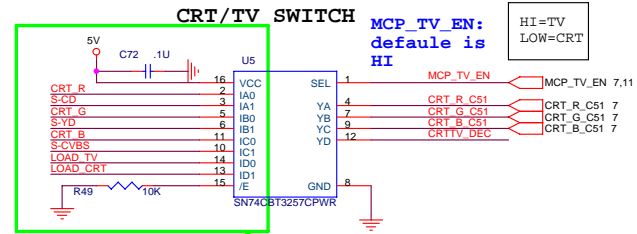




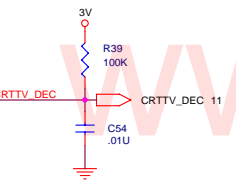








LOAD\_CRT -- TV WORK  
LOAD\_TV -- CRT WORK  
WORK

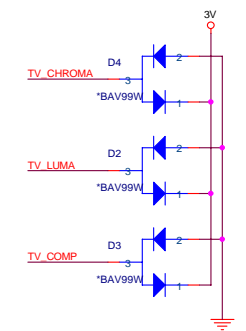


close within 600mils (close data switch)

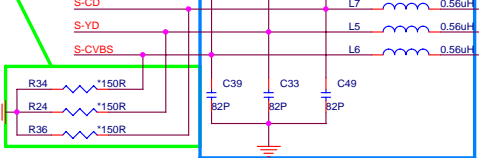


S-CVBS	R47	10K	LOAD TV
S-YD	R45	10K	LOAD TV
CRT B	R46	10K	LOAD CRT

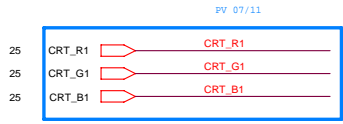
That is for CRT and TV choose.. used impedance and driver to choose



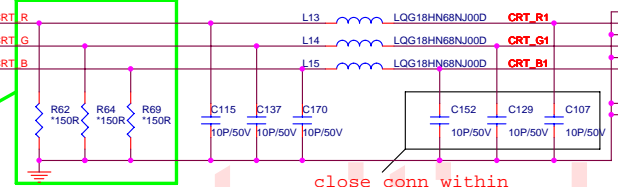
Change from nVIDIA for B-test



150-R as possible as closed to Tv connector (close with in 600 mil)

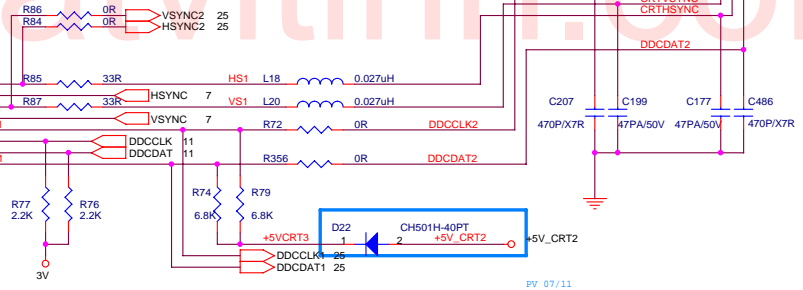
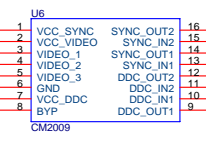


150-R as possible as closed to CRT connector (close with in 600 mil)

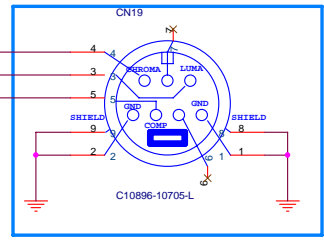


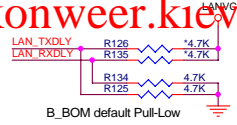
close conn within 600mils

**ESD PROTECTION**

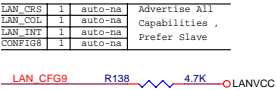
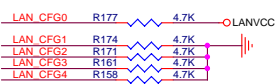
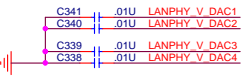
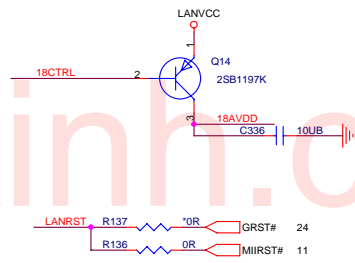
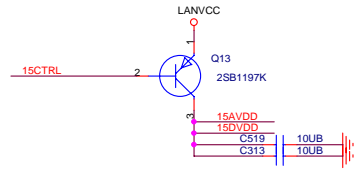
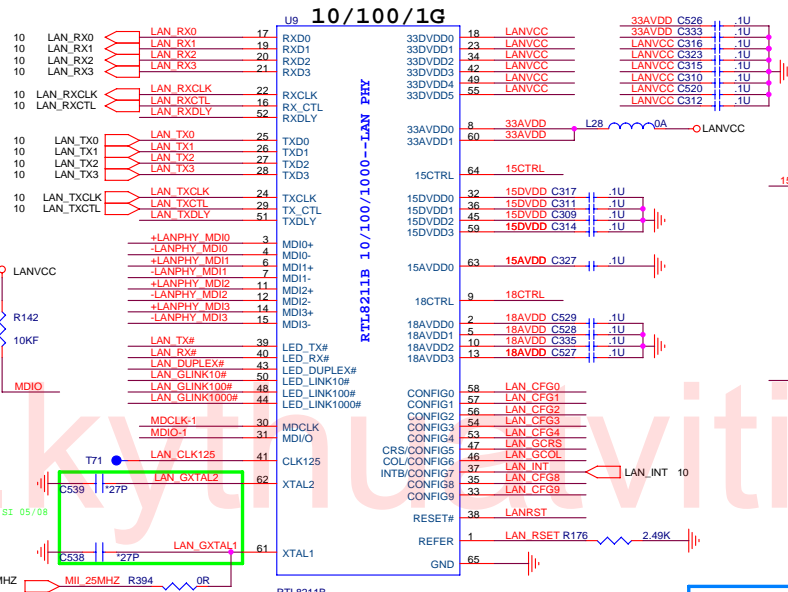
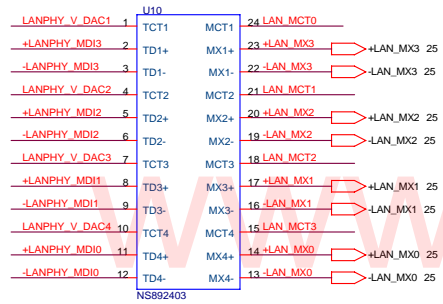


**TV\_OUT**

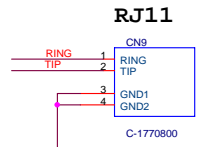
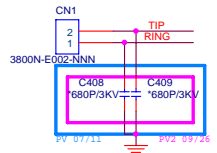
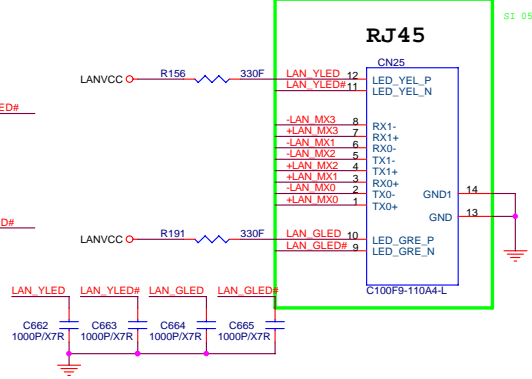
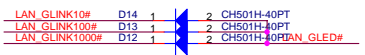
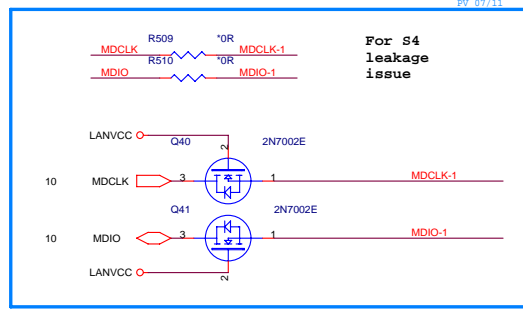




NS892403 : GIGABIT

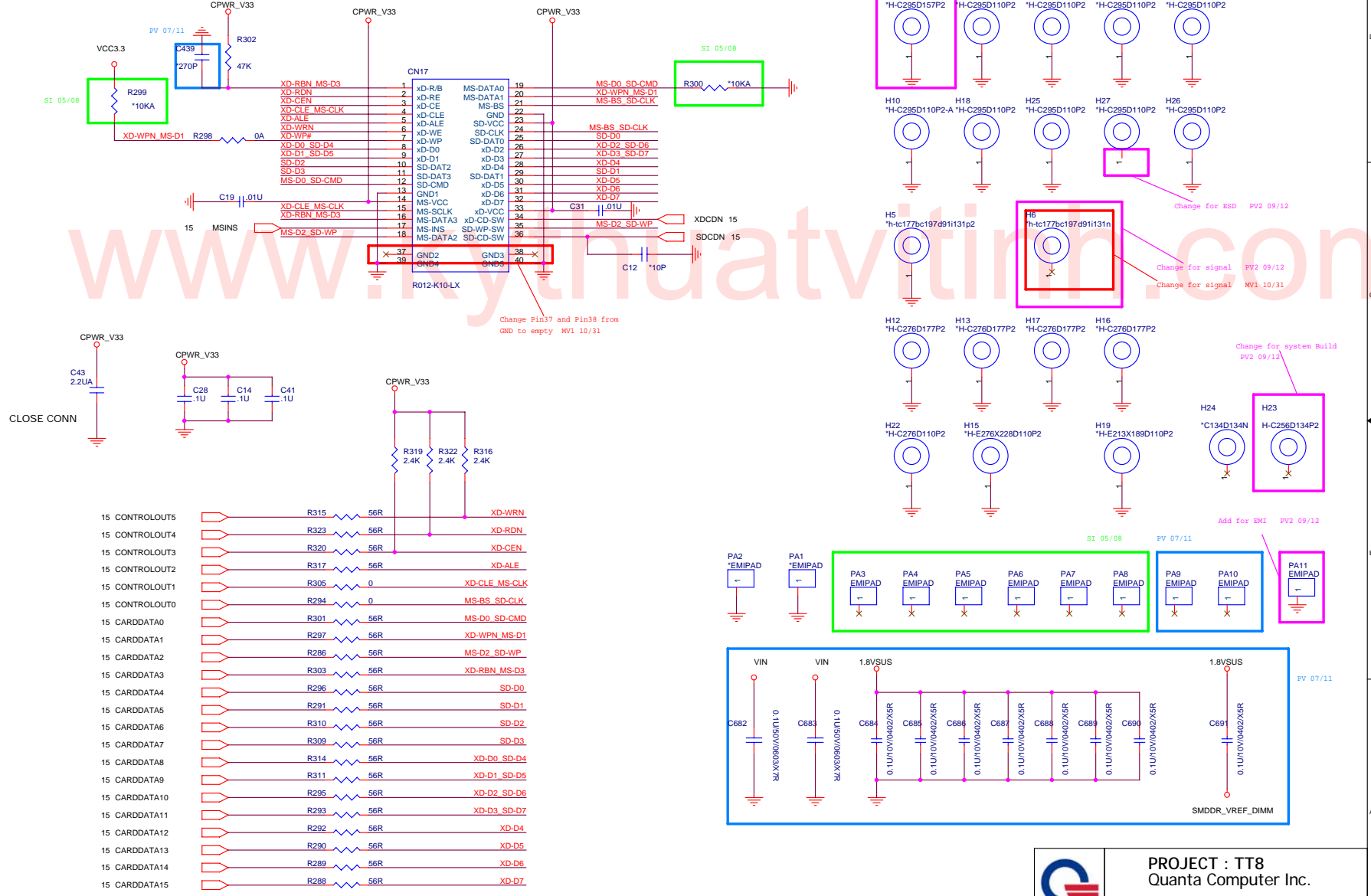


1:ROMII/MII to COPPER

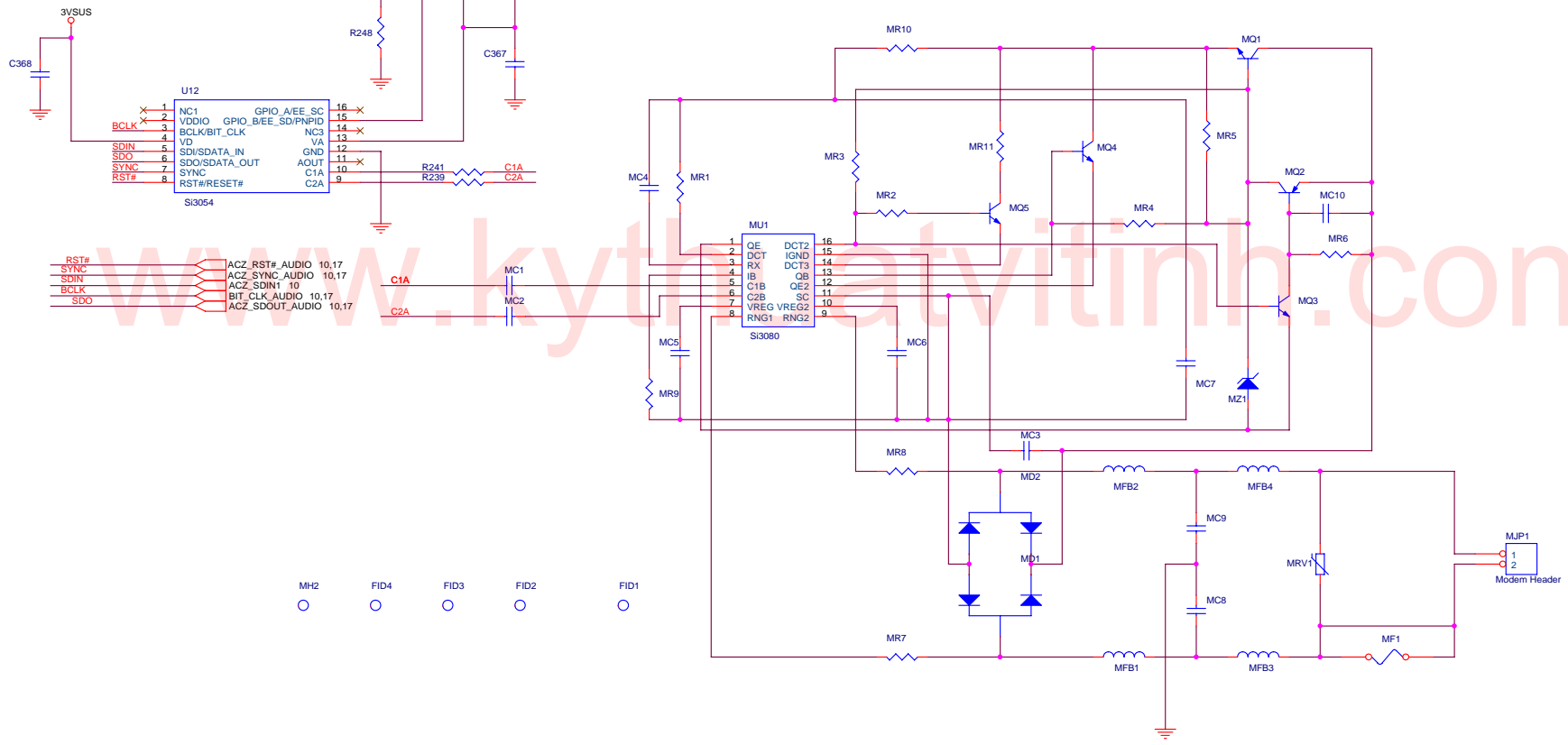




### 4 IN1 CARD READER XD, MMC/SD, MS/MSP



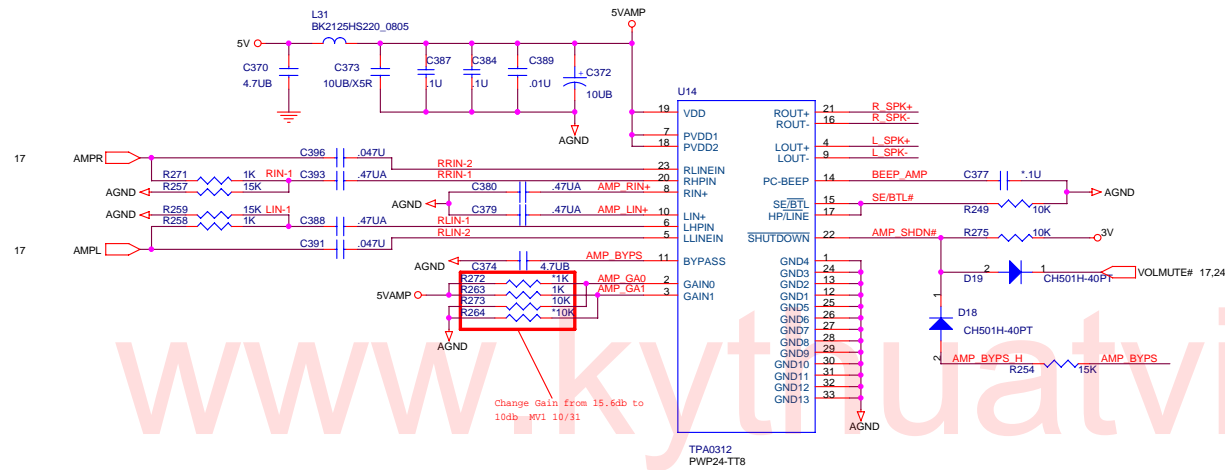




No Ground Plane In DAA Section  
Homologation Area

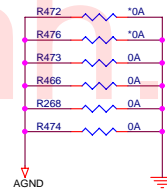
DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL



0312 Gain Table

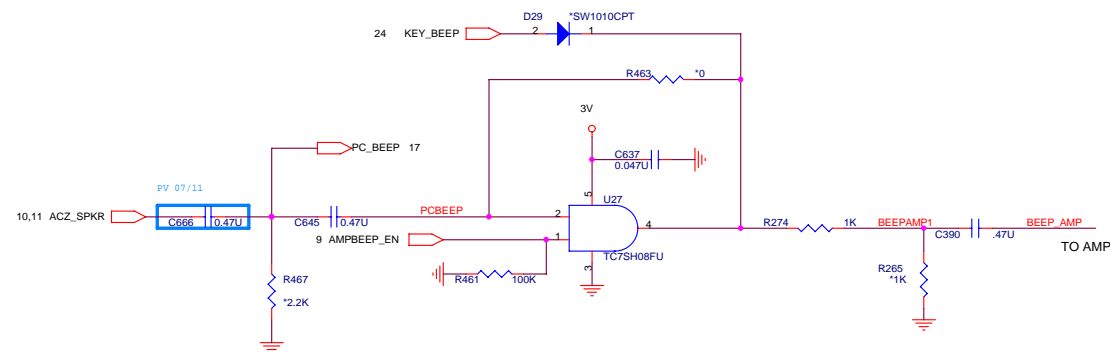
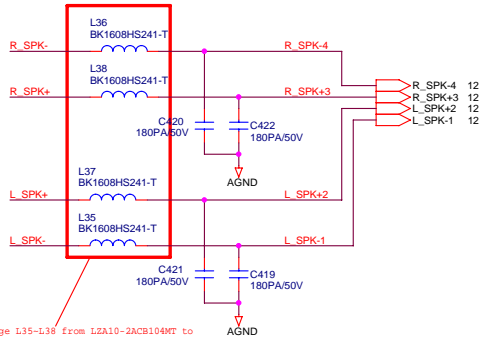
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



Change Gain from 15.6db to 10db - MV1 10/31

INT. SPEAKER

PCSPK BEEP

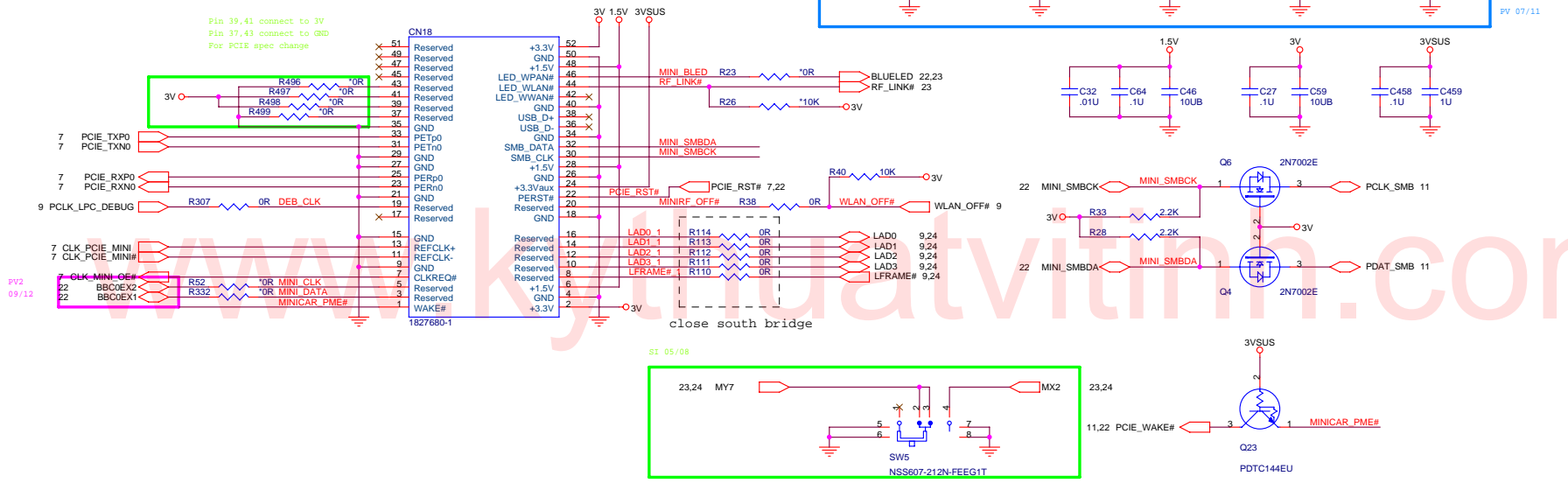


PROJECT : TT8  
Quanta Computer Inc.



### Mini PCI-E Card 1 WLAN

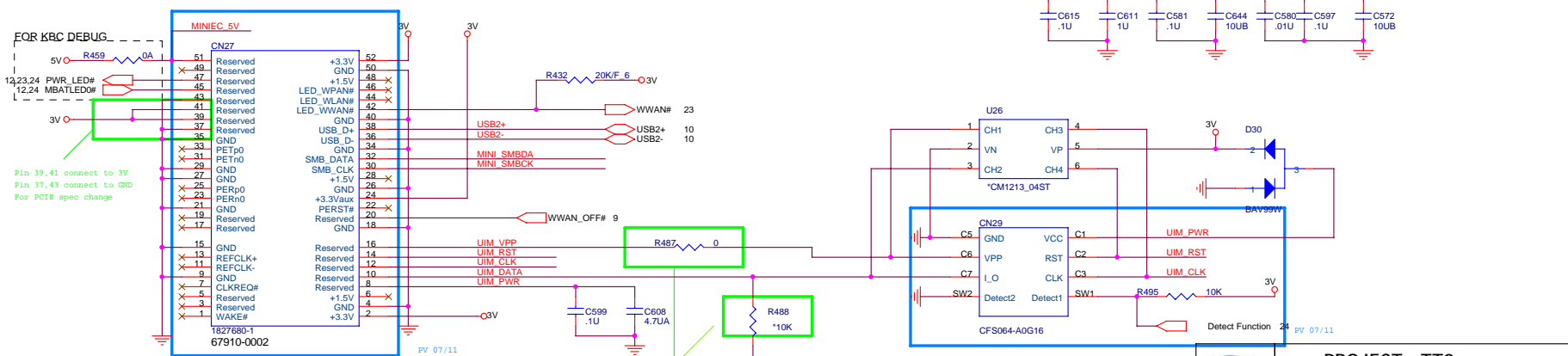
Pin 39,41 connect to 3V  
Pin 37,43 connect to GND  
For PCIE spec change



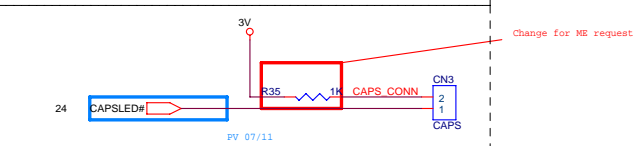
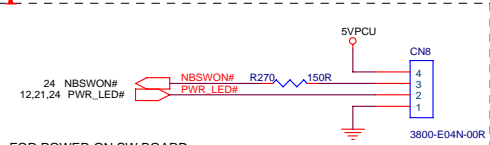
### Mini PCI-E Card 2 WWAN(W/SIM)

FOR KBC DEBUG

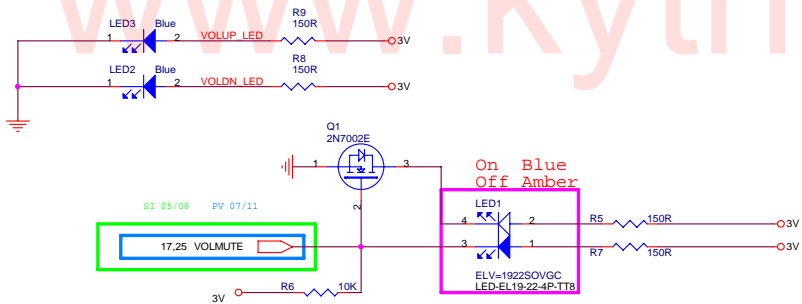
Pin 39,41 connect to 3V  
Pin 37,43 connect to GND  
For PCIE spec change







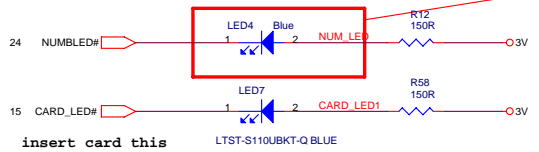
for caps lock LED board



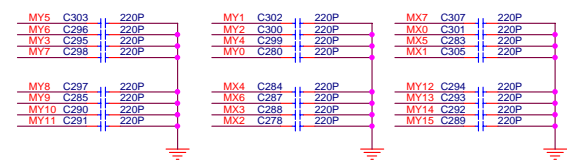
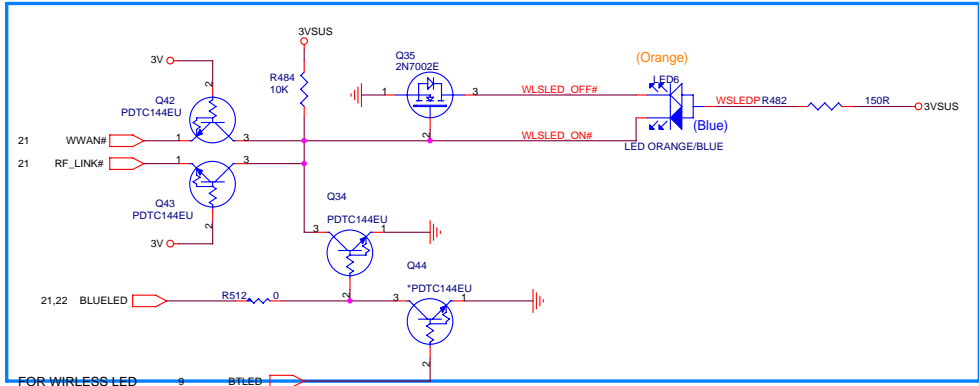
17.25 VOLMUTE

ELV=1922SOVGC  
LED-EL19-22-4P-TT8

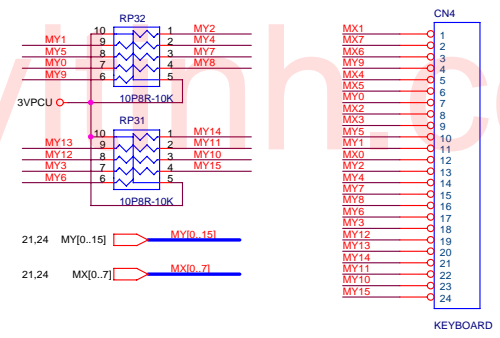
Change the LED for  
MB requests MW1  
10/31

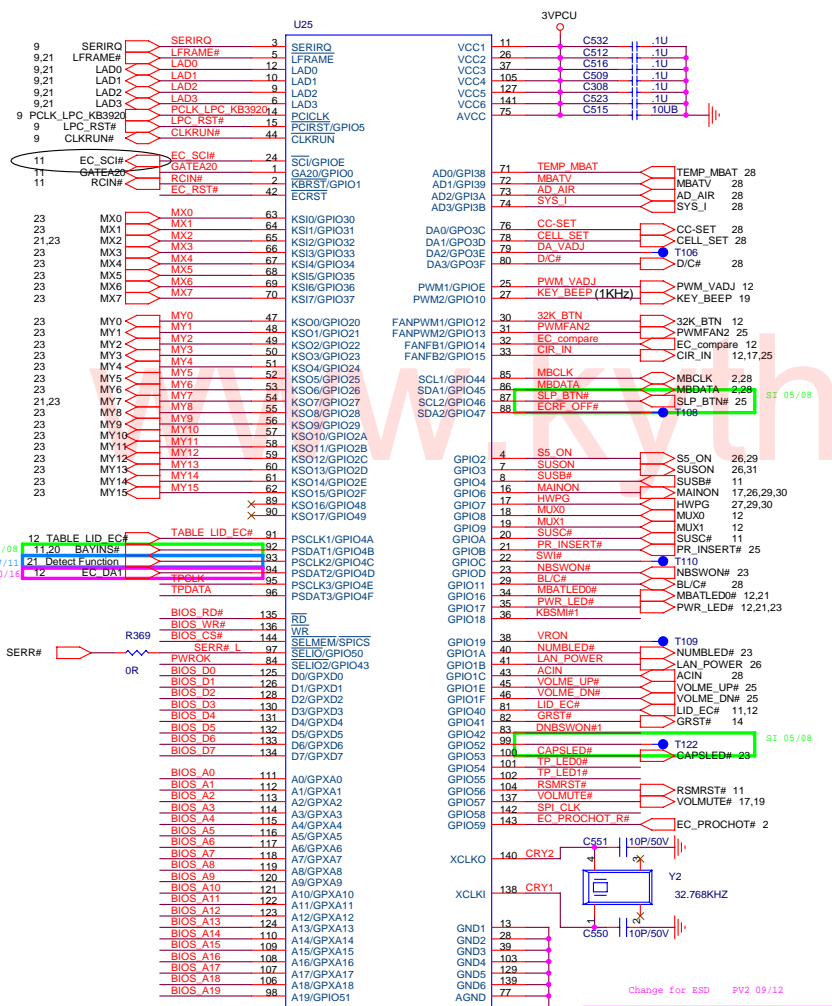


PV 07/11



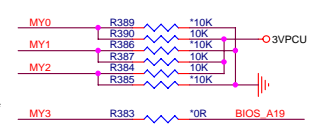
KEYBOARD PULL-UP



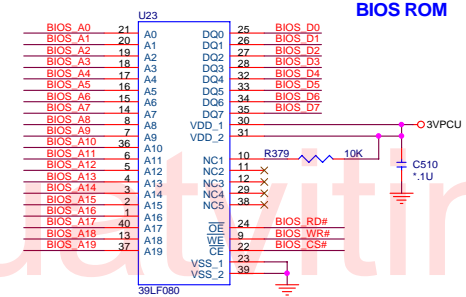


STRAP PIN

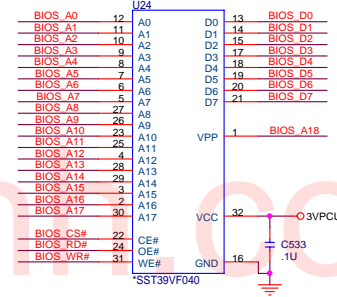
MY0	47	TP_TEST: Clock Test Mode Low: Test Mode HIGH: 32KHz clock in normal runing
MY1	48	TP_PLL: DPPLL Test Mode Low: Test Mode HIGH: Normal operation
MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode



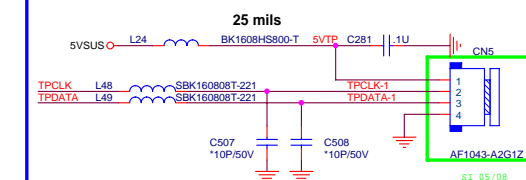
8Mbit (1M Byte), TSSOP40



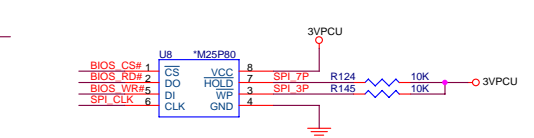
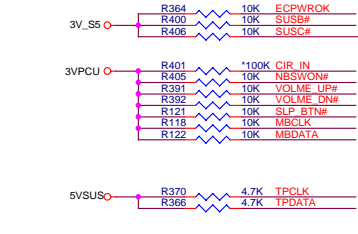
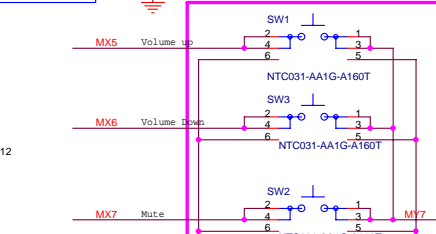
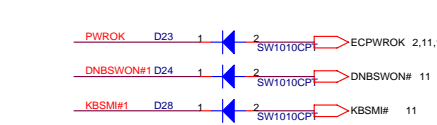
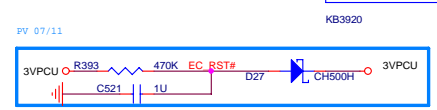
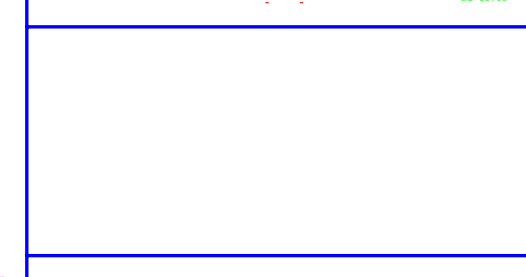
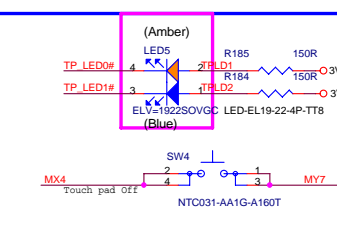
4Mbit (512k Byte), PLCC

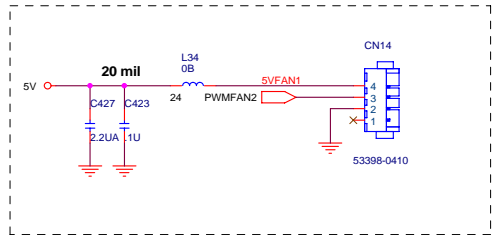
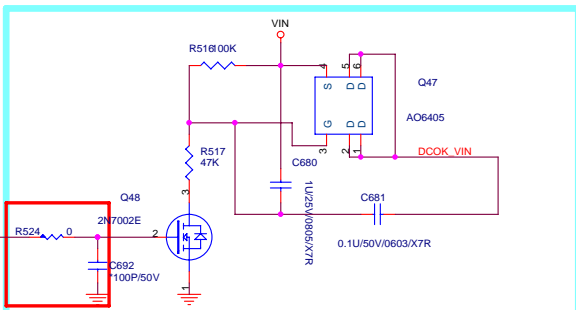
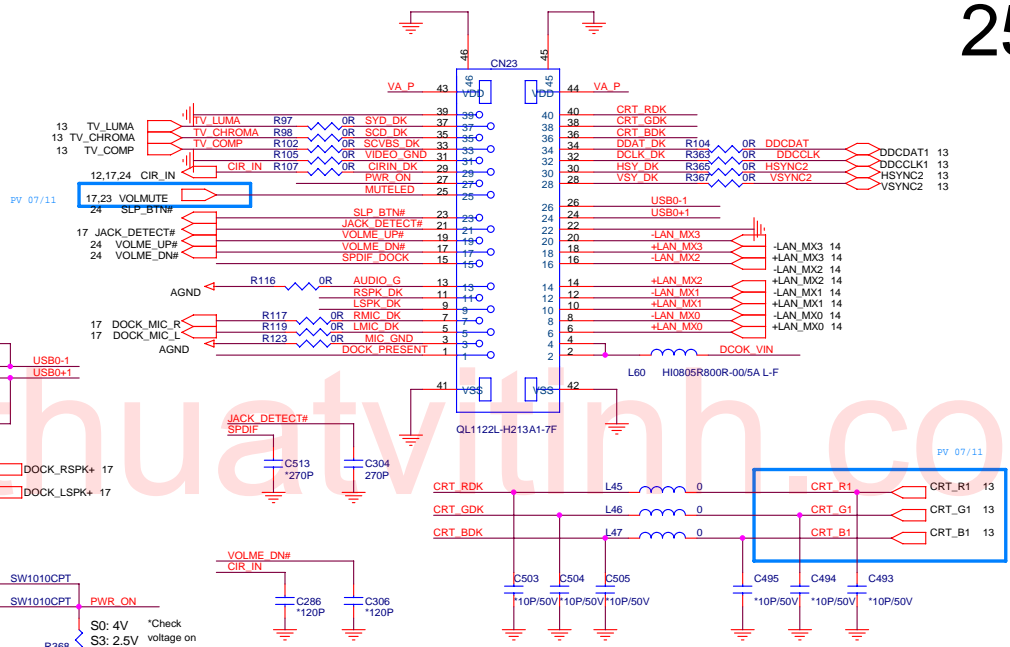
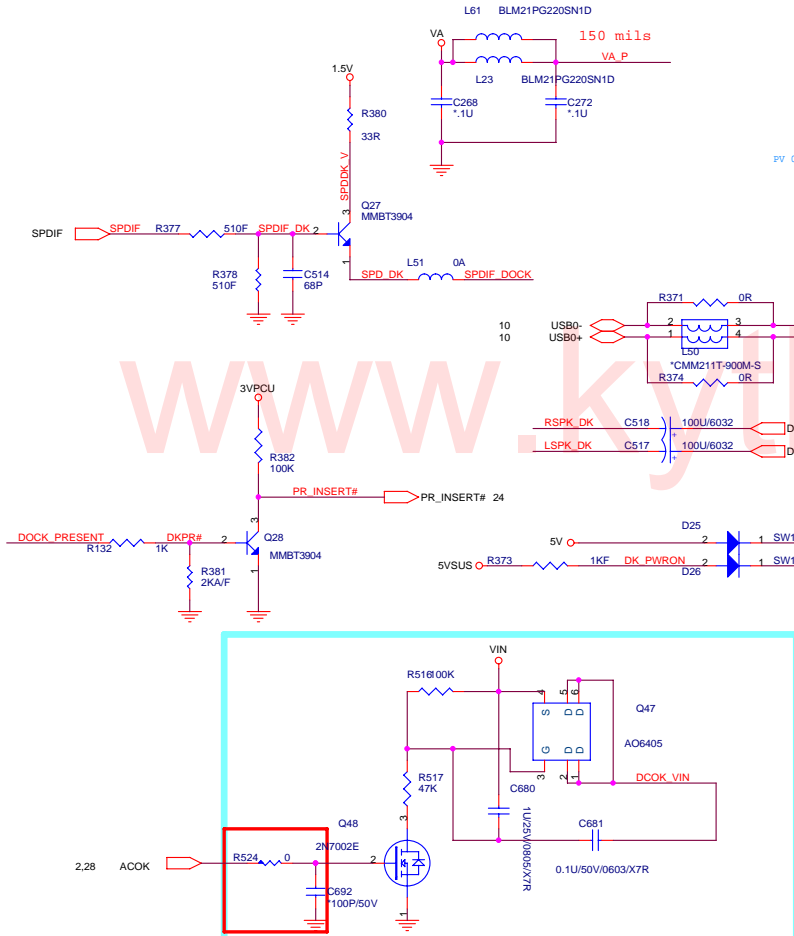


TOUCH PAD CONNECTOR



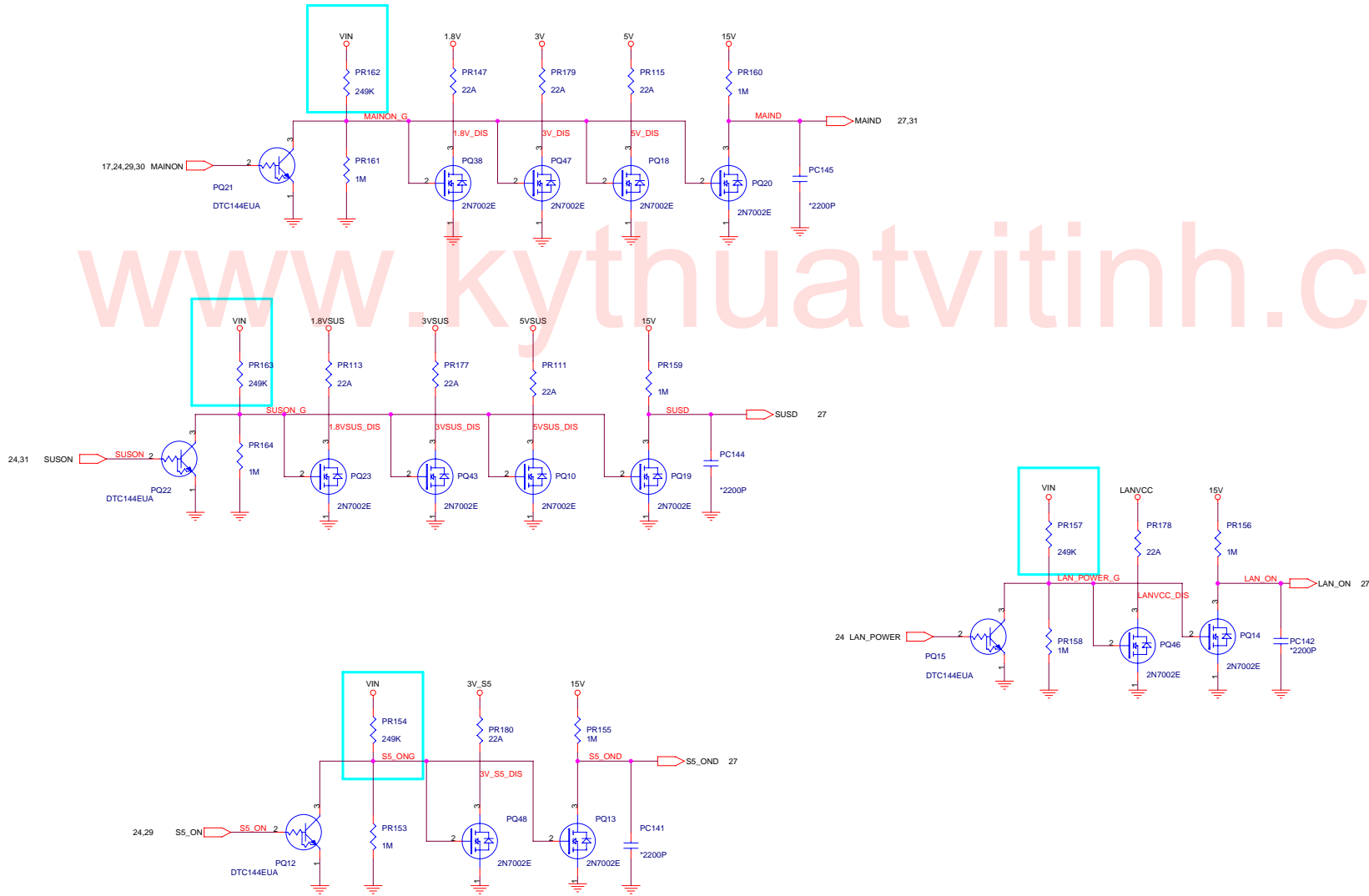
ROM CHIP P/N: AKE34ZAPK01





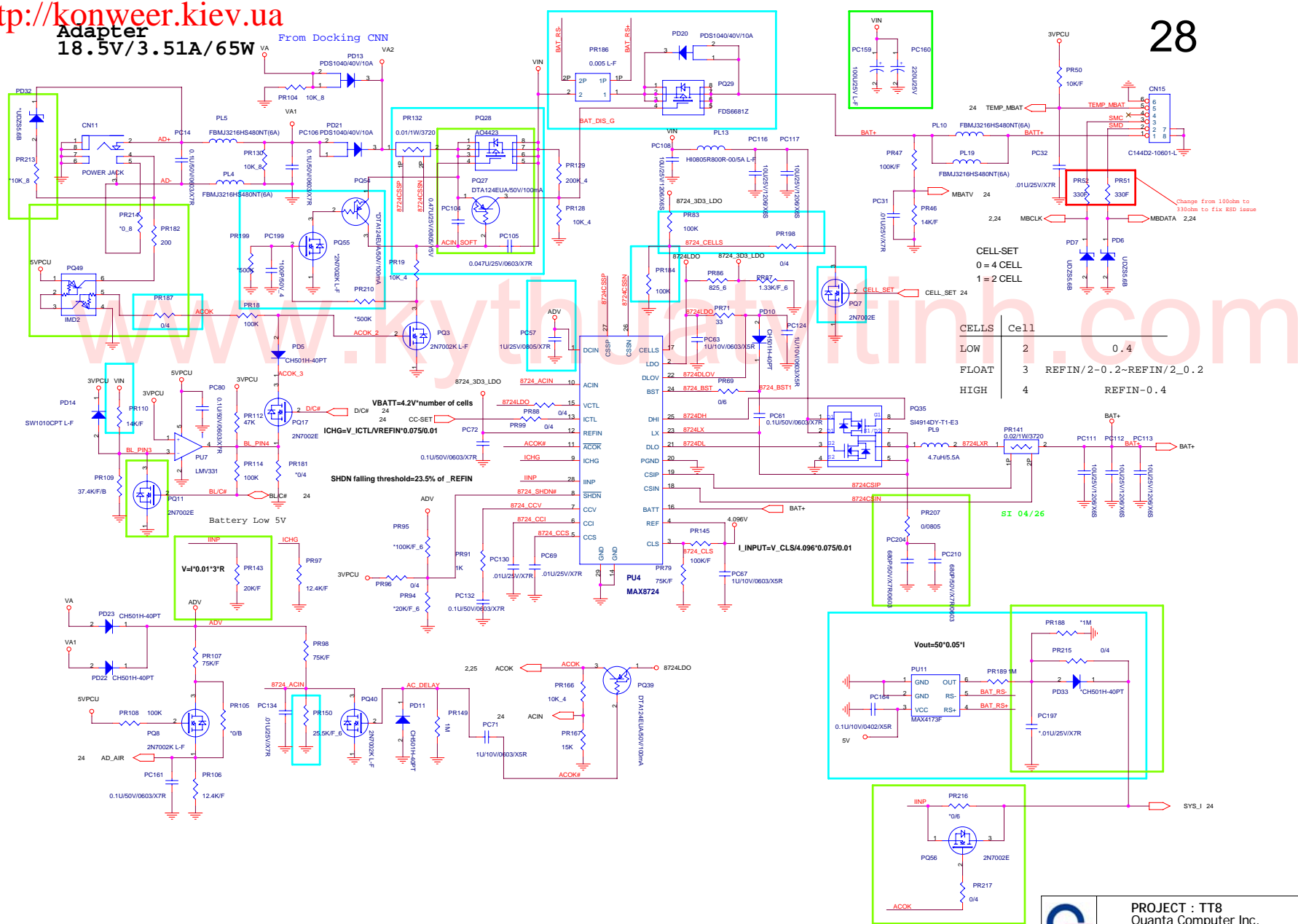
FAN1 PWM CONNECTOR

**FAN**





# Adapter 18.5V/3.51A/65W

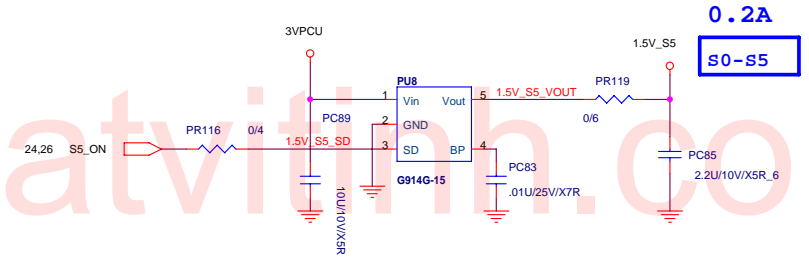
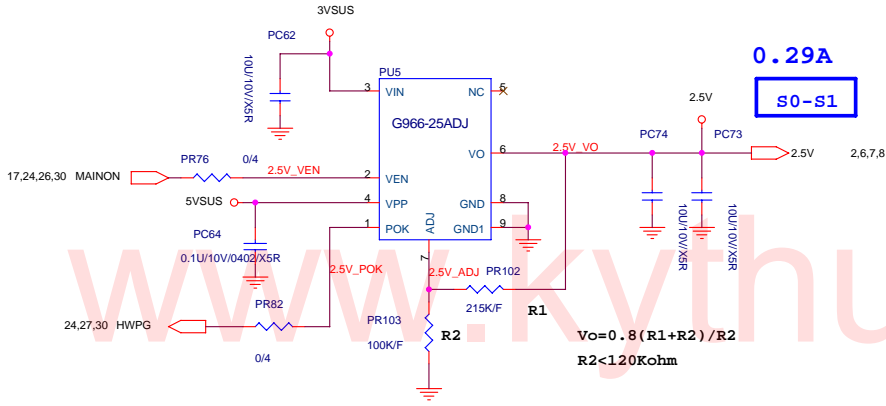


CELL-SET  
0 = 4 CELL  
1 = 2 CELL

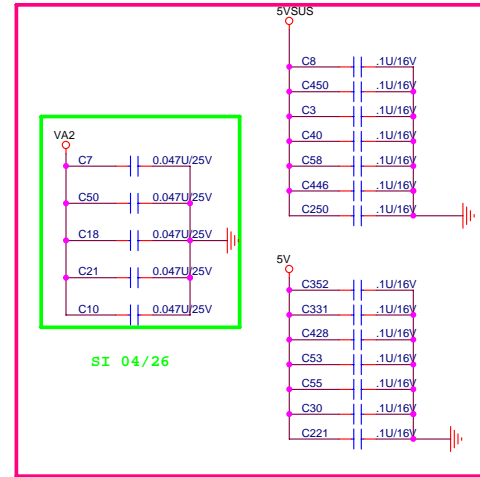
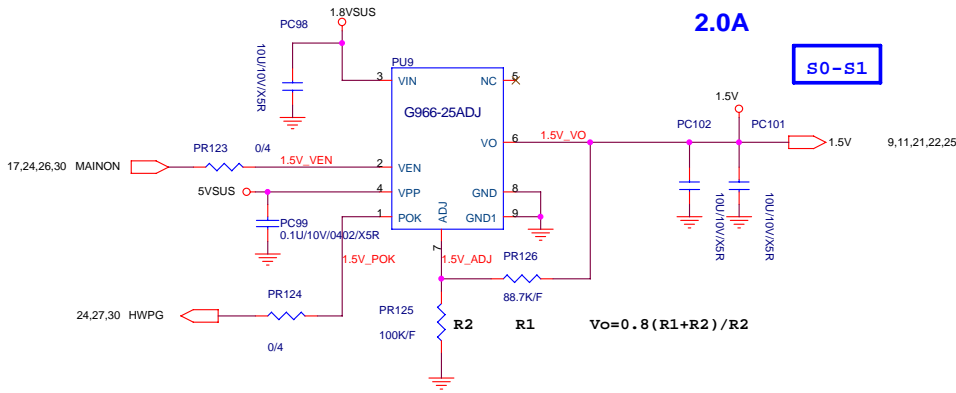
CELLS	Cell	
LOW	2	0.4
FLOAT	3	REFIN/2-0.2-REFIN/2_0.2
HIGH	4	REFIN-0.4

Change from 100ohm to 330ohm to fix RSJ Issue

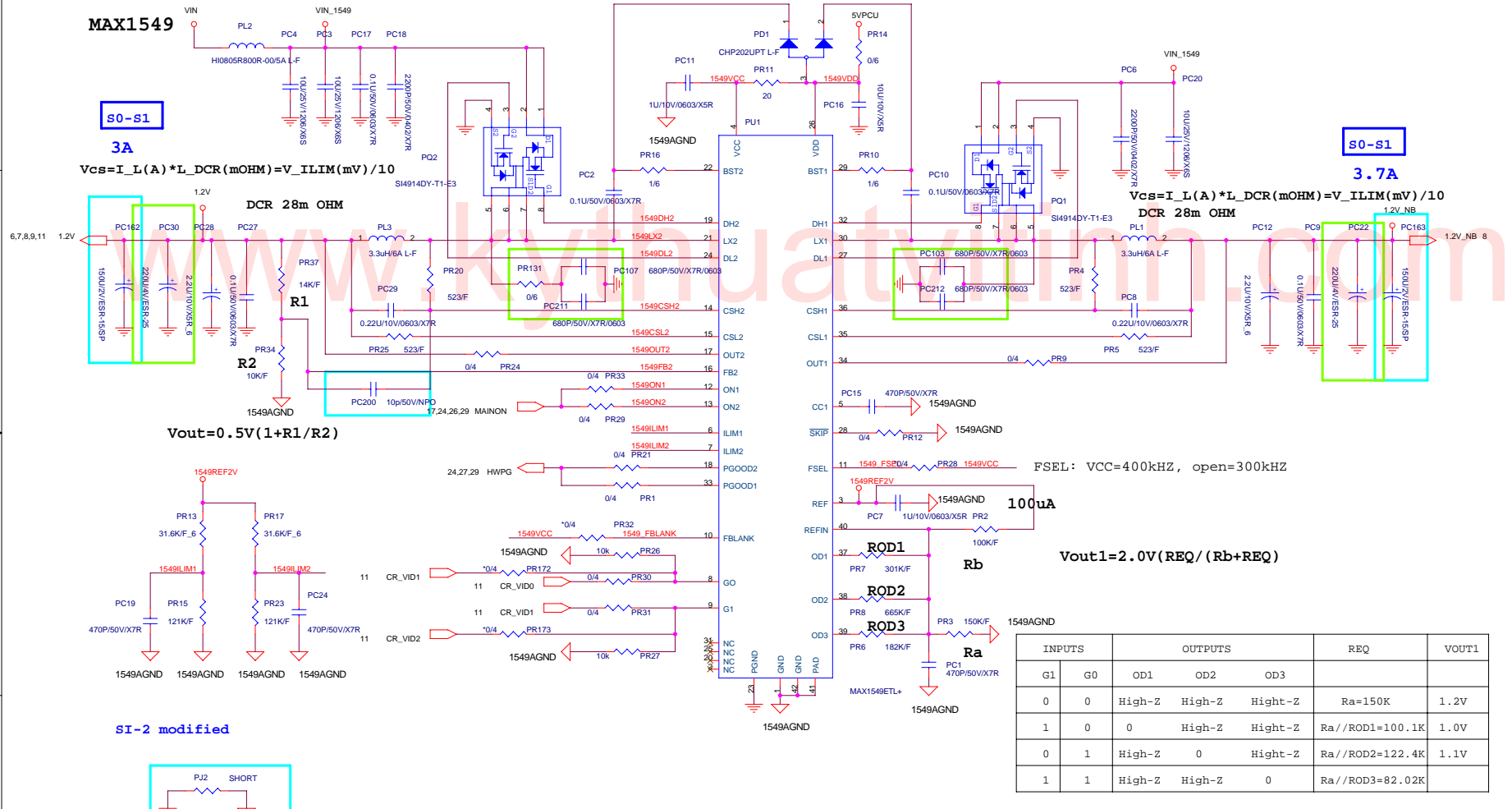
SI 04/26



EMI



PROJECT : TT8  
Quanta Computer Inc.



MAX1549

S0-S1

3A

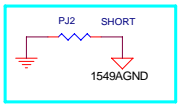
$$V_{cs} = I_L(A) * L_{DCR}(m\Omega H M) = V_{ILIM}(mV) / 10$$

DCR 28m OHM

$$V_{out} = 0.5V(1 + R1/R2)$$

1549REF2V

SI-2 modified



S0-S1

3.7A

$$V_{cs} = I_L(A) * L_{DCR}(m\Omega H M) = V_{ILIM}(mV) / 10$$

DCR 28m OHM

FSEL: VCC=400kHz, open=300kHz

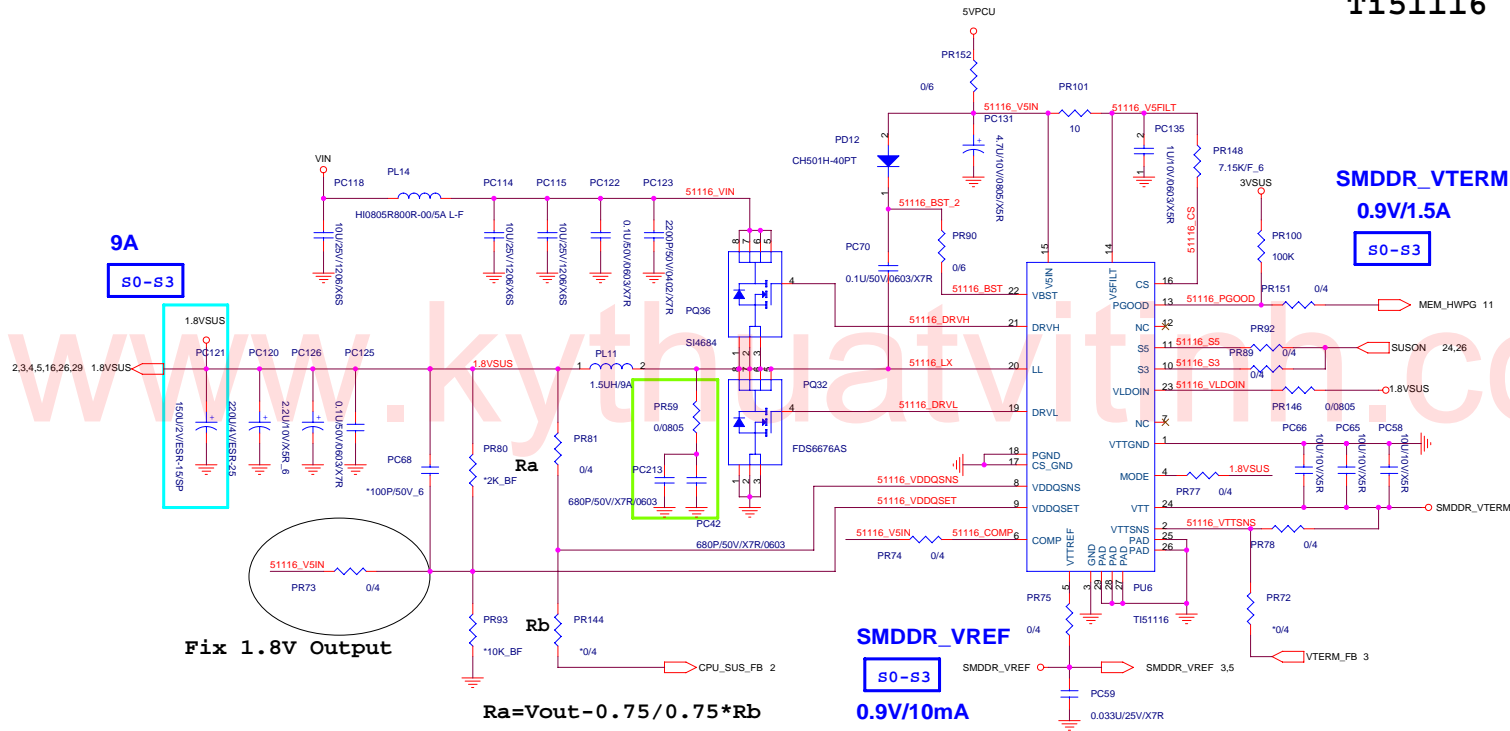
$$V_{out1} = 2.0V(REQ / (Rb + REQ))$$

INPUTS		OUTPUTS			REQ	VOUT1
G1	G0	OD1	OD2	OD3		
0	0	High-Z	High-Z	Hight-Z	Ra=150K	1.2V
1	0	0	High-Z	Hight-Z	Ra / ROD1=100.1K	1.0V
0	1	High-Z	0	Hight-Z	Ra / ROD2=122.4K	1.1V
1	1	High-Z	High-Z	0	Ra / ROD3=82.02K	

FBLANK				
VCC	OPEN	REF	GND	
150us	100us	50us	blanking disabled	OUI fault protection and FGO1 blanking
150us	100us	50us	100us	OUI forced-PWM transition operation

**PROJECT : TT8**  
Quanta Computer Inc.

Size Custom	Document Number	MAX1549 1.2V/1.2V_NB	Rev 1A
Date: Friday, November 24, 2006		Sheet 30	of 36



Fix 1.8V Output

$$R_a = V_{out} - 0.75 / 0.75 * R_b$$

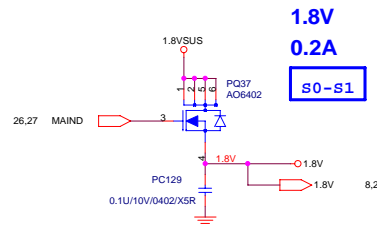
R<sub>b</sub> value from 100K to 300K ohm

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$$V\_TRIP(mV) = R\_TRIP(Kohm) * 10(uA)$$

$$I\_OCP = V\_trip / Rds\_on + I\_Ripple / 2$$

VDDQSET	VDDQ(V)	VTTRF and Vtt	Note
GND	2.5	V_ vddqns/2	DDR
V5IN	1.8	V_ vddqns/2	DDR2
FB	adjustable	V_VDDQNS/2	1.5V < VDDQ < 3V



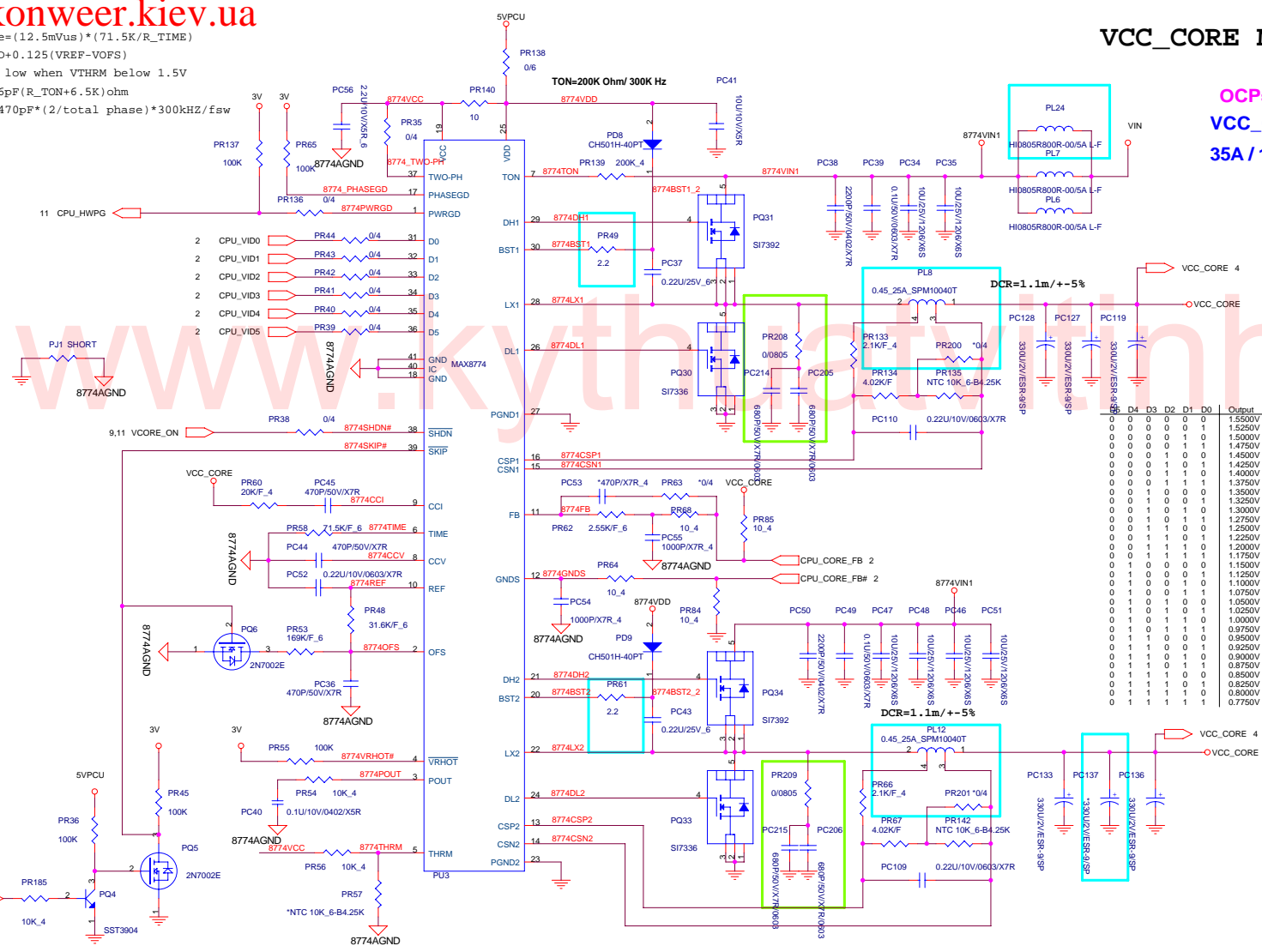
**SMDDR\_VTERM**  
0.9V/1.5A  
S0-S3

**SMDDR\_VREF**  
S0-S3  
0.9V/10mA

**1.8V**  
0.2A  
S0-S1

Slew rate=(12.5mV/us)\*(71.5K/R\_TIME)  
 VFB=V\_VID+0.125\*(VREF-V\_OFS)  
 VRHOT is low when VTHRM below 1.5V  
 Tsw=16.26pF\*(R\_TON+6.5K)ohm  
 CCV CAP=470pF\*(2/total phase)\*300KHZ/fsw

OCp=44A  
 VCC\_CORE  
 35A / 1.05V



D6	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V	1	0	0	0	0	0	0.7625V
0	0	0	0	0	1	1.5250V	1	0	0	0	0	1	0.7500V
0	0	0	0	1	0	1.5000V	1	0	0	0	1	0	0.7375V
0	0	0	0	1	1	1.4750V	1	0	0	0	1	1	0.7250V
0	0	0	1	0	0	1.4500V	1	0	0	1	0	0	0.7125V
0	0	0	1	0	1	1.4250V	1	0	0	1	0	1	0.7000V
0	0	0	1	1	0	1.4000V	1	0	0	1	1	0	0.6875V
0	0	0	1	1	1	1.3750V	1	0	0	1	1	1	0.6750V
0	0	1	0	0	0	1.3500V	1	0	1	0	0	0	0.6625V
0	0	1	0	0	1	1.3250V	1	0	1	0	1	0	0.6500V
0	0	1	0	1	0	1.3000V	1	0	1	0	1	1	0.6375V
0	0	1	0	1	1	1.2750V	1	0	1	0	1	1	0.6250V
0	0	1	1	0	0	1.2500V	1	0	1	1	0	0	0.6125V
0	0	1	1	0	1	1.2250V	1	0	1	1	0	1	0.6000V
0	0	1	1	1	0	1.2000V	1	0	1	1	1	0	0.5875V
0	0	1	1	1	1	1.1750V	1	0	1	1	1	1	0.5750V
0	1	0	0	0	0	1.1500V	1	1	0	0	0	0	0.5625V
0	1	0	0	0	1	1.1250V	1	1	0	0	0	1	0.5500V
0	1	0	0	1	0	1.1000V	1	1	0	0	1	0	0.5375V
0	1	0	0	1	1	1.0750V	1	1	0	0	1	1	0.5250V
0	1	0	1	0	0	1.0500V	1	1	0	1	0	0	0.5125V
0	1	0	1	0	1	1.0250V	1	1	0	1	0	1	0.5000V
0	1	0	1	1	0	1.0000V	1	1	0	1	1	0	0.4875V
0	1	0	1	1	1	0.9750V	1	1	0	1	1	1	0.4750V
0	1	1	0	0	0	0.9500V	1	1	1	0	0	0	0.4625V
0	1	1	0	0	1	0.9250V	1	1	1	0	0	1	0.4500V
0	1	1	0	1	0	0.9000V	1	1	1	0	1	0	0.4375V
0	1	1	0	1	1	0.8750V	1	1	1	0	1	1	0.4250V
0	1	1	1	0	0	0.8500V	1	1	1	1	0	0	0.4125V
0	1	1	1	0	1	0.8250V	1	1	1	1	0	1	0.4000V
0	1	1	1	1	0	0.8000V	1	1	1	1	0	1	0.3875V
0	1	1	1	1	1	0.7750V	1	1	1	1	1	1	0.3750V



PROJECT : TT8  
 Quanta Computer Inc.

MODEL

CHANGE LIST

Model OT1 MB BOARD

MODEL	DB1 --->S11	CHANGE LIST	Model	OT1 MB BOARD	
			Page	FROM	TO
TT8 MB 31TT8MB0006	4/17-4/20	1.Change Audio port and senser pin resistor. Internal MIC change from Pin14,15 to Pin16,17 Docking Mic Change from Pin16,17 to Pin14,15 Docking spk change from Pin23,24 to Pin 43,44 Swap Pin30 and Pin31 Change R486 from Pin 13 to Pin 34 and change from 5.1KK to 10K Change R251 10K to R485 5.1K 2.Change WWAN and WLAN Pin define Add R487 and R488 3.Change TEMP Control chip for leakage, Change Q9 and Q10 to BAM70020074 4.Change HDD connector type, RJ45/CRT connector footprint 5.Swap LCD connector signal from machine require 6.Swap U5 CRT/TV singnal from nVIDIA require 7.Change battery and D30 footprint 8.Change C251,C242,C138,C66,C71,C276,C277 footprint from 0603 to 0402 9.Add Q36,Q37,R489,C661,R490 for Docking MIC detect 10.Change SW5 and CN8 footprint for machinecal request 11.Change L41 to PBY201209T-300Y-N (Footprint : 0805) 12.Delect H3 and H4 for machinecal change 13.Change C20 from 0.1U to 1U (Fix LCD rise time) 14.Move Net "SLP_BTN#" from pin99 to pin87 15.Modify Docking mute LED circuit 16.Modify U25 SCI# signal from BIOS request, AddR491,R492 17.Modify Buletooth switch and ODD BAYINS# to EC 18.Change caps lock connector footprint from machencal request 19.Add U30,R495,R494,R493,Q38 for reserve SIM card 20.Change 4-in-1 card footprint 21.Add R44,R43,R48 Remove R62,R64,R69,R34,R24,R36 22.Change L45,L46,L47 to 0 ohm Del C503,C504,C505,C493,C494,C495 for D-SUB function	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	1A	
			20	1A	
			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	

CHANGE LIST

MODEL	SI1 ---->PV1		Model	OT1 MB BOARD	
			Page	FROM	TO
<b>TT8 MB</b> <b>31TT8MB0006</b>	5/17-7/11	1.Exchange Audio port External MIC Exchange Pin22 and Pin21 CD Line Exchange Pin18 and Pin20 Internal MIC Exchange Pin16 and Pin17 Docking Mic Exchange Pin14 and Pin15  3.Change R478 from 22ohm to 0ohm 4.Change R462 0ohm to C666 0.47u for Audio chip distortion 5.Exchange R272 and R263, R273 and R264 for amplifier gain change 6.Change Q8 from BAM51030Z15 to BAM23010Z30 for Rdsn issue 7.Remove C439 for MS pro card can not detect 8.Add C667,C668,C669,C670,C671,C672,C673,C674,C675,C676 for WLAN con not detect issue 9.Add reverse circuit for LED issue 10.Delect Q7 for Cap lock LED 11.Add EMI Cap C93,C118,C496,C497,C499,C566,C589,C555,C334,C337 12.Change CN19,CN27,CN28,CN29 footprint 14.Change Sim connector (Add detect pin) 15.Move Docking CRT signal after PI circuit 16.Add R500, R501 for Audio chip function 17.Add D37 and R502 for nVIDIA solution 18.Move D22 from +5VCRT to +5VCRT3 19.Change Docking detect circuit 20.Delet H20 H21 21.Exchange MINI_DATA and MINI_CLK 22.Add Diode for SATA and ODD LED control 23.Add power controller for 5V shutdown 24.Change WLAN LED circuit 25.Add Res for ACZ signal 26.Delete H7 and H14 for ME change 27.Modify SB to Audio and Modem signal	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	1A	
			20	1A	
			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	

MODEL

CHANGE LIST

Model OT1 MB BOARD

Page FROM TO

TT8 MB  
31TT8MB0006

PV1 --->PV2  
9/8-10/17

- 1.Page17 change voltage from +3V to 3V fix the Mic can not work
- 2.Page17 change R14 from 4.7K to 5.6K to fix LCCVDD rise time
- 3.Page17 change LCD cable Pin22 and Pin15 for switch function, Pin7 change to 32K\_BTN
- 4.Page24 add GPIO for switch function
- 5.Page10 Change cap from 18p to 22p
- 6.Page17 Change C392 and C395 from 10U to 1U to fix Docking noise
- 7.Page16 add PA11(EMI spring)
- 8.Page21 Exchange BBC0EX1 and BBC0EX2
- 9.Page20 remove C614, C607, C406, C414, C404, C405
- 10.Page20 Change C635, C415, C416 from TAN to ELEC
- 11.Page11 Del R205 and Add R207 for Bios check

1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	
31	1A	
32	1A	
33	1A	

www.kythuatvitinh.com

CHANGE LIST

TT8 MB  
31TT8MB0006

PV2 --->MV1  
10/17-11/15

- 1.Page10 Exchange USB0+/- with USB3+/- signal
- 2.Page12 Change CN12 Pin1 from 5VSUS to 3V
- 3.Page17 Change C648 and C656 from 4.7U to 22U to fix Vista issue
- 4.Page19 Change L35-L38 from LZA10-2ACB104MT to BK1608HS241-T
- 5.Page19 Change Gain from 15.6db to 10db
- 6.Page17 Del R260,R267,D312,D322 for Docking MIC
- 7.Page17 ADD R520,R521,R522,R523 for Docking MIC
- 8.Page21 Change PR51 PR52 from 100ohm to 330ohm to fix ESD issue
- 9.Page20 unstuff R188 to fix ODD problem
- 10.Page11 Change the board ID1 from low to high
- 11.Page15 Change Cap (C60,C56,C441,C44,C45)from 0.1u to 1u
- 12.Page15 Change Res (R318,R313,R312)from 39K to 10K
- 13.Page17 Add 0.01u(C693, C694) to fix high frequency problem
- 14.Page14 remove the cap(C408,C409) from MV build
- 15.Page7 Reserve C696 for nVIDIA
- 16.Page15 Reserve R525 and C695 for 3VSUS drop
- 17.Page23 Change LED4 for ME requests

Page	FROM	TO
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	
31	1A	
32	1A	
33	1A	

www.kythuativinh.com